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Three-Phase Hybrid Rectifier for HVDC Distribution System in More Electric Aircrafts

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Abstract — **High voltage direct current (HVDC) transmission systems have become popular, mainly within the scope of the More Electric Aircraft (MEA), where converters with high power density and robustness are required. In this context, this article presents a proposal of a Rectifier Unit (RU) based on a Three-Phase Hybrid Rectifier for MEA, which is denominated as TPHR-HVDC-MEA. The architecture of this RU is based on a Diode Bridge Rectifier Unit (DBRU) and on a three-phase Boost converter associated with a LLC Series Resonant converter (Boost+LLCSR). The main benefits of the proposed hybrid architecture are in reduced system size and higher conversion efficiency, since the Boost+LLCSR process only 50% of the rated power. Therefore, the robustness and reliability can be increased due to the reduced thermal stresses to which the semiconductors are subjected. A 1.2kW prototype was built in laboratory to corroborate the obtained results showing high efficiency (97%), great dynamic response for frequency variations at the alternating current (AC) power supply (400Hz to 800Hz) and compliance with the DO-160F standard (DHTi of 3.9%) are achieved.**

Index Terms—Digital signal processor (DSP), high voltage DC (HVDC), hybrid rectifiers, more electric aircraft (MEA), power factor correction.

I. INTRODUCTION

The Electric Power System (EPS) in aircraft has been the subject of frequent study in recent years, concerns such as CO_2 consumption, energy conversion efficiency, replacement of mechanical / hydraulic drives by electric ones, brings up the More Electric Aircraft (MEA) concept [1], [2]. With the purpose of massive electrification in an aircraft, the search for improvements in electrical converters is the key to systems with high efficiency and reliability. Thus, the use of new semiconductor technologies (SiC and GaN) help in the performance of these converters, which are influenced by harsh environment, low pressures and cosmic radiation present at high altitudes [3]. Additionally, the qualitative aspects of the converters need to comply with standards such as MIL-STD-704 [4], meet voltage regulation and current total harmonic distortion (THDi) levels imposed by DO-160F and ISO-1540 [5], [6].

As for the EPS architecture, the AC power systems can operate at fixed frequency (115V/400Hz), or at variable frequency (115V/360-800Hz) such as observe in Boeing 787. Regarding the HVDC transmission system in the output bus of the converters, levels of 400V and +/-270V are normally used [7].

In order to reduce the weight of the conductors and, consequently, the fuel consumption in the aircraft, HVDC output busbars are used [2]. The main concern with protection systems for HVDC has been the occurrence of electrical arcs in situations of switching and fault detection, however, there have been evolutions to mitigate these problems, including the use of HVDC hybrid circuit breakers [8]. Thus, it becomes feasible to use voltage levels of 540V to supply loads in MEA. Hybrid AC-DC converter topologies with specific configurations stand out – generally multi-port, multi-level, modular and interleaved converters – that allow reduced current and voltage efforts in semiconductors. The last factor is fundamental in HVDC topologies, since higher altitudes also decreases the voltage isolation capacity of semiconductors. In addition, high levels of power density and efficiency are desired [9].

In this scenario, a three-port three-phase rectifier (TPTPRs) with high-voltage and low-voltage DC output is proposed in [10]. The efficiency achieved was around 97% at full load for a specific high voltage supply condition, but the THDi can also be high depending on the voltage levels used. The developed control strategy is based on SVPWM modulation and requires the use of eight (8) sensors (voltage and/or current) in total and the design of four (4) PI controllers. However, all power processing takes place entirely through switched converters, which can limit the reliability of the system.

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In [11], the authors proposed a single-phase AC-DC dual-voltage rectifier wich presents a characteristic similar to the DC bus voltage compensation technique used in the proposed TPHR-HVDC-MEA. The output bus is provided by two LLC Series Resonant (LLCSR) converters, only one of which is controlled. The THDi is 4% for 50Hz and the converter achieves 96% efficiency. The system is capable of operating in two modes –constant current or constant voltage modes, but uses a considerable amount of sensors and controllers. Again, all power processing is done entirely by switching converters.

Another family of single-stage modular converters which uses the LLC converter for galvanic isolation is called single-stage high-frequency-link modular three-phase LLC AC-DC converter and was presented in [12]. Low THDi (2-3%) is achieved, but the input inductors operate on Discontinuous Conduction Mode (DCM) requiring additional filtering. Deploying a hybrid control satrategy based on phase shift pulsewidth-modulation (PS-PWM) and pulse frequency modulation (PFM), it is capable of operating in constant current and voltage modes at the output. Only two sensors are used and the efficiency at rated load is 91.5%, but for 50% of the rated power the efficiency drops to about 75%, which is expected for LLC converters and also demonstrated in [13].

In this context, Hybrid Rectifiers (HR) emerge as an attractive solution to MEA. The main benefits of the HR concerns the reduced system size and higher conversion efficiency since an ordinary Diode Bridge Rectifier Unit (DBRU) operates with low switching frequency (AC line frequency) and process 50% of the rated power. Therefore, the power processing requirements of switches, diodes and energy storage elements deployed at the switched converters are considerably reduced, in a manner that the robustness and also the reliability of the RU is increased [14]-[19]. Additionally, switching converters with high power capacity have statistically higher failure rates [20].

In [19], the authors proposed a single-phase HR with series DC voltage compensation technique for applications in DC microgrids. The premise of using few sensors was fulfilled, but the use of an isolated SEPIC converter limits the overall power rating. Therefore, for series DC voltage compensation it is essential to use an isolated converter, either AC-DC or DC-DC. One of the most popular isolated DC-DC converters is the LLCSR, which has been widely deployed in the transportation sector due to the high efficiency and high power density provided. It should be noted that there are many topological variants of the LLCSR converter and, additionally, several control strategies wich can increase the numbers of sensors and the complexity of implementation [21]-[24].

In [25] the authors presented a HR with series DC-link voltage compensation. An isolated Full-bridge (FB) converter is used for the voltage regulation. Some of the disadvantages of this configuration is the fact that, despite using an isolated converter fed by a front-end converter, the topology does not offer electrical isolation between the load and the AC grid. Moreover, as observed in other topologies, the fact of using converters with multi-stage topology increases the number of semiconductor devices required for its implementation. In addition, to achieve higher power density levels, the switching frequency of SiC devices is high, requiring current sensors with high bandwidth. Although this requirement is important, the price of sensors in the MHz band has become attractive [26].

That being said, it should be noted that the herein proposed TPHR-HVDC-MEA is an evolution of this converter and presents the following contributions: 1) Higher efficiency due to the deployment of an optimized LLCSR converter which always operates at fixed frequency and at resonance; 2) New control methodology supported by the specific operation of the LLCSR converter and the need for a design of only one voltage controller; 3) HVDC operation in MEA context, which required a control strategy with high sampling rate – especially for hysteresis current controllers – and a Pulse Reduction Strategy (PRS) to mitigate switching losses and operating in conjunction with a SOGI-PLL supporting AC line frequency variations.

To present the results obtained and to prove the effectiveness of the proposed TPHR-HVDC-MEA, the remainder of this article is structured as follows. In Section II, the working principle of the TPHR-HVDC-MEA is detailed. In Section III the conception of the control strategy is presented. In Section IV the controller design is presented and its performance analyzed. Section V presents the experimental results obtained in the laboratory, as well as insightful discussions. Finally, in Section VI, conclusions about the work are made.

II. TPHR-HVDC-MEA

A schematic diagram of the Three-Phase Hybrid Rectifier with HVDC output bus for MEA applications (TPHR-HVDC-MEA) is portrayed in Fig. 1.

A. Power System Architecture

Fig 1 illustrates the power structure and also the sensors used, three for current and four for voltage. Note that there is no need to sense the voltage on the DC-link of the three-phase Boost converter and control techniques for charge balance in TPHR-HVDC-MEA capacitors. The voltage sensing is mandatory in most modular and multi-level converters [27]. For a converter to fit into the HR schemes, there must be a diode bridge (Graetz bridge) or even a thyristor-based converter switched at low frequency, i.e., at the line frequency [14]-[17]. A brief discussion about the converters that make up the TPHR-HVDC-MEA structure, as well as their main operational characteristics are described below.

1) Three-phase Boost: this converter is one of the most popular Active Front-end Rectifiers (AFR) topologies, with commercially optimized modules widely available. It is important to outline that, for this application, the AFR converter needs to be bidirectional in order to comply with the THDi requirements established by DO-160F [28].

2) LLC Series Resonant (LLSR): this converter is cascaded with the three-phase Boost converter and its electrical isolation is essential for the correct functioning of the series voltage composition at the output, as also observed in [25]. Its design is fundamental to achieve high efficiency levels. It is noteworthy

Fig. 1. Power structure of the TPHR-HVDC-MEA.

that it assures the operational characteristic that made possible to achieve 97% efficiency at rated load with a configuration of three-phase Boost and LLCSR cascaded converters. The voltage gain of this converter is composed of three factors. The first is the topology on the primary side (full-bridge or half-bridge). The second is the transformation ratio given by Np:Ns1:Ns2. The third is the frequency response of the tank circuit, which has an influence on the efficiency and on the semiconductors switching losses. The last factor is analyzed below.

The relationship between leakage and magnetizing inductance is given by (1). This relationship provides the concept of flexibility in output voltage regulation. Thus, high values allow a wide range of regulation at the output. In this work, however, reduced values of this variable are desired because it makes possible to design the converter with the high frequency transformer and L_d in a single physical unit, which turns the response curve flat close to the resonant frequency [29].

$$\lambda = \frac{L_d}{L_m} \tag{1}$$

The choice of high values for magnetizing inductance decreases the magnetizing current, as a consequence, the conduction losses in the MOSFETs and in the transformer primary windings are lower. However, it is necessary to consider the influence on the discharge time of the intrinsic capacitances of the MOSFETs to achieve Zero Voltage Switching (ZVS). Thereafter, L_m must obey (2). Where td is the dead time between gate driver pulses, f_s is the switching frequency and C_{total} is the intrinsic capacitance of the switches plus other parasitic elements [30].

$$L_m = \frac{t_d}{16 f_s C_{total}} \tag{2}$$

The normalized frequency f_n is defined by (3), where f_r is the resonant frequency of the tank circuit.

$$f_n = \frac{f_s}{f_r} \tag{3}$$

The quality factor Q, is defined by (4) and is related to the output resistance reflected to the stage of the oscillator circuit R_{ac} and the capacitance of the tank circuit C_r, together with L_d.

$$Q = \frac{\sqrt{\frac{L_d}{C_r}}}{R_{ac}} \tag{4}$$

Finally, considering (3) and (4), the voltage gain M, considering the first harmonic approximation is defined in (5) [30].

$$M = \frac{f_n{}^2}{\sqrt{[f_n{}^2(\lambda+1)-\lambda]^2 + [f_n Q(f_n{}^2-1)]^2}} \tag{5}$$

One should note that, for f_n equal to 1, i.e., operation in the resonance range, the frequency response presents unity gain and is independent of the final power delivered to the load. Therefore, it can be concluded that the LLCSR is acting as a DC transformer with fixed gain (DCX), as demonstrated in [31]-[33]. This characteristic highlights the advantage of open loop LLCSR operation in the highest efficiency regime, and thus eliminates the need for specific controllers for the LLCSR converter, in addition to allowing the absence of sensing the three-phase Boost output voltage for the TPHR-HVDC-MEA. Under these circumstances, the only determining factor for the gain of LLCSR is the $N_p:N_{s1}:N_{s2}$ transformation ratio. This in turn, is determined in such a way to provide enough voltage for the Boost to be able to impose current and compose the output voltage of the TPHR-HVDC-MEA.

3) Diode Bridge Rectifier Unit (DBRU): It is usually composed of a low frequency commutated GRAETZ bridge unity with low EMI levels, high efficiency and robustness [15], [28]. Its purpose in the TPHR-HVDC-MEA is to provide about half of the rated power required by the load and thus reduce the power requirements of the semiconductors used to implement the Boost+LLCSR.

B. Input line current composition

According to Fig. 1, the instantaneous input line current of are given by (6)-(8). As portrayed in Fig. 2, one can note that the operating mode of currents $i_{DBRU(a)}$, $i_{DBRU(b)}$, $i_{DBRU(c)}$, is close to the DCM of operation. This is because the quality factor of the inductors L_{DBRU}, and its respective internal windings resistance, translates into a physically smaller inductor. Therefore, the efficiency of the TPHR-HVDC-MEA converter as a whole is optimized.

$$i_a(t) = i_{DBRU(a)}(t) + i_{Boost(a)}(t) \qquad (6)$$

$$i_b(t) = i_{DBRU(b)}(t) + i_{Boost(b)}(t) \qquad (7)$$

$$i_c(t) = i_{DBRU(c)}(t) + i_{Boost(c)}(t) \qquad (8)$$

The input line currents of the DBRU in the time domain are obtained by solving differential equations and using computation methods. The periods (t_1, t_2, ..., t_8) described in Fig. 2 are established by the switching states of the DBRU in relation to the line voltages. The current composition result for line A, for example, is shown in Fig. 3. For the sake of brevity, the detailed solution of the differential equations will not be demonstrated in this work.

As expected, one can observe that $i_{DBRU}(a)$ is the current found at the input of an ordinary three-phase diode bridge rectifier with inductive filter on the AC side. Once that the main target of the input current controller is to impose sinusoidal current on the AC grid, $i_{Boost}(a)$ assumes the waveform for this objective to be achieved, according to (6)-(8). In such a way that, the role of the three-phase Boost converter is to impose a complementary current in such a way as to obtain PF close to unity and AC input line currents with reduced THD. Therefore, one can conclude that, in fact, the sum of $i_{DBRU}(a)$ and $i_{Boost}(a)$ results in a sinusoidal input line current with low THD. The developed PRS technique has the function of changing only the internal switching currents of the Boost+LLCSR converter (i_{Boost}), therefore, (6)-(8) are valid for the Boost+LLCSR operating with and without PRS and the theoretical input line currents of the DBRU will be the same in both cases.
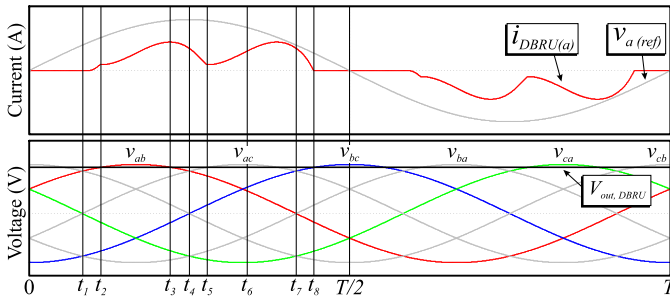
Fig. 2. At the input of the DBRU: on the top - input line current and line-to-neutral voltage; on the botton - line-to-line voltages highlighting the time interval related to the switching states of the diode bridge.
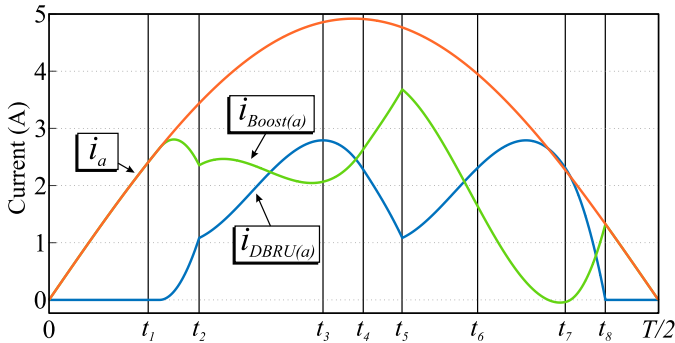
Fig. 3. Theoretical input line current composition based on differential and computational solutions.

C. Output Voltage Composition

Again, by the representation of Fig. 1, the composition of voltages on the output bus is defined by (9).

In steady state, the average power processed by each converter is given by the relationship between its output voltage and that of the HVDC bus. It is important to note that, for output series compensation, the amount of power processed for each converter is given by (10) and (11), considering a lossless TPHR-HVDC-MEA converter. For most HR presented with the common output bus [15], the power rating of each rectifier group requires an additional algorithm for the input current controller in order to establish an optimal level of THDi.

$$V_{out}(t) = V_{out,DBRU}(t) + V_{out,LLC}(t) \qquad (9)$$

$$P_{Boost} = P_{LLC} = \left(\frac{V_{out,LLC}}{V_{out}}\right) \times P_{out} \qquad (10)$$

$$P_{DBRU} = \left(\frac{V_{out,DBRU}}{V_{out}}\right) \times P_{out} \qquad (11)$$

For the HVDC application, the power rating of the line commutated converter, the DBRU, determines the level of robustness and even guarantees higher power density to the TPHR-HVDC-MEA. For example, for 400V at the DC-link, the power rating of the DBRU can reach about 73% of the rated power [25], but the assumption of conductors weight reduction would be lost due to the lower DC-link voltage.

III. CONTROL STRATEGY

The algorithm was developed in C language and embedded in the multi-core DSP TMS320F28379D from Texas Instruments. It has a clock of 200MHz and four parallel processing units – 2 CPU's and 2 Control Law Accelerators (CLA) associated to each CPU. In addition, the Trigonometric Math Unit (TMU) functionality improves the bandwidth of the controller, especially with sine operations presented in the PLL algorithm. The control scheme is shown in Fig. 4, where G1-G10 correspond to the signals sent to the gate drivers responsible for the command of switches Q1-Q10 shown in Fig. 1. As mentioned previously, the LLCSR converter is optimized to operate at resonance and with static gate driver pulses, which facilitates the overall control of the TPHR-HVDC-MEA and eliminates the need of sensing the output voltage of the Boost converter.

Thus, each core control loop is triggered by the interrupts of the four ADCs available in the DSP. The CPU1 is sampled at a rate of 200kHz and it is responsible for executing the external voltage loop, generating the reference currents, the PWM pulses for the LLCSR converter and executing three single-phase SOGI-PLL. In this work, the single-phase SOGI-PLL was used not only for its excellent response to transients and low frequency oscillations [34], but its main function is to provide unitary references of the phase voltages for the PRS performed in the remaining cores.

With the help of the CLA, the other cores – CPU1.CLA, CPU2, CPU2.CLA – are assigned to the routine of the PRS and

the hysteresis controller at a sampling rate of 400kHz. It is noteworthy that this high sampling rate improves the response of the current controller and limits the maximum switching frequency at 200kHz on the Boost converter. Which in turn, is predominantly influenced by the value of L_{Boost} and delays such
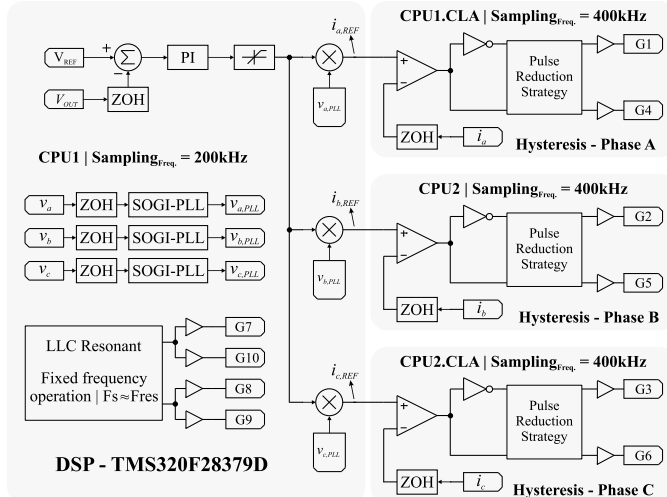

Fig. 4. Control scheme implmented with a multi-core DSP TMS320F28379D.

as: the current sensor bandwidth, ADC acquisition window duration, code execution, dead time, propagation delay and noise immunity of the gate driver IC (UCC5350MC). These factors reinforce the need for parallel operation between cores.

The PRS, similar to the one applied in [35], consists of two comparisons. The first is the sign of the PLL reference, the second is the threshold level in relation to the absolute value of the PLL defined by (12).

$$Threshold > \sin(60°) \tag{12}$$

Fig. 5 illustrates the comparison process described for phase A, as an example. Two distinct signals are generated as a clamp logic for the gate pulses of switches Q1, Q4, connected to phase A. At these moments, the current in phase A is indirectly controlled by phases B and C, totaling a 120º reduction of the pulse applied per period in order to mitigate the switching losses. For a three-phase balanced system, i.e., no current flowing through the neutral point, by applying the KCL at neutral, the current in phase A is defined by (13). It is important to point out that the composition of currents shown in Fig 3, also described by (6), (7) and (8), is the same with or without the application of the PRS algorithm. Therefore, this strategy changes only the switching current portrayed in the periods indicated in Fig. 5.

$$i_a = -(i_b + i_c) \tag{13}$$

One of the criteria that allows the flexibility of current controller is the correct adjustment of the SOGI-PLL. In this way, the Low-pass Filter (LPF) characteristic of the PLL is

responsible for the dynamic response with minimal phase displacement and is adjusted according to (14), assuring stable
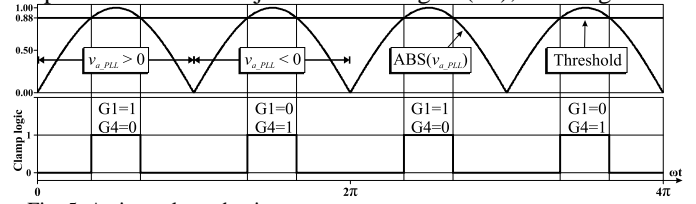
Fig. 5. Active pulse reduction strategy.

operation over the entire range of AC power supply frequency variation expected in an aircraft (400Hz to 800Hz).

$$LPF_{PLL}(s) = K_{PLL}\left(1 + \frac{1}{sT_{PLL}}\right) \tag{14}$$

Where: $K_{PLL} = 7$, is the LPF gain.
$T_{PLL} = 0.005$, is the time constant of the LPF.

One relevant aspect is that the reference signals for the Boost currents comes from the SOGI-PLL ($v_{a,PLL}$, $v_{b,PLL}$, $v_{c,PLL}$). In this manner, if the SOGI-PLL is designed incorrectly allowing high phase oscillations, the THDi could increase or even prevent the correct functioning of the PRS under the occurrence of disturbance at the AC grid.

IV. CONTROLLER DESIGN

As mentioned before, one of the advantages of the TPHR-HVDC-MEA is the lack of control by the LLCSR converter. It operates as a voltage source both at the input and output, defining a gain mostly depended on the turns ratio ($N_p:N_{s1}:N_{s2}$). As for the design and survey of the current plant, they can be omitted, since the bandwidth of the internal current loop is much larger than the voltage loop and, additionally, the current imposition by the hysteresis controller is also fast, as expected [16]. In this sense, the only controller designed is the PI of the external voltage loop. Therefore, the open loop behavior of the TPHR-HVDC-MEA is investigated from a step applied in the Boost current reference.

The closed loop block diagram of the TPHR-HVDC-MEA is illustrated in Fig. 6(a). It considers the current and voltage composition already mentioned in (6)-(9), in addition to synthesizing the equivalent system of the Boost and LLCSR cascaded converters – *Gvi_BoostLLC(s)*. Thus, for the voltage PI design, it is necessary to find the equivalent transfer function of the system (*Gvi_eq(s)*) represented by Fig. 6(b), where the manipulated variable – $I_{REF}(s)$ is the input of the system and the controlled variable – $V_{OUT}(s)$ is the output.

In order to verify the response in *Gvi_eq(s)*, a disturbance in the form of a step in the reference current is performed in all phases of the TPHR-HVDC-MEA [36]. Fig. 7(a) illustrates the process performed for phase A. The output voltage behavior of the TPHR-HVDC-MEA is approximated to first order systems, as illustrated in Fig. 7(b). In this way, it is possible to estimate the transfer function – *Gvi_eq(s)*, from the initial and final values of the current disturbance and, from the initial and final values of the output voltage. In addition, the period which the response reaches 63% of its value in steady state is calculated.

Thus, the approximate equivalent system, *Gvi_eq(s)*, for the control of the TPHR-HVDC-MEA is described by (15)-(17).

$$G_{vi\_eq}(s) = \frac{V_{OUT}(s)}{I_{REF}(s)} = k\frac{a}{s+a} \quad (15)$$

$$k = \frac{V_{OUT(final)} - V_{OUT(initial)}}{I_{REF(final)} - I_{REF(initial)}} \quad (16)$$

$$a = \frac{1}{T_{(63\%)}} \quad (17)$$

Where:
a – is the pole frequency of the first order system.
k – is the gain of the first order system.

This analysis of the converter behavior by applying a disturbance in the reference current, when using the hysteresis controller, is performed preliminarily in computer simulation to determine the response of the converter. For different converters, the assumed behavior can be second-order [36]. It is therefore possible to find the substitute sets of equations (15-17) for the correct representation of the supposed system.

The block diagram portrayed in Fig. 8 shows the closed loop equivalent system. In summary, the open loop equivalent system is characterized predominantly by the charge in the output capacitor voltage of the LLCSR through the step in the input reference current – $I_{REF}(s)$. In this manner, the equivalent system can be controlled by only one PI voltage controller.
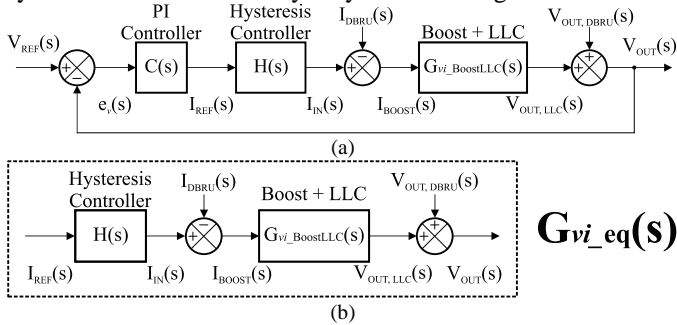
Fig. 6. Block diagrams of the equivalent system (a) TPHR-HVDC-MEA converter operating in closed loop and (b) the open loop equivalent system, represented by G*vi_eq*(s).
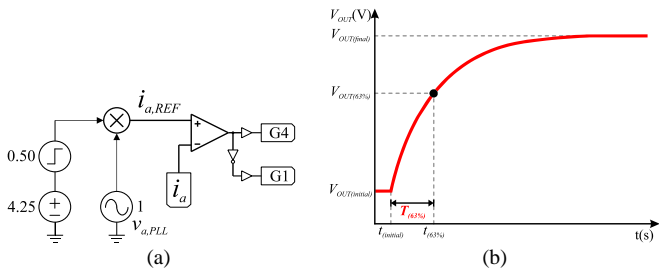
Fig. 7. Current controller used in the transient test response.
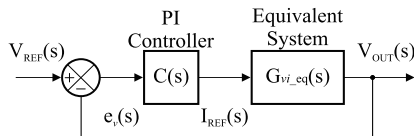
Fig. 8. Equivalent diagram of the closed Loop TPHR-HVDC-MEA converter system.

As mentioned previously, the methodology described by Fig. 7 can be performed via computer simulation, although for the TPHR-HVDC-MEA, the test was practical and adapted the inaccuracies and parasitic components that were not considered during simulation analysis. Therefore, the function *Gvi_eq(s)* is given by (18) and it was found substituting (15) and (16) into (16). It's interesting to note that this equation leads to the evidence of a LPF behavior described before.

$$G_{vi\_eq}(s) = \frac{458.5}{s+9.92} \quad (18)$$

After obtaining the equivalent system transfer function and with the help of the *Matlab Simulink Tool*, the PI controller is designed according to (19). The control objective adopts a conservative design assumption with a phase margin of 78.7º and a bandwidth of 11.5Hz. Fig. 9 shows the Bode diagram and Fig. 10 shows the Root Locus for the open loop compensated system [37]. The step response for the closed loop compensated system showed an overshoot of 8% and a settling time of 114ms, as shown in Fig. 11.

$$C(s) = K_{PI} \times \left(\frac{sT_{PI}+1}{sT_{PI}}\right) \quad (19)$$

Where:
$K_{PI} = 0.15$, is the PI gain.
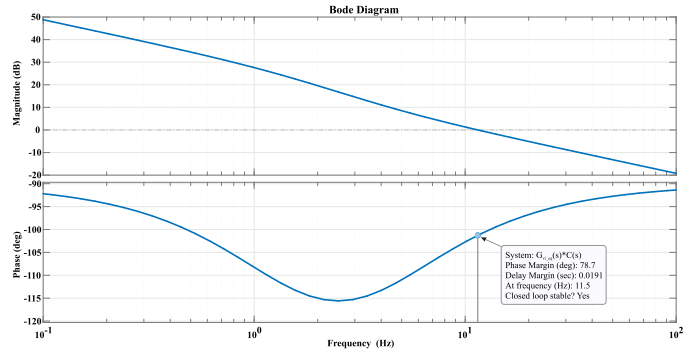$T_{PI} = 0.025$, is the time constant of the PI.

Fig. 9. Bode Diagram of the open loop compensated equivalent system.
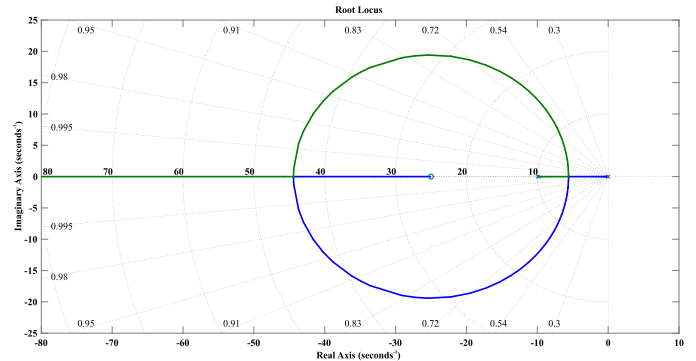

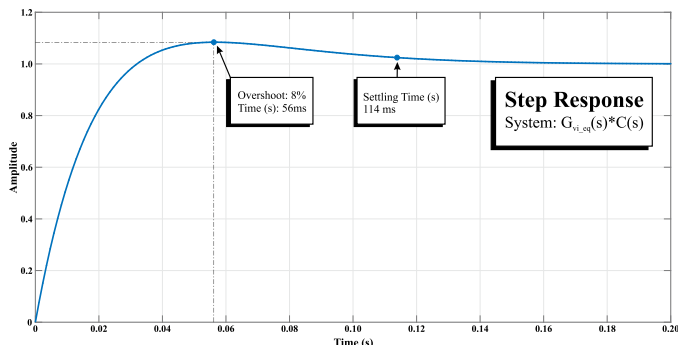Fig. 10. Root Locus of the open loop compensated equivalent system.

Fig. 11. Response to the unit step of the closed loop compensated equivalent system.

V. RESULTS AND DISCUSSION

In order to validate the theoretical analysis about the power structure and the control of the proposed TPHR-HVDC-MEA, a prototype 1.2kW was developed and analyzed in the laboratory, as illustrated in Fig. 12. The converter assembled, along with a module comprising the DSP and a fully electric isolated signal conditioning system (Texas Instruments AMC3330 for voltage and for current Aceinna MCA1101-5-3). The current sensor has a bandwidth of 1.5 MHz and for proper operation of the hysteresis controller, it needs to have at least the same sampling frequency of the current controller – 400 kHz in this case. It is necessary to consider that even if the converter is not isolated from the AC grid, the use of isolated sensors assist in noise immunity, in addition to protecting the entire digital control system interconnected in the aircraft and its operators [38]. Table I summarizes the specifications of the implemented prototype.

In Figs. 13(a) and (b), the current composition at the input of the TPHR-HVDC-MEA is shown. From the slow reverse recovery characteristic of the DBRU, GRAETZ bridge, it is important to emphasize the importance of the bandwidth for the hysteresis controller. The input line current follow the sinusoidal reference imposed by the controller and the bidirectionality of the Boost converter allows a perfect sinusoidal current imposition. It can be observed that the period in which the Boost current ($i_{Boost(a)}$) assumes negative values, it compensates the period in which the DBRU current ($i_{DBRU(a)}$) assumes values greater than the line current (i_a), assisting the imposition of a perfectly sinusoidal current at the input of the converter.

Fig. 14 shows the PRS algorithm execution with the voltage blocking on the switches Q1 and Q4. During the interval where the phase voltage is around the maximum value, the input line current is not directly controlled by the respective phase, e.g. phase A. It is noted that the displacement angle between v_a and i_a is nearly zero, corroborated by the SOGI-PLL reference. Fig 15(a) and (b) shows the three input currents for 400Hz and 800Hz at rated power.

Figs. 16(a) and (b) show the average levels of output voltages of the DBRU, Boost and the output bus. According to (10)-(11), the power processing for the DBRU confirms the robustness of the TPHR-HVDC-MEA and little changes for 400Hz and 800Hz operation, with 48.7% and 48.1% of rated power being processed by an ordinary three-phase DBRU, respectively.
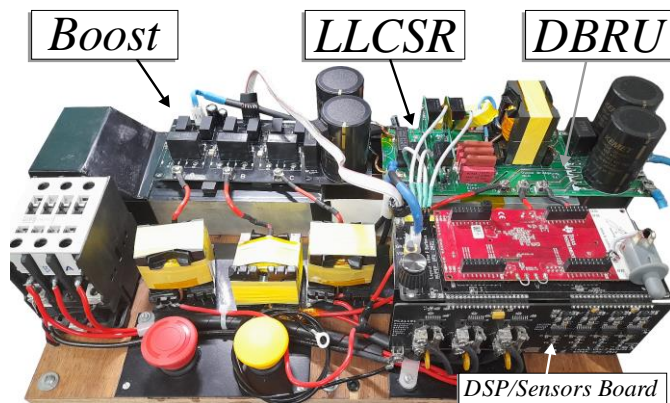

Fig. 12. Picture of the 1.2kW TPHR-HVDC-MEA prototype.

TABLE I
PARAMETER SPECIFICATIONS OF THE TPHR-HVDC-MEA

Specification	Value
Supply voltage/frequency	115V / 400Hz-800Hz
Output DC-bus	540V
Rated output power	1200W
Efficiency	97% / 400Hz
THDi	3.9% / 400Hz
Diode Bridge Rectifier Unit	
Processed power ratio	48.7% / 400Hz
Graetz bridge	DMA40U1800GU (40A/1800V)
L_{DBRU}	500uH
C1	1mF/450V
Boost	
Processed power ratio	51.3% / 400Hz
Maximum switching frequency	200kHz
Q1-Q6	C3M0120065K (120mΩ/650V)
L_{BOOST}	1mH
C_{BOOST}	500uF/900V
LLC Series Resonant	
Processed power ratio	51.3% / 400Hz
Switching frequency	200kHz
Q7-Q10	C3M0045065K (45mΩ/650V)
Cr	56nF
Ld	12uH
Lm	220uH
Np:Ns1:Ns2	29:19:19
Transformer core / material	PQ50-50 / N87
Litz wire (parallel AWG38)	N_p: (84) / $N_{s1,2}$: (70)
D1,D2	C4D15120D (15A/1200V)
C2	1mF/450V

The choice for center tapped transformer configuration for the implementation of the LLCSR converter reflects on the asymmetry of the resonant current. A two winding transformer configuration would make L_d more symmetrical, but there would be more conduction losses if four diodes were used. Fig. 17(a) shows the zero voltage switching (ZVS) on switch Q7 and operation at approximately 200kHz switching frequency. The voltage gain is visualized in Fig. 17(b), the relation between the mean measurements shows a value close to the turns ratio of the high frequency transformer for 400Hz.

To corroborate the proposed control strategy design, the assay established in Fig. 18 shows the output voltage dynamics through a step in the current reference on all phases, from 4.25A to 4.75A. It is possible to notice the behavior similar to first
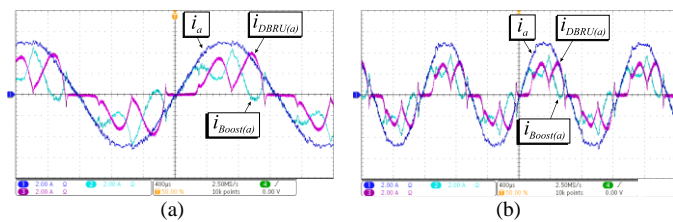
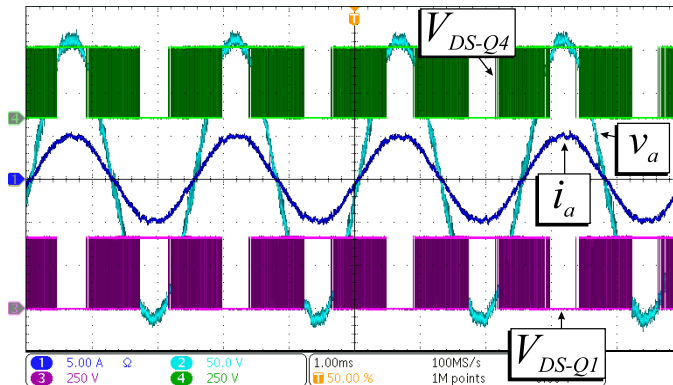Fig. 13. Input line current composition for (a) 400Hz and (b) 800Hz.

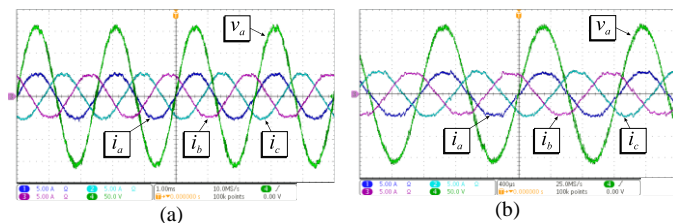Fig. 14. Active pulse reduction by 120º for phase A.

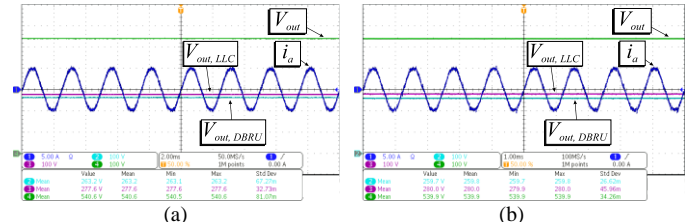Fig. 15. Line currents and phase A voltage for (a) 400Hz and (b) 800Hz.

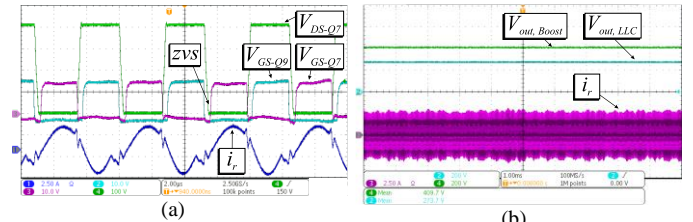Fig. 16. Voltage ratio at the TPHR-HVDC-MEA output for (a) 400Hz and (b) 800Hz.

Fig. 17. (a) LLCSR converter operation in resonance and (b) steady state voltage gain M.
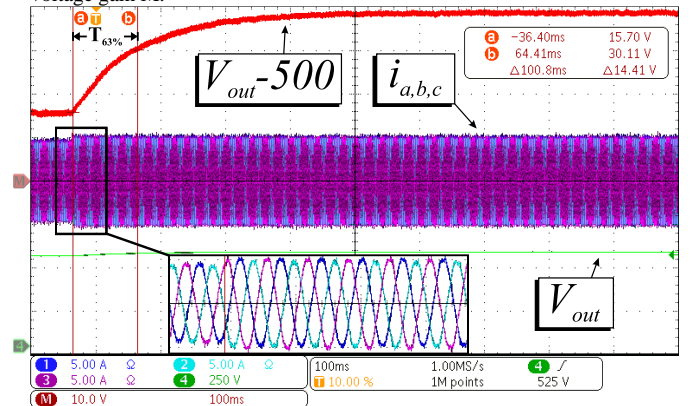

Fig. 18. Current reference step and output voltage response.
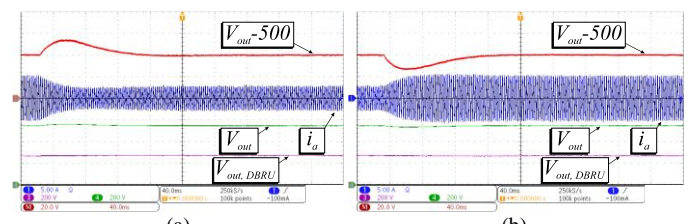

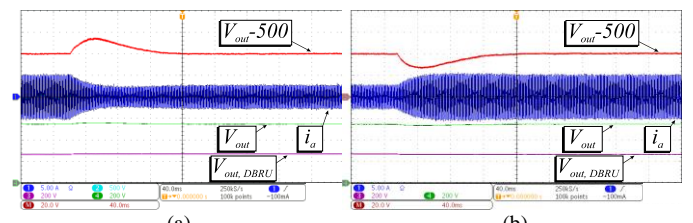Fig. 19. Load step at 400Hz from (a) 100% to 50% and (b) 50% to 100% of rated power.

Fig. 20. Load step at 800Hz from (a) 100% to 50% and (b) 50% to 100% of rated power.

order systems, where the interval that the response reaches 63% ($T_{63\%}$) is 100.8 ms, as expected.

Tests with load variations were performed from 50% to 100% of rated power and for both supply frequencies. Voltage control followed conservative criteria of overshoot below 3% and settling time of 56ms for 400Hz. Tests at 800Hz showed transient characteristics similar to those at 400Hz. By Figs. 19 and 20 it is noted that the voltage at the output of the DBRU suffers little variation due to the typical characteristic found in passive converters.

Analysing Fig. 21, the SOGI-PLL filter response proved to be effective, both in the pulse reduction technique and for the phase error, by ramping the frequency from 400Hz to 800Hz in 200ms.

Fig. 22 shows the performance parameters of the TPHR-HVDC-MEA, the converter reaches 96.9% efficiency at 400Hz with a THDi of 3.91%.

Figs. 23 and 24 show the harmonic spectrum for 400Hz and 800Hz respectively. The THDi levels satisfy the DO-160F standard, however, the use of the PRS contributes to the low order harmonic level by increasing the THDi slightly.

The efficiency of the TPHR-HVDC-MEA without the PRS is 96.7% for a THDi of 2.53%. This difference is due to the fact that the MOSFET used is optimized for high frequency operation. For higher power conditions, the efficiency disparity, with and without PRS can be considerable.
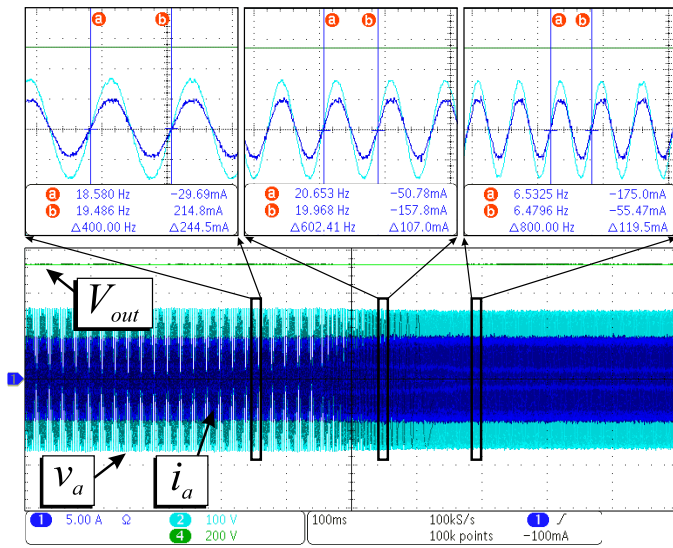
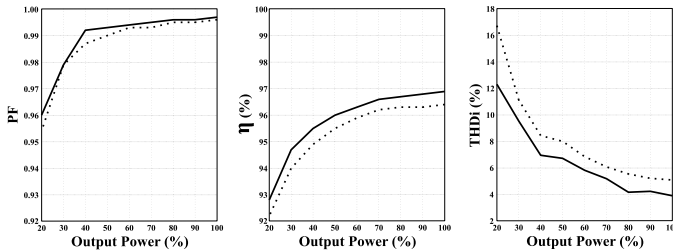Fig. 21. Transient frequency test from 400Hz to 800Hz supply.

Fig. 22. From the left to the right: PF, efficiency, THDi curves as a function of load power, obtained with YOKOGAWA WT230 (full line 400Hz, dashed 800Hz).
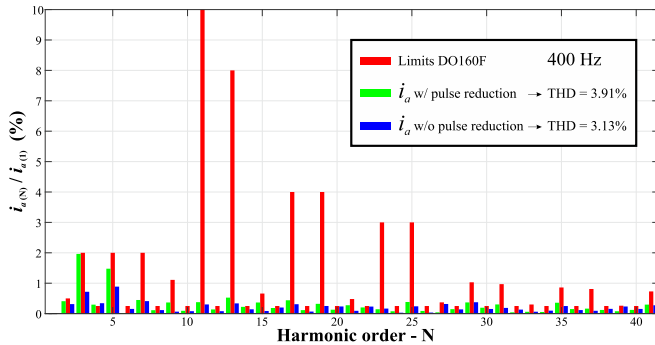

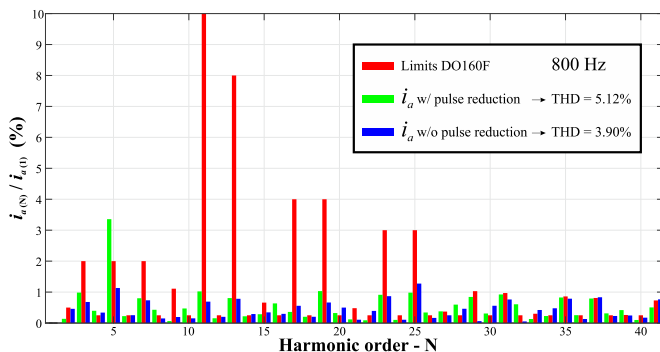Fig. 23. Harmonic spectrum for 400Hz with and without pulse reduction strategy.

Fig. 24. Harmonic spectrum for 800Hz with and without pulse reduction strategy.

Finally, to illustrate the performance of the proposed converter in terms of efficiency, a new experimental test was performed to obtain efficiency results from each converter that makes up the TPHR-HVDC-MEA. The power contribution of each converter was maintained as desired, that is, 48% for the DBRU and 52% for the Boost+LLCSR. Therefore, THDi was kept around 5% as desired. Analyzing the results presented in Fig. 25, one can observe that the DBRU has efficiency results between 98-99% for a wide range of load variation (20% to 100%), as expected. The deployment of the PRS technique was very effective for the Boost+LLSCR at full load, where switching losses on the Boost converter is dominant for the deployed SiC MOSFET and efficiency above 92% from 40% of rated power is assured for both AC grid frequency operation (400Hz and 800Hz). Therefore, analyzing the efficiency results presented in Fig. 25, it can be concluded that the DBRU parallel association with Boost+LLCSR promotes a significant improvement as the TPHR-HVDC-MEA operates with efficiency above 94% from 25%-30% of rated power, ensuring greater robustness and reliability, as well as suppressing the disadvantage of the LLCSR efficiency at low load mentioned previously.
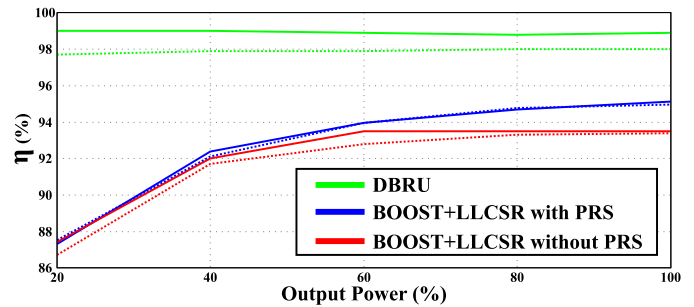

Fig. 25. Separated efficiency measurements for DBRU and Boost+LLCSR cascaded converters with and without PRS technique (full line 400Hz, dashed line 800Hz).

VI. CONCLUSIONS

In this work, a new converter of the HR family for applications in HVDC (540V) was presented. It is denominated as Three-Phase Hybrid Rectifier with HVDC output bus for MEA applications TPHR-HVDC-MEA. The entire power structure and control methodology – executed in a multi-core DSP – was designed in order to corroborate the choice of optimized LLC Series Resonant converter with fixed frequency operation.

The TPHR-HVDC-MEA converter was implemented with a simplified control stratregy based on a single voltage controller and reduced number of sensors, wich can increase the reliability since less variables/signals/information are needed to assure the desired performance.

With the series DC-link voltage compesantion technique, it is possible to assure that the DBRU process about 50% of the rated power. This operational characteristic not only improves the reliability and efficiency of the proposed RU, but also reduces voltage and current stresses on the switches of the

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Boost+LLCSR converter, which reduces termal stress and the size of heat sink.

The converter presented good performance, including reduced overshoot for load steps and perfect voltage and current synchronization during supply frequency variation (from 400Hz to 800Hz). Additionally, at rated power, the THDi met the DO-160F standard with 3.9% and 97% efficiency. All this results make the TPHR-HVDC-MEA a promising candidate for application in DC distribution system for MEA, as well as for On-board microgrids.

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