


Letters

DC Voltage Stability Analysis and Enhancement for Grid-Forming-Based MTDC Systems

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Abstract—This letter first identifies a new mode of low-frequency harmonic instability when combining grid-forming control with the typical dc voltage droop control necessitated in multiterminal high voltage direct-current transmissions. This mode does not exist when grid-following control is applied and its mechanism is explicitly revealed by the dc-side input admittance modeling of the converter. Then, a phase compensator plus a virtual power system stabilizer are introduced to pacify the input admittance within the critical frequency range and derisk the related instability. Last, it is also demonstrated that the proposed control strategy achieves excellent performance in contingent active power imbalance ride-through in the dc system. All the analyses are verified by electro-magnetic-transient simulations with a modular multilevel converter model comprising 278 submodules per arm.

Index Terms—DC voltage droop (DVD), grid-forming, harmonic instability, MMC, multiterminal high voltage direct-current (MTDC), phase compensator, virtual power system stabilizer (VPSS).

I. INTRODUCTION

GRID-FORMING control (GFMC) is considered essential for the stability of future inverter-based resources (IBRs) dominated power systems [1]. Meanwhile, construction and expansion of multiterminal high-voltage dc (MTDC) grid is taking place in Europe due to its enhancement of flexibility, reliability, and resilience in multiarea interconnections. Although GFMC has been broadly studied in the literature in IBR applications, very few works have focused on its applications in MTDC systems. In general, the unique challenges in MTDC operation (no dc storage assumed) can be summarized as follows.

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- 1) Given that the popular choice of converter topology is MMC, there is very limited capacitive energy stored in the dc system.
- 2) An automatic power sharing control between different stations is needed, which is typically realized by dc voltage droop (DVD) control.
- 3) It is required to redistribute the active power reliably after a contingency of active power imbalance (e.g., triggered by a converter outage) while keeping the dc voltage within operational limits (typically $\pm 10\%$).

These unique features of MTDC systems necessitate aggressive droop gains to translate a small dc voltage deviation into a large ac power reference modification. (e.g., 1 p.u. dc voltage variation corresponds to 5–10 p.u. ac power variation [2]). As pointed out in this letter, such a range of droop gains though functions well with grid-following control (GFLC) [2], can interact with the typical GFMC and induce low-frequency (LF) harmonic instability, which could become a major obstacle in the vast adaption of GFMC in MTDC grids. It should be noted that such LF instability is triggered by small-signal voltage disturbances at steady-state rather than frequency events caused by large ac transients. It is therefore fundamentally different than the LF oscillations studied in [3].

To resolve this problem, a simple phase compensator (PCom) and a virtual power system stabilizer (VPSS) are introduced in this letter, which not only pacify the converter dc admittance within the critical frequency range and avoid LF harmonic instability, but also deliver excellent transient performance in contingency ride-through. The proposed control is verified in EMPT-rv simulations with an MMC model with circulating current suppression control (CCSC).

II. UNDERSTUDIED SYSTEM AND DC INPUT ADMITTANCE MODELING

The MTDC grid under study is shown in Fig. 1 with monopolar configuration in the MMC stations. The GFMC within each station implemented as in Fig. 2, which mainly comprises of three blocks, namely, the active power control (APC), which consists of a virtual synchronous machine (VSM) plus a phase-lock-loop (PLL), the ac voltage control (AVC) with constant

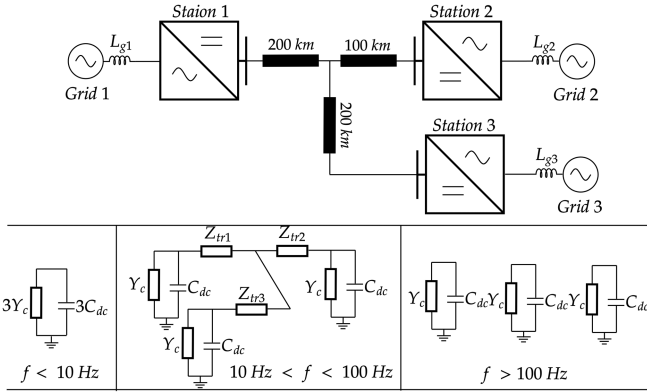


Fig. 1. Understudied 3-terminal monopolar MTDC grid and its simplified equivalent circuits in different frequency ranges. $Z_{tr1,2,3}$ represent the DC network impedances between stations including both DC cables and DCRs.

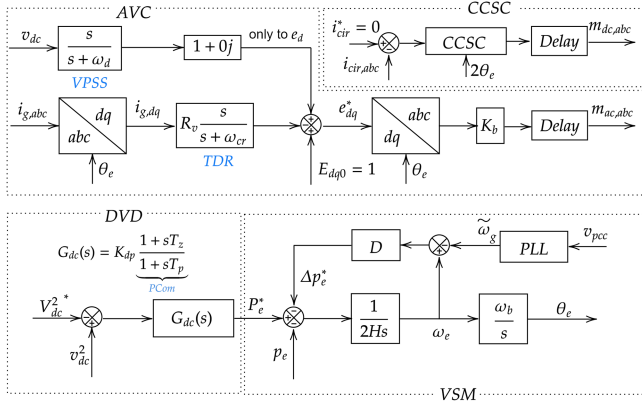


Fig. 2. Overall structure of the GFMC adopted in this letter.

voltage magnitude modulation plus transient damping resistors and the proposed VPSS, and the DVD which can be a simple droop gain or droop gain in series with the PCom. The PLL is utilized to ensure that APC can follow its reference when the grid frequency deviates from 1 p.u.. Without it, the dc voltage could deviate significantly during frequency events to maintain synchronization, which can violate the tight dc voltage tolerance in MTDC network. It should be noted that the well-known PLL weak-grid instability issues result from its combination with the current source dynamics of GFLC. It does not induce the same issue with the GFMC voltage source dynamics. More detailed analyses on PLL in GFMC will be provided in future work. In addition, this AVC structure is chosen due to its superiority in providing voltage stiffness and enhancing system small-signal stability over that with inner current loops [4]. AC over-current protection during ac faults can be realized via virtual impedance, which is not modeled in this letter because it is not activated in the studied operations.

DC-side Impedance-based modeling (IM) [5] is adopted in this letter to model the harmonic instability. A complete IM of an MMC is complex due to its time-periodic nature and the harmonic coupling between ac and dc internal states [6].

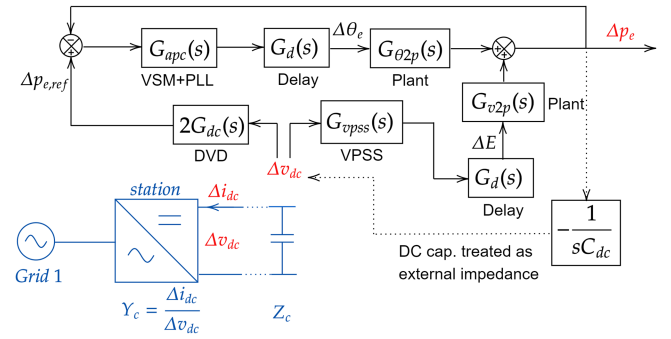


Fig. 3. Signal paths to derive Y_c based on $G_{dp} = \Delta p_e / \Delta v_{dc}$, i.e., the converter active power response Δp_e to DC voltage disturbance Δv_{dc} based on the control structure in Fig. 2 and simplifying the MMC as an equivalent 2-level VSC. The DC capacitors are not included in the modeling of Y_c .

However, this letter demonstrates that if the dc-side current of MMC is not controlled (only CSCC applied), the studies on the LF harmonic instability resulting from the interaction between DVD and the APC in GFMC can be simplified with sufficient accuracy by modeling the MMC as an equivalent two-level voltage source converter (VSC) with its equivalent dc-link capacitance calculated as $C_{dc} = 6C_{sub}/N$ (C_{sub} – sub-module capacitance; N – number of module per arm).

Fig. 3 shows the signal paths of the control structure in Fig. 2, from which $G_{dp} = \Delta p_e / \Delta v_{dc}$ can be derived as in (1), where $G_{\theta2p}$ and G_{v2p} are the full-dynamic plant models of a VSC describing its active power responses to an angle and a voltage magnitude perturbation. Its detailed derivation can be found in [7]. Then, assuming that converter losses are negligible, i.e., $\Delta p_{dc} \approx \Delta p_e$, the response on dc current and subsequently the dc input admittance of the converter is derived in (2), where I_{dc0} and V_{dc0} are the dc current and voltage operating points of the converter. Notice that in the dc admittance modeling processes, the dc capacitor is not included and will be treated as a part of the external dc impedance. The interaction between the converter input admittance and the external dc impedance will determine the harmonic stability

$$G_{dp} = \frac{2G_{dc}G_f + G_{vpss}G_{v2p}G_d}{1 + G_f}, G_f = G_{apc}G_dG_{\theta2p} \quad (1)$$

$$Y_c = \frac{\Delta i_{dc}}{\Delta v_{dc}} = \frac{(\Delta p_e - \Delta v_{dc}I_{dc0})}{\Delta v_{dc}V_{dc0}} = \frac{G_{dp} - I_{dc0}}{V_{dc0}}. \quad (2)$$

III. MODELLING OF THE LF HARMONIC STABILITY

As discussed in [5], the return ratio based on IM is a general way to describe the small-signal stability of converter-converter or converter-network interactions and it is essentially an open loop transfer function (or matrix) of the modeled systems—if the modeled system is single-input-single-output (SISO), its phase and gain margin describe the stability of the interactions. In this analysis, the return ratio $L(s) = Y_c(s)Z_c(s)$ is used to analyze the LF instability by describing the interaction between converter input admittance $Y_c(s)$ and the dc capacitors impedance $Z_c(s)$. In Fig. 4, $Y_c(s)$ derived in (2) is plotted

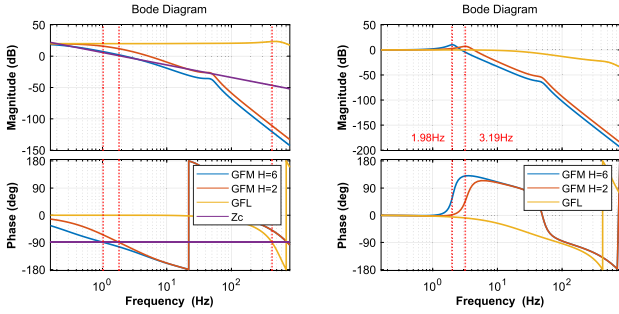


Fig. 4. Converter input admittances obtained with GFMC and GFLC plotted with the DC capacitor impedance, all in p.u. (left) and the closed-loop frequency response of the return ratio, $G_{cl} = \frac{L(s)}{1+L(s)}$ (right). The bode diagram of G_{cl} indicates a right-half-plane (RHP) pole at 1.98 Hz when $H = 6$ and a RHP pole at 3.19 Hz when $H = 2$, which is precisely confirmed by EMT simulations in Fig. 6(a).

together with $Z_c(s)$, from which it can be observed that within the control bandwidth of the APC, power reference is tightly followed and therefore the DVD plus the APC leads to 0° on the input admittance. However, due to the general low-bandwidth low-pass filter (LPF) nature of APC, the phase of the input admittance starts to decrease at very LF and crosses -90° around 1–5 Hz, which plus the -90° of the capacitor impedance leads to $\angle L(s) \leq -180^\circ$. Since the capacitor impedance is considerably large at such LF, $\|L(s)\|$ easily exceeds 1 when $\angle L(s) \leq -180^\circ$ if the droop gain is high (10 p.u. in this case) and thus results in harmonic instability. Further, the input admittance when GFLC is combined with the same droop gain is also compared in Fig. 4, with its ac current loop control bandwidth and phase margin designed to be 350 Hz and 45° , assuming that the MMC control delay is 350 μ s. If the ac power reference is directly divided by the ac voltage magnitude to generate the current references, it would imply that the control bandwidth of APC in this case is also up to 350 Hz, resulting in the phase of the input admittance crossing -90° at much higher frequency (425 Hz), where $\|Z_c(s)\|$ is significantly reduced and therefore $\|L(s)\| \ll 1$ when $\angle L(s) \leq -180^\circ$, namely, the risk of harmonic instability is negligible. Admittedly, it is theoretically possible to drastically reduce the inertia coefficient in GFMC so that $\angle L(s) \leq -180^\circ$ occurs in the same frequency range as with GFLC. However, this would overly diminish the virtual inertia effects demanded by the TSOs [8]. The closed-loop response of $L(s)$ is also plotted in Fig. 4, where right-half-plane (RHP) poles are identified with GFMC, whereas none are found with GFLC. It should be noted that this instability phenomenon is different from the uncontrolled zero-sequence currents in MMC with CCSC [6].

Although only single converter dynamics are captured in the model above, the stability analysis is directly applicable to an MTDC system if all converter stations are identical. Because the studied harmonic instability occurs at such LFs that voltage drop on the total dc inductance between two stations (e.g., 500 mH to 1 H, contributed by cables and dc reactors (DCRs) only amounts to around 0.01–0.06 p.u. dc impedance, whereas it can be seen in

Fig. 4 that the capacitor impedance is in the range of 1 p.u. This implies that within the critical frequency range, the dc network can be treated effectively as 3 dc capacitors in direct parallel with three converter admittances (see Fig. 1). Therefore, the total return ratio of the system is the approximately the same as the single converter, i.e., $L_{MTDC,3}(s) \approx 3Y_c(s)\frac{Z_c(s)}{3} = L(s)$, which is confirmed in EMT simulations in Fig. 6(a).

It can be additionally deduced that if constant energy-based control (EBC) of MMC is used instead of CCSC, the stability would be further deteriorated since the internal capacitors of MMC do not buffer any active power, which further reduces the dc capacitance and increases $\|Z_c(s)\|$ and $\|L(s)\|$.

IV. DC INPUT ADMITTANCE PASSIVITY DESIGN AND EMT SIMULATION RESULTS

Passivity has been introduced as a design guideline to avoid harmonic instability with its main indicator being that the real part of the converter input admittance must be equal or larger than 0. Fig. 5(a) and (b) plots the real part of $Y_c(s)$ without PCom and VPSS. As expected, increasing the droop gain leads to larger negative real parts and higher risks of instability. Further, while reducing inertia may help securing dc voltage during ac transients [9], it could deteriorate the nonpassive behavior and pose risks of harmonic instability. The damping ratio of the VSM is kept the same in all analyses.

Since the negative resistance generally occurs between 1 and 10 Hz as a result of the phase of APC decreasing below -90° , a viable countermeasure would be to lift up the phase within this frequency range by introducing a zero in series with the DVD and the APC reference. Then, a pole is placed to cancel the zero at high frequency to avoid susceptibility to high-frequency noise. Placing the described zero and the pole would result in the well-known PCom popularly used in power supply control, which is also often referred to as lead-lag compensator and assumes a form as indicated in Fig. 2, with T_z and T_p chosen as 0.8 and 3.33×10^{-4} , respectively. With the PCom introduced, it can be seen in Fig. 5(c) that the real parts around 1–10 Hz become positive in strong grid, and hence the harmonic instability within this range is inhibited. EMT simulations in Fig. 6(a) verify this finding by first operating the MTDC stably with the proposed control and then by-passing the PCom at $t = 4$ s, after which the harmonic instability is excited with its frequency matching the IM prediction in Fig. 4. It is also worth pointing out that the PCom has a unity gain at 0 Hz and therefore does not interfere with the steady-state power sharing between stations enforced by DVD. Even though combining Pcom with DVD has been proposed in [10], it serves a completely different purpose of transient gain reduction to mitigate transient dc voltage oscillations when GFLC is used. It is not addressing the same issues and its parameter tuning is also completely different.

However, PCom cannot completely pacify the converter in weak grid and it leads to a new negative resistance region around 10–100 Hz, which could also be detrimental by amplifying the resonances formed by the dc capacitors and the DCRs [see Fig. 6(b)]. To address this problem, the VPSS in Fig. 2 is

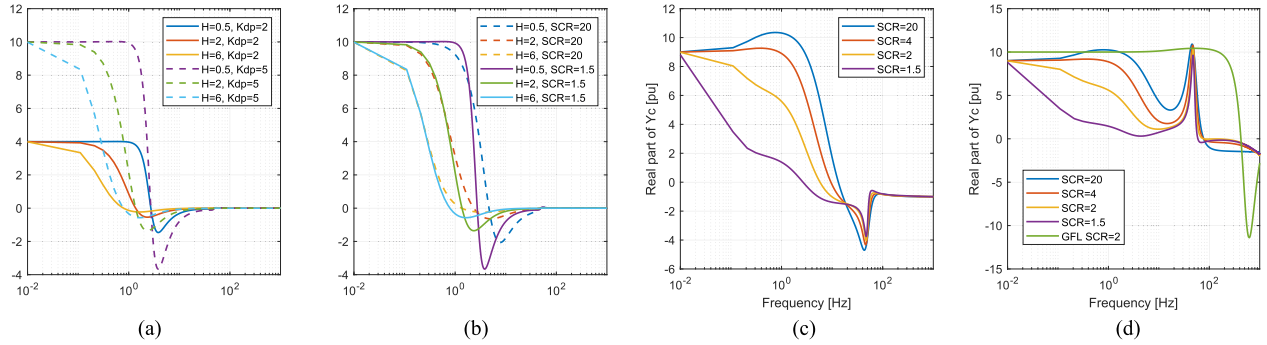


Fig. 5. Real parts of the converter DC input admittance. (a) Increasing the droop gain leads to larger negative real parts and high risks of instability. (b) Reducing the inertia value in VSM does not improve the passivity. (c) Including the PCom pacifies the admittance in the original critical region in strong grid but is inefficient in weak grid and introduces a new nonpassive region at higher frequencies, which can be pacified by the VPSS. (d) Real parts with both PCom and VPSS included at the worst operating point. The converter is passive from DC to around 100 Hz in all grid strength but nonpassive above 100 Hz, with both proposed GFMC and typical GFLC. Nonetheless, it poses little risk of instability due to $\|L(s)\| \ll 1$ above 100 Hz.

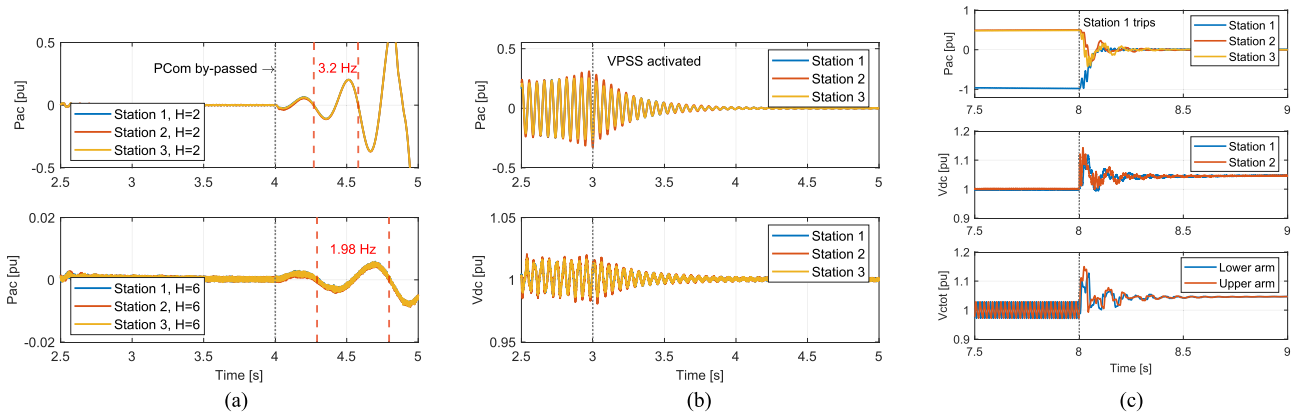


Fig. 6. EMT simulation results obtained with the 3-terminal MTDC in Fig. 1 including MMC models with 278 sub-modules per arm, DCRs and wide-band DC cable models. The droop gain is chosen as 10 p.u. in all cases. (a) PCom is by-passed at $t = 4$ s and LF harmonic instability is excited with its frequency matching precisely the model prediction in Fig. 4. (b) DC network resonance of 18 Hz gets suppressed once VPSS is applied at $t = 3$ s. (c) Contingency ride-through: At $t = 8$ s, the DC breaker around station 1 opens and stations 2 and 3 successfully ride through with the proposed control.

introduced ($\omega_d = 31.4$ rd/s), which essentially imposes a positive dc current response to a positive dc voltage disturbance by increasing the ac voltage magnitude and thereby the active power from dc to ac. Consequently, the input admittance becomes passive from dc to around 100 Hz in all grid strengths, as shown in Fig. 5(d). Traditionally, PSS is used to balance the active power in ac system by modulating the generator internal voltage. Here, VPSS is used to balance the active power in the dc system by modulating the internal voltage of the VSM and thus given the name of VPSS. Its effectiveness is demonstrated in Fig. 6(b).

With both Pcom and VPSS added, as shown in Fig. 5(d), in the frequency range above 100 Hz the converter admittance can still exhibit negative real part due to control delays and the constant power operating points [see (2)]. However, this is not considered problematic since above 100 Hz, the impedance between terminals mainly formed by the DCRs (>500 mH) is generally above 1 p.u., whereas the dc capacitance is below 0.01 p.u., meaning that the converters are isolated from each other on the dc side and only see their own dc capacitor impedance in the return ratio (see Fig. 1), which has a magnitude of far

below 1 above 100 Hz and poses virtually no risks of instability. Admittedly, harmonic instability can still occur above 100 Hz due to internal control and dynamics of the MMC [6], but those are not issues introduced by GFMC and are out of the scope of this letter.

At last, the proposed control is tested for contingency ride-through by first operating Station 1 in rectifying mode at 1 p.u. active power and Station 2 and 3 in inverter mode at 0.5 p.u. active power and then opening the breaker of Station 1 at $t = 8$ s. Fig. 6(c) demonstrates a successful ride-through of Station 2 and 3.

V. CONCLUSION

A new phenomenon of LF frequency harmonic instability is identified in the letter for grid-forming-based MTDC systems. The proposed control with PCom and VPSS not only successfully resolves this issue but also provides excellent performance in contingency ride-through.

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