# A Systematic Method for Studying the Use of DC/DC Converters With Three Discontinuous Conduction Modes as Automatic PFCs

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***Abstract*—This article describes a general method for studying the behavior of converters with three discontinuous conduction modes as automatic power factor correctors (PFCs). Some converters with a single discontinuous conduction mode (such as Buck-Boost, Flyback, SEPIC, Ćuk, and Zeta converters) can behave as automatic PFCs when operating in that discontinuous conduction mode, with a nearly constant duty cycle during each cycle of the line voltage. There are also dc/dc converters that, due to multiple diodes and inductors, can operate in different discontinuous conduction modes. A systematic method for studying these three discontinuous conduction modes was recently presented. This article extends that method to using the aforementioned dc/dc converters as part of an ac/dc converter with low harmonic injection in the line, identifying when the converters behave as "ideal automatic resistor emulators" (i.e., configuring ideal automatic PFCs) and when they behave as "quasi-ideal automatic resistor emulators" (i.e., as quasi-ideal automatic PFCs). As an example, the article examines a SEPIC converter used as a resistor emulator. In this case, three discontinuous conduction modes are possible, if the inductance of the input inductor is low enough to allow the input bridge rectifier diodes to stop conducting when the transistor is OFF. The study allows us to determine of the line current waveform when the converter operates in any of the possible discontinuous conduction modes. The results show that quasi-ideal automatic PFC behavior can be achieved in discontinuous conduction modes with low inductance values. Moreover, the results for the SEPIC can be easily extended to the Ćuk converter operating in the same manner. Finally, the theoretical predictions for the line current from the proposed study were verified through simulation using PSIM (in the case of both the SEPIC and Ćuk topologies), and through experimentation (in the case of SEPIC).**

***Index Terms*—Conduction modes in dc/dc converters, power factor correctors (PFCs), resistor emulators (REs), SEPIC and Ćuk converters.**

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## I. Introduction

POWER factor correctors (PFCs) are circuits in charge of ensuring low line distortion in single-phase ac/dc converters. Active PFCs use a dc/dc converter with a nonlimited dc conversion ratio placed between the line rectifier and the capacitor that stores energy during half-periods of the line voltage. This converter must operate as a resistor emulator (RE), meaning that it exhibits a resistive input impedance in such a way that the load seen by the line rectifier appears to be a resistor. The value of this resistor must match the power demanded by the converter from the line. There are two main ways to achieve this behavior (Fig. 1). They are as follows.

1) Providing the converter with an input current feedback loop that ensures that the input current is proportional to the input voltage. This requires adjusting the proportionality constant that determines the RE's input resistance, depending on the power demanded from the line. This is achieved using an analog multiplier that modulates the amplitude of the waveform used as reference for the current loop [1], [2]. As Fig. 1(a) shows, this multiplier has two input signals: 1) a waveform proportional to the input voltage (and, therefore, variable over time); and 2) a signal that must remain almost constant each line period. As this signal comes from the output-voltage feedback loop, this loop must be slow enough to exhibit this behavior. This type of control can be used in any converter conduction mode, the only condition being that the converter dc conversion ratio must be nonlimited.
2) Implementing a very simple control that maintains a constant duty cycle in each line period, while operating in a special mode that achieves the desired proportionality between the input voltage and the input current [see Fig. 1(b)]. This behavior can be achieved when the dc/dc converter operates in discontinuous conduction mode (DCM) [3], [4], [5], [6], [7], [8] or when it is a resonant converter operating at a specific operation point [9]. As in the previous control, the dc/dc converter must also exhibit an unlimited dc conversion ratio. Although this control mode offers the advantage of extreme simplicity, it does have a drawback: these modes increase the current stress on some semiconductors. Despite this drawback,

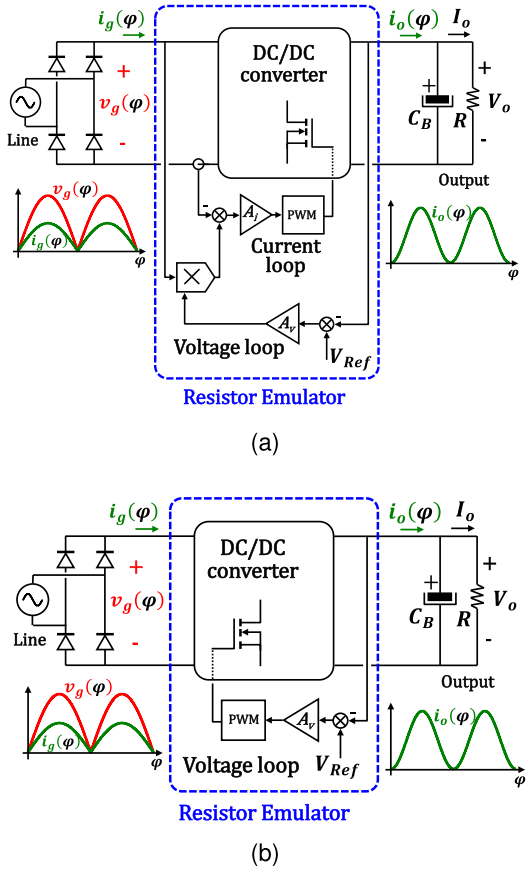


Fig. 1. Implementations of active PFCs based on the use of DC/DC converters working as RE: (a) Control based on the use of an analog multiplier. (b) Control when the DC/DC works as an automatic RE.

this is an attractive control strategy for low-power and low-cost applications. The single-phase ac/dc converters that implement this control are called automatic PFCs in this article.

As noted above, using some dc/dc converters operating in DCM allows us to build automatic PFCs. Therefore it is very important to determine when a converter operates in this mode.

In conventional dc/dc converters with a single diode, there are only two possible conduction modes: 1) the aforementioned DCM; and 2) continuous conduction mode (CCM). The boundary between these two modes is well known [10]. The extension of this study to converters that behave as REs was found in [11]. That study also focused on converters with only one diode and therefore with only one DCM.

On the other hand, some dc/dc converters with several diodes can exhibit several DCMs. A general method for studying these converters was presented in [12]. That paper examined the use of a Versatile Buck-Boost converter. This same method was applied in [13] to address the case of SEPIC and Ćuk converters with an additional diode in series with their input inductors. In all of these cases (Versatile Buck-Boost and the modified versions of the SEPIC and Ćuk converters) three DCMs are possible, and their main characteristics were correctly identified and verified in both papers. It should be noted that in all these cases, the converters operated as conventional dc/dc converters, and their operation as REs in an ac/dc converter has so far not been addressed.

Some dc/dc converters with only one diode (and, therefore, only one DCM) can be designed to always operate in DCM, even when they are used as an RE in an ac/dc converter [11]. In the case of the Buck-Boost, Flyback [4], SEPIC [5], Ćuk [6], and Zeta [8] converters, designing them to always operate in DCM allows these converters to be used as ideal automatic REs. This is because they exhibit proportionality between the line current (averaged in a switching period) and the input voltage if the converter duty cycle remains constant each line period. Thus, very simple REs can be implemented using those topologies always operating in DCM.

However, the situation is very different for converters with several DCMs, including implementations of SEPIC and Ćuk converters with low inductance values. In this case, the first question to answer is whether the converter can be designed to always operate in one of the DCMs (or in several of them) when it is working as part of an ac/dc converter. As Fig. 1(b) shows, the converter will be placed in between a line rectifier (which means full-wave rectified sinusoidal input voltage) and a bulk capacitor (which means constant output voltage), and its duty cycle will be kept constant each line period, thus implementing an RE. If the converter can be designed to always operate in one or several DCMs in these conditions, the next question to answer is the state of the line current. If it is a perfect sinusoid, then the final converter will work as an ideal automatic PFC. On the other hand, if the line current exhibits some distortion, then the final converter will work as a quasi-ideal automatic PFC. Moreover, if the distortion is high enough, using the converter as an automatic RE will not be possible. It should be noted that these remain open questions. The main objective of the present article is to propose a systematic method that will allow these questions to be answered.

In summary, the main objective of this article is to provide a general method to evaluate the performance of any dc/dc converter with multiple DCMs as a potential automatic RE in an ac/dc power conversion scheme, as the one given in Fig. 1(b). The interest in studying the case of multiple DCMs is for two main reasons as follows.

1) Operation in DCMs is always associated with low inductor values, which in general means a smaller converter size for a given switching frequency.
2) As Fig. 1(b) shows, the control scheme for an automatic RE is very simple. However, the line current waveform corresponding to operate following a given sequence of DCMs has not yet been addressed. The quality of the line current waveform obtained following the proposed method determines whether the converter can work as an ideal or quasi-ideal automatic RE, or must be discounted as an automatic RE.

The rest of this article is organized as follows. Section II provides a brief review of three important issues: 1) the study of the conduction mode boundaries in dc/dc converters with only one DCM that are operating as conventional dc/dc converters; 2) the study of the conduction mode boundaries in dc/dc converters with only one DCM that are operating as PFCs; and 3) the study

of the conduction modes of dc/dc converters with three DCMs that are operating as conventional dc/dc converters. Section III proposes a general method for studying the conduction modes of dc/dc converters with three DCMs that are operating as PFCs, which is the main objective of the article. Section IV provides example cases where the proposed method is applied to several implementations of PFCs based on SEPIC and Ćuk topologies, designed with low enough values of input inductance to generate three DCMs. Section V describes verification of the predicted operation modes and of the line current waveforms, using simulation and an experimental prototype of the SEPIC converter. Finally, Section VI concludes this article.

## II. Review of Conduction Mode Boundaries

This section presents a brief review of the study of the boundaries between conduction modes in dc/dc converters. Three different situations are considered as follows.

1) DC/DC converters with only one diode (and therefore only one DCM) working as conventional dc/dc converters (i.e., with constant output voltage, input voltage changing in quite a limited range of variation, and controlled by fast changing the converter duty cycle when the input voltage and/or the load change).
2) Converters with only one diode (and therefore only one DCM) working as ideal REs [11] (i.e., with constant output voltage, input voltage continuously changing from zero to the peak value of the line voltage, and controlled in such a way that the input current is proportional to the input voltage). The two main implementations for achieving this behavior are shown in Fig. 1.
3) Converters with two diodes that remain in inductive branches when the transistor is OFF (and therefore converters with three DCMs), working as conventional dc/dc converters [12], [13] (i.e., as in the first case, constant output voltage, limited input voltage variation, and fast duty cycle variation characterize their operation).

### A. DC/DC Converters With Only One DCM Working as Conventional DC/DC Converters

Conventional dc/dc converters with only one diode have only two possible conduction modes: 1) DCM; and 2) CCM. The boundary between these two modes is well-known [10]. First, the dimensionless conduction parameter $k$ is defined:

$$k(R) = \frac{2L}{RT_s} \tag{1}$$

where $L$ is the value of the inductance of the converter inductor, $R$ is the load resistance, and $T_s$ is the switching period. The critical value of $k$ that defines the boundary between CCM and DCM in closed-loop, $k_{crit\_cl}$, is a function of the ratio $M$, which is the dc conversion, defined as $M = V_o/V_g$. The converter operates in CCM when

$$k(R) > k_{crit\_cl}(M) \tag{2}$$

and in the DCM when

$$k(R) < k_{crit\_cl}(M). \tag{3}$$

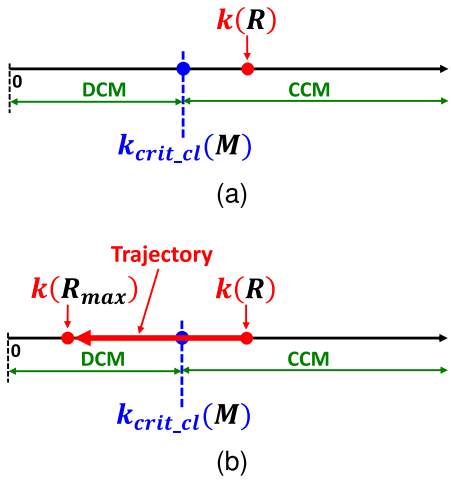


Fig. 2. Graphical determination of the conduction mode: (a) Converter operating in the CCM. (b) Change of conduction mode when load resistance $R$ increases up to $R_{\max}$.

The conduction mode can be easily analyzed by placing the values of $k$ and $k_{crit\_cl}$ on a straight line, as shown in Fig. 2(a). When the load value changes, then the value of parameter $k$ also changes, as shown in Fig. 2(b), and the conduction mode can change.

### B. DC/DC Converters With Only One DCM Working as Resistor Emulators

The extremely simple method described in the previous subsection was proposed for converters operating as conventional dc/dc converters. Expanding that study to converters that behave as REs was reported in [11]. That study also focused on converters with only one diode and consequently, only one DCM.

The key for that study is that both the converter dc conversion ratio and the load seen by the converter are not constant in this case (although $R$ is constant), but instead continuously and synchronously change according to the line angle $\varphi$ [11]. The variation of the dc conversion ratio with $\varphi$ allows us to redefine it as $m(M_{\pi/2}, \varphi)$

$$m(M_{\pi/2}, \varphi) = \frac{V_o}{v_g(\varphi)} = \frac{V_o}{V_g|\sin(\varphi)|} = \frac{M_{\pi/2}}{|\sin(\varphi)|} \tag{4}$$

where $M_{\pi/2}$ is the value of the converter dc conversion ratio at the peak value of the line voltage, $V_g$

$$M_{\pi/2} = \frac{V_o}{V_g}. \tag{5}$$

If the converter operates as an ideal RE due to a control scheme such as in Fig. 1(a), then its input current can be expressed as

$$i_g(\varphi) = I_g|\sin(\varphi)| \tag{6}$$

where $I_g$ is the peak value of the RE input current for a certain load value $R$. The power balance between the converter input and output ports for each line angle yields

$$V_g I_g \sin^2(\varphi) = V_o i_o(\varphi). \tag{7}$$

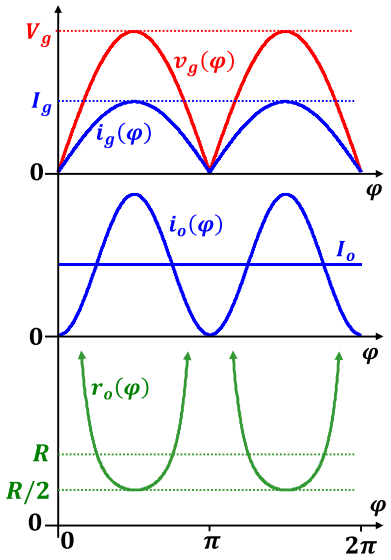


Fig. 3. Main quantities involved in the operation of an RE.

In (7), $i_o(\varphi)$ is the current injected by the dc/dc converter into the parallel circuit made up of the bulk capacitor $C_B$ (designed to filter the current component of twice the line frequency) and the load resistor $R$. It should be noted that bulk capacitor $C_B$ is large enough to ensure that voltage $V_o$ remains constant in spite of the double-line frequency instantaneous power mismatch. Averaging the converter input and output power over one line half-cycle and equalizing both values produces the average value of $i_o(\varphi)$, defined as $I_o$

$$I_o = \frac{V_g I_g}{2V_o} = \frac{I_g}{2M_{\pi/2}}. \tag{8}$$

Therefore, (6) and (7) can be expressed as

$$i_g(M_{\pi/2}, R, \varphi) = 2I_o M_{\pi/2} |\sin(\varphi)|, \tag{9}$$

$$i_o(R, \varphi) = 2I_o \sin^2(\varphi) = 2\frac{V_o}{R}\sin^2(\varphi). \tag{10}$$

Using (10), the load that the dc/dc converter sees before the capacitor $C_B$ can be defined as follows:

$$r(R, \varphi) = \frac{V_o}{i_o(\varphi)} = \frac{R}{2\sin^2(\varphi)}. \tag{11}$$

The main quantities involved in the operation of an RE are shown in Fig. 3.

As the load seen by the converter changes according to line angle $\varphi$, then parameter $k$ also changes according to $\varphi$. Therefore, $k$ can be redefined as follows:

$$k(R, \varphi) = \frac{2L}{r(\varphi)T_s} = \frac{4L}{RT_s}\sin^2(\varphi). \tag{12}$$

The conduction mode of an RE with only one DCM will be the CCM for the values of $\varphi$ and $R$ that satisfy

$$k(R, \varphi) > k_{crit\_cl}(m(M_{\pi/2}, \varphi)). \tag{13}$$

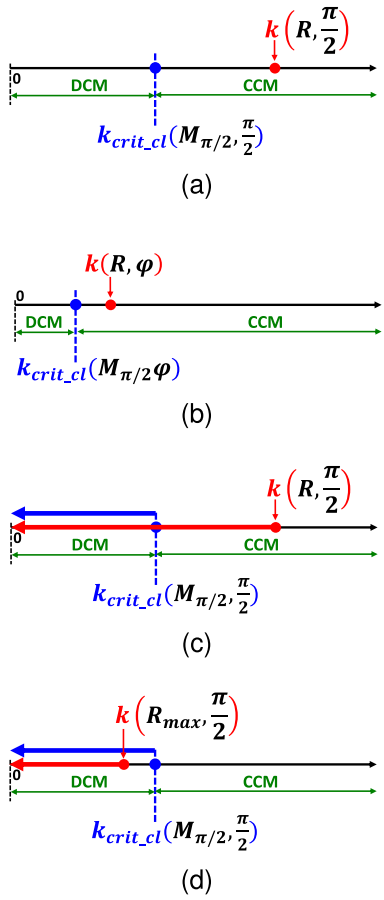


Fig. 4. Graphical evolution of the conduction mode of a converter with only one DCM when it is working as ideal RE: (a) Situation corresponding to operate in the CCM when $\varphi = \pi/2$. (b) Situation corresponding to operate in the CCM when $0 < \varphi < \pi/2$. (c) Movement of $k(R, \varphi)$ and $k_{crit\_cl}(M_{\pi/2}, \varphi)$ when $0 \leq \varphi \leq \pi/2$. (d) Change of conduction mode when load resistance $R$ increases up to $R_{\max}$.

For the sake of simplicity, this inequality can be rewritten as follows:

$$k(R, \varphi) > k_{crit\_cl}(M_{\pi/2}, \varphi). \tag{14}$$

Conversely, the conduction mode of the RE with only one DCM will be the DCM for the values of $\varphi$ that satisfy:

$$k(R, \varphi) < k_{crit\_cl}(M_{\pi/2}, \varphi). \tag{15}$$

As a result of these inequalities, an RE with a single diode that supplies power to a certain load $R$ can operate in the following three possible modes.

1) Always in the CCM, if (14) is satisfied for the entire range of $\varphi$.
2) Always in the DCM, if (15) is satisfied for the entire range of $\varphi$.
3) Partially in CCM and DCM, if (14) is satisfied for values of $\varphi$ around the peak value of the line voltage and, conversely, (15) is satisfied for values of $\varphi$ around the zero-crossing of this voltage.

Of course, this situation can change when the load $R$ changes.

Fig. 4(a) shows the relative situation of $k(R, \varphi)$ and $k_{crit\_cl}(M_{\pi/2}, \varphi)$ when the converter has been designed to

TABLE I
POSSIBLE CONDUCTION MODES

| $D_1$ | $D_2$ | Conduction mode | Region name |
|---|---|---|---|
| 1 | 1 | CCM | CCM |
| 1 | 0 | DCM | DCM1 |
| 0 | 1 | DCM | DCM2 |
| 0 | 0 | DCM | DCM3 |

operate in CCM. In Fig. 4(b), the converter is still operating in CCM when $0 < \varphi < \pi/2$. The idea of the movement of both $k(R, \varphi)$ and $k_{crit\_cl}(M_{\pi/2}, \varphi)$ when $\varphi$ decreases from $\pi/2$ to 0 (or increases from $\pi/2$ to $\pi$) is represented in Fig. 4(c), where the converter is operating in CCM at $\varphi = \pi/2$. Finally, the situation corresponding to operating in DCM by increasing the load resistance up to $R_{\max}$ is shown in Fig. 4(d). In all cases, the values of $k$ and $k_{crit\_cl}$ reach their maximum values at the peak of the line voltage, and they tend to zero when the line voltage also tends to zero.

The design of an RE with a single diode can be such that it always operates in DCM (for any range of variation of input voltage and load). This type of design allows it to be used as the core of an automatic PFC. As mentioned previously, in Buck-Boost, Flyback [4], SEPIC [5] and Ćuk [6], [7], and Zeta [8] converters operating in DCM, RE behavior is achieved when the converter duty cycle is kept constant during each line cycle. This means that the simple control strategy shown in Fig. 1(b) can be used in these cases. In summary, ideal automatic PFCs can be built from these topologies once they have been designed to operate in DCM. This means that the control circuitry can be dramatically simplified. A Boost converter can operate as a quasi-ideal automatic PFC if it operates in DCM and works at constant frequency [3]. To work as an ideal automatic PFC, it must operate just in the boundary between CCM and DCM [14] (also known as critical conduction mode).

### C. DC/DC Converters With Three DCMs Working as Conventional DC/DC Converters

Let us consider conventional dc/dc converters, but now with two diodes and two inductors ($L_1$ and $L_2$). If the two diodes remain in two inductive branches (made up of inductances $L_1$ and $L_2$ or a combination of the two) when its transistor is in OFF state, then the converter will have four conduction modes, one CCM and three DCMs [12], [13], [15], [16]. An example of the current passing through the converter diodes is shown in Fig. 5. The possible conduction modes in the case of three DCMs are shown in Table I, where the diode conduction states are represented by logical values. Thus, the ON state of a diode at the end of the switching period corresponds to logical level 1, whereas the OFF state of a diode at the end of the switching period corresponds to logical level 0. For example, operation in DCM2 implies that diode $D_1$ is OFF and diode $D_2$ is ON at the end of the switching period. In summary, converter conduction modes can be easily identified by observing the conduction state of each diode at the end of the switching period.

When the converter is working in closed loop and the input voltage remains constant, both the input and the output voltage

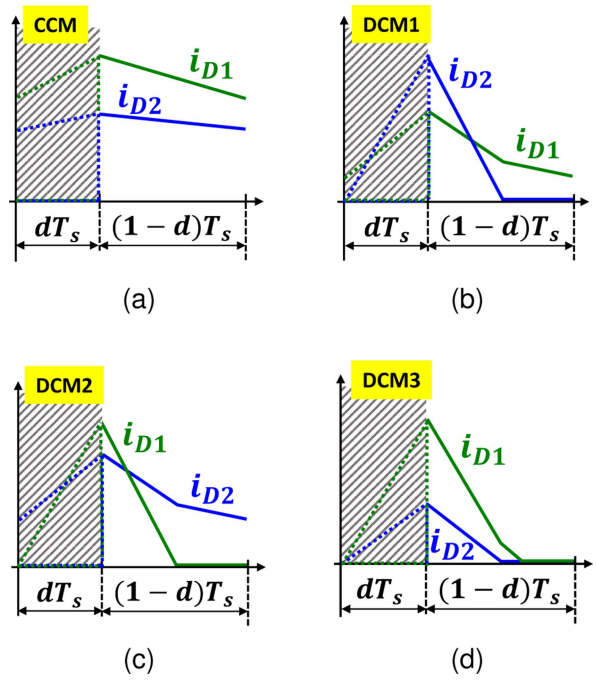


Fig. 5. Example of waveforms corresponding to the current passing through the diodes in a DC/DC converter with one CCM and three DCMs: (a) CCM. (b) DCM1. (c) DCM2. (d) DCM3.

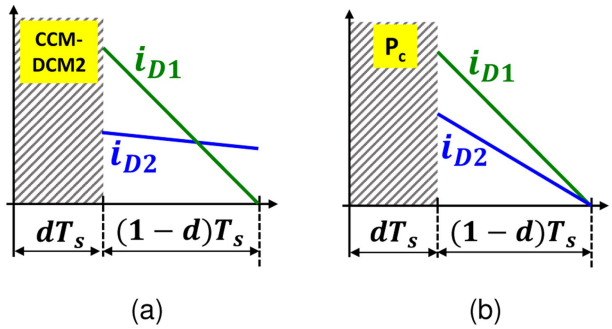


Fig. 6. Waveforms corresponding to the current passing through the diodes in two examples of boundary conditions: (a) Boundary between CCM and DCM2. (b) Central point $P_C$.

are constant. Consequently, the slopes of the current passing through the converter inductors remain also constant. Therefore, the slope of the current passing through the diodes during the transistor OFF period also remains constant. If the converter is operating in the CCM [see Fig. 5(a)] and the load decreases, then the average current passing through the inductors and diodes must decrease. The converter will operate in the CCM at constant duty cycle until one of the diode currents reaches zero just at the end of the switching period. If this current is $i_{D1}$, then the converter works in the boundary between the CCM and DCM2 [see Fig. 6(a)]. If the load continues decreasing, the average value of $i_{D1}$ must decrease. As the slope remains constant, the converter duty cycle must decrease, leading to operate in DCM2 [one example of the waveform corresponding to this mode is given in Fig. 5(c)]. An additional decrease of the load implies an additional decrease of the converter duty cycle. The operation mode corresponding to zero load will depend on the converter

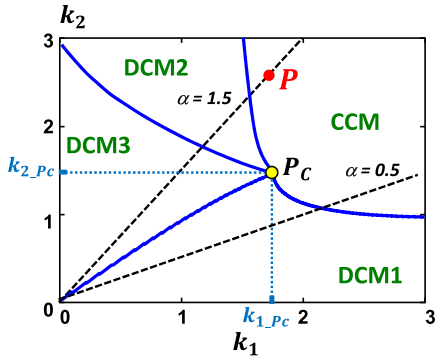


Fig. 7. Example map of conduction modes for a given value of $M$.

under study. Thus, the converter can either continue in DCM2 or change to DCM3 when reaching zero load.

Obviously, a similar process will take place if $i_{D2}$ is the current that reaches zero just at the end of the switching period when the load decreases from operation in the CCM. In this case, the converter will evolve from CCM to DCM1 [see Fig. 5(b)]. As in the previous case, an additional decrease of the load until zero can imply either to continue in DCM1 or to enter in DCM3.

A very special situation is represented in Fig. 6(b). In this figure, both diode currents reach zero just at the end of the switching period. This situation is the boundary between the four conduction modes. As will be explained later, this boundary is of primary concern when analyzing and designing the converter.

To study the conduction modes, a plane is established from parameters $k_1$ and $k_2$ [12], which are defined as usual

$$k_1 = \frac{2L_1}{RT_s} \tag{16}$$

$$k_2 = \frac{2L_2}{RT_s}. \tag{17}$$

The operation of the dc/dc converter can be characterized by a family of maps plotted in the $k_1k_2$ plane, such as in Fig. 7. Each map contains the regions of conduction modes for a particular value of the dc conversion ratio $M$. Each region corresponds to a specific conduction mode. The boundaries between adjacent conduction modes are curves drawn in this plane. The shapes of these curves are arbitrary in Fig. 7 because this map does not correspond to a specific converter. However, there are several general rules regarding the location of the conduction modes in the map. Since operation in CCM implies larger inductors than operation in any of the DCMs, the CCM region is the one farthest from the origin of the $k_1k_2$ plane (i.e., the bottom left corner) and from the axes. In contrast, regions corresponding to the DCMs are closer to the origin and the axes. The operation point of the converter moves along a straight line called a "trajectory," which is determined by slope $\alpha = L_2/L_1$. In the example given in Fig. 7, operation point $P$ is in the CCM, on a trajectory defined by $\alpha = 1.5$. As the load resistance $R$ increases, operation point $P$ moves along the trajectory toward the origin of the $k_1k_2$ plane, due to the synchronous variation of parameters $k_1$ and $k_2$ according to (16) and (17). In the example in Fig. 7, operation point $P$ could move from CCM to DCM2, or even to DCM3 if the increase of $R$ is great enough.

When the value of $M$ changes due to a variation of the input voltage, the boundaries between the conduction regions change in the map, resulting in a new map of regions. Therefore, each value of $M$ will have a corresponding map of conduction regions.

The dc conversion ratio for the converter can be expressed using equations that take the following form:

1) In the CCM

$$M_0 = f_0(d) \tag{18}$$

where $M_0$ is the value of $M$ in this mode and $d$ is the converter duty cycle.

2) In the DCMx

$$M_x = f_x(d, k_1, k_2) \tag{19}$$

where $M_x$ is the value of $M$ in this mode.

The boundaries between adjacent regions DCMx and DCMy can be easily calculated by equalizing the dc conversion ratios of these regions, $M_x$ and $M_y$. The steps to follow are as follows.

1) To replace $M_x$ and $M_y$ with $M$ in the two expressions in the form (19).
2) Eliminate variable $d$ from the two expressions in the form (19).

The equation thus obtained for the boundary between DCMx and DCMy is as follows:

$$F_{x-y}(M, k_1, k_2) = 0. \tag{20}$$

As previously explained, an example of current waveforms in one of the boundaries between regions (conduction modes) is shown in Fig. 6(a). Also as previously explained, all the conduction regions (conduction modes) intersect at a single point called the central point, $P_C$. The value of the coordinates of the central point for a given value of $M$, $k_{1\_Pc}$ and $k_{2\_Pc}$, can be determined by using either two equations in the form (20) or three equations in the forms (18) and (19). Therefore, the coordinates of the central point are exclusively functions of $M$. The current waveforms in central point $P_C$ are shown in Fig. 6(b).

## III. A General Method for Studying the Operation of DC/DC Converters With Three Discontinuous Conduction Modes Working as Resistor Emulators

### A. General Considerations

If we consider a dc/dc converter with only one inductor working at a constant load, then the conduction mode is completely defined by inequalities (2) and (3). This situation is perfectly described by the position of dimensionless parameter $k$ on a straight line, where the boundary $k_{crit\_cl}$ also lies (Fig. 2). When the load changes and the dc conversion ratio remains constant, parameter $k$ changes its position along the straight line while $k_{crit\_cl}$ remains constant, thus allowing a change in the conduction mode [Fig. 2(b)].

The situation is different if that converter is forced to work as an RE in an ac/dc conversion scheme [Fig. 1(a)], even if

the load $R$ remains constant. In this case, the conduction mode may depend on the line angle, because both the converter dc conversion ratio and the load "seen" by the RE are continuously changing according to the line angle, in spite of having a constant value for $R$ (Figs. 3 and 4). Obviously, the situation becomes more complex if $R$ also changes [Fig. 4(d)].

Coming back to the case of a dc/dc converter working as a conventional dc/dc converter instead of working as an RE, the situation is different again if the converter has three DCMs. In this case, two dimensionless parameters $k$ must be defined, determining a plane instead of a line [12]. Now, the boundaries between conduction modes are curves instead of a point, making a map of conduction regions. If the load $R$ is constant, then the operation point lies in a specific conduction region of the map. The operation point describes a straight line on the map (the trajectory) if load $R$ changes. The trajectory can pass through different regions (conduction modes) of the map.

Now, let us consider the use of this converter, not in a conventional dc/dc conversion scheme, but as a part of an ac/dc converter, working as the RE in this power conversion scheme. To the authors' best knowledge, this scenario has not been studied before. As mentioned previously, the converter must have an unlimited dc conversion ratio (otherwise it cannot operate as an RE). Moreover, let us consider a control strategy as simple as the one shown in Fig. 1(b). In these conditions, we need to determine whether the converter can operate either as an ideal RE or as a quasi-ideal RE, or is a long way from this desirable behavior. None of the existing methods can be directly applied to determine the converter input current waveform, $i_g(\varphi)$, for the following reasons.

1) Three DCMs are possible.
2) The dc conversion ratio is continuously changing (because of the rectified sine input voltage).
3) The load seen by the RE also changes according to the line voltage.

It should be noted that, in this case, the input voltage is continuously changing according to the line angle, whereas the converter duty cycle remains constant. Consequently, the slopes of the current passing through the converter diodes will change (case of currents depending on the line voltage) or will remain constant (case of currents depending on the output voltage, exclusively). Moreover, the conduction mode must always be one of the DCMs for any possible conduction mode and load, in order to enable the possibility of operating as an RE. Therefore, the sequence of DCMs that the converter is going to follow in this case is clearly different from the one previously described for the case of operating as a conventional dc/dc converter.

The objective of this article is to present a methodology for studying the operation of dc/dc converters that involve three DCMs when they are used as automatic PFCs. Particular attention has been paid to input current modeling in order to properly evaluate the performance of the converters in this application.

### B. Determining the Converter Input Current Waveform

Let us consider a dc/dc converter with three DCMs and with an unlimited dc conversion ratio. This converter is used as the RE in an ac/dc conversion scheme, like the one shown in Fig. 1(b), where the converter duty cycle is kept constant during each line cycle. In these conditions, the converter input voltage is continuously changing according to a rectified sine waveform, whereas the converter output voltage is kept constant due to bulk capacitor $C_B$. Therefore, the converter satisfies (4) and (5). To normalize the study, a base value for the converter currents can be defined from $L_1$, as follows:

$$I_{\text{base1}} = \frac{V_o T_s}{2L_1}. \tag{21}$$

Similarly, an alternative base value could be defined from $L_2$

$$I_{\text{base2}} = \frac{V_o T_s}{2L_2}. \tag{22}$$

The values of the dimensionless parameters $k_1$ and $k_2$ that the converter is seeing can be computed as follows:

$$k_1(\varphi) = \frac{2L_1}{r(\varphi)T_s} \tag{23}$$

$$k_2(\varphi) = \frac{2L_2}{r(\varphi)T_s}. \tag{24}$$

If the capacitance of capacitor $C_B$ [Fig. 1(b)] is large enough to ensure negligible voltage ripple across it, then the current injected by the converter into the output $RC_B$ network is

$$i_o(\varphi) = \frac{V_o}{r(\varphi)}. \tag{25}$$

By using (21)–(24), (25) becomes

$$i_o(\varphi) = I_{\text{base1}} k_1(\varphi) = I_{\text{base2}} k_2(\varphi) \tag{26}$$

and, therefore, the normalized value of $i_o(\varphi)$ can be expressed by either of the two following equations:

$$i_{on1}(\varphi) = \frac{i_o(\varphi)}{I_{\text{base1}}} = k_1(\varphi), \tag{27}$$

$$i_{on2}(\varphi) = \frac{i_o(\varphi)}{I_{\text{base2}}} = k_2(\varphi). \tag{28}$$

Equations (26)–(28) show that the evolution of $k_1(\varphi)$ and $k_2(\varphi)$ faithfully reflects the evolution of $i_o(\varphi)$.

Now, let us establish a power balance between the converter input and output ports. First, this balance is established for each line angle $\varphi$, averaging the electrical quantities over a switching period. Taking into account (5), the converter input current gives

$$i_g(\varphi) = \frac{M_{\pi/2}}{|\sin(\varphi)|} i_o(\varphi). \tag{29}$$

It should be noted that $i_g(\varphi)$ is the average value (averaged over a switching period) of the actual input current. Taking into account (26), (29) becomes

$$i_g(\varphi) = M_{\pi/2} I_{\text{base1}} \frac{k_1(\varphi)}{|\sin(\varphi)|} = M_{\pi/2} I_{\text{base2}} \frac{k_2(\varphi)}{|\sin(\varphi)|}. \tag{30}$$

This is a very important equation because it shows that the converter input current can be easily computed once the evolution of either $k_1(\varphi)$ or $k_2(\varphi)$ has been determined during a

line half-cycle. Moreover, the normalized expressions of $i_g(\varphi)$ can be obtained directly from (4) and (30)

$$i_{gn1}(\varphi) = \frac{i_g(\varphi)}{I_{\text{base1}}} = M_{\pi/2}\frac{k_1(\varphi)}{|\sin(\varphi)|} \tag{31}$$

$$i_{gn2}(\varphi) = \frac{i_g(\varphi)}{I_{\text{base2}}} = M_{\pi/2}\frac{k_2(\varphi)}{|\sin(\varphi)|}. \tag{32}$$

Extending the power balance between the converter input and output ports to a line half-cycle, and taking into account the electric charge balance in capacitor $C_B$, produces the following equation:

$$I_o = \frac{V_o}{R} = \frac{1}{\pi}\int_o^\pi i_o(\varphi)d\varphi. \tag{33}$$

Taking into account (26), (33) becomes

$$I_o = I_{\text{base1}}K_{1\text{avg}} = I_{\text{base2}}K_{2\text{avg}}. \tag{34}$$

where $K_{1\text{avg}}$ and $K_{2\text{avg}}$ are the average values of $k_1(\varphi)$ and $k_2(\varphi)$, respectively, in a line half-cycle

$$K_{1\text{avg}} = \frac{1}{\pi}\int_o^\pi k_1(\varphi)d\varphi \tag{35}$$

$$K_{2\text{avg}} = \frac{1}{\pi}\int_o^\pi k_2(\varphi)d\varphi. \tag{36}$$

From (34), the converter output power can finally be expressed as follows:

$$P_o = V_oI_{\text{base1}}K_{1\text{avg}} = V_oI_{\text{base2}}K_{2\text{avg}}. \tag{37}$$

Equation (37) is essential for the converter design, as it relates the converter power to either inductance $L_1$ through (21) or $L_2$ through (22). However, the values of either $K_{1\text{avg}}$ or $K_{2\text{avg}}$ must be known to properly design a converter with (37). Therefore, determining the evolution of $k_1(\varphi)$ (or $k_2(\varphi)$) is essential for the following two very important reasons.

1) To determine the input current waveform, according to (30). Once this waveform is known, the line current harmonic distortion can be computed, which is a key concern in evaluating the use of the converter as an RE.
2) To properly design the converter, according to (37) and the set of (21) and (35), or (22) and (36).

Finally, $K_{1\text{avg}}$ is of primary concern in producing a small-signal linear model for any dc/dc converter working as an automatic RE, because this type of model is based on averaging $i_o(\varphi)$ in a half-cycle of the line period. After linearizing $K_{1\text{avg}}$, a canonical first order circuit may be obtained, and a control transfer function can be derived from it. However, the transfer function thus obtained would depend on the particular converter selected to work as an automatic RE. Consequently, a more detailed study of this transfer function is beyond the scope of this article.

### C. Determining $k_1(\varphi)$ Evolution

Before determining the evolution of $k_1(\varphi)$ it is important to identify the map of the converter's conduction modes when it is working as a conventional dc/dc converter (i.e., when not only is the output voltage constant, but also the input voltage). As noted previously, this map is a function of the dc conversion ratio $M$. Once this map is known for any possible value of $M$, the map corresponding to $M_{\pi/2}$ (calculated according to (5)) must be selected. This value corresponds to the value of $m(M_{\pi/2},\varphi)$ when $\varphi = \pi/2$. The values of the dimensionless parameters $k_1$ and $k_2$ in the map corresponding to $M_{\pi/2}$ are $k_1(\pi/2)$ and $k_2(\pi/2)$, respectively.

The first step in determining the evolution of $k_1(\varphi)$ is to place the operation point $P$ in the map corresponding to $M_{\pi/2}$. This operation point will be called $P_{\pi/2}$. The coordinates of $P_{\pi/2}$ in this map are denoted as $k_{1\_P_{\pi/2}}$ and $k_{2\_P_{\pi/2}}$ in Fig. 8(a). Obviously, to achieve behavior as an RE, $P_{\pi/2}$ must be placed in one of the three DCMs. If DCMx is selected, then the value of the converter duty cycle $d_{\text{DCM}}$ can be easily obtained from (19) after the following transformations.

1) $M_x$ must be replaced with $M_{\pi/2}$ (known).
2) $k_1$ and $k_2$ must be replaced with $k_{1\_P_{\pi/2}}$ and $k_{2\_P_{\pi/2}}$, respectively (known).
3) $d$ must be replaced with $d_{\text{DCM}}$ (unknown).

The final equation is

$$d_{\text{DCM}} = f_{dx}(M_{\pi/2}, k_{1\_P_{\pi/2}}, k_{2\_P_{\pi/2}}). \tag{38}$$

It should be noted that the value of $d_{\text{DCM}}$ thus obtained is kept constant while $M_{\pi/2}$ and $R$ are also constant.

Once $P_{\pi/2}$ is placed in the map corresponding to $\varphi = \pi/2$ and, therefore, $k_{1\_P_{\pi/2}}$, $k_{2\_P_{\pi/2}}$ and $d_{\text{DCM}}$ are known, the next step is to determine the value of $k_1(\varphi)$ for different values of $\varphi$. Due to the symmetry of $v_g(\varphi)$ with respect to $\varphi = \pi/2$, we can select either the interval from $\varphi = \pi/2$ to $\varphi = \pi$ or the interval from $\varphi = \pi/2$ to $\varphi = 0$ to study the evolution of $k_1(\varphi)$. For the sake of simplicity, the second option is selected here.

When $\varphi$ decreases from $\pi/2$ towards 0, less current is injected by the RE into the output $RC_B$ network, which means that $i_o(\varphi)$ decreases and therefore the value of $k_1(\varphi)$ also decreases, as (26) shows. As $L_2 = \alpha L_1$, $k_2(\varphi) = \alpha k_1(\varphi)$, which means that the operation point goes down along the trajectory [see Fig. 8(b) and (c)]. The operation point corresponding to each value of $\varphi$ is called $P_\varphi$.

For each value of $m(M_{\pi/2},\varphi)$, a new map should be drawn [see Fig. 8(b) and (c)], because the boundaries between conduction regions depend on the converter dc conversion ratio, which is $m(M_{\pi/2},\varphi)$ now. If the operation point $P_\varphi$ remains in DCMx, then the value of $k_1(\varphi)$ can easily computed from (19) again, but now after the following transformations.

1) $M_x$ must be replaced with $m(M_{\pi/2},\varphi)$ (known).
2) $d$ must be replaced with $d_{\text{DCM}}$ (known).
3) $k_1$ must be replaced with $k_1(\varphi)$ (unknown).
4) Once $k_1(\varphi)$ is known, $k_2(\varphi) = \alpha k_1(\varphi)$, is also known.

The final equation is

$$k_1(\varphi) = f_{k1x}(M_{\pi/2}, d_{\text{DCM}}, \alpha, \varphi). \tag{39}$$

This equation gives the value of $k_1(\varphi)$ while the converter remains in DCMx. Due to the movement of both the operation point (along the trajectory) and the boundaries when $\varphi$ decreases, the converter can reach other DCMs, e,g,, DCMy. In general, the equation corresponding to the boundary between DCMx and DCMy can be easily computed from a modified

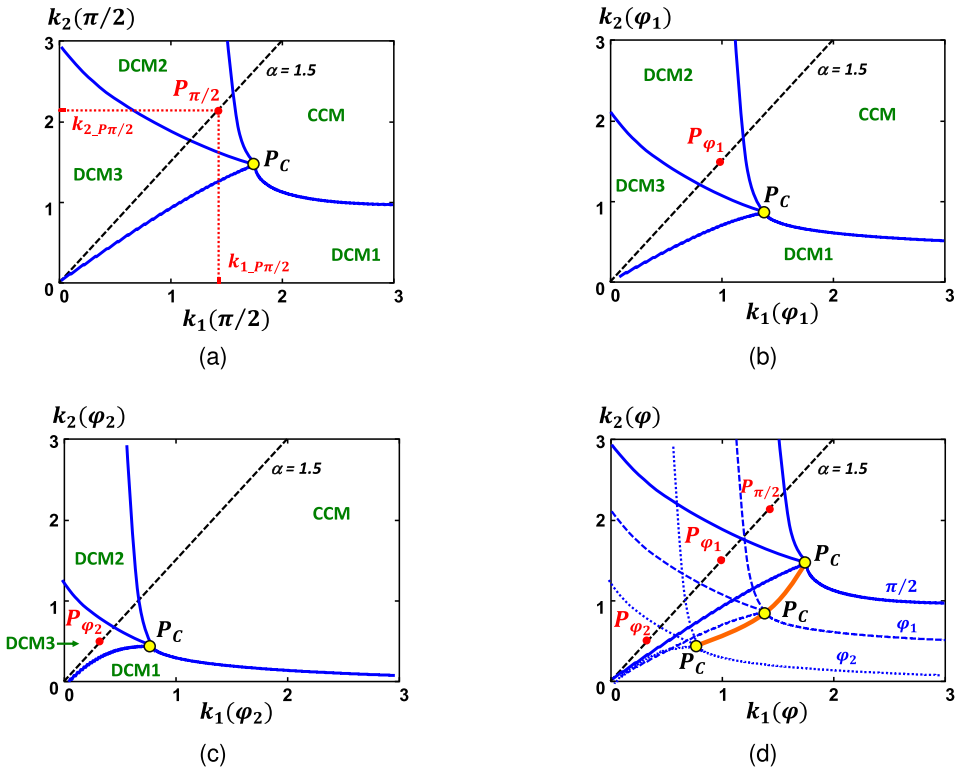


Fig. 8. Evolution of the converter operation when $\varphi$ changes from $\pi/2$ to 0: (a) Conduction map when $\varphi = \pi/2$. (b) Conduction map when $\varphi = \varphi_1 < \pi/2$. (c) Conduction map when $\varphi = \varphi_2 < \varphi_1 < \pi/2$. (d) Several conduction maps are drawn together.

version of (20), obtained by replacing $M$ with $m(M_{\pi/2}, \varphi)$, $k_1$ with $k_1(\varphi)$ and $k_2$ with $k_2(\varphi)$. The final equation is

$$F_{\mathrm{RE}x-y}(M_{\pi/2}, \varphi, k_1, k_2) = 0. \tag{40}$$

The value of $\varphi$ corresponding to this boundary can be computed from (39) and (40), taking into account that $k_2(\varphi) = \alpha k_1(\varphi)$. The value of $\varphi$ thus obtained is denoted as $\varphi_{x-y}$

$$\varphi_{x-y} = f_{x-y}(M_{\pi/2}, d_{\mathrm{DCM}}, \alpha). \tag{41}$$

Once the operation point is placed in DCMy, the evolution of $k_1(\varphi)$ can be obtained from an equation similar to (39), but valid for DCMy

$$k_1(\varphi) = f_{k1y}(M_{\pi/2}, d_{\mathrm{DCM}}, \alpha, \varphi). \tag{42}$$

This process is repeated until $k_1(\varphi) = 0$, at $\varphi = 0$. The DCM corresponding to this final state may be any of the three DCMs, depending on the position of $P_{\pi/2}$ on the map corresponding to $M_{\pi/2}$. In fact, the complete evolution of $k_1(\varphi)$ will depend strongly on this position, and in consequence, the line waveform (and its distortion) will depend on it. Therefore, the position of $P_{\pi/2}$ in the map corresponding to $M_{\pi/2}$ is a primary concern when analyzing the converter design.

The set of maps of conduction modes corresponding to values between $\varphi = 0$ and $\varphi = \pi/2$ can be summarized in a unified map in the $k_1(\varphi)k_2(\varphi)$ plane [see Fig. 8(d)], where the boundaries between regions continuously change as a function of $\varphi$. These boundaries always correspond to equations in the form (40).

A flowchart describing the procedure for determining the evolution of $k_1(\varphi)$ is shown in Fig. 9.

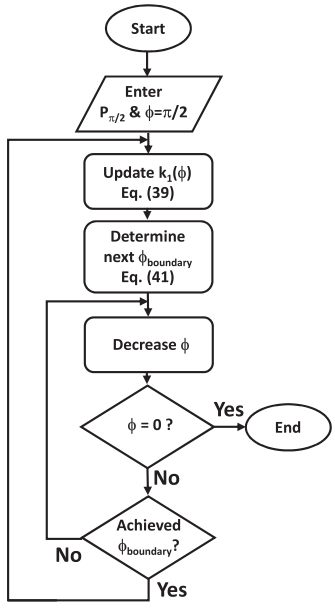


Fig. 9. Flowchart determining the $k_1(\varphi)$ evolution.

### D. Design Procedure

The input data for the design will be the output voltage and current, $V_o$ and $I_o$, and the peak value of the line voltage, $V_g$. Consequently, $M_{\pi/2}$ is input data as well (see (5)).

1) The first step in the design procedure is to select the position of $P_{\pi/2}$ on the map corresponding to $M_{\pi/2}$, according

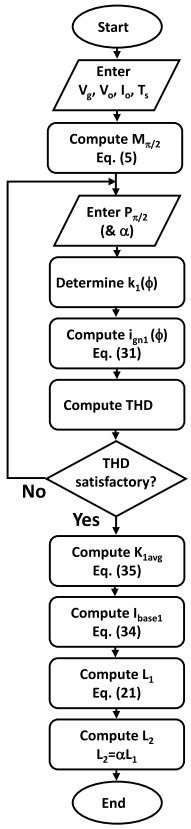


Fig. 10. Flowchart determining the design process.

to several possible criteria (line distortion, conduction, and switching losses, etc.), but always in a DCM. Once the coordinates of $P_{\pi/2}$ are known, the value of $\alpha$ is fixed. Using (38), the value of $d_{\rm DCM}$ can be obtained.

2) The second step is to determine the evolution of $k_1(\varphi)$ from $\varphi = 0$ to $\varphi = \pi$ (in fact, determining evolution from $\varphi = 0$ to $\varphi = \pi/2$ is enough, due to the waveform symmetry). The value of $K_{1\rm avg}$ will be obtained using (35).
3) The third step is to compute the value of $I_{\rm base1}$ from (34). This value allows us to determine the value of $L_1$ for a given value of switching period $T_s$, according to (21). Obviously, $L_2 = \alpha L_1$.

A flowchart describing the design procedure is shown in Fig. 10.

## IV. Example of Using the Proposed Method: The SEPIC and Ćuk Converters Working as Automatic REs

Fig. 11 shows several implementations of PFCs based on the SEPIC and Ćuk topologies. The converter shown in Fig. 11(a) is the classical implementation based on the use of the SEPIC topology and a full-wave rectifier at the input [5], [7]. It should be noted that if the inductance of $L_1$ is relatively low, the current passing through inductor $L_1$ tends to reverse during the transistor OFF state, but cannot reverse due to the diodes in the full-wave rectifier.

This circuit can be modified to avoid using the full-wave rectifier (bridge rectifier), thus obtaining the bridgeless SEPIC topology shown in Fig. 11(b) [17]. In this case, the topology avoids the voltage drop across one of the bridge rectifier diodes, at the expense of having two transistors. During the positive line half-cycle, transistor $S_1$ is always in the ON state, whereas transistor $S_2$ is switching. After analyzing a switching period in this line half-cycle, it can be observed that diode $D_{B2}$ is connected in series with inductor $L_1$ during transistor $S_2$ OFF state. Therefore, an additional DCM can occur in the current passing through inductor $L_1$, besides the one essentially due to inductor $L_2$, leading to three DCMs. Obviously, a similar situation occurs in the negative line half-cycle due to diode $D_{B1}$, when transistor $S_2$ is always in the ON state, transistor $S_1$ is switching and the current passing through inductor $L_1$ has the opposite direction. The only difference between this and the previous case [Fig. 11(a)] is that $i_g(\varphi)$ (which is the value of the current passing through inductor $L_1$ averaged over a switching period) is always positive, whereas $i'_g(\varphi)$ [see Fig. 11(b)] changes its direction each line half-cycle (i.e., it is an ac current).

All of these considerations can be extrapolated to the classical Ćuk [see Fig. 11(c)] [6], [7] and the bridgeless Ćuk [see Fig. 11(d)] [18]. Moreover, other bridgeless PFCs based on SEPIC and Ćuk topologies have been proposed [19], [20], [21], [22], [23], [24], [25], [26]. In many of them, DCM operation is forced to achieve automatic PFC operation. In spite of having several diodes and inductors, only one DCM is considered, because the value of some inductors is high enough to avoid multiple DCMs. In this case, the method proposed here allows us to evaluate the operation of these converters with lower inductor values.

The study of PFC implementations based on the SEPIC topology [see Fig. 11(a) and (b)] with three DCMs must start by examining how this topology behaves working as conventional dc/dc converter, but with an additional diode at the input port [see Fig. 12(a)]. This converter has been already studied in [13]. Its main current waveforms appear in Fig. 12(b). The map of conduction mode regions for $M = 0.6$ is shown in Fig. 13. Two different trajectories have been drawn in this figure: $\alpha = 1$ and $\alpha = 0.3$. The expressions that define the dc conversion ratios for each conduction mode [expressions in the forms (18) and (19)], are as follows [13]:

$$M_0 = f_0(d) = \frac{d}{1-d} \tag{43}$$

$$M_1 = f_1(d, k_1, k_2) = \frac{d}{\sqrt{\dfrac{k_1 k_2}{k_1 + k_2}}}, \tag{44}$$

$$M_2 = f_2(d, k_1) = \frac{k_1 + \sqrt{k_1(4 + k_1)}}{2k_1} d, \tag{45}$$

$$M_3 = f_3(d, k_1, k_2) = \frac{A + \sqrt{A^2 + \dfrac{16k_2^2}{k_1}}}{4k_2} d \tag{46}$$

where

$$A = -d + \sqrt{d^2 + 4k_2}. \tag{47}$$

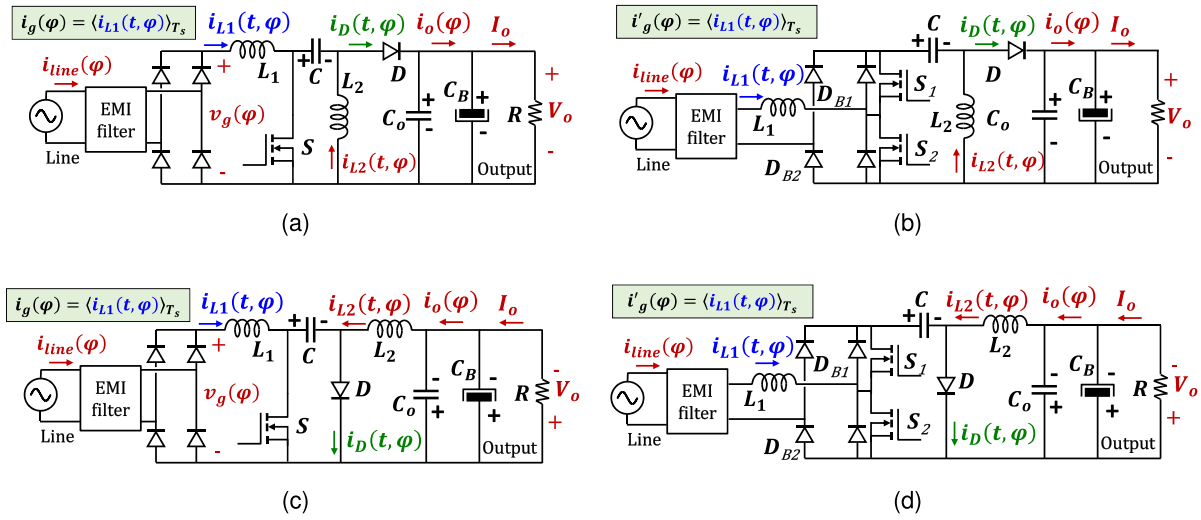


Fig. 11. Several implementations of PFCs based on the SEPIC and Ćuk converters: (a) Classical SEPIC. (b) Bridgeless SEPIC. (c) Classical Ćuk. (d) Bridgeless Ćuk.

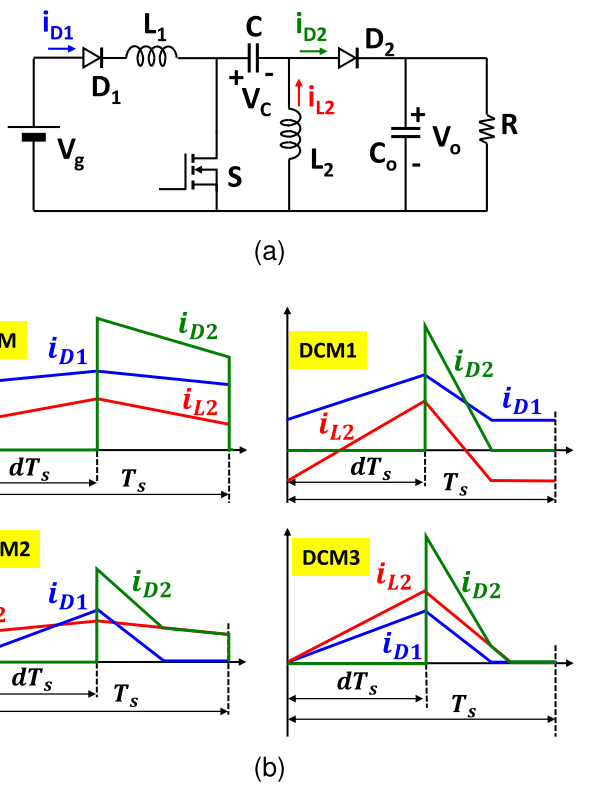


Fig. 12. SEPIC converter with an additional diode added at the input port: (a) Schematic. (b) Waveforms corresponding to the current passing through diodes and inductors.

The coordinates of central point $P_C$ can be easily deduced by replacing $M_0$, $M_1$, and $M_2$ with $M$ in (43)–(45), and by solving the resulting set of equations, thus obtaining the values of $k_1$ and $k_2$ for a given value of $M$. The final result is

$$k_{1\_P_c} = \frac{1}{M(M+1)}, \qquad k_{2\_P_c} = \frac{1}{(M+1)}. \tag{48}$$

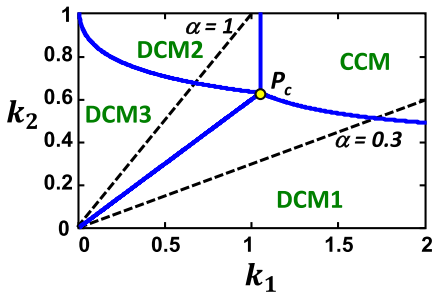


Fig. 13. Map of conduction modes for the converter shown in Fig. 12(a), when $M = 0.6$. The trajectories $\alpha = 1$ and $\alpha = 0.3$ have been drawn on the map.

The boundaries between conduction regions, obtained from (44)–(47) are [13]

$$F_{0-1}(M, k_1, k_2) = k_2 - \frac{k_1}{(1+M)^2 - 1} = 0 \tag{49}$$

which is the boundary CCM-DCM1, valid for $k_1 > k_{1\_P_c}$.

$$F_{0-2}(M, k_1) = k_1 - \frac{1}{M(M+1)} = 0 \tag{50}$$

which is the boundary CCM-DCM2, valid when $k_2 > k_{2\_P_c}$.

$$F_{1-3}(M, k_1, k_2) = k_2 - Mk_1 = 0 \tag{51}$$

which is the boundary DCM1-DCM3, valid for when $0 < k_1 < k_{1\_P_c}$.

$$F_{2-3}(M, k_1, k_2) = k_2 - 1 + \frac{-k_1 + \sqrt{k_1(4+k_1)}}{2} M = 0 \tag{52}$$

which is the boundary DCM2-DCM3, also valid for $0 < k_1 < k_{1\_P_c}$.

As demonstrated in [13], (42)–(51) are also valid for a Ćuk converter with an additional diode at its input port.

The operation of the REs shown in Fig. 11(a) and (b) must be addressed from the operation of the converter given in Fig. 12(a) (just described), but considering that the dc conversion ratio is continuously changing. As the input voltage follows a rectified sine waveform, central point $P_C$ and the boundaries between conduction regions will also change according to the line angle $\varphi$. The set of (44)–(48) will be now transformed as has been previously explained, the final result is as follows.

1) In DCM1 (22)

$$\frac{M_{\pi/2}}{|\sin(\varphi)|} = \frac{d_{\text{DCM}}}{\sqrt{\dfrac{\alpha}{1+\alpha}k_1(\varphi)}}. \tag{53}$$

2) In DCM2 (23)

$$\frac{M_{\pi/2}}{|\sin(\varphi)|} = \frac{k_1(\varphi)+\sqrt{k_1(\varphi)(4+k_1(\varphi))}}{2k_1(\varphi)}d_{\text{DCM}}. \tag{54}$$

3) In DCM3 (24) and (25)

$$\frac{M_{\pi/2}}{|\sin(\varphi)|} = \frac{A(\varphi)+\sqrt{A(\varphi)^2+16\alpha^2k_1(\varphi)}}{4\alpha k_1(\varphi)}d_{\text{DCM}} \tag{55}$$

where

$$A(\varphi) = -d_{\text{DCM}} + \sqrt{d_{\text{DCM}}^2 + 4\alpha k_1(\varphi)}. \tag{56}$$

Equations (53)–(56) allow us to obtain the value of $k_1(\varphi)$ in each conduction mode. Regarding the coordinates of central point $P_C$, its value can be easily deduced from (48), by replacing $M$ with $m(M_{\pi/2},\varphi)$. The result is

$$k_{1\_P_c}(M_{\pi/2},\varphi) = \frac{\sin^2(\varphi)}{M_{\pi/2}(M_{\pi/2}+|\sin(\varphi)|)},$$
$$k_{2\_P_c}(M_{\pi/2},\varphi) = \frac{|\sin(\varphi)|}{M_{\pi/2}+|\sin(\varphi)|}. \tag{57}$$

The boundaries between conduction regions can be obtained by replacing $M$ with $m(M_{\pi/2},\varphi)$ in (49)–(52). The results are as follows.

1) Boundary CCM-DCM1

$$k_2(\varphi) - \frac{k_1(\varphi)\sin^2(\varphi)}{(|\sin(\varphi)|+M_{\pi/2})^2k_1(\varphi)-\sin^2(\varphi)} = 0 \tag{58}$$

which is valid for $k_1(\varphi) > k_{1\_Pc}(M_{\pi/2},\varphi)$.

2) Boundary CCM-DCM2

$$k_1(\varphi) - \frac{\sin^2(\varphi)}{M_{\pi/2}(M_{\pi/2}+|\sin(\varphi)|)} = 0 \tag{59}$$

valid when $k_2(\varphi) > k_{2\_Pc}(M_{\pi/2},\varphi)$.

3) Boundary DCM1-DCM3

$$k_2(\varphi) - \frac{M_{\pi/2}}{|\sin(\varphi)|}k_1(\varphi) = 0 \tag{60}$$

valid for values verifying $0 < k_1(\varphi) < k_{1\_Pc}(M_{\pi/2},\varphi)$.

4) DCM2-DCM3

$$k_2(\varphi) - 1 + \frac{-k_1(\varphi)+\sqrt{k_1(\varphi)(4+k_1(\varphi))}}{2|\sin(\varphi)|}M_{\pi/2} = 0 \tag{61}$$

which is also valid for $0 < k_1(\varphi) < k_{1\_Pc}(M_{\pi/2},\varphi)$.

The map corresponding to $M_{\pi/2} = 0.75$ and $\varphi = \pi/2$ is given in Fig. 14(a). The coordinates of central point $P_C$ can be easily obtained from (57)

$$k_{1\_P_c}\left(M_{\pi/2},\frac{\pi}{2}\right) = \frac{1}{M_{\pi/2}(M_{\pi/2}+1)},$$
$$k_{2\_P_c}\left(M_{\pi/2},\frac{\pi}{2}\right) = \frac{1}{M_{\pi/2}+1}. \tag{62}$$

The maps corresponding to other specific values of $\varphi$ are shown in Fig. 14(b)–(d), where the movement of the region boundaries and of central point $P_C$ can be observed. In Fig. 15, these maps are collected in a map that summarizes the information given in the previous maps. This map also shows the movement of central point $P_C$ when $\varphi$ changes. The equation that describes this movement on plane $k_1(\varphi)k_2(\varphi)$ can be easily obtained by eliminating $\sin(\varphi)$ in the set of (57)

$$k_{1\_P_c}(\varphi) - \frac{k_{2\_P_c}^2(\varphi)}{1-k_{2\_P_c}(\varphi)} = 0. \tag{63}$$

To study the evolution of the boundaries between conduction regions, let us describe the evolution of the straight line that defines the boundary between DCM1 and DCM3 when $\varphi$ changes. From (57), the slope of this straight line is

$$\frac{k_{2\_P_c}(M_{\pi/2},\varphi)}{k_{1\_P_c}(M_{\pi/2},\varphi)} = \frac{M_{\pi/2}}{|\sin(\varphi)|}. \tag{64}$$

As (64) shows, the slope of the DCM1-DCM3 boundary becomes vertical when $\varphi$ approaches zero. This conclusion is extremely important to understanding converter operation, as will be explained below.

As the proposed method establishes, the positioning of point $P_{\pi/2}$ on the map corresponding to $k_1(\pi/2)k_2(\pi/2)$ is a key point for analyzing converter operation. Let us draw a straight line from point $P_C$ to the origin. This straight line meets the boundary between DCM1-DCM3. From (64), the slope of this straight line is

$$\frac{k_{2\_P_c}(M_{\pi/2},\frac{\pi}{2})}{k_{1\_P_c}(M_{\pi/2},\frac{\pi}{2})} = M_{\pi/2}. \tag{65}$$

As the slope of the trajectory is $\alpha$ and $P_{\pi/2}$ must be placed in any of the DCMs, then two possible situations must be taken into consideration (Fig. 16) as follows.

1) *Case 1:* $\alpha < M_{\pi/2}$. In this case, point $P_{\pi/2}$ is placed in DCM1.
2) *Case 2:* $\alpha > M_{\pi/2}$. In this case, point $P_{\pi/2}$ is placed in either DCM2 or DCM3.

If the converter is designed in Case 1, the operation point will remain in DCM1 when line angle $\varphi$ changes from $\pi/2$ to 0 (or from $\pi/2$ to $\pi$), due to the movement of central point $P_C$ (see Fig. 15). Consequently, the evolution of $k_1(\varphi)$ can be computed

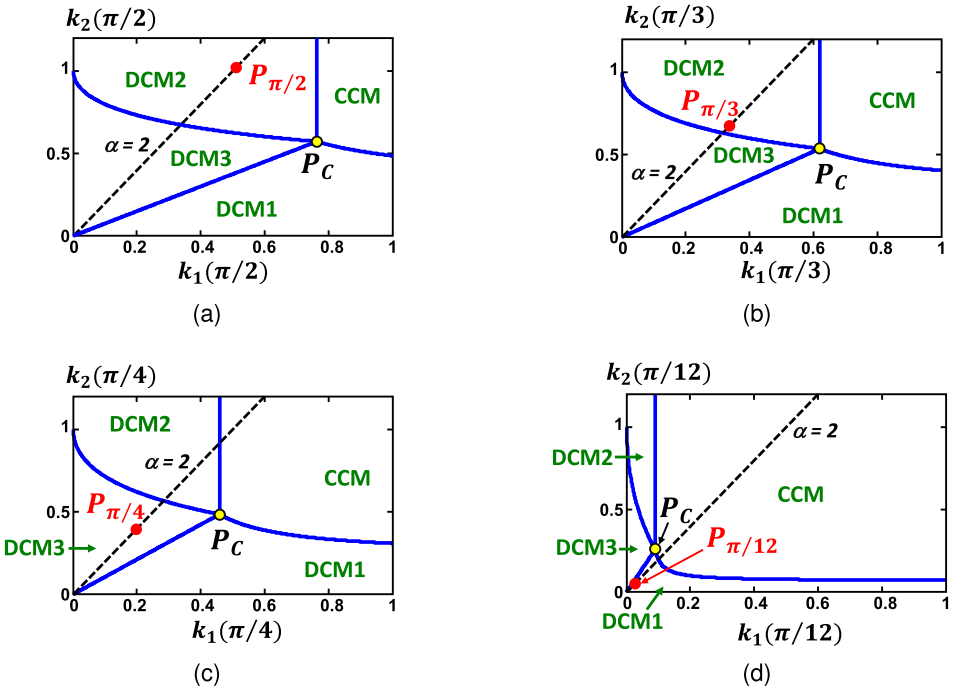


Fig. 14. Evolution of conduction maps of a SEPIC RE designed with $M_{\pi/2} = 0.75$, $\alpha = 2$ and $d_{\text{DCM}} = 0.378$, when $\varphi$ changes from $\pi/2$ to 0: (a) $\varphi = \pi/2$. (b) $\varphi = \pi/3$. (c) $\varphi = \pi/4$. (d) $\varphi = \pi/12$.

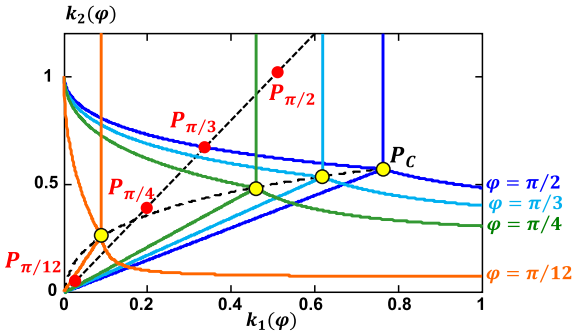


Fig. 15. Conduction map that summarizes the information given in the maps in Fig. 14.

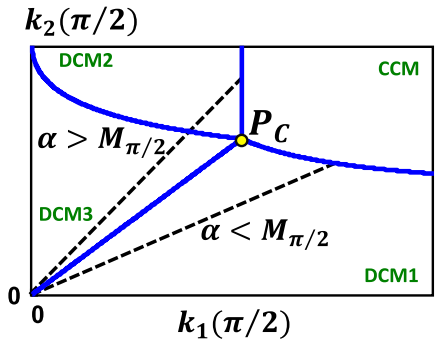


Fig. 16. Types of possible trajectories. Case 1: $\alpha < M_{\pi/2}$. Case 2: $\alpha > M_{\pi/2}$.

from (53).

$$k_1(\varphi) = \frac{1+\alpha}{\alpha}\left(\frac{d_{\text{DCM}}}{M_{\pi/2}}\right)^2 \sin^2(\varphi). \tag{66}$$

Taking into account (21) and (66), and that $i_g(\varphi)$ is obtained by averaging inductor $L_1$ current over a switching period, then (30) becomes

$$i_g(\varphi) = \langle i_{L_1}(t,\varphi)\rangle_{T_s} = \frac{d_{\text{DCM}}^2(1+\alpha)T_s}{2\alpha L_1} V_g|\sin(\varphi)| \tag{67}$$

where $i_{L_1}(t,\varphi)$ is the current passing through inductor $L_1$. This result demonstrates that the converter operates as an ideal automatic RE when designed in Case 1. As a pair of the input diodes shown in Fig. 11(a) or one of the input diodes in Fig. 11(b) are always conducting, the result is consistent with the description given in [5] and [17] for the same converters with a single DCM. To prevent the converter from operating in CCM when $\varphi = \pi/2$, it is derived from (43) that the following condition must be satisfied:

$$d_{\text{DCM}} < d_o(M_{\pi/2}) = \frac{M_{\pi/2}}{M_{\pi/2}+1}. \tag{68}$$

On the other hand, $P_{\pi/2}$ is placed in either DCM2 or DCM3 in Case 2. If placed in DCM2, the value of $k_1(\varphi)$ while the converter remains in this mode is easily deduced from (54), the result is

$$k_1(\varphi) = \frac{d_{\text{DCM}}^2}{M_{\pi/2}\left(M_{\pi/2} - d_{\text{DCM}}|\sin(\varphi)|\right)}\sin^2(\varphi). \tag{69}$$

A comparison of (66) and (69) allows us to predict that the evolution of $i_g(\varphi)$ in this mode does not correspond to a sinusoidal evolution.

As the angle moves away from $\pi/2$, the operation point also moves along the trajectory until it reaches a certain value of $\varphi$, labeled $\varphi_{2-3}$, corresponding to leaving DCM2 and entering

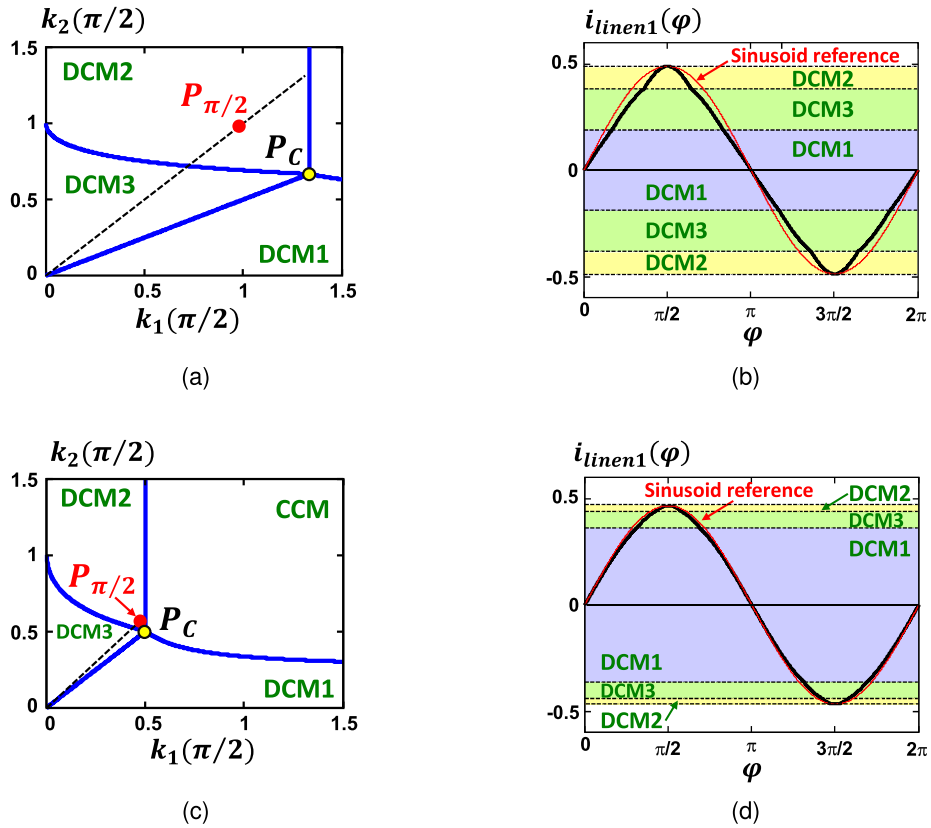


Fig. 17. Map of regions for $\varphi = \pi/2$ (left side) and normalized line current (right side), in two designs where the point $P_{\pi/2}$ is placed in DCM2. (a) and (b): Design with $M_{\pi/2} = 0.5$, $\alpha = 1$ and $d_{\text{DCM}} = 0.307$. (c) and (d): Design with $M_{\pi/2} = 1$, $\alpha = 1.2$ and $d_{\text{DCM}} = 0.489$.

DCM3. The value of this angle can be computed from (61) and (69) and the definition of $\alpha$, obtaining

$$\varphi_{2-3} = arc\sin\left(\frac{d_{\text{DCM}} - 1 + B}{2\alpha d_{\text{DCM}}} M_{\pi/2}\right) \tag{70}$$

where

$$B = \sqrt{(1 - d_{\text{DCM}})(1 - d_{\text{DCM}} + 4\alpha)}. \tag{71}$$

Once the operation point enters the region corresponding to DCM3, the value of $k_1(\varphi)$ is determined by (55) and (56). However, the operation point always enters DCM1 when $\varphi$ continues decreasing. In other words, the converter always operates in DCM1 near the line zero crossing. This is due to the slope of the curve described by $P_C$ (see (64)), which is vertical near the line zero crossing. When the slope of the straight line that defines the boundary DCM1-DCM3 is steeper than the slope of the trajectory, then the converter starts operating in DCM1. From (60) and the definition of $\alpha$, we obtain

$$\varphi_{3-1} = arc\sin\left(\frac{M_{\pi/2}}{\alpha}\right) \tag{72}$$

where $\varphi_{3-1}$ is the value of $\varphi$ corresponding to this boundary. As the converter is operating in DCM1, $k_1(\varphi)$ is calculated again using (66).

In order to prevent the converter from operating in CCM when $\varphi = \pi/2$, inequality (68) must be satisfied. Furthermore, if the objective is to ensure that the converter operates in DCM2 at $\varphi = \pi/2$, the determination of the duty cycle value at the DCM2-DCM3 boundary becomes critical. From (54) and (61), we obtain the value of the duty cycle needed to design the converter just in that boundary

$$d_{\text{DCM2-3}} = \frac{M_{\pi/2}}{2(\alpha - M_{\pi/2})}\left(\sqrt{(1 - M_{\pi/2}^2) + 4\alpha} - M_{\pi/2} - 1\right). \tag{73}$$

Therefore, the following inequality must be verified to place $P_{\pi/2}$ in DCM2

$$d_{\text{DCM2-3}} < d_{\text{DCM}} < \frac{M_{\pi/2}}{M_{\pi/2} + 1}. \tag{74}$$

On the other hand, $P_{\pi/2}$ is placed in DCM3 if

$$0 < d_{\text{DCM}} < d_{\text{DCM2-3}}. \tag{75}$$

According to the proposed method and the equations already obtained for the SEPIC REs given in Fig. 11(a) and (b), the normalized line current waveform can be obtained. Two design examples are shown in Fig. 17. In both examples, $P_{\pi/2}$ is placed in DCM2.

In the first (Fig. 17(a)), the design values are $M_{\pi/2} = 0.5$, $\alpha = 1$ and $k_1(\pi/2) = k_2(\pi/2) = 0.977$. The value of the duty cycle corresponding to placing $P_{\pi/2}$ in this position is obtained from (54), the result being $d_{\text{DCM}} = 0.307$. The values of line angles where the conduction mode changes are $\varphi_{2-3} = 64.7^\circ$ and $\varphi_{3-1} = 30^\circ$, obtained from (70)–(72). The equation for

$k_1(\varphi)$ is (69) when operating in DCM2, it must be obtained from (55) and (56) in DCM3, while it is (66) in DCM1. Once the evolution of $k_1(\varphi)$ is completely determined, the normalized line current $i_{gn1}(\varphi)$ is directly obtained from (31). Line current waveform $i_{\text{line}}(\varphi)$ can be easily built from $i_g(\varphi)$, which is a rectified version of $i_{\text{line}}(\varphi)$. A normalized version of $i_{\text{line}}(\varphi)$ can be defined as

$$i_{\text{line}n1}(\varphi) = \frac{i_{\text{line}}(\varphi)}{I_{\text{base1}}}. \tag{76}$$

The waveform obtained for this quantity is shown in Fig. 17(b).

In the second example (Fig. 17(c)), the design values are $M_{\pi/2} = 1$, $\alpha = 1.2$, $k_1(\pi/2) = 0.467$, and $k_2(\pi/2) = 0.56$. The value of the duty cycle is $d_{\text{DCM}} = 0.489$ and the boundary angles are $\varphi_{2-3} = 75.77°$ and $\varphi_{3-1} = 56.44°$. The final waveform obtained for the normalized line current is shown in Fig. 17(d). As this figure shows, the line current is almost a perfect sinusoid, because the converter is operating in DCM1 during a large part of the line period.

Both examples show that low distorted line current waveforms can be obtained when the SEPIC converter is designed to operate in Case 2 ($\alpha > M_{\pi/2}$). This is an important conclusion, because designing in Case 1 implies a large value of inductor $L_1$, according to the definition of $\alpha$. Therefore, quasi-ideal RE behavior can be achieved even if the value of inductor $L_1$ is similar to the value of inductor $L_2$. A detailed analysis of the possible designs as a function of the position of $P_{\pi/2}$ in the map of conduction regions is beyond the scope of this article, which mainly focuses on proposing a general method for studying the operation of converters with three DCMs as REs. The SEPIC converter is an example to demonstrate how the method can be applied in a specific case.

As [13] showed, all of the equations that represent the operation of the converter shown in Fig. 12(a) are the same as those corresponding to a conventional dc/dc Ćuk converter with an additional diode at its input port. Consequently, all the conduction maps agree for both converters. Because of that, the variation of the region boundaries with the line angle when the Ćuk converter is working as an RE [according to the control scheme given in Fig. 1(b)], also agree. Therefore, all the considerations for the SEPIC RE can also be applied to the Ćuk converter when used as an RE.

## V. Validation of the Proposed Method With Several Implementations of SEPIC and Ćuk Converters Working as Automatic REs

In this section, the proposed method to determine the line current of automatic PFCs based on converters with three DCMs is verified on several examples of SEPIC and Ćuk converters. This verification involved both simulation using PSIM software and experimentation on a real prototype.

### A. Validation by Simulation

The first circuit simulated is the one shown in Fig. 11(a), which is the classical implementation of a SEPIC converter used as an automatic PFC. The values of the main components are given in Table II. It should be noted that both inductors have been selected with the same value, which means $\alpha = 1$. As the peak value of line voltage is $V_g = 110\sqrt{2}$ V and the output voltage is $V_o = 77.8$ V, then $M_{\pi/2} = 0.5$. This means $\alpha > M_{\pi/2}$ and, therefore, $P_{\pi/2}$ must be placed in either DCM2 or DCM3, according to Fig. 16. Two different options for $P_{\pi/2}$ have been selected for the simulations, both in DCM2 (see Fig. 18). They are as follows.

1) Point $P_{\pi/2-A}$: $P_{\pi/2}$ is located in DCM2, but far from the boundary between this mode and DCM3. This position is achieved with $d = 0.33$ and $R = 73.1\,\Omega$.
2) Point $P_{\pi/2-B}$: $P_{\pi/2}$ is also placed in DCM2, but very close to the boundary between this mode and DCM3. This position is attained with $d = 0.282$ and $R = 110\,\Omega$.

The coordinates of $P_{\pi/2-A}$ are $k_1(\pi/2) = k_2(\pi/2) = 1.28$, whereas those of $P_{\pi/2-B}$ are $k_1(\pi/2) = k_2(\pi/2) = 0.73$.

Theoretical and simulated line current waveforms for the design corresponding to $P_{\pi/2-A}$ are shown in Fig. 19(a) and (b), respectively. The theoretical line waveform (in normalized version) was derived by evaluating $k_1(\varphi)$. The values of line angles where the conduction mode changes are $\varphi_{2-3} = 56.38°$ and $\varphi_{3-1} = 30°$, obtained from (70)–(72). Fig. 20 shows simulated $i_{L1}(t,\varphi)$ and $i_D(t,\varphi)$ waveforms during a switching period corresponding to several significant line angles. As expected, the waveform shown in Fig. 20(a) corresponds to operation in DCM2 (i.e., $i_{L1}(t,\varphi)$ reaches zero before the end of the switching period, when $i_D(t,\varphi)$ is still positive). Operation in the boundary between DCM2 and DCM3 is observed in Fig. 20(b), also as predicted. It should be noted that this boundary is achieved when $i_D(t,\varphi)$ reaches zero just at the end of the switching period, as Fig. 20(b) shows. Fig. 20(c) shows the boundary between DCM3 and DCM1, where $i_{L1}(t,\varphi)$ and $i_D(t,\varphi)$ reach zero at the same time and remain at zero until

TABLE II
Parameter Values Used in Simulations and Experimental Results

| Parameter | Value |
|---|---|
| $L_1$ | 200 $\mu$H |
| $L_2$ | 200 $\mu$H |
| $C$ | 330 $n$F |
| $C_o$ | 6.8 $\mu$F |
| $C_B$ | 11800 $\mu$F |
| $T_s$ | 10 $\mu$s |
| $f_{line}$ | 50 Hz |

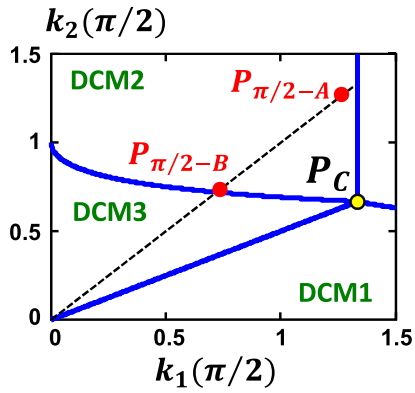


Fig. 18. Design points used for validating the theoretical predictions.

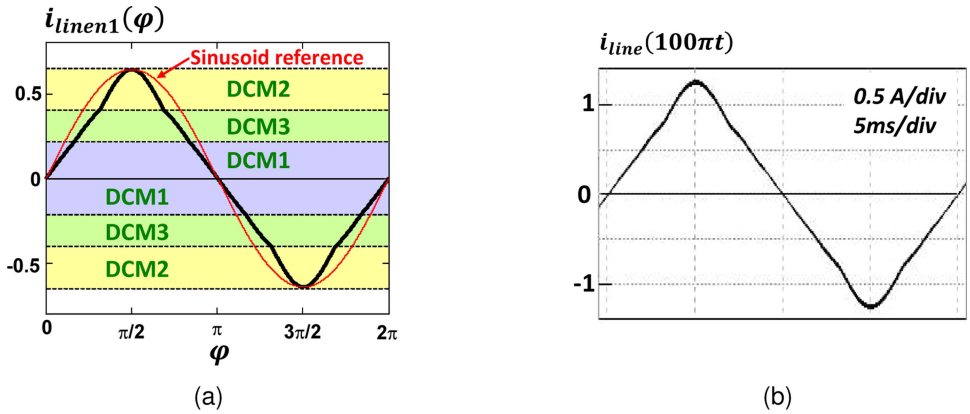


Fig. 19. Line current waveforms corresponding to the SEPIC PFC shown in Fig. 11(a) working in design point $P_{\pi/2-A}$: (a) Predicted normalized waveform. (b) Simulated waveform.

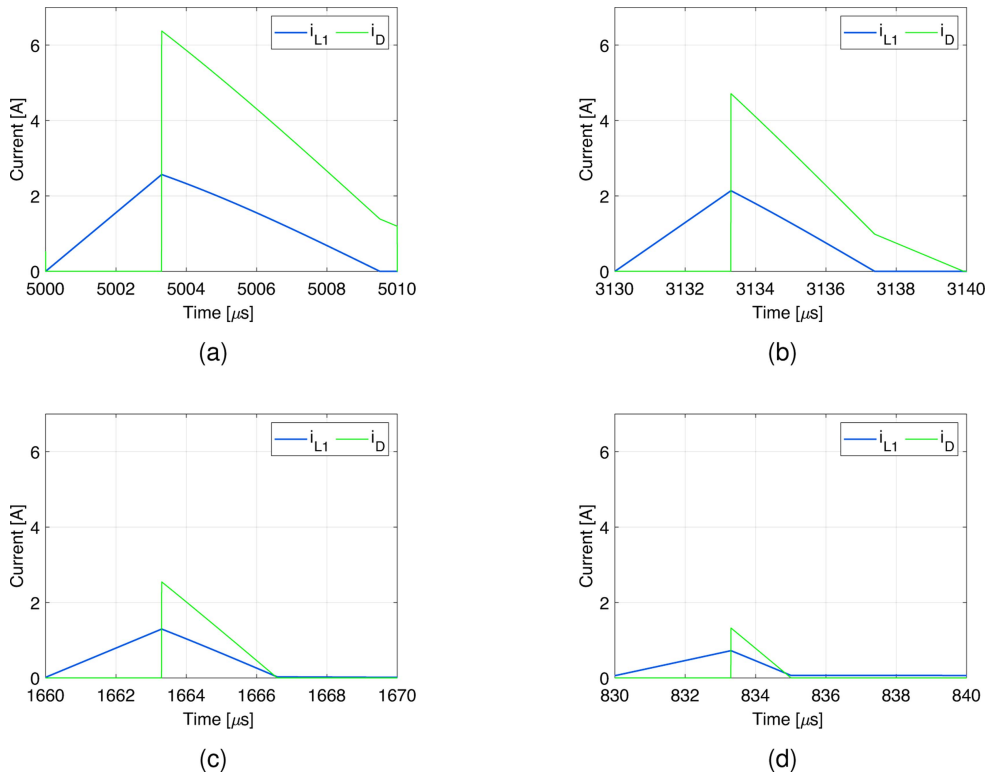


Fig. 20. Simulated $i_{L1}(t,\varphi)$ and $i_D(t,\varphi)$ waveforms corresponding to the SEPIC PFC shown in Fig. 11(a) working in design point $P_{\pi/2-A}$: (a) $\varphi = 90°$. (b) $\varphi = 56.38°$. (c) $\varphi = 30°$. (d) $\varphi = 15°$.

the end of the switching period. Finally, Fig. 20(d) corresponds to operation in DCM1, as can be deduced after comparing it with Fig. 12(d). It should be noted that the value of $i_{L1}(t,\varphi)$ remains slightly positive when $i_D(t,\varphi)$ reaches zero, according to the operation in DCM1.

Similarly, theoretical and simulated line current waveforms for the design corresponding to $P_{\pi/2-B}$ are shown in Fig. 21(a) and (b), respectively. In this case, $\varphi_{2-3} = 84.24°$ and $\varphi_{3-1} = 30°$, which means that the converter is operating in DCM3 a wider line angle interval than the previous case. Simulated $i_{L1}(t,\varphi)$ and $i_D(t,\varphi)$ waveforms during a switching period for several significant angles are given in Fig. 22. As in the previous case, operation in DCM2 at $\varphi = 90°$, in the boundary between DCM2 and DCM3 ($\varphi_{2-3} = 84.24°$), in the boundary between DCM3 and DCM1 ($\varphi_{3-1} = 30°$), and in DCM1 at $\varphi = 30°$ can be easily verified from this figure.

The bridgeless version of the SEPIC PFC shown in Fig. 11(b) has been also simulated with the component values given in Table II and for the same values of $P_{\pi/2-A}$ and $P_{\pi/2-B}$ as in the previous cases.

Transistors $S_1$ and $S_2$ are controlled as explained at the beginning of Section IV. The line current waveforms thus obtained were exactly the same as those given in Figs. 19(b) and 21(b). Simulated $i_{L1}(t,\varphi)$ and $i_D(t,\varphi)$ waveforms for $P_{\pi/2-A}$ when

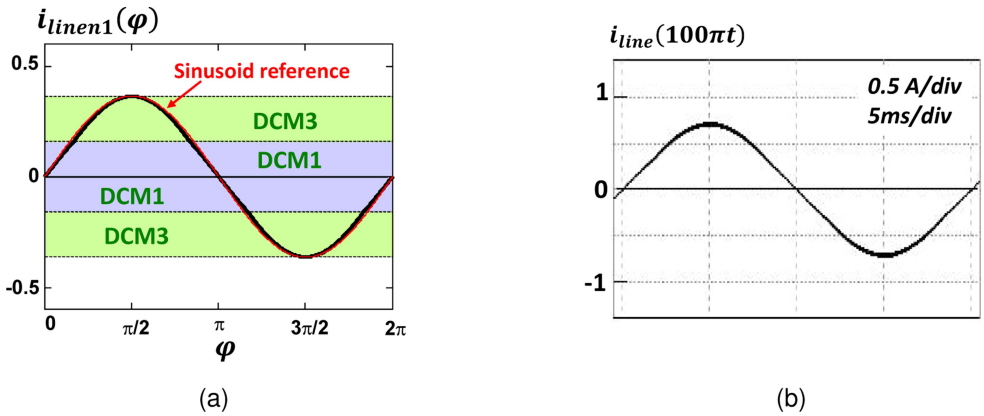


Fig. 21. Line current waveforms corresponding to the SEPIC PFC shown in Fig. 11(a) working in design point $P_{\pi/2-B}$: (a) Predicted normalized waveform. (b) Simulated waveform.

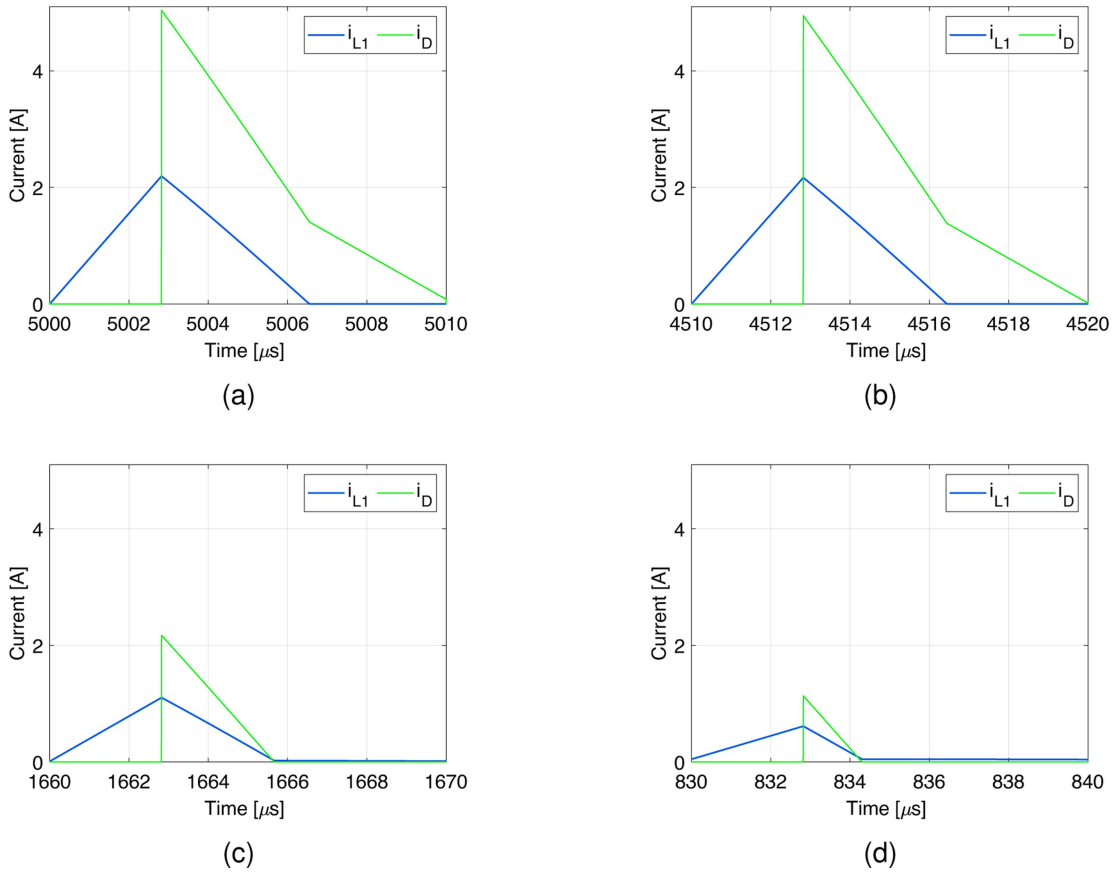


Fig. 22. Simulated $i_{L1}(t,\varphi)$ and $i_D(t,\varphi)$ waveforms corresponding to the SEPIC PFC shown in Fig. 11(a) working in design point $P_{\pi/2-B}$: (a) $\varphi = 90°$. (b) $\varphi = 84.2°$. (c) $\varphi = 30°$. (d) $\varphi = 15°$.

$\varphi = 90°$, $\varphi = 270°$, $\varphi_{3-1} = 30°$, and $\varphi_{3-1} = 210°$ are shown in Fig. 23. These waveforms agree with those in Fig. 20 for the same line angles, the only difference being that $i_{L1}(t,\varphi)$ is negative when the line voltage is also negative, as expected.

Finally, the Ćuk PFC shown in Fig. 11(c) was simulated in the same conditions as the SEPIC PFC given in Fig. 11(a). The results for the line current during a line period and for currents $i_{L1}(t,\varphi)$ and $i_D(t,\varphi)$ during a switching period agree with those for the SEPIC PFC.

### B. *Validation by Experimental Results*

A prototype SEPIC PFC was used as testing bench to verify the method proposed in this article for studying the operation

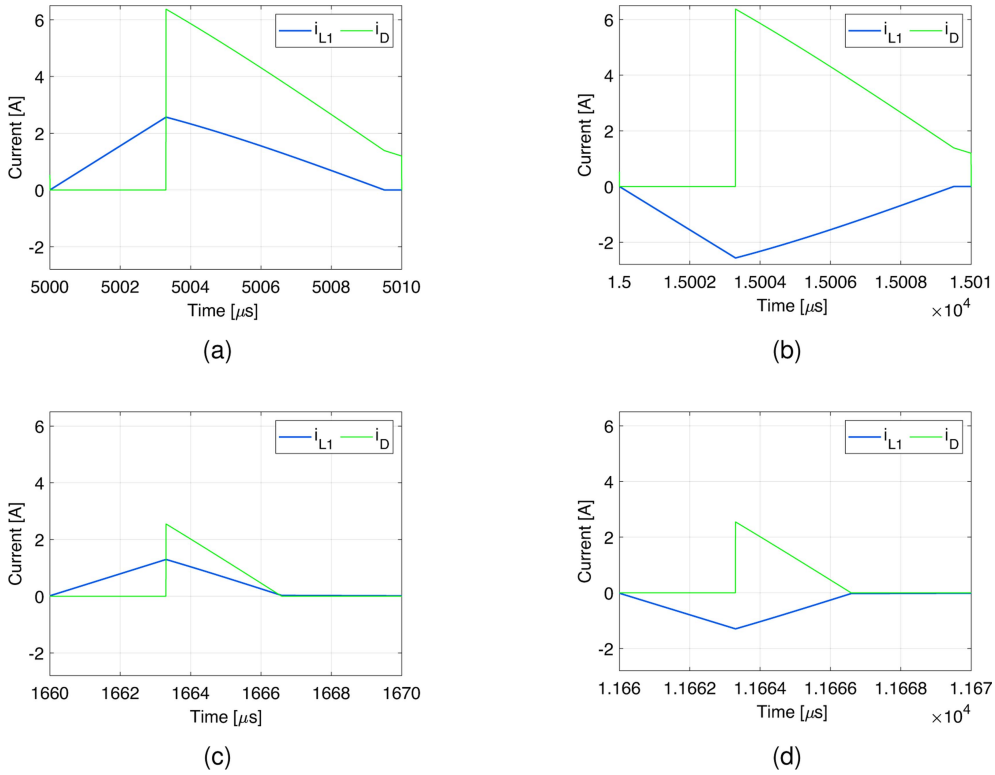


Fig. 23. Simulated $i_{L1}(t,\varphi)$ and $i_D(t,\varphi)$ waveforms corresponding to the SEPIC PFC shown in Fig. 11(b) working in design point $P_{\pi/2-A}$: (a) $\varphi = 90°$. (b) $\varphi = 270°$. (c) $\varphi = 30°$. (d) $\varphi = 210°$.

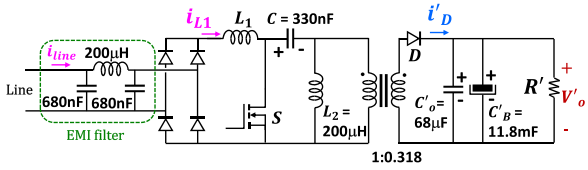


Fig. 24. SEPIC converter used for the experimental validation.

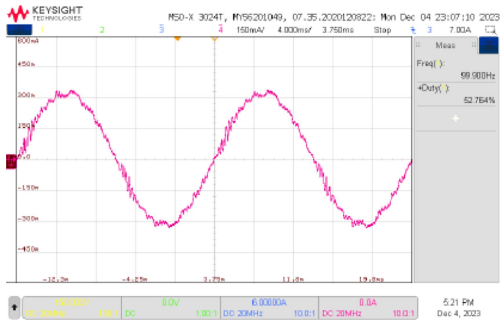


Fig. 25. Line current waveforms corresponding to operate in DCM1 ($L_1 = 3.22$ mH).

of automatic PFCs with three DCMs. The SEPIC prototype has galvanic isolation, as shown in Fig. 24. Bearing in mind that the transformer turns ratio was 1:0.318, the values of the components placed in the transformer secondary side were selected to agree with those in Table II (corresponding to a converter without galvanic isolation). Thus, $C'_o = 10C_o$, $C'_B = 10C_B$, and $R' = R/10$. Regarding electrical quantities, $V'_o = 0.318V_o$ and $i'_D = i_D/0.318$.

This prototype was initially designed to operate as ideal automatic RE, i.e., in Case 1, meaning $\alpha < M_{\pi/2}$ and $P_{\pi/2}$ placed in DCM1. To achieve the operation at this point, $L_1 = 3.22$ mH, $R' = 20.9\,\Omega$ and $d_{\text{DCM}} = 0.3$. Fig. 25 shows the line current waveform in these conditions, whereas Fig. 26 shows the waveforms corresponding to $i_{L1}$ and $i'_D$ for $\varphi = 90°$ and $\varphi = 15°$. As predicted, placing $P_{\pi/2}$ in DCM1 means operating in this mode for the entire line angle. This can be easily deduced by comparing Figs. 26 and 12(b). As expected, the line waveform was an almost perfect sinusoid. In fact, the measured THD was $4.4\%$.

The value of $L_1$ was changed by replacing the original inductor ($L_1 = 3.22$ mH) with an inductor of lower value ($L_1 = 200\,\mu$H), which means $\alpha = 1$. With this value of $L_1$, the conditions corresponding to operating in point $P_{\pi/2-A}$ and in point $P_{\pi/2-B}$ could be replicated in the prototype. The results are shown in Fig. 27 (line waveforms) and Figs. 28 and 29 ($i_{L1}$ and $i'_D$ waveforms). Regarding line waveforms, the measured THD values are $11\%$ and $5.6\%$ for operating points $P_{\pi/2-A}$ and $P_{\pi/2-B}$, respectively, whereas the predicted values were $13\%$ and $3.7\%$. The experimental waveforms obtained for $i_{L1}$ and $i'_D$ when the converter is designed to operate in point $P_{\pi/2-A}$ are shown in Fig. 28. These waveforms correspond to the same significant line angles given in Fig. 20. To properly compare the two sets of waveforms, it is important to consider the fact that $i_{L1}$ waveforms (blue traces in the simulations and pink

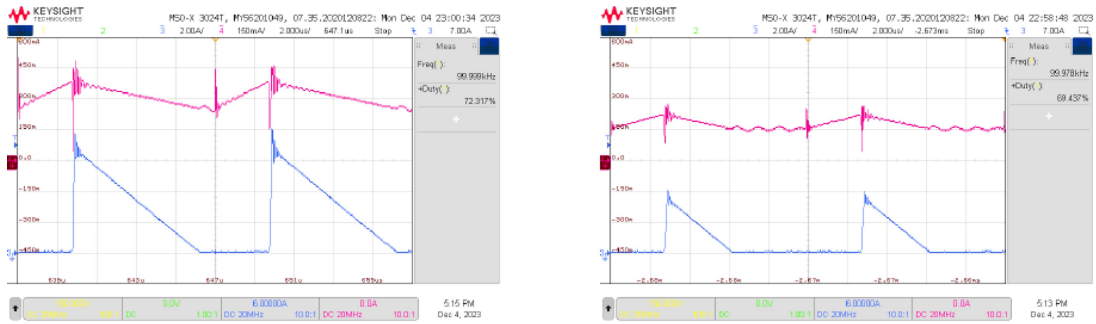


Fig. 26. Experimental $i_{L1}$ and $i'_D$ waveforms operating in DCM1 ($L_1 = 3.22$ mH): (a) $\varphi = 90°$ (approx. 5 ms). (b) $\varphi = 15°$ (approx. 0.83 ms).

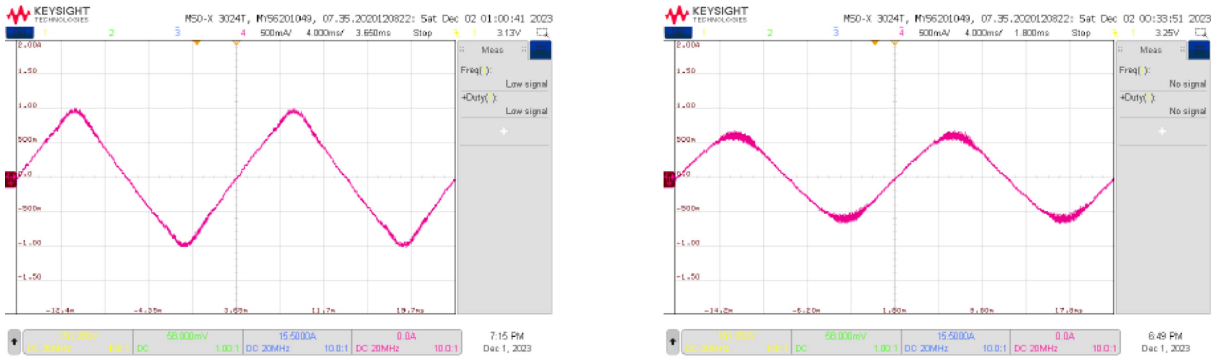


Fig. 27. Line current waveforms corresponding to place $P_{\pi/2}$ in DCM2 ($L_1 = 200\,\mu$H): (a) Working in design point $P_{\pi/2-A}$. (b) Working in design point $P_{\pi/2-B}$.

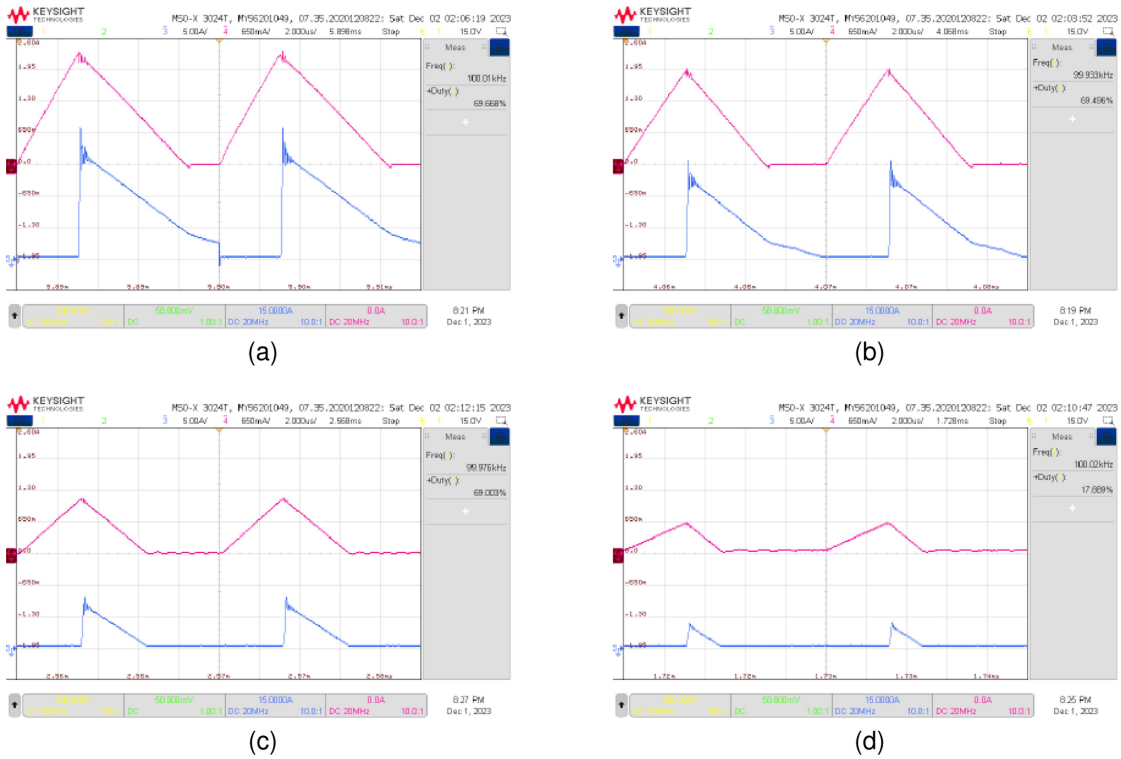


Fig. 28. Experimental $i_{L1}$ and $i'_D$ waveforms working in design point $P_{\pi/2-A}$: (a) $\varphi = 90°$ (approx. 5 ms). (b) $\varphi = 56.38°$ (approx. 3.13 ms). (c) $\varphi = 30°$ (approx. 1.67 ms). (d) $\varphi = 15°$ (approx. 0.83 ms).

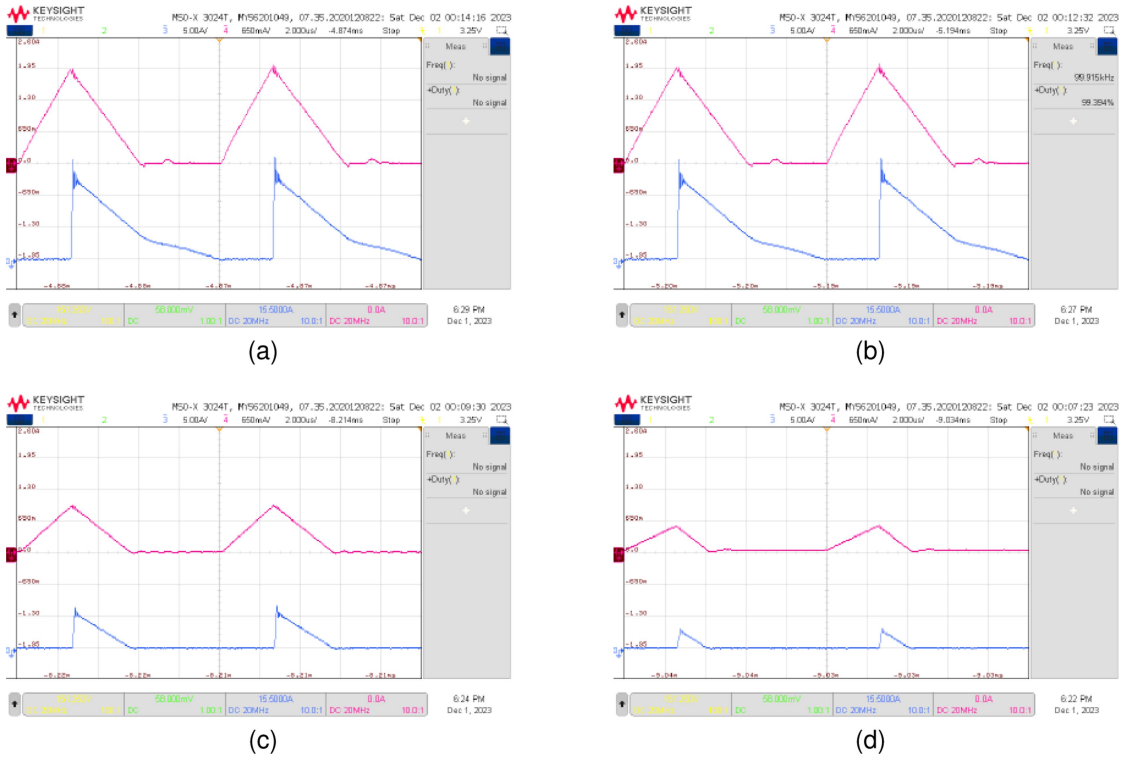


Fig. 29. Experimental $i_{L1}$ and $i'_D$ waveforms working in design point $P_{\pi/2-B}$: (a) $\varphi = 90°$ (approx. 5 ms). (b) $\varphi = 84.2°$ (approx. 4.5 ms). (c) $\varphi = 30°$ (approx. 1.67 ms). (d) $\varphi = 15°$ (approx. 0.83 ms).

traces in the experimental results) are both on the transformer primary side, whereas $i'_D$ is placed on the transformer secondary side. Therefore, $i'_D$ values (blue traces in experimental results) must be $1/0.318 = 3.145$ times as high as $i_D$ (green traces in simulations). In all cases, there was excellent agreement between simulated (Fig. 20) and experimental (Fig. 28) results, helping to validate the method proposed in this article, not only by simulation, but also by experimental results. These comments can be extended to the waveforms shown in Figs. 21 and 29 for the converter operating at point $P_{\pi/2-B}$.

## VI. Conclusion

This article presents a general, systematic method for studying the operation of dc/dc converters that involve three DCMs when they are used as automatic PFCs. This study enables accurate determination of the line current, which is essential for evaluating converter performance in this application. When a dc/dc converter is used for this purpose, the converter duty cycle is kept constant during the line period, the input voltage is a rectified sinusoidal waveform, and the output voltage is kept constant due to a bulk capacitor connected at the output port. In this situation, determination of the input current waveform is a primary concern for evaluating the feasibility of the converter as an automatic PFC.

The procedure to analyze the feasibility of a given dc/dc converter with three DCMs to be used as automatic PFC starts with a thorough study of the converter as a conventional dc/dc converter operating in a closed loop. To that end, two dimensionless parameters $k_1$ and $k_2$ must be defined. Moreover, a map of four conduction mode regions (one CCM and three DCMs) can be drawn in a plane called the $k_1k_2$ plane. For any value of the converter dc conversion ratio, a map of conduction regions can be drawn. The operation of the converter at a given constant dc conversion ratio and load corresponds to placing the operating point (defined by the values of $k_1$ and $k_2$) in the proper conduction region of the appropriate map. If the dc conversion ratio changes and the load remains constant, then the operating point remains constant, but the map changes and therefore the operating point may be placed in a different conduction mode region. On the other hand, if the dc conversion ratio remains constant and the load changes, then the map remains constant, but the operating point moves along a straight line called the "trajectory," determined by $\alpha = L_2/L_1$, (the ratio of inductances). Consequently, the operating point may again be placed in a different conduction mode region.

After this thorough study of the converter working as a conventional dc/dc converter, we can determine: 1) the value of the dc conversion ratio in each conduction mode as a function of $k_1$, $k_2$, and the converter duty cycle; 2) the mathematical equations that determine the boundaries between conduction modes in the $k_1k_2$ plane, i.e., on the map.

Once these sets of equations are obtained for operation as a conventional dc/dc converter, the study of it as a part of an automatic PFC can be addressed. That must consider the following: 1) the converter dc conversion ratio is continuously changing according to line angle $\varphi$, because the input voltage is a

rectified sinusoidal waveform. Therefore, the map of conduction regions is also continuously changing according to $\varphi$, even if the peak value of the line voltage is constant; 2) even with a constant load connected at the converter output, the load seen by the dc/dc part of the automatic PFC (i.e., the RE in Fig. 1) is continuously and synchronously changing according to line angle $\varphi$, thus moving the converter operating point along the trajectory from a given point to zero. Therefore, the two dimensionless parameters $k_1$ and $k_2$ must be replaced with $k_1(\varphi)$ and $k_2(\varphi)$.

After taking into account these continuous, synchronous variations and the conditions for working as an automatic PFC (constant duty cycle, rectified input voltage, and constant output voltage), we can finally determine the evolution of $k_1(\varphi)$ (and $k_2(\varphi) = \alpha k_1(\varphi)$) along a quarter of the line period. The evolution of $k_1(\varphi)$ during the entire line period can be easily deduced due to line current symmetries. The values of $k_1(\pi/2)$ and $\alpha$ determine the converter's starting operating point on the trajectory, which is a key concern in converter analysis and design. To work as an automatic PFC, the point with coordinates $k_1(\pi/2)$ and $\alpha k_1(\pi/2)$, called $P_{\pi/2}$ in the article, must be placed in a DCM.

As demonstrated, the evolution of $k_1(\varphi)$ is the key point in determining the converter input current, and therefore the line current. In fact, the article demonstrates that the input current is proportional to $k_1(\varphi)/|\sin(\varphi)|$.

The article included an example using the proposed method: SEPIC and Ćuk converters used as automatic PFCs. The study shows that by placing $P_{\pi/2}$ in DCM1, ideal automatic PFC (sinusoidal input current) is achieved, which is a well known result. However, converter behavior when $P_{\pi/2}$ was placed in either DCM2 or in DCM3 (lower value of the input inductor) had not been determined before. Applying the proposed method, the input current waveform was calculated in these cases, showing that the design in these conditions leads to low distortion in the line current, and therefore quasi-ideal automatic PFC can be achieved. These analytical conclusions were validated by simulation and experimental results, verifying the predicted line current and diode waveforms in several significant line angles ($90^\circ$ and line angles corresponding to conduction mode changes).

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