Capacitor Voltage Balancing Method for the Hybrid Multilevel Converter Considering Grid Voltage Sags

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***Abstract*—Compared to the traditional modular multilevel converter and alternative arm converter, the hybrid multilevel converter (HMC) exhibits superiority in terms of cost and volume. In the HMC, the pulse width of the direction switch (DS) is conventionally utilized to maintain capacitor voltage balancing (CVB). However, this method has certain limitations, including a restricted range of modulation indices and the inability to support pure reactive power operation. To address these drawbacks, a new CVB method based on the phase angle of the DS is proposed in this article. Compared to the traditional method, the proposed method enables the HMC to achieve a full range of modulation index and four-quadrant operation. Additionally, it demonstrates improved performance in terms of SM capacitance and capacitor voltage ripple, especially under severe grid voltage sags and low power factors. A comparative analysis is conducted between two CVB methods, focusing on the SM number, switch number, and SM capacitance. Furthermore, a unified control strategy considering asymmetrical and symmetrical grid voltage sags is proposed for these two CVB methods. Finally, the effectiveness and superiority of the proposed CVB methods are verified by simulation and experimental testing.**

***Index Terms*—Capacitor voltage balancing, grid voltage sag, high-voltage direct current (HVdc) transmission system, hybrid multilevel converters.**

I. Introduction

With the rapid development of new energy power generation, such as wind power and photovoltaic power, long-distance high-voltage direct current (HVdc) transmission for new energy has emerged [1], [2], [3]. The ac–dc converter plays a crucial role in voltage conversion, and reducing its size and cost has become a significant research topic of concern to scholars worldwide [4]. The modular multilevel converter (MMC) based on the half-bridge submodule (HBSM) is commonly applied in HVdc transmission systems due to its simple structure and high modularity. However, it has some drawbacks such as low submodule (SM) utilization, significant SM capacitance, and inability to block dc faults, which result in suboptimal performance in terms of size and cost [5], [6]. Although the MMC based on full-bridge SM (FBSM) endows dc fault-blocking capabilities, it requires twice the number of power switches.

To address the aforementioned drawbacks of MMC, Davidson and Trainer [7] introduced a variety of hybrid converters, including the alternative arm converter (AAC) and hybrid multilevel converter (HMC). The AAC and HMC both utilize a combination of two-level directional switches (DSs) and cascaded FBSMs to provide a smaller SM number, lower capacitor energy fluctuations, and the ability to block dc faults [8], [9]. Compared to the AAC, the HMC has a much higher SM utilization, as well as a smaller volume and cost. Thereby, it is particularly well-suited for applications with limited space, such as offshore wind power substations and receiving-end converter stations in developed cities [10]. For MMC, the cascaded SMs are always connected in parallel with the dc side, so that their total energy can be always balanced. However, the cascaded SMs of HMC or AAC are alternately connected in series with the positive or negative rail of the dc side and cannot directly absorb/release energy from/to the dc side. To achieve the capacitor voltage balancing of FBSMs, supplemental control strategies are required to guarantee that their total energy accumulation over the fundamental period is equal to zero [8]. Therefore, the conventional capacitor voltage balancing (CVB) methods used for MMC are not sufficient for AAC or HMC, which has hindered their practical application.

For a long time, there have been fewer studies on the CVB method of the HMC. Xue et al. [11] first proposed a CVB control method based on the regulation of the pulse width (PW) of DSs, which is called the PW-CVB method in this article. However, the HMC with this method has limited operational capabilities as it can merely operate effectively within a narrow range of modulation index and is unable to handle severe grid voltage sags. In contrast, the current research covers a broader range of CVB methods for AAC, some of which have the potential to be applied to HMC. The most well-known CVB method for AAC is the overlap control [12], [13], [14], by which both the upper and lower bridge arms are simultaneously activated for a short duration of overlap, thus enabling control of the circulating current to achieve the CVB of the FBSMs.

Depending on the duration of the overlap period, it can be categorized as short-overlap and extended-overlap control. The

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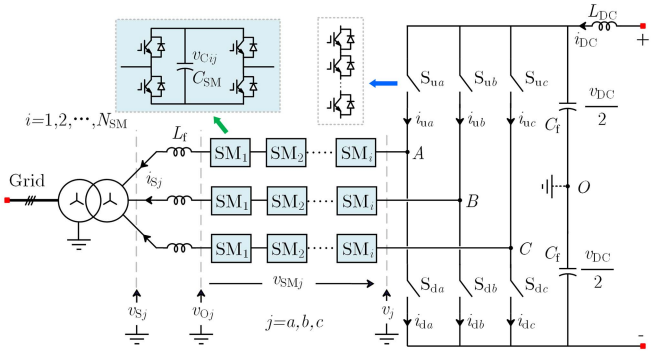


Fig. 1. Topology of HMC.

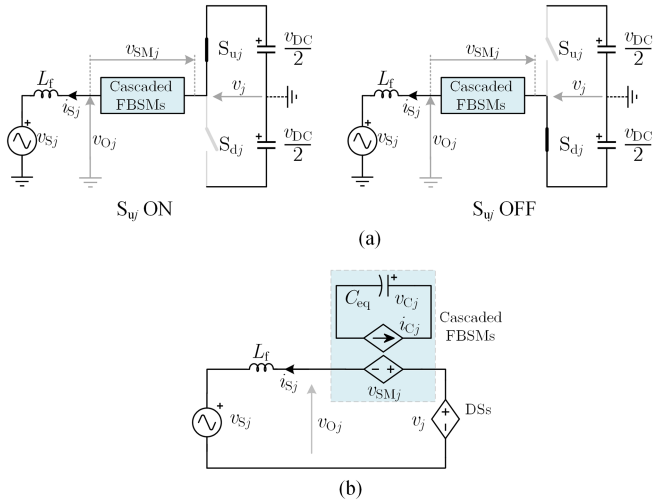


Fig. 2. Operational principle and equivalent circuit of the HMC. (a) Operational principle. (b) AC side equivalent circuit.

duration of the short-overlap control is generally less than 10° [15], [16]. However, in the case of severe grid voltage sags, the extreme imbalance of FBSMs will result in a substantial surge in the demand for circulating current [17], which may exceed the maximum current limit of the power switches. To improve the CVB capability, the extended-overlap control with a duration of 60° can be implemented [18], [19], [20]. However, the operation mode of the AAC with extended-overlap control is similar to that of a conventional MMC, leading to extra SMs, abundant DSs, and increased loss [9]. Unfortunately, the overlap control cannot be applied to the HMC due to the placement of the cascaded FBSMs on the ac side. The FBSMs are unable to establish an energy balance path with the dc link, as the upper and lower DS are not permitted to overlap (short-circuit). In addition to the overlap control, Nguyen et al. [21] proposed a CVB method for AAC based on the phase angle of the grid current. Nevertheless, the active and reactive power of AAC with this method cannot be independently controlled, as the converter must absorb reactive power from the grid. In [22], a third-order harmonic injection scheme is proposed for the CVB control of the time-sharing AAC. Yet, it also has a limited range of modulation index, which restricts the ac fault ride-through ability of the AAC. Although the methods presented in [21] and [22] can be easily applied to HMC, they still have these unavoidable drawbacks and inherent limitations. To enhance the operating capability of AAC under a lower modulation index, CVB methods based on regulating the switching pattern of DSs were proposed in [17], [23], and [24]. Furthermore, a zero-sequence voltage injection scheme was introduced to address the imbalance issue between the upper and lower bridge arms [17]. However, it should be emphasized that HMC has only one branch of cascaded FBSMs in each phase and does not suffer from such imbalance issues, thereby, these methods are challenging to implement in HMC.

To address the limitations of the existing CVB methods for HMC, this article proposes a new CVB method based on the phase angle (PA) of DSs, which is named the PA-CVB method. The main contribution and advantages of the proposed method include the following.

1) Unifying the theory on the CVB method of HMC, i.e., the energy balance of HMC can be achieved by adjusting the PW or phase angle of the DS's switching signal.
2) Effectively solving the CVB issues even under different symmetrical and asymmetrical grid voltage sags.
3) Enabling the operation of HMC across the full range of modulation index and four quadrants with a smaller SM capacitance requirement and faster response speed compared to the traditional PW-CVB method.

The rest of this article is organized as follows. Section II introduces the operating principle and CVB control methods of the HMC. Section III compares the differences between the traditional and the proposed CVB method. Section IV proposes an overall control strategy for HMC. Sections V and VI carry out simulation and experimental verification, respectively. Finally, Section VII concludes this article.

II. Operation and Energy Balance Method

A. Topology and Operating Principle

The topology of HMC is illustrated in Fig. 1 [5], [7], [11]. Each phase of the converter is comprised of two parts: 1) the cascaded FBSMs and 2) the upper/lower direction switches S_{uj} and S_{dj} (j = a,b,c). Each DS is composed of N_{DS} series connected IGBTs. In Fig. 1, L_f and L_{dc} are filter inductors on the ac side and dc side, respectively. C_{SM} and C_f are SM capacitors and dc side filter capacitors, respectively. v_{dc} and i_{dc} represent the dc voltage and current, respectively. i_{uj} and i_{dj} represent the current of the upper and lower DSs, respectively. v_{Sj} and i_{Sj} represent the grid current and voltage, respectively. v_{Oj} is the output voltage of the converter, v_j is the ABC port voltage, v_{SMj} is the voltage of the cascaded FBSMs, and v_{Cij} (i = 1, 2, 3, …, N_{SM}) is the capacitor voltage of the ith FBSM in the phase j.

The grid voltage v_{Sj} and current i_{Sj} are defined as

$$v_{Sj} = V_m \sin(\omega t + \theta_j),\ i_{Sj} = I_m \sin(\omega t + \varphi + \theta_j) \quad (1)$$

where V_m and I_m are the amplitudes of grid voltage and current, respectively, ω is the grid angular frequency, φ is the power factor angle, and θ_j is the initial phase of j-phase grid voltage.

Fig. 2(a) illustrates the single-phase operational principle of the HMC during DSs switching. The voltage equation on the ac

side can be expressed as

$$v_{\mathrm{S}j} + L_{\mathrm{f}}\frac{\mathrm{d}i_{\mathrm{S}j}}{\mathrm{d}t} = v_{\mathrm{O}j}, v_{\mathrm{O}j} = v_j - v_{\mathrm{SM}j} \tag{2}$$

where $v_{\mathrm{O}j}$ is approximately equal to $v_{\mathrm{S}j}$ in steady state, due to the relatively small voltage drop across L_{f}. Besides, $S_{\mathrm{u}j}$ and $S_{\mathrm{d}j}$ are strictly complementary conducted. When $S_{\mathrm{u}j}$ turns ON, v_j is equal to $0.5v_{\mathrm{dc}}$. When $S_{\mathrm{u}j}$ turns OFF, v_j is equal to $-0.5v_{\mathrm{dc}}$. Then, $v_{\mathrm{SM}j}$ is approximately equal to

$$v_{\mathrm{SM}j} = \begin{cases} {}^1\!/_2 v_{\mathrm{dc}} - v_{\mathrm{S}j}, S_{\mathrm{u}j}\mathrm{on} \\ -{}^1\!/_2 v_{\mathrm{dc}} - v_{\mathrm{S}j}, S_{\mathrm{u}j}\mathrm{off} \end{cases}. \tag{3}$$

Thus, by controlling the output branch voltage $v_{\mathrm{SM}j}$ of the cascaded FBSMs, the HMC can theoretically operate in four quadrants.

Based on the average modeling approach [1], the single-phase equivalent circuit for the ac side of the HMC can be obtained, as shown in Fig. 2(b). The switching characteristic of the DSs can be equivalent to a voltage source v_j on the ac side. The cascaded FBSMs can be equivalent to one FBSM with capacitance and capacitor voltage equal to

$$C_{\mathrm{eq}} = C_{\mathrm{SM}}/N_{\mathrm{SM}}, v_{\mathrm{C}j} = \sum_{i=1}^{N_{\mathrm{SM}}} v_{\mathrm{C}ij}. \tag{4}$$

Then, the ac side of the equivalent FBSM is represented by a voltage source $v_{\mathrm{SM}j}$, while the dc side is represented by a current source $i_{\mathrm{C}j}$. These sources are interconnected by the following equations:

$$v_{\mathrm{SM}j} i_{\mathrm{S}j} = i_{\mathrm{C}j} v_{\mathrm{C}j}, i_{\mathrm{C}j} = C_{\mathrm{eq}}\frac{\mathrm{d}v_{\mathrm{C}j}}{\mathrm{d}t}. \tag{5}$$

Thus, $v_{\mathrm{C}j}$ can be solved as

$$v_{\mathrm{C}j} = \sqrt{\frac{2}{C_{\mathrm{eq}}}\int v_{\mathrm{SM}j} i_{\mathrm{S}j}\mathrm{d}t + {v_{\mathrm{C}j0}}^2} \tag{6}$$

where $v_{\mathrm{C}j0}$ is the initial voltage of C_{eq}. To maintain the voltage or energy balance of the C_{eq}, it is important to ensure that the integral term in (6), which represents the total energy of the cascaded FBSMs, has a value of 0 within a fundamental period. By combining this with (3), it becomes evident that controlling the switching signal of the DSs can adjust the total energy of the cascaded FBSMs. Furthermore, the PW and phase angle are two main factors of a switching signal.

B. Conventional PW-CVB Method

For the conventional PW-CVB method, the PW of the DS is applied. The key voltage and current under this method are shown in Fig. 3(a). The switching signal of the DS can be expressed as

$$S_{\mathrm{u}j} = \bar{S}_{\mathrm{d}j} = \mathrm{sgn}\left(\sin(\omega t + \theta_j) + V_{0j}\right) \tag{7}$$

where $\mathrm{sgn}(x)$ is a sign function, when $x \geq 0$, $\mathrm{sgn}(x) = 1$, otherwise $\mathrm{sgn}(x) = 0$. $V_{0j} \in [-1, 1]$ is the offset value of j-phase. By adjusting V_{0j}, the PW of DS can be changed from 0% to 100%.

Take phase a as an example for analysis, and set $\theta_a = 0$. Then, the energy of the cascaded FBSMs $E_{\mathrm{SM}a}$ over a fundamental period can be calculated by integrating the product of $i_{\mathrm{S}a}$ and $v_{\mathrm{SM}a}$, i.e.,

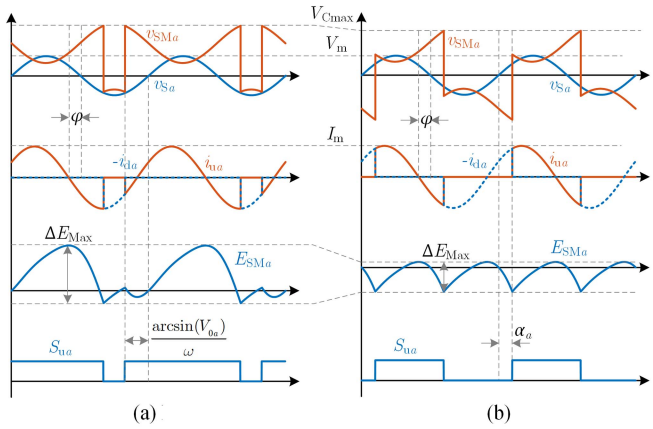


Fig. 3. Key voltage and current waveforms of the HMC. (a) PW-CVB method. (b) PA-CVB method.

$$\begin{aligned} E_{\mathrm{SM}a} = &\int_{t1}^{t2} ({}^1\!/_2 V_{\mathrm{DC}} - V_{\mathrm{m}}\sin(\omega t)) I_{\mathrm{m}}\sin(\omega t + \varphi)\mathrm{d}t \\ &+ \int_{t2}^{t3} (-{}^1\!/_2 V_{\mathrm{DC}} - V_{\mathrm{m}}\sin(\omega t)) I_{\mathrm{m}}\sin(\omega t + \varphi)\mathrm{d}t \end{aligned} \tag{8}$$

with

$$t_1 = -\frac{\arcsin(V_{0a})}{\omega}, t_2 = \frac{\pi}{\omega} - t_1, t_3 = \frac{2\pi}{\omega} + t_1. \tag{9}$$

By solving (9) and (8), the following (10) can be obtained:

$$E_{\mathrm{SM}a} = \frac{I_{\mathrm{m}}\cos(\varphi)\left(2V_{\mathrm{dc}}\sqrt{1 - {V_{0a}}^2} - \pi V_{\mathrm{m}}\right)}{\omega}. \tag{10}$$

Set $E_{\mathrm{SM}j} = 0$, the value of V_{0j} for maintaining the capacitor energy balance of the HMC can be expressed as

$$V_{0j} = \pm\sqrt{1 - \left(\frac{\pi}{4}M_j\right)^2} \tag{11}$$

where $M_j = 2V_{\mathrm{m}}/V_{\mathrm{dc}}$, which is defined as the modulation index of phase j. Previous research [11] suggests that to maintain the dc voltage, the PW of DS needs to be limited. Thus, the HMC can only operate within a narrow modulation index range of $[2\sqrt{3}/\pi, 4/\pi]$. However, based on (11), the HMC can theoretically operate within the modulation index range of $[0, 4/\pi]$. Fig. 4(a) illustrates the relationship between V_{0j} and M_j. It can be inferred that if grid voltage sag causes the modulation index M_j to change from M_1 to M_2, the capacitor voltage balance can be maintained by adjusting V_{0j} from V_{01} to V_{02}. Either positive or negative V_{0j} is feasible, but we only use the positive one in this article.

C. Proposed PA-CVB Method

To solve the drawbacks of the traditional PW-CVB method, a new capacitor voltage balancing control method based on the phase angle of DS is proposed in this article. The key voltage

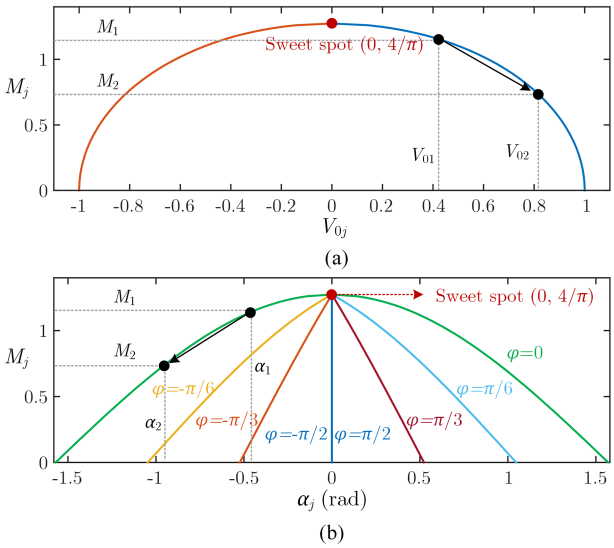


Fig. 4. Required V_{0j} and α_j for maintaining SM capacitor voltage balance under different modulation indices M_j. (a) PW-CVB method. (b) PA-CVB method.

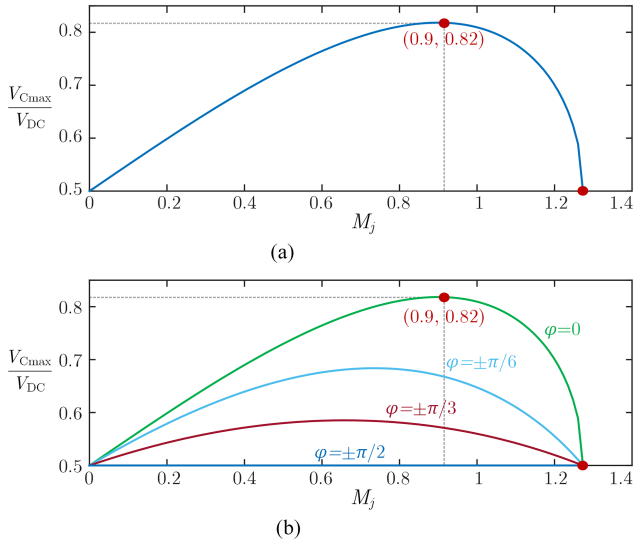


Fig. 5. Required maximal SM branch voltage under (a) traditional PW-CVB method and (b) proposed PA-CVB method. (a) PW-CVB method. (b) PA-CVB method.

and current under the PA-CVB method are shown in Fig. 3(b). The switching signal of the DS can be expressed as

$$S_{\mathrm{u}j} = \bar{S}_{\mathrm{d}j} = \mathrm{sgn}\left(\sin(\omega t + \theta_j - \alpha_j)\right) \tag{12}$$

where $\alpha_j \in [-\pi/2, \pi/2]$ is the phase angle at which the conduction moment of the upper DS $S_{\mathrm{u}j}$ lags behind the grid voltage of the phase j. The PW of the DS is kept constant at 50% which is different from that of the PW-CVB method. Similarly, the energy of the cascaded FBSMs $E_{\mathrm{SM}a}$ over a fundamental period can be also calculated by integrating the product of $i_{\mathrm{S}a}$ and $v_{\mathrm{SM}a}$, i.e.,

$$\begin{aligned} E_{\mathrm{SM}a} &= \int_{\alpha_a/\omega}^{(\pi+\alpha_a)/\omega} (1/2 V_{\mathrm{dc}} - V_{\mathrm{m}} \sin(\omega t)) I_{\mathrm{m}} \sin(\omega t + \varphi) \mathrm{d}t \\ &+ \int_{(\pi+\alpha_a)/\omega}^{(2\pi+\alpha_a)/\omega} (-1/2 V_{\mathrm{dc}} - V_{\mathrm{m}} \sin(\omega t)) I_{\mathrm{m}} \sin(\omega t + \varphi) \mathrm{d}t \\ &= \frac{I_{\mathrm{m}} \ (2\, V_{\mathrm{dc}} \ \cos(\alpha_a + \varphi) - \pi\, V_{\mathrm{m}} \ \cos(\varphi))}{\omega}. \end{aligned} \tag{13}$$

Set $E_{\mathrm{SM}j} = 0$, the value of α_j for maintaining HMC capacitor energy balance can be expressed as

$$\alpha_j = \begin{cases} -\arccos\left(\frac{\pi M_j \cos\varphi}{4}\right) - \varphi, \varphi \in \left[-\frac{\pi}{2}, 0\right) \\ \arccos\left(\frac{\pi M_j \cos\varphi}{4}\right) - \varphi, \varphi \in \left[0, \frac{\pi}{2}\right]. \end{cases} \tag{14}$$

Fig. 4(b) presents the values of α_j under different M_j and φ conditions. It can be observed that the polarity of α_j aligns with that of φ, and α_j decreases as $|\varphi|$ increases. Under the PA-CVB method, the HMC can also operate within a wide modulation range of $[0, 4/\pi]$. When the grid voltage sag causes the modulation index M_j to change from M_1 to M_2, if α_j is adjusted from α_1 to α_2, then the energy of the cascaded FBSMs can be remaintained at 0. Compared with the PW-CVB, the ripple frequency of $v_{\mathrm{C}j}$ is twice the fundamental frequency, thereby leading to a reduced SM capacitance.

III. Component Design and Comparisons

A. Number of SMs

The selection of SM number mainly considers two aspects as follows.

1) When a dc short-circuit fault occurs, the FBSMs should be able to block the fault current. Thus, the maximum total voltage of the cascaded FBSMs V_{Cmax} needs to be

$$V_{\mathrm{C\,max}} \geq V_{\mathrm{m}} = 1/2 V_{\mathrm{dc}} M_j. \tag{15}$$

2) When V_{0j} or α_j changes, the cascaded FBSMs should be able to synthesize the required branch voltage.

According to Fig. 3, varying grid voltage sag (modulation index) can lead to different maximum output voltages V_{Cmax} of the cascaded FBSMs. Under the traditional PW-CVB method, V_{Cmax} can be calculated as

$$\begin{aligned} V_{\mathrm{C\,max}} &= 1/2 V_{\mathrm{dc}} + V_{\mathrm{m}} \left|\sin(\omega T)\right|, T = \arcsin(V_0)/\omega \\ &\Rightarrow V_{\mathrm{C\,max}} = 1/2 V_{\mathrm{dc}} + V_{\mathrm{m}} \left|V_0\right|. \end{aligned} \tag{16}$$

By substituting (11) to (16), we can obtain

$$\frac{V_{\mathrm{C\,max}}}{V_{\mathrm{dc}}} = \frac{1}{2} + \frac{1}{2} M_j \sqrt{1 - \left(\frac{\pi}{4} M_j\right)^2}. \tag{17}$$

Fig. 5(a) shows the relationship between $V_{\mathrm{Cmax}}/V_{\mathrm{dc}}$ and M_j. It can be observed that as M_j decreases, $V_{\mathrm{Cmax}}/V_{\mathrm{dc}}$ initially increases and then decreases, reaching a maximum value of approximately 0.82 when M_j is around 0.9.

Under the proposed PA-CVB method, the maximum total voltage of the FBSMs V_{Cmax} can be calculated as

$$V_{\mathrm{C\,max}} = 1/2 V_{\mathrm{dc}} + V_{\mathrm{m}} \left|\sin\alpha\right|. \tag{18}$$

By substituting (14) to (18), we can obtain

$$\frac{V_{\mathrm{C\,max}}}{V_{\mathrm{dc}}}$$

$$= \begin{cases} \frac{1}{2} + \frac{M_j}{2}\left|\sin\left[-\arccos\left(\frac{\pi M_j \cos\varphi}{4}\right) - \varphi\right]\right|, \varphi \in \left[-\frac{\pi}{2}, 0\right) \\ \frac{1}{2} + \frac{M_j}{2}\left|\sin\left[\arccos\left(\frac{\pi M_j \cos\varphi}{4}\right) - \varphi\right]\right|, \varphi \in \left[0, \frac{\pi}{2}\right]. \end{cases} \tag{19}$$

The relationship of $V_{\mathrm{Cmax}}/V_{\mathrm{dc}}$ versus M_j and φ is shown in Fig. 5(b). It can be found that the curve when $\varphi = 0$ remains consistent with the traditional method. However, as $|\varphi|$ increases, the peak value of $V_{\mathrm{Cmax}}/V_{\mathrm{dc}}$ decreases. Since a certain amount of reactive power (i.e., $|\varphi|>0$) needs to be injected into the grid when grid voltage sags, the proposed method will have a slightly smaller V_{Cmax} compared to the traditional one. For simplicity, this article assumes that the two methods have the same V_{Cmax}. To generate this voltage throughout the full-range modulation index, the total capacitor voltage of all SMs in the cascaded FBSMs should be larger than $0.82V_{\mathrm{dc}}$. This condition also satisfies the requirements stated in (15). Assume the nominal SM capacitor voltage is V_{CN}, the SM number in each phase can be determined as

$$N_{\mathrm{SM}} = 0.82V_{\mathrm{dc}}/V_{\mathrm{CN}}. \tag{20}$$

For traditional HBSM-MMC, the number of SMs per phase is calculated as $2V_{\mathrm{dc}}/V_{\mathrm{CN}}$. Therefore, HMC can reduce SM number by 59%.

B. Number of Switches

The switch number in the DS is independent of the control method. When the upper or lower DS is turned ON, the opposite DS always needs to withstand the full dc voltage V_{dc}. Therefore, assuming that the switch type used in DS is the same as that used in FBSMs, the total number of switches per phase for HMC can be determined as

$$N = 4N_{\mathrm{SM}} + 2N_{\mathrm{DS}} = 5.28V_{\mathrm{dc}}/V_{\mathrm{CN}}. \tag{21}$$

For traditional HBSM-MMC and FBSM-MMC, the total number of switches per phase is calculated as $4V_{\mathrm{dc}}/V_{\mathrm{CN}}$ and $8V_{\mathrm{dc}}/V_{\mathrm{CN}}$, respectively. The HMC falls in between these two converters in terms of switch number, but the HMC is capable of dc fault blocking.

C. SM Capacitance

The energy and voltage fluctuations of the SM capacitor are closely affected by different CVB methods, thereby impacting the SM capacitance. The voltage expression of the equivalent SM capacitance, i.e., (6), can be rewritten as

$$1/2C_{\mathrm{eq}}\left({V_{Cj\_\mathrm{Max}}}^2 - {V_{Cj\_\mathrm{Min}}}^2\right) = \int_{t_{\mathrm{Min}}}^{t_{\mathrm{Max}}} v_{\mathrm{SM}j} i_{\mathrm{S}j} \mathrm{d}t = \Delta E_{\mathrm{Max}} \tag{22}$$

where V_{Cj_Max} and V_{Cj_Min} are the maximum and minimum voltage at time t_{Max} and t_{Min}, respectively. ΔE_{Max} is the peak-to-valley difference of SM capacitor energy, which is also called maximum energy fluctuation. Assuming the average voltage V_{C} is equal to $0.5(V_{Cj\_\mathrm{Max}}+V_{Cj\_\mathrm{Min}})$, and the voltage fluctuation

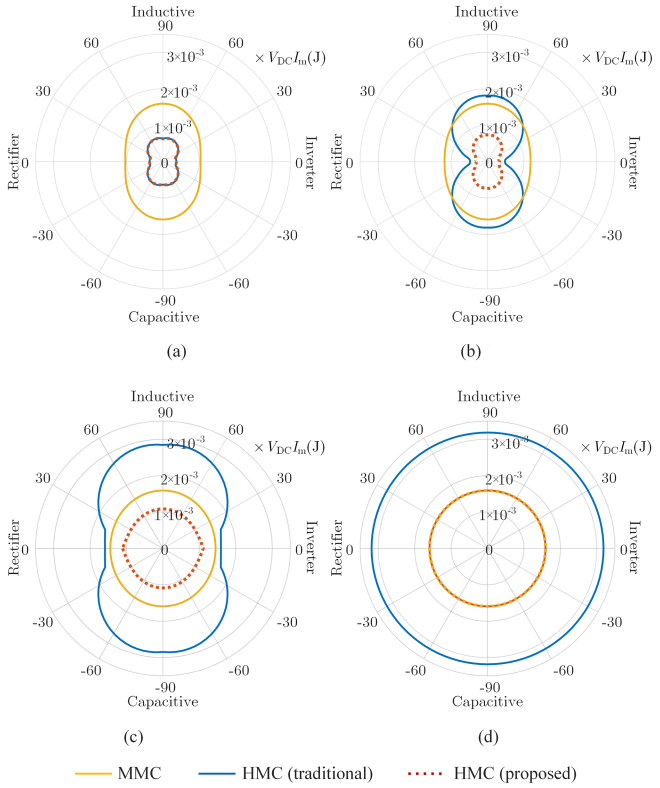


Fig. 6. Maximum energy fluctuation of the MMC, HMC with traditional PW-CVB method, and HMC with proposed PA-CVB method. (a) M (MMC) = 1, M (HMC) = $4/\pi$. (b) M (MMC) = 0.85, M (HMC) = $0.85*4/\pi$. (c) M (MMC) = 0.5, M (HMC) = $0.5*4/\pi$. (d) M (MMC) = 0, M (HMC) = 0.

ΔV is equal to $0.5(V_{Cj\_\mathrm{Max}}-V_{Cj\_\mathrm{Min}})$, then the SM capacitance can be calculated by

$$C_{\mathrm{SM}} = \frac{N\Delta E_{\mathrm{Max}}}{2V_{\mathrm{C}}\Delta V}. \tag{23}$$

By substituting (1) and (3) to (22), we can obtain the ΔE_{Max} waveforms of HMC using both the conventional and proposed methods, as shown in Fig. 6. This figure also includes the ΔE_{Max} waveforms of the conventional half-bridge MMC as a reference. These waveforms are calculated under different modulation indexes and power factor angles, including rectifier and inverter operation states.

When comparing the HMC under the two methods, it is observed that the ΔE_{Max} of the two methods remains consistent when the modulation index M is $4/\pi$ (the sweet-spot). As M decreases, the ΔE_{Max} of both methods increases, but the ΔE_{Max} of the traditional method is generally 2 to 3 times larger than that of the proposed method. Thus, the SM capacitance of the traditional method is greater than the proposed method. Under the traditional method, it can be also found that ΔE_{Max} becomes extremely large when $M = 0$. This indicates that the voltage fluctuation of the SM capacitor will be much higher after a grid voltage sag, which can hinder the safe and stable operation of the converter. When comparing the traditional MMC and the HMC using the proposed PA-CVB method, it is evident that the

TABLE I
SINGLE-PHASE PARAMETER REQUIREMENTS FOR MMC AND HMC

Parameters	MMC	HMC (traditional)	HMC (proposed)
N_{SM}	122*2	100	100
N_{DS}	0	122	122
N	488 (HBSM) 976 (FBSM)	644	644
C_{SM}	7.92 mF	3.86 mF	2.67 mF
ΔE_{max}	259.70*2 kJ	105.04 kJ	72.78 kJ

ΔE_{Max} of the proposed method is consistently smaller than that of MMC, except when $M = 0$.

The electrical parameters at the rated operating point are generally used for capacitor design. Taking $M(\mathrm{MMC}) = 0.85$, $M(\mathrm{HMC}) = 0.85\times 4/\pi$, $\varphi = 0$, $V_{\mathrm{dc}} = 200$ kV, $I_{\mathrm{m}} = 1.1$ kA, $\Delta V = 5\%V_{\mathrm{C}}$, and $V_{\mathrm{CN}} = 1.65$ kV as an example, based on (20), (21), and (23), the single-phase component parameter requirements for different converters can be obtained, as shown in Table I. It can be noticed that the number of SMs N_{SM} in HMC is reduced by 59% compared to MMC. Compared to the HBSM-MMC and FBSM-MMC, the number of switches N in the HMC has increased by 32% and decreased by 34%, respectively, but the HMC has dc fault-blocking capability. In addition, the SM capacitance of the HMC under the proposed PA-CVB method is only 2.67 mF, which is 30.8% lower than that of the HMC under the traditional PW-CVB method and 66.3% lower than that of classical MMC. The superiority of the proposed method in terms of cost and size can, thus, be obtained.

D. Power Loss Estimation

To simplify the calculation of the power loss, the following assumptions are made.

1) Only the conduction loss of the IGBT/diode is considered, as the switching loss is relatively small.
2) The forward voltages of the IGBT and the diode are the same, expressed as V_{f}, and other parameters such as internal resistance are neglected.
3) The FBSMs and DSs use the same type of switches.

According to the operation principle of the FBSM, two switching devices (two IGBTs, two diodes, or one IGBT and one diode) are always activated to carry the grid current irrespective of whether the FBSM is positively inserted, negatively inserted, or bypassed, and regardless of the direction of grid current [17], [23]. Thus, the conduction power loss of the cascaded FBSMs per phase under the two CVB methods can be calculated by

$$\begin{aligned} P_{\mathrm{SM}}(\mathrm{PW-CVB}) &= P_{\mathrm{SM}}(\mathrm{PA-CVB}) \\ &= 2N_{\mathrm{SM}}V_{\mathrm{f}} \times \frac{1}{T}\int_0^{2\pi/\omega} |I_{\mathrm{m}}\sin(\omega t+\varphi)|\,\mathrm{d}t \\ &= \frac{4N_{\mathrm{SM}}V_{\mathrm{f}}I_{\mathrm{m}}}{\pi} = \frac{3.28V_{\mathrm{dc}}V_{\mathrm{f}}I_{\mathrm{m}}}{\pi V_{\mathrm{CN}}}. \end{aligned} \tag{24}$$

The IGBTs and diodes in DSs conduct when the arm current is positive and negative, respectively. The conduction power losses of DSs per phase under the two CVB methods are calculated by

$$\begin{aligned} P_{\mathrm{DS}}(\mathrm{PW-CVB}) &= \underbrace{\frac{1}{T}N_{\mathrm{DS}}V_{\mathrm{f}}\int_{t1}^{t2} |I_{\mathrm{m}}\sin(\omega t+\varphi)|\,\mathrm{d}t}_{\mathrm{upperDS}} \\ &+ \underbrace{\frac{1}{T}N_{\mathrm{DS}}V_{\mathrm{f}}\int_{t2}^{t3} |I_{\mathrm{m}}\sin(\omega t+\varphi)|\,\mathrm{d}t}_{\mathrm{lowerDS}} = \frac{2N_{\mathrm{DS}}V_{\mathrm{f}}I_{\mathrm{m}}}{\pi} \\ &= \frac{2V_{\mathrm{dc}}V_{\mathrm{f}}I_{\mathrm{m}}}{\pi V_{\mathrm{CN}}} \end{aligned} \tag{25}$$

$$\begin{aligned} P_{\mathrm{DS}}(\mathrm{PA-CVB}) &= \underbrace{\frac{1}{T}N_{\mathrm{DS}}V_{\mathrm{f}}\int_{\alpha_a/\omega}^{(\pi+\alpha_a)/\omega} |I_{\mathrm{m}}\sin(\omega t+\varphi)|\,\mathrm{d}t}_{\mathrm{upperDS}} \\ &+ \underbrace{\frac{1}{T}N_{\mathrm{DS}}V_{\mathrm{f}}\int_{(\pi+\alpha_a)/\omega}^{(2\pi+\alpha_a)/\omega} |I_{\mathrm{m}}\sin(\omega t+\varphi)|\,\mathrm{d}t}_{\mathrm{lowerDS}} = \frac{2N_{\mathrm{DS}}V_{\mathrm{f}}I_{\mathrm{m}}}{\pi} \\ &= \frac{2V_{\mathrm{dc}}V_{\mathrm{f}}I_{\mathrm{m}}}{\pi V_{\mathrm{CN}}}. \end{aligned} \tag{26}$$

It can be found from (25) and (26) that the power loss of DSs under the two methods is also the same. Therefore, the total power loss of the switches per phase can be obtained by

$$\begin{aligned} P_{\mathrm{Loss}}(\mathrm{PW-CVB}) &= P_{\mathrm{Loss}}(\mathrm{PA-CVB}) = P_{\mathrm{SM}} + P_{\mathrm{DS}} \\ &= \frac{5.28V_{\mathrm{dc}}V_{\mathrm{f}}I_{\mathrm{m}}}{\pi V_{\mathrm{CN}}}. \end{aligned} \tag{27}$$

However, under the traditional PW-CVB method, since t_1–t_3 [see (9)] differs with M, the upper and lower DSs have different power losses except when $M = \pi/4$. It can result in inconsistent heat generation and lifespan of power switches, potentially affecting the reliability of the system.

The total power loss of switches per phase of a typical FBSM-MMC can be expressed as [11]

$$\begin{aligned} &P_{\mathrm{Loss}}(\mathrm{FB-MMC}) \\ &= \frac{2V_{\mathrm{DC}}V_{\mathrm{f}}I_{\mathrm{m}}}{\pi V_{\mathrm{CN}}}\left[\begin{array}{l} 2\sqrt{1-\left(1/2 m\cos\varphi\right)^2} \\ +m\cos\varphi\arcsin\left(1/2 m\cos\varphi\right) \end{array}\right]. \end{aligned} \tag{28}$$

The power loss of the HMC and FBSM-MMC under different M and φ is presented in Fig. 7. It can be seen that the power loss of the HMC is greater than that of the FBSM-MMC, as the main power has to flow through both the DS and cascaded FBSMs. Therefore, the HMC is more suitable for applications where space is at a premium.

IV. CONTROL STRATEGY FOR HMC

To ensure that the SM capacitor voltage remains balanced even during conditions such as load variation, faults, parameter differences, and sampling errors, the closed-loop controllers are necessary to dynamically generate the corresponding V_{0j} and α_j. The PW and phase angle are two control dimensions of the switching signal of the DS. Thus, this article presents

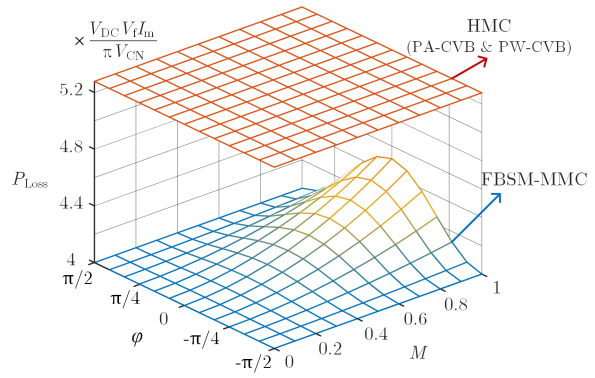
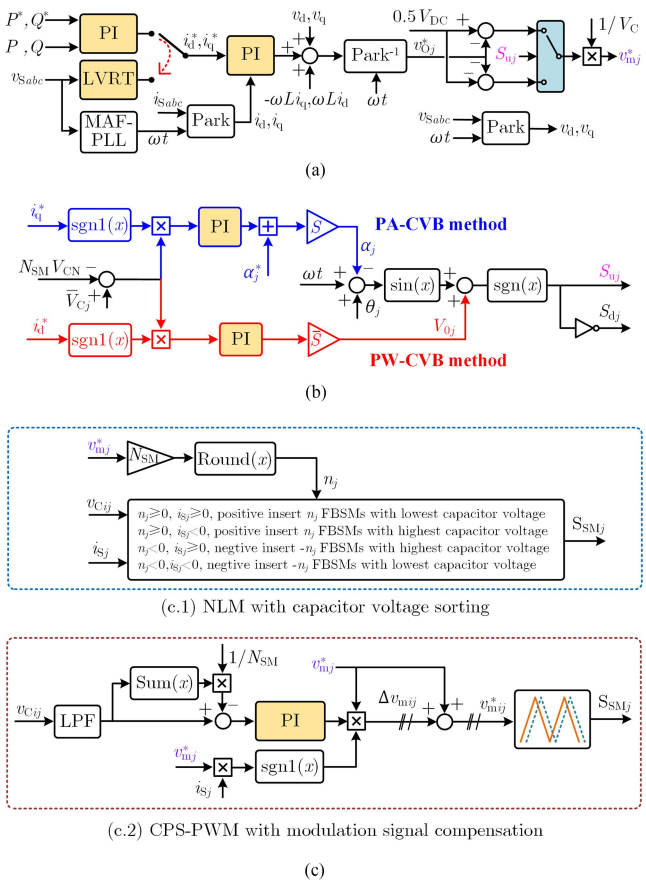


Fig. 7. Power loss comparison of the HMC and FB-MMC.



(a)

(b)

(c.1) NLM with capacitor voltage sorting

(c.2) CPS-PWM with modulation signal compensation

(c)

Fig. 8. Unified closed-loop control strategy for both the traditional PW-CVB method and the proposed PA-CVB method. (a) Grid-connected Control. (b) Total Capacitor Energy Balancing Control. (c) Individual Capacitor Voltage Balancing Control.

a unified closed-loop control strategy that applies to both the traditional PW-CVB method and the proposed PA-CVB method, as illustrated in Fig. 8.

A. Grid-Connected Control

The grid-connected control strategy of HMC is similar to that of the classical MMC [1], [6], as shown in Fig. 8(a). During normal operation, HMC utilizes a dual-loop control method, specifically the PQ power outer loop and the grid current inner loop in the *dq* coordinate. In the event of grid voltage sag, the PQ power outer loop is switched to the low voltage ride-through (LVRT) control. Referring to Chinese grid code GB/T 19963.1-2021, the active current reference needs to be reduced and the reactive current reference needs to be increased based on the depth of the grid voltage sag [25]. To suppress the negative-sequence component of the grid current under asymmetric grid voltage sags, the moving-average-filter-based phase-locked-loop (MAF-PLL) [26] and a dq-frame grid voltage feedforward loop is applied. Finally, the modulation signal of FBSM in phase *j*, e.g., $v^*_{\text{m}j}$, is generated based on the switching signal of DS and voltage expression of (3).

B. Total Capacitor Energy Balancing Control

The total capacitor energy balancing of FBSMs is maintained by adjusting the PW or phase angle of the DS's switching signal, as shown in Fig. 8(b). The total capacitor voltage of all FBSMs can serve as an indicator of their overall energy level. Yet, the alternative conduction of DS will result in low-frequency fluctuations in the total capacitor voltage of all SMs in each phase. Thus, the MAF is applied to filter out these low-frequency ripples. In the PW-CVB method and the PA-CVB method, we select the average frequency to be the fundamental frequency and twice the fundamental frequency, respectively. Thus, the averaged total capacitor voltage of all FBSMs in phase *j* can be expressed as

$$\bar{V}_{\text{C}j} = \text{MAF}\left(\sum_{i=1}^{N} v_{\text{C}ij}\right). \tag{29}$$

When applying the traditional PW-CVB method, it can be proved from (8) that the energy of the FBSMs monotonically increases with V_{0j} as $i^*_{\text{d}} \geq 0$, and monotonically decreases with V_{0j} as $i^*_{\text{d}} < 0$. Therefore, the closed-loop control expression of offset value V_{0j} can be expressed as

$$V_{0j} = \left(K_{\text{P1}} + \frac{K_{\text{I1}}}{s}\right)\left[\text{sgn1}(i^*_{\text{d}})\left(\bar{V}_{\text{C}j} - N_{\text{SM}}V_{\text{CN}}\right)\right] \tag{30}$$

where K_{P1} and K_{I1} are the proportional and integral coefficients of the PI controller, while NV_{CN} represents the reference value of the total capacitor voltage of phase *j*. The function sgn1(x) is another sign function, which returns 1 when $x \geq 0$ and -1 otherwise. The error of the PI controller needs to be multiplied by sgn1(i^*_{d}) due to the opposite monotonicity of (8) when i^*_{d} signs are different.

For the proposed PA-CVB method, it can be derived from (13) that the energy of the FBSMs monotonically increases with α_j as $i^*_{\text{q}} \geq 0$, and monotonically decreases with α_j as $i^*_{\text{q}} < 0$. Therefore, the closed-loop control expression of phase angle α_j can be expressed as

$$\alpha_j = \left(K_{\text{P2}} + \frac{K_{\text{I2}}}{s}\right)\left[\text{sgn1}(i^*_{\text{q}})\left(\bar{V}_{\text{C}j} - N_{\text{SM}}V_{\text{CN}}\right)\right] + \alpha^*_j \tag{31}$$

TABLE II
SIMULATION PARAMETERS

Parameters	Symbol	Value
Dc bus voltage	$V_{\rm dc}$	200 kV
Grid voltage (magnitude)	$V_{\rm m}$	108 kV
Grid current (magnitude)	$I_{\rm m}$	1.1 kA
Fundamental angular frequency	ω	100 π rad/s
Grid filtering inductor	$L_{\rm f}$	10 mH

where $K_{\rm P2}$ and $K_{\rm I2}$ are the proportional and integral coefficients of the PI controller. The error of the PI controller needs to be multiplied by $\mathrm{sgn1}(i_{\rm q}^*)$ due to the opposite monotonicity of (13) when $i_{\rm q}^*$ signs are different. Additionally, to enhance control response speed during power factor variation, the reference phase angle α_j^* is feedforward into the control link, which can be calculated by (14) with $\varphi^* = \arctan(i_{\rm q}^*/i_{\rm d}^*)$.

Combining (7) and (12), the switching signal of DS can be obtained as

$$S_{{\rm u}j} = \bar{S}_{{\rm d}j} = \mathrm{sgn}\left(\sin(\omega t + \theta_j - S\alpha_j) + \bar{S}V_{0j}\right) \tag{32}$$

where ωt is the synchronization signal, which can be obtained by the MAF-PLL of the grid voltage. S is the selection switch used for different control methods. When $S = 0$, the traditional PW-CVB method is chosen. When $S = 1$, the proposed PA-CVB method is chosen.

It is notable that if the HMC is operated in nearly pure reactive power mode, the phase angle φ is close to $\pm\pi/2$. In the event of a disturbance causing the total capacitor voltage of the cascaded FBSMs to deviate from the nominal value, under the traditional PW-CVB method, (8) indicates that since $\cos(\varphi)$ is close to 0, $E_{{\rm SM}\,a}$ remains nearly 0 regardless of changes in $V_{0\,a}$. Consequently, the feedback control is unable to restore the normal voltage, thereby disabling the stable operation of the HMC. In contrast, under the proposed PA-CVB method, according to (9), despite $\cos(\varphi)$ being close to 0, adjusting α_a still results in changes to $E_{{\rm SM}\,a}$, demonstrating that the feedback control remains effective. Therefore, the HMC can effectively maintain capacitor voltage balance and ensure stable operation.

C. Individual Capacitor Voltage Balancing Control

Since the total capacitor energy of each phase is controlled to be balanced, voltage balancing of individual capacitors can be easily achieved by traditional ways of classical MMC. For a large SM number application, the nearest level modulation with capacitor voltage sorting control is usually applied [15], as shown in Fig. 8(c.1). For a small SM number application, the carrier phase-shift pulsewidth modulation (CPS-PWM) with modulation signal compensation control is usually applied, as shown in Fig. 8(c.2).

V. SIMULATION VERIFICATION

Simulation tests of a single-ended HMC-based HVdc system are conducted to ensure the effectiveness and superiority of the proposed PA-CVB method. The simulation parameters are listed in Tables I and II.

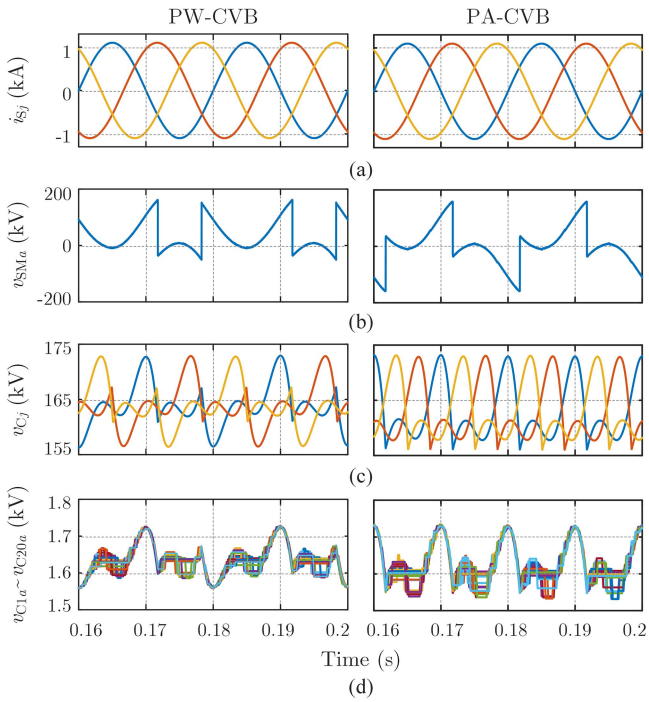


Fig. 9. Steady-state simulation results of HMC under the traditional PW-CVB method (left) and the proposed PA-CVB method (right). (a) Three-phase grid currents. (b) Branch voltage of cascaded FBSMs in phase a. (c) Total capacitor voltage of all SMs in each phase. (d) Partial SM capacitor voltage in phase a.

A. Steady-State Operation

Fig. 9 shows the steady-state simulation results of the HMC under nominal operation conditions ($M = 0.85\times4/\pi$, $\varphi = 0$). The total harmonic distortion (THD) of grid currents is about 0.2% and agrees with the grid-tied operating standards. The branch voltages of the cascaded FBSMs are consistent with the theoretical ones shown in Fig. 3. The total capacitor voltage of all SMs $v_{{\rm C}j}$ under the PW-CVB and PA-CVB methods varies at the frequency of 50 Hz and 100 Hz, respectively. The voltage fluctuations for both methods are close to 8.25 kv, which is approximately equal to the design value of 5%. Fig. 9(d) illustrates the voltage waveforms of the partial SM capacitor in phase a. It is observed that these voltages fluctuate around the nominal value of 1.65 kV and exhibit similar characteristics to those of the classical MMC.

B. Four-Quadrant Operation

Fig. 10 shows the simulation results of the HMC under four-quadrant operation conditions. At time intervals, I and V, the HMC operates at the rectifier and inverter modes, respectively. At time intervals III and VII, the HMC operates at the capacitive and inductive modes, respectively. As can be seen from Fig. 10(a), $i_{\rm d}$, and $i_{\rm q}$ accurately track their reference values under different operating points, verifying the effectiveness of the grid-connected control of the HMC. As depicted in Fig. 10(b), the PW-CVB method demonstrates a well-balanced $v_{{\rm C}j}$ during time intervals I∼II, IV∼VI, and VIII. However, the balancing performance weakens during time intervals III and VII when the

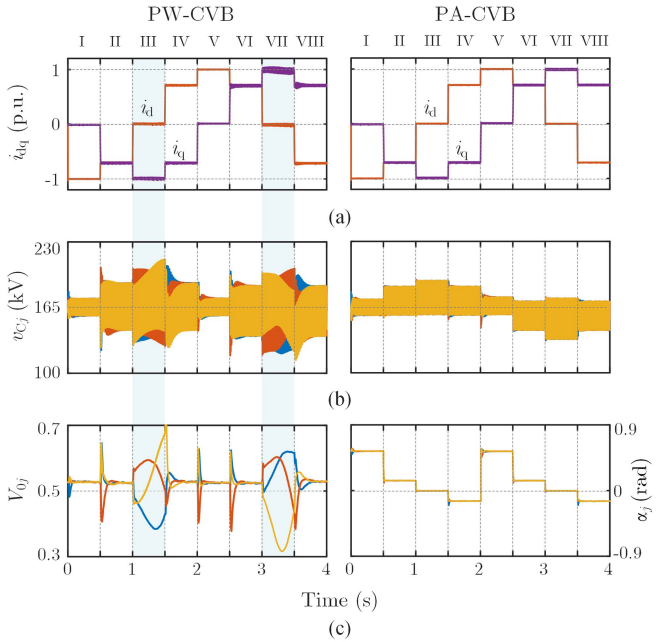


Fig. 10. Simulation results of four-quadrant operating of HMC under the traditional PW-CVB method (left) and the proposed PA-CVB method (right). (a) *dq* components of the grid currents. (b) Total capacitor voltage of all SMs in each phase. (c) Offset value and phase angle in each phase.

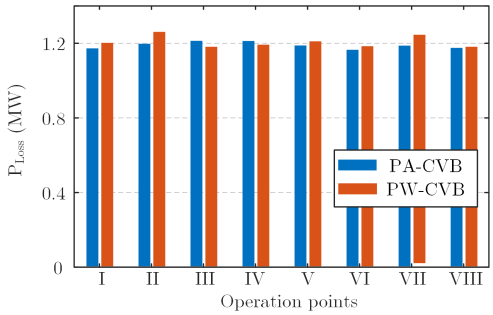


Fig. 11. Simulation results of power loss under PW-CVB and PA-CVB method.

HMC operates in pure-reactive power modes. This is because there is no steady-state operating point for V_{0j} [see left-side of Fig. 10(c)], making the capacitor voltage uncontrollable during these time intervals. In contrast, the PA-CVB method consistently demonstrates a satisfactory balancing performance of v_{Cj} under four-quadrant operation. The phase angle α_j varies with the power factor angle, as shown in Fig. 10(b). Furthermore, the voltage ripples of v_{Cj} during time intervals III and IV are smaller compared to the PW-CVB method, aligning with the theoretical analysis shown in Fig. 6(b).

Fig. 11 presents the simulation results of power loss under the PW-CVB and PA-CVB methods at various operation points. The results demonstrate that the discrepancies in power loss between different CVB methods and operational points are relatively small, thereby corroborating the earlier power loss estimation findings.

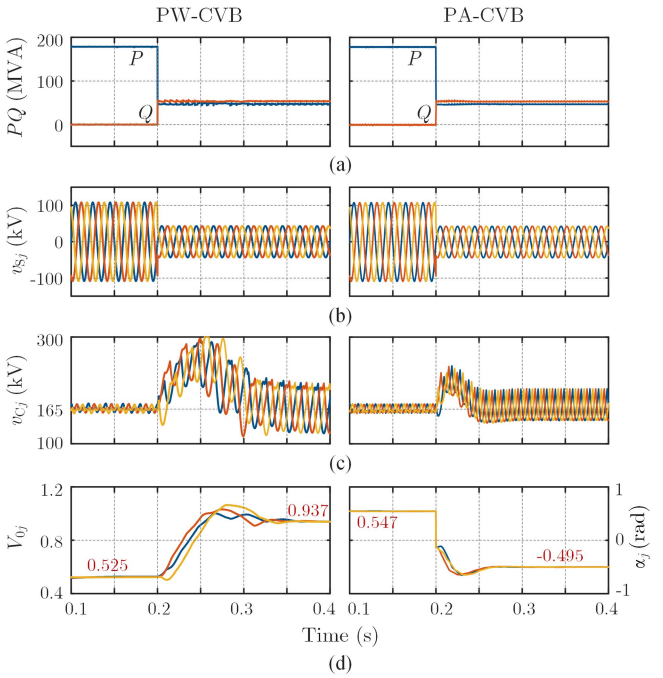


Fig. 12. Simulation results of the symmetrical grid voltage sag of HMC under the traditional PW-CVB method (left) and the proposed PA-CVB method (right). (a) Active and reactive power. (b) Three-phase grid voltages. (c) Total capacitor voltage of all SMs in each phase. (d) Offset value and phase angle in each phase.

C. Symmetrical Grid Voltage Sag

Fig. 12 shows the simulation results of the HMC under symmetrical grid voltage sag. At 0.2 s, the grid voltage decreases from 108 kV to 43 kV, resulting in a decrease in the modulation degree from 1.08 to 0.43. Consequently, the PQ control switches to LVRT control, according to the grid code, i_q^* is changed from 0 p.u. to -0.75 p.u., and i_d^* is changed from 1 p.u. to 0.66 p.u., resulting in a decrease in active power and an increase in reactive power. As depicted in Fig. 12(b), both CVB methods demonstrate the ability to maintain capacitor voltage balancing following a grid voltage sag. However, the PA-CVB method has a smaller regulation time and exhibits a smaller voltage fluctuation of v_{Cj} when the modulation index is low, indicating its superior performance. Furthermore, to achieve capacitor voltage balancing, the V_{0j} is varied from 0.525 to 0.937, and α_j is varied from 0.547 to -0.495, as shown in Fig. 12(d). These variations align with the theoretical values calculated using (11) and (14), respectively.

D. Asymmetrical Grid Voltage Sag

Fig. 13 illustrates the simulation results of the HMC in the presence of an asymmetrical grid voltage sag. Specifically, at 0.2 s, the voltage of phase *a* drops from 108 kV to 43 kV (from 1 p.u. to 0.4 p.u.). Through LVRT control, the MAF-PLL and grid voltage feedback loop work together to suppress the negative-sequence component of the grid current. Consequently, following an unbalanced grid voltage sag, the grid current in the dq-frame, namely i_d and i_q, remains relatively constant,

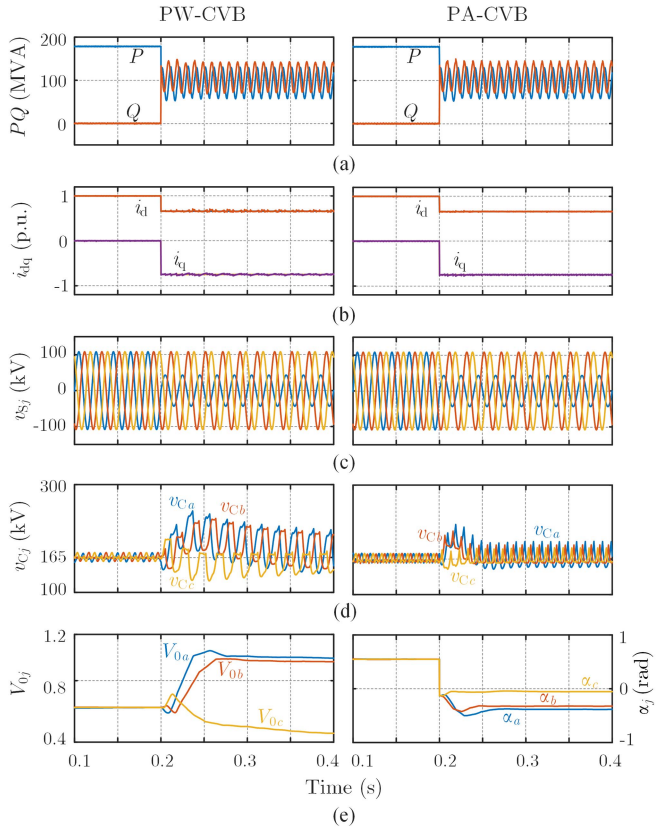


Fig. 13. Simulation results of the asymmetrical grid voltage sag of HMC under the traditional PW-CVB method (left) and the proposed PA-CVB method (right). (a) Active and reactive power. (b) Grid current in dq-frame. (c) Three-phase grid voltages. (d) Total capacitor voltage of all SMs in each phase. (e) Offset value and phase angle in each phase.

while the active and reactive power exhibit 100 Hz oscillations. From Fig. 13(d), the total capacitor voltages of all FBSMs in each phase remain balanced when using these two CVB methods. Notably, the proposed PA-CVB method demonstrates faster response speed and smaller voltage pulsations. Given the unbalanced nature of the HMC system, the steady-state values of V_{0j} and α_j differ.

VI. Experimental Verification

The effectiveness of the proposed PA-CVB method is further demonstrated through a hardware-in-the-loop test, as shown in Fig. 14. The main circuits of the HMC are constructed on the RTDS, while the control strategy is executed on the RTU-Box that utilizes a digital signal processor and field-programmable gate array architecture. The experimental parameters are provided in Table III, with 5 FBSMs used in each phase. Since the SM number is small, the CPS-PWM with modulation signal compensation is applied for the individual capacitor voltage balancing control.

Fig. 15 presents the steady-state experimental results of the HMC when utilizing the proposed PA-CVB method with $M = 0.85\times4/\pi$ and $\varphi = 0$. The branch voltage of cascaded FBSMs $v_{\mathrm{SM}j}$ in each phase exhibits an 11-level staircase wave. The

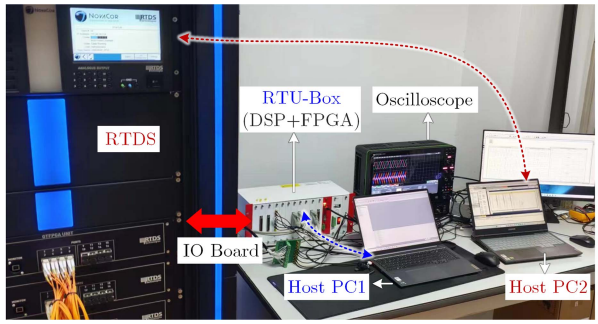


Fig. 14. Hardware-in-the-loop experimental setup of the HMC.

TABLE III
Experimental Parameters

Parameters	Symbols	Values
Dc bus voltage	V_{dc}	10 kV
Grid voltage (magnitude)	V_{m}	5.4 kV
Grid current (magnitude)	I_{m}	0.55 kA
Fundamental angular frequency	ω	100 π rad/s
Switching frequency	f_{s}	5 kHz
Grid filter inductance	L_{f}	3 mH
Nominal SM capacitor voltage	V_{CN}	1.65 kV
SM capacitance	C_{SM}	5 mF

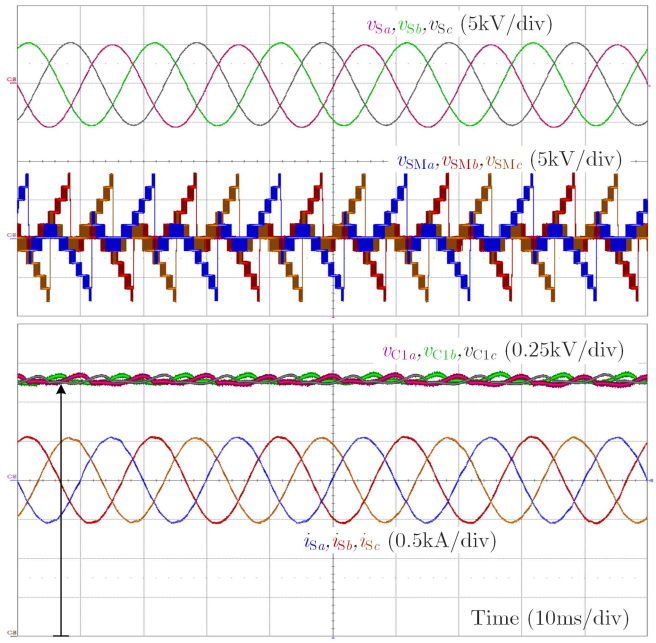


Fig. 15. Steady-state experimental results of HMC with the proposed PA-CVB method.

three-phase current exhibits low THD while the voltages across the SM capacitors in all three phases stay balanced.

Fig. 16 illustrates the performance of the PA-CVB method under four-quadrant operation conditions. The dq-frame grid current i_{d} and i_{q} are effectively regulated to their respective references. Since the eight operation points (from I to VIII) are situated on the unit current circle, the magnitudes of the grid currents $i_{\mathrm{S}j}$ remain constant during each operation point.

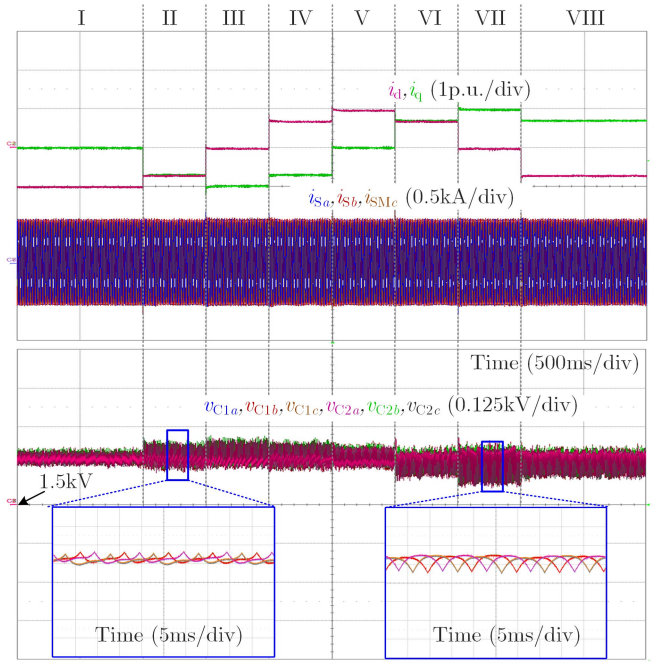


Fig. 16. Experimental results of four-quadrant operating of HMC with the proposed PA-CVB method.

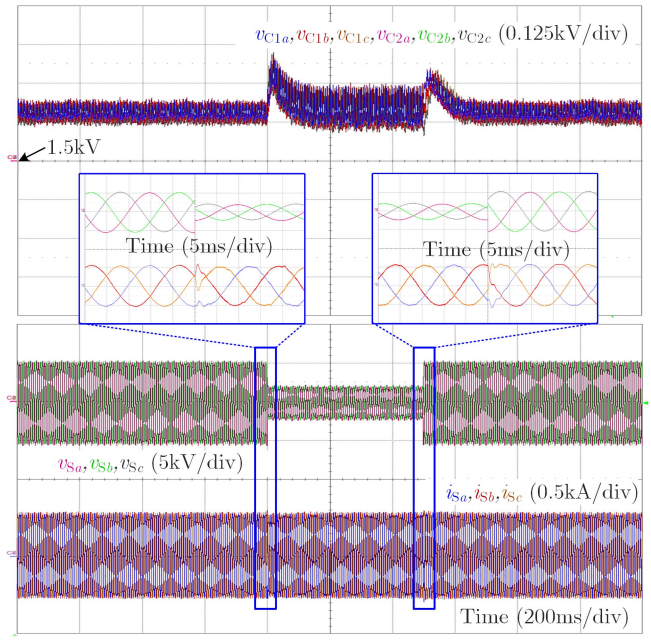


Fig. 17. Experimental results of HMC with the proposed PA-CVB method under symmetrical grid voltage sag.

Furthermore, the SM capacitor voltages in all three phases consistently hover around the reference value of 1.65 kV.

When the magnitude of the three-phase grid voltage decreases from 5.4 kV (1 p.u.) to 2.16 kV (0.4 p.u.), the HMC utilizing the proposed PA-CVB method is still able to maintain balanced SM capacitor voltages, as illustrated in Fig. 17. Upon switching from PQ control to LVRT control, the active power decreases and the reactive power increases, while the magnitude of grid currents remains constant with no significant distortion observed. Moreover, there is a slight increase in capacitor voltage ripple during the sag period, but the transient regulation time of the capacitor voltage remains short.

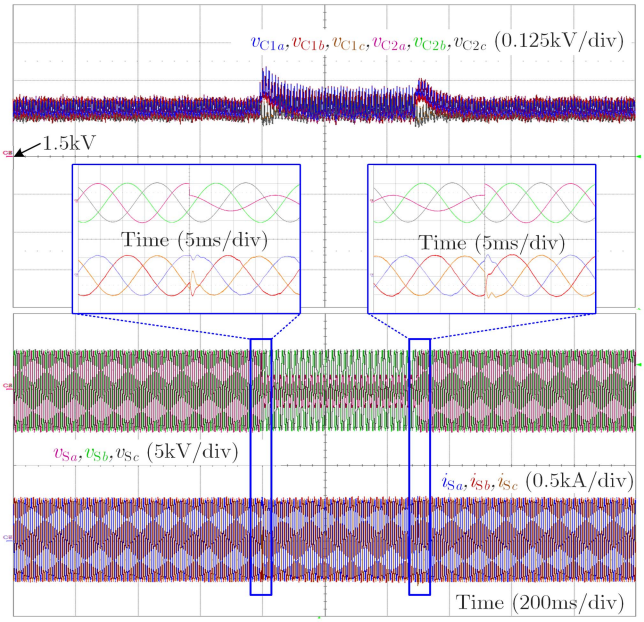


Fig. 18. Experimental results of HMC with the proposed PA-CVB method under asymmetrical grid voltage sag.

To further verify the effectiveness of the proposed PA-CVB method, the HMC is tested under conditions of asymmetrical grid voltage sag. Specifically, the grid voltage of phase *a* drops to 2.16 kV (0.4 p.u.) in 500 ms, with the experimental results depicted in Fig. 18. Consistent with the simulation results, the grid currents exhibit smooth transitions and a constant magnitude. Besides, the SM capacitor voltages of all phases remain balanced throughout. All of the experimental results demonstrate the effectiveness of the proposed PA-CVB method.

VII. Conclusion

This article aims to address the CVB issue of the HMC. Comparative analysis, control strategy design, and verification tests are conducted for both the proposed PA-CVB method and the traditional PW-CVB method. The following conclusions can be drawn.

1) The PW and phase angle are two control dimensions of the DS's switching signal. They can be used to regulate the energy balance of the cascaded FBSMs in the HMC. The HMC under either of the two CVB methods can operate at the full modulation index range of $[0, \pi/4]$ and deal with symmetrical/asymmetrical grid voltage sags.
2) Compared to the traditional PW-CVB method, the proposed PA-CVB method demonstrates identical SM number and switch number but showcases reduced SM capacitance and capacitor voltage pulsations, particularly in scenarios of low modulation index and low power factor.

3) The HMC under the PA-CVB method can maintain capacitor voltage balancing in four quadrant modes, unlike the traditional PW-CVB method, which fails to achieve balanced capacitor voltage in pure reactive power modes.

Future studies will be conducted to solve the high dv/dt in the output voltage of the cascaded FBSMs when using these CVB methods, as it could potentially impact the insulation and electromagnetic compatibility of the converter.

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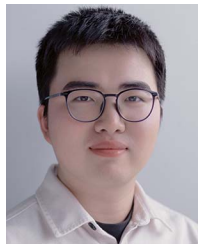

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