Substrate Embedded Power Electronics Packaging for Silicon Carbide MOSFETs

Ameer Janabi, Luke Shillaber, *Student Member, IEEE*, Wucheng Ying, Wei Mu, *Graduate Student Member, IEEE*, Borong Hu, *Member, IEEE*, Yunlei Jiang, *Member, IEEE*, Nikolaos Iosifidis, *Graduate Student Member, IEEE*, Li Ran, *Fellow, IEEE*, and Teng Long, *Member, IEEE*

***Abstract*—This article proposes a new power electronic packaging for discrete dies, namely, a standard cell, which consists of a step-etched active metal brazing (AMB) substrate and a flexible printed circuit board (flex-PCB). The standard cell exhibits high thermal conductivity, complete electrical insulation, and low stray inductance, thereby enhancing the performance of SiC MOSFET devices. The standard cell has a stray power loop inductance of less than 1 nH and a gate loop inductance of less than 1.5 nH. The standard cell has a flat body with surface-mounting electrical connections on one side and direct thermal connections on the other. The use of flex-PCB die interconnection enables maximum utilization of source pads while providing a flexible gate-source connection and the converter PCB. This article presents the design concept of the standard cell and experimentally validates its effectiveness in a converter system.**

***Index Terms*—Advanced packaging of power electronics, embedded die, integrated power electronics, standard cell.**

I. Introduction

SiC power devices possess superior attributes compared to their Si counterparts. This is due to their intrinsic characteristics, such as their high breakdown voltage, which allows for the use of thinner drift layers, resulting in lower on-resistance and hence reduced conduction losses. Additionally, SiC devices exhibit a saturated electron drift velocity nearly twice that of Si, resulting in faster rise and fall times during switching, leading to lower switching losses [1].

The legacy packaging technologies were developed around former silicon-based devices. While both Si devices and legacy packaging technologies have demonstrated reliable performance, developing a packaging approach that fully exploits the potential of SiC devices presents significant challenges [2], [3], [4], [5], and [6]. The primary one is the power loop stray inductance, which causes voltage spikes across the device during turn-OFF events, thereby limiting the operating voltage of the device excessively below its rated voltage [7], [8]. This also leads to additional electromagnetic interference (EMI) with surrounding circuits and systems [9]. High stray inductance imposes a significant limit on the maximum rise/fall time of the current di/dt that can be achieved by SiC devices, resulting in higher switching losses [10]. Addressing these challenges is critical for realizing the full potential of SiC devices in power electronics applications.

When the power loop stray inductance is below 1 nH, the switching transition will be limited by the gate driver current, the impedance along the gate drive loop, and the device's internal gate resistance. To achieve equal transient current sharing and prevent gate resonance among paralleled devices, the gate loop inductance must be minimized and symmetrically designed [11]. Die integration has the potential to achieve exceptionally low levels of stray inductances due to the close proximity of the electronic components [12], [13]. The effectiveness is dependent on the die-interconnect technique, which can lead to higher level of inductance [14]. In addition, many die integration approaches do not adequately address the significant challenge of achieving low thermal resistance between the device and the cooling channel. In [15] and [16], convection cooling is used, which conveniently allowed differing the discussion on how the 1.2 kV die can be electrically insulated for liquid cooling. Convection cooling introduces large heat sinks, contradicting the purpose of die embedding and resulting in low-power density converters. The fan-out die embedding method represents another excellent approach for double-sided cooled PCBs with low junction-to-case thermal resistance [17], [18]. Further development of these methods, including the integration of liquid cooling, is necessary for employing this technology in high-voltage, high-power SiC dies. Similarly, the flip-chip method presented in [19] does not demonstrate a solution for achieving electrically insulated liquid cooling for high-voltage dies. When employing a flip-chip configuration with liquid cooling, its utilization merely serves as a substitute for conventional bonding wires [20], resulting in packages that exhibit only a marginal reduction in stray power loop inductance.

The common structure of the SiC MOSFET bare die chip is vertical, where the device drain is located on the bottom side and the source and gate pads are on the top. This vertical structure

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Ameer Janabi, Luke Shillaber, Wucheng Ying, Wei Mu, Borong Hu, and Teng Long are with the Electrical Engineering Division, Department of Engineering, University of Cambridge, CB3 0FA Cambridge, U.K. (e-mail: ahaj2@cam.ac.uk; ls669@cam.ac.uk; wy256@cam.ac.uk; wm338@cam.ac.uk; bh529@cam.ac.uk; TL322@cam.ac.uk).

Yunlei Jiang is with SpaceX, Hawthorne, CA 90250 USA (e-mail: yunlei.jiang@spacex.com).

Nikolaos Iosifidis and Li Ran are with the School of Engineering, University of Warwick, CV4 7AL Coventry, U.K. (e-mail: nikos.iosifidis@warwick.ac.uk; L.Ran@warwick.ac.uk).

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has necessitated electrical insulation of thermal connection when the cooling plate is grounded. To achieve very low thermal resistance, power modules commonly employ a direct bond copper (DBC) or active metal brazing (AMB) substrate between the die drain and the cooling plate. Alternatively, specialized isolating adhesives can be used, though such methods may result in significant derating of the device's maximum current-handling capabilities due to their higher thermal resistance compared to ceramic materials [21], [22].

Conventional device interconnection involves ultrasonic wire-bonding, which should not be made with sharp turns such as semicircle to achieve manageable stress in the wire bond neck and heel [23]. The long, noncoupled path of the wire bonds results in an additional unwanted inductance [24]. Advanced methods for interconnecting the top source pad allow for a more integrated approach, such as the use of laser-drilled microvias [21], [25], [26], in which holes are drilled in the resin that covers the die. These holes are then electroplated to connect to the source pads for electrical connection. The electroplating process requires a copper metallization of the die chip. The standard aluminum metallization is not suitable for the microvia process because it gets damaged during the laser drilling process and it is not compatible with the subsequent chemical cleaning and galvanic filling process. On the other hand, the double-side microvia technology utilizes adhesive-based isolation. The isolation of high-voltage die requires a thicker adhesive layer, resulting in a considerable rise in thermal resistance. As a consequence, this technology is currently confined to low-voltage applications.

The Semikron SKiN technology [27], [28] allows the implementation of silver sintering to the source pads and 80% utilization of the source pad area [29]. The use of flexible printed circuit board (flex-PCB) within SKiN technology facilitates the reduction of stray power loop inductance to a low level.

Several novel properties are associated with the standard cell, setting it apart from other techniques utilizing flex-PCB, such as SKiN technology.

1) The step etching of the top layer of the isolated substrate provides a cavity to embed power electronic die chip into the isolated substrate. This embedding structure offers excellent electrical connection by using printed circuits such as flex-PCB to significantly reduce stray inductance. At the same time, this structure retains the balanced and preferable insulation and thermal conduction performance of using ceramic substrates for power electronics packaging.
2) The etched cavity facilitates flux cancellation for achieving extremely low stray inductance. Extending the drain connection of the vertical SiC MOSFET to the surrounding plateau sets the drain and the source of the device at the same lateral level, enabling surface mount layout and high flux cancellation at the system level. The plateau also provides an additional thermal pathway to the system PCB.
3) The flex-gate enables flexibility in integrating the gate driver either on the same power stage board or on a separate board. This is accomplished without introducing considerable gate loop inductance and eliminates the potential mechanical complexities linked to rigid pins found in conventional power modules.
4) The flex-PCB within the standard cell processes current over a very short distance. This leverages the benefits of flex-PCB die interconnect while still using regular PCB for the dc-link with thicker copper. In contrast, in SKiN technology, the flex-PCB forms the entire half-bridge circuit, which is only 70 μm in thickness.

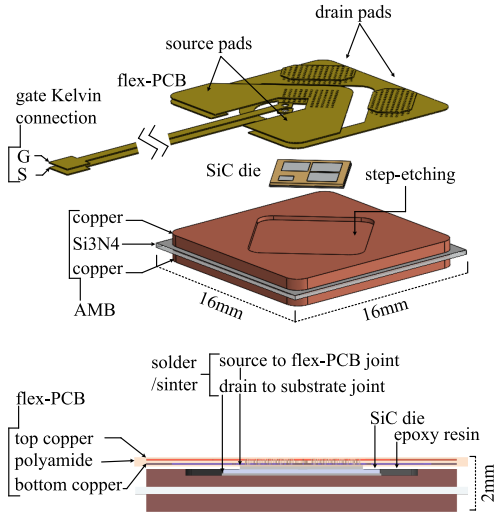


Fig. 1. Exploded and cross-sectional views showing the main component forming the standard cell.

This article introduces a new power device packaging design and its application in power converters. The proposed design achieves the power loop stray inductance of less than 1 nH without compromising the thermal impedance between the die and the cooling plate. The gate loop inductance has been reduced to 1.5 nH.

II. Structure of the Standard-Cell

The design principle of the standard cell is oriented toward minimizing the stray inductance of the power and gate loops without compromising thermal conduction and galvanic insulation. The standard cell depicted in Fig. 1 consists of three primary components: the power semiconductor die, the substrate, and the flex-PCB interconnection. Most SiC dies feature a vertical structure where the drain is located on the bottom, and the source and gate are on the top. The SiC die utilized in this study is the *SCT116N120G3DXAG* from STMicroelectronics, which has a 1200 V blocking voltage and 14.6 mΩ conduction resistance when switched on at $I_d = 100$ A and gate to source voltage $V_{gs} = 18$ V and 25 °C. The proposed methodology is fully adaptable to accommodate dies from other vendors too with voltage rating equal or lower than 1200 V. The drain pad metallization of the device in this work is *Ti/Ni/Ag*, while the source pad metallization is *Al/Cu(0.5%)/Si(1%) + Ti/Ni/Ag(98.5%)*, making it compatible with both soldering and sintering of die attach and interconnection.

The direct bond copper (DBC) or active metal brazing (AMB) isolated substrate is commonly used to provide electrical

TABLE I
TOLERANCES FOR THE AMB SUBSTRATE WITH THE STEP-ETCHING

Copper thickness top/bottom	$0.8 \pm 0.08\ mm$
Ceramic thickness	$0.32 \pm 0.05\ mm$
Half-etch depth	$0.29 \pm 0.02\ mm$
Radius of round angles	$1 \pm 0.3\ mm$
Ag-plating thickness	$0.45 \pm 0.15\ \mu m$

isolation, heat spreading, and electrical conduction at the same time. The most prevalent AMB joint comprises silver and copper, with additions of 1%–10% of titanium as a bonding agent and indium to reduce the melting temperature. The brazing temperature is typically in the range of 850–950 °C, above the liquid phase line of the filler metal and below the solid phase line of the base material [30], [31].

In order to maximize flux cancellation, the drain and source pads are desired to be positioned at the same level to reduce the loop length from arching the connection between the bottom side to the top side of the device. The top side copper of the substrate needs to be designed to bridge the vertical device electrodes to the same level. A step etching method is used to offset the thickness of the die. A $7 \times 7\,\mathrm{mm}^2$ cavity oriented at the center of the top copper has been stepped-etched. The depth of the cavity is 290 μm, thus, the bare die can be fully immersed into this cavity, as shown in Fig. 1. Copper chemical etching is performed using a ferric chloride ($FeCl_3$) solution with antifoaming and chelating additives to improve etching quality. Chemical etching offers several advantages over other methods such as micromachining and laser etching because it leaves the metal stress-free and burr-free. The tolerances achieved with controlled chemical etching are shown in Table I.

The surface of the copper substrate is metallized with a 0.45 μm thick silver layer to allow soldering or sintering of the die. Instead of bonding wires, the standard cell utilizes a flex-PCB to electrically interconnect electrodes of the die to the terminals of the standard cell package, using copper traces 70 μm in thickness to reduce the conduction loss. The flex-PCB incorporates a polyimide layer, 70 μm in thickness, designed to provide insulation between the top and bottom copper layers. The close proximity of two copper traces in the flex-PCB facilitates flux cancellation, which reduces the stray inductance of the current loop.

The discrete device package of the standard cell, in theory, gives power converter designers more flexibility by using elements at a lower granularity. The number of devices in parallel or in series and the type of topologies are entirely determined by the design when using discrete device packages. Conventional discrete device packages for more than 400 V applications are predominantly the TO series, which is outdated and significantly compromises the true performance of the SiC power semiconductors.

The standard cell, a fully insulated package, provides a clear advantage over traditional discrete devices like TO type packaging. It can be directly attached to the cooling plate, functioning as an effective surface-mount package, eliminating through-hole leads, as illustrated in Fig. 1. The unique structure of the standard cell transforms the vertical die electrode structure into a lateral equivalent through a step-etched cavity on the top copper of the substrate. Using flex-PCB with a cavity structure enables effective reduction of stray inductance by employing a highly negatively coupled lateral connection for drain and source conductors. This negative coupling technique, illustrated in Figs. 1 and 2, facilitates a Kelvin connection, allowing extension of the gate length for connection to the external gate driver circuitry without a significant increase in gate loop inductance.

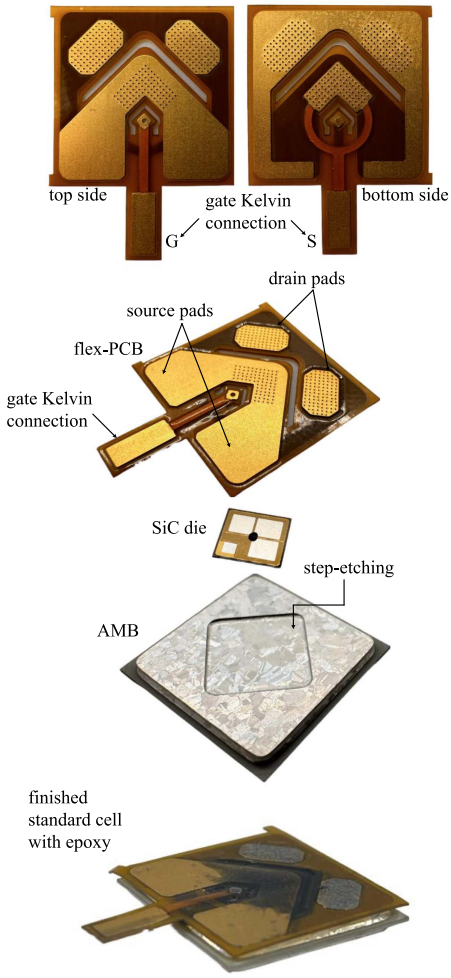


Fig. 2. Standard cell main components and finished build.

III. DESIGN AND ANALYSIS OF THE STANDARD CELL INTEGRATION

The proposed standard cell design will be validated by four critical-to-quality axioms: the power (drain-source) and control (gate-source) loop stray inductance, thermal performance, current density distribution within the standard cell, and voltage isolation.

A. Stray Inductance

Power loop stray inductance is not only a source of voltage spikes that limit the device's rated voltage but also a primary source of EMI. One significant approach to reducing the power loop inductance is to create a highly negative coupling between the conductors of the dc-link and the device power loop. This can

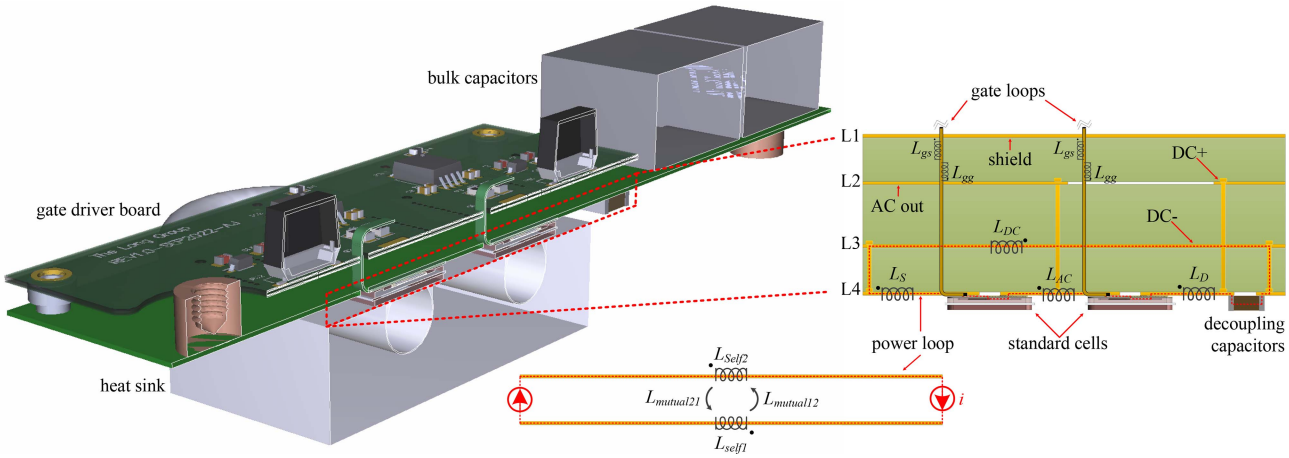


Fig. 3. Cross-sectional view of the half-bridge topology with an enlarged perspective of the four-layer power stage PCB. The red-dotted line highlights the negatively coupled power loop.

be achieved by placing these two conductors in close proximity while maintaining electrical insulation. The negative coupling generated between the forward and return rectangular paths is given in [32], where

$$L_{\text{stray}} \propto \frac{\text{distance} \cdot \text{length}}{\text{width}}. \tag{1}$$

Readers with interests can refer to [33] and [34] for more detailed explanation of the concept of negative coupling. The effectiveness of flux cancellation increases with higher values of mutual inductance

$$L_{\text{stray}} = \underbrace{L_{\text{self1}} + L_{\text{self2}}}_{\text{self inductance}} - \underbrace{(L_{\text{mutual12}} + L_{\text{mutual21}})}_{\text{negative coupling}}. \tag{2}$$

Due to the cavity of the substrate, the die chip is immersed in the top copper, which is connected to the the bottom side (drain) of the die chip, resulting in the same height of the source, gate, and drain. This structure effectively transfers the vertical connection of a power MOSFET to a lateral connection arrangement. The lateral connection of the discrete devices allows the same height of connection of all terminals of the high side and low side devices, resulting in a single height of the power loop path of the half-bridge. Not only can the standard cell's same-height connection be surface-mounted to a PCB, but also the power paths (dc+ and dc-) can be positioned closely within the PCB layers to achieve highly negative coupling for very low stray inductance.

The standard cells can be surface-mounted to the converter circuit PCB. The drain and source connections of each cell are connected through Layer 4 of the PCB as shown in Fig. 3. The return path (dc-) is routed through buried vias from Layer 4 to Layer 3 to prevent interference with the phase ac connection path, which is on Layer 2. This arrangement takes the advantage of close proximity of two conductors separated by the PCB prepreg layer at the vertical direction, which offers much increased negative coupling comparing to conventional lateral loops used in power module chip layout.

The parasitic inductance from the PCB layout is extracted using the finite element tool *ANSYS Q3D*. The overall power loop inductance is 0.716 nH at 100 MHz. This is further validated by the experimental result shown in the final section.

On the other hand, the gate loop inductance is optimized by means of the same negative coupling concept. The gate trace is coupled with the source trace along the entire path from the gate driver chip to the inside of the cell as shown in Fig. 1. This tight control of the gate loop provides flexibility in adjusting the length of the gate loop while maintaining the gate loop inductance very small. The linear relationship between the gate loop inductance and the length of the flex-gate is

$$L_g\,(nH) = 1 + 0.16 \cdot l \tag{3}$$

where l is the length of the flex-gate in mm.

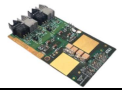
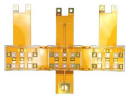
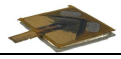
The proposed standard cell exhibits significantly lower stray inductance values compared to state-of-the-art and legacy packages. Table II illustrates the significant reduction in stray inductances when compared to other packages.

B. Current Density Distribution in the Standard Cell

The decrease in die size, thinning of the die attach layer, and compact die interconnect all lead to current crowding, which can lead to electromigration. Without delving into the details of electromigration, it is important to recognize the importance of optimizing the current density within the package copper and solder or the sintering material. Fig. 4(a) shows the effect of drain pad placement on the current density distribution within the copper and solder material of the standard cell when a 100 A current is applied. The current density can be significantly reduced by placing the drain pad in symmetrical and close proximity to the source pads. Therefore, to keep the symmetry at system level and minimize the current crowding, the die is rotated by 45° such that the source pads have a larger area interfacing drain pads and hence, a larger effective area is created to conduct the device current. The current density is also more equally distributed around the die, which also gives lower conduction resistance to the package.

Fig. 4(b) shows the current density in the 70 μm flex-PCB layer when a 100 A current has been applied. The Semikron SKiN technology, where the flex-PCB covers a large portion of

TABLE II
POWER LOOP AND GATE LOOP STRAY INDUCTANCE VALUES FOR STATE-OF-THE-ART PACKAGES COMPARED TO THE PROPOSED STANDARD CELL; THE SUPERSCRIPTS * AND ** REFER TO VALUES OBTAINED BY SIMULATION AND EXPERIMENTAL METHODS, RESPECTIVELY; OTHERWISE, REFERENCES ARE INDICATED

Package type	Illustration	$L_g(nH)$	$L_p(nH)$	The limiting factor
ST P AK/IDPAK		20*	21*	The return path of the power loop is in non-PCB structure placed above the package resulting in a larger loop. The gate loop uses bonding wires.
TO-247-4L/TO247plus		20.5*	36.9*	Uses bonding wired for both power power and gate loops. Terminals are aligned on one side through a hole connection which makes it difficult to make the negative coupling of the flux.
Schweizer p^2 Pack		Low/ layout depen- dent	1.45[22]	The source connection passes through laser vias located in the layer above the PCB stack, which prevents the use of this layer for the return path and hinders achieving high negative coupling.
AG (AT&S)/CPES		2.2[16]	2.3[16]	Due to the double-sided cooling arrangement, the power loop planes needs to traverse layers twice. To meet the 1.2 kV isolation requirement, a larger area will not be negatively coupled, which results in higher inductance.
GE POL-kW		$(20-30)$*	2.6[35], 5[36]	-High gate loop inductance due to long path from die to gate driver. -No inductance cancellation in the power loop because there is no negative coupling. The low inductance is a result from the flat structure of the flex layer compared with semicircle layout of wire-bond. The reduction in stray inductance is 45% compared to conventional wire-bond technology.
Semikron eMPack®/SKiN		$(20-30)$*	$(2.5-6)$**	-High gate loop inductance due to long path from die to gate driver. -Unsymmetrical stray inductances between parallel dies. -Unavoidable total power loop stray inductance of 6 nH as a result of the laser welded connection with dc-link caps.
3D-Hybrid package		$(20-30)$*	2.4[35]	-The flex-PCB makes contact with the substrate only leaving the top side connection to be wire-bond. -The entire DC-link is made of flex PCB with maximum available thickness of 70 μm. -DC link caps are not integrated with the power stage, which makes it require a high inductance connection.
Proposed standard cell		1.5*	0.716*,1**	N/A

the dc-link and device-to-device interconnect, in the standard cell, the flex-PCB only processes the device current for lengths less than 5 mm. The device current passes vertically through the standard cell drain and source pads to the rigid-PCB part of the system that forms the dc-link and device-to-device connection. The rigid-PCB can use thicker copper, which allows for handling the large current.

C. Insulation and the Electric Field Gradient

The compact integration and the die inside the standard cell leave a very small distance between the source, drain, and gate interconnect. The dielectric materials in this case experience a high electric field gradient, particularly in the sharp edges of each energized conductor.

When designing a standard cell, achieving the necessary isolation levels requires a special geometry. The isolation required between the source and drain of the standard cell is functional isolation, while the isolation required between the drain and source of the device and the chassis (AMB bottom copper and the heat sink) is the reinforced isolation. To calculate the required creepage and clearance of the standard cell, the conventional method follows the *IEC-60664-1* and *IEC-60664-4* standards. These steps are highlighted in Figs. 17 and 18 in the appendix. However, the conventional methods will devise the standard cell with overengineered clearance and creepage, which results in a low power density.

To achieve high power density packaging, the electric field (E-field) gradient between the critical gaps is numerically evaluated. Specifically, the isolation between the source pads on top of the SiC die and the surface of the copper layer of the AMB. The die thickness is 0.19 mm, which, even assuming a linear voltage gradient, results in a gradient of 6.3 kV/mm, more than twice the voltage breakdown limit of air at 3 kV/mm. Therefore, it is essential to surround the die with insulating medium such as silicone gel or epoxy. The simulation result shown in Fig. 5 demonstrates the electric field distribution around the die when silicone gel or epoxy is filled into the cavity around the die.

In addition, a reduction of the E-field gradient between the top and bottom copper of the AMB is achieved by filling the corners of the standard cell by 1 mm radius. The top layer of the standard cell is made of a flex-PCB that uses polyamide (*DuPont Pyralux AP*) as an isolation layer, with a breakdown field limit of 256 kV/mm.

IV. STANDARD CELL BUILD PROCESS

The build process of the standard cell can be presented in three main stages and a fourth stage to finally assemble the standard cell with the converter PCB as shown in Fig. 6. First, the SiC die is attached to the step-etched AMB using a vacuum reflow soldering process or silver sintering. The silver sintering could be lengthier process but achieves lower thermal resistance and can handle a larger amount of thermo-mechanical stress.

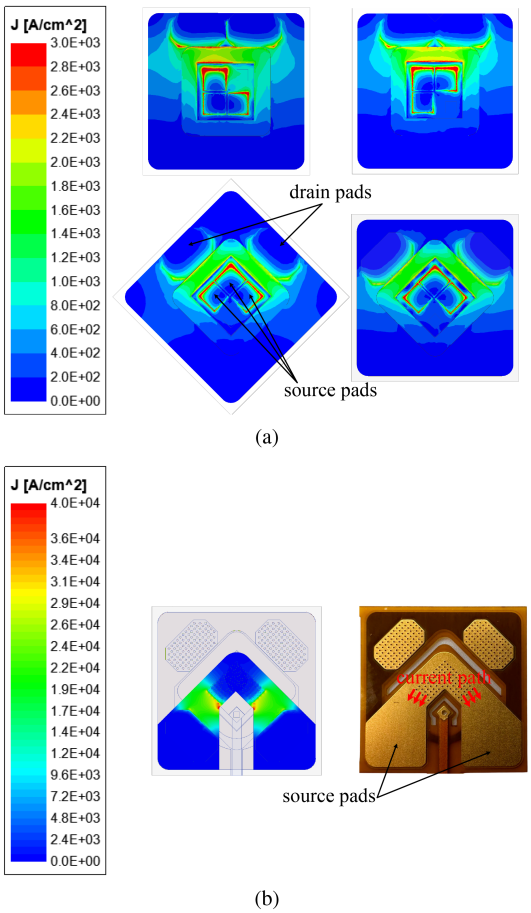


Fig. 4. (a) Die and substrate orientation and current density distribution. (b) Current density in the flex-PCB from the die source pads to the standard cell source pads.

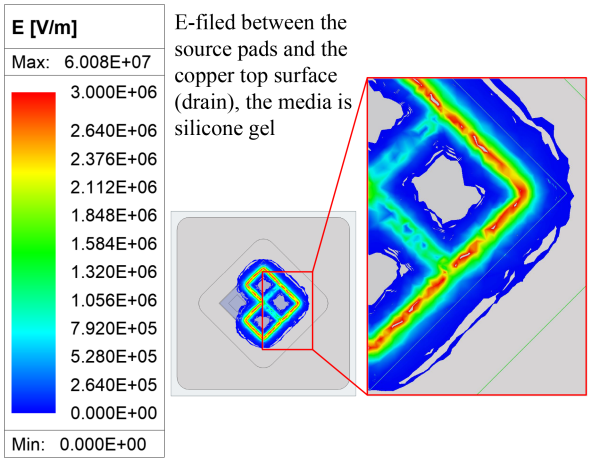


Fig. 5. E-field between the source pads on top of the die and the top copper surface of the AMB. The applied potential difference is 1 kV.

In the demonstration presented in this article, the solder alloy *Sn96.5/Ag3.0/Cu0.50* was utilized for the drain and source sides.

In the second stage, the top source and gate interconnect with the flex-PCB is completed. For the die used in this study, both the source and gate pads are silver metalized. Solder paste is applied on the flex-PCB bottom layer using a stencil. Epoxy resin or silicone gel can be injected to surround the die inside the standard cell package to enhance the electrical isolation. After this stage, the standard cell is built and will undergo electrical isolation, thermal impedance, and other qualification tests. The standard cell can then be assembled to the converter PCB using a standard surface mount soldering process alongside the other components on the board.

V. Experimental Verification

The integrated half-bridge module shown in Fig. 6 is used for experimental validation. The double-pule test (DPT) is used for switching transient analysis and switching energy calculation. Using the same half bridge for DPT with the same dc-link capacitor and power and gate loops can reveal the real switching transient in a power converter as well as demonstrate the advantage of low stray inductance of both the standard cell package and the converter power loop, both of which are enabled by the structure and design of the standard cell.

To capture the fast dynamic of the turn-ON and turn-OFF events of the standard cell, high bandwidth probes must be utilized. The test setup utilizes an isolated high-voltage probe TIVP1L from Tektronix to measure the V_{ds}, and an isolated low-voltage TIVM1 form Tektronix to measure the V_{gs} both have a bandwidth of 1 GHz. The existing current probes are either limited in bandwidth or have high insertion inductance, therefore a proprietorial ultrafast current shunt with a 1.6 GHz bandwidth is used to measure the lower device source current [37] as shown in Fig. 7. This ultrafast current shunt exhibits a minimal insertion inductance of less than 100 pH, ensuring minimal impact on transient behavior.

The load inductor was made of air core wire winding to form a 33 uH inductance. Accordingly, the first pulse and second pulse width were set to 5 and 1.8 us, respectively. The test was conducted at ambient room temperature and 800 V dc-link.

A. Fast Transient Behavior of the Standard Cell: Zero Gate Resistor

The turn-ON event is shown in Fig. 8(a). The current slew rate is approximately 40 A/ns and the voltage slew rate is approximately 75 V/ns. The turn-ON event transient can be divided into two main regions as follows.

1) t_1–t_2: At the start of this time interval, the lower device is OFF and the drain-to-source voltage is $V_{\rm dc}$. Due to the conduction of the upper device body diode, the $C_{\rm oss}$ of the upper device is depleted while the lower device $C_{\rm oss}$ is charged by $V_{\rm dc}$. When the current starts transition from the upper device body diode to the lower device channel, the upper device $C_{\rm oss}$ will have to be charged and the lower device $C_{\rm oss}$ will have to be discharged. Those capacitive currents are captured during the interval t_1-t_2 as the current overshoot. Those additional current components contribute to the turn-ON energy losses of the lower device.
2) t_2–t_4: This interval begins at the descent of the source current of the lower device, where the capacitive current components start to decrease and the current is asymptotically leveling to the load current. There are two distinctive

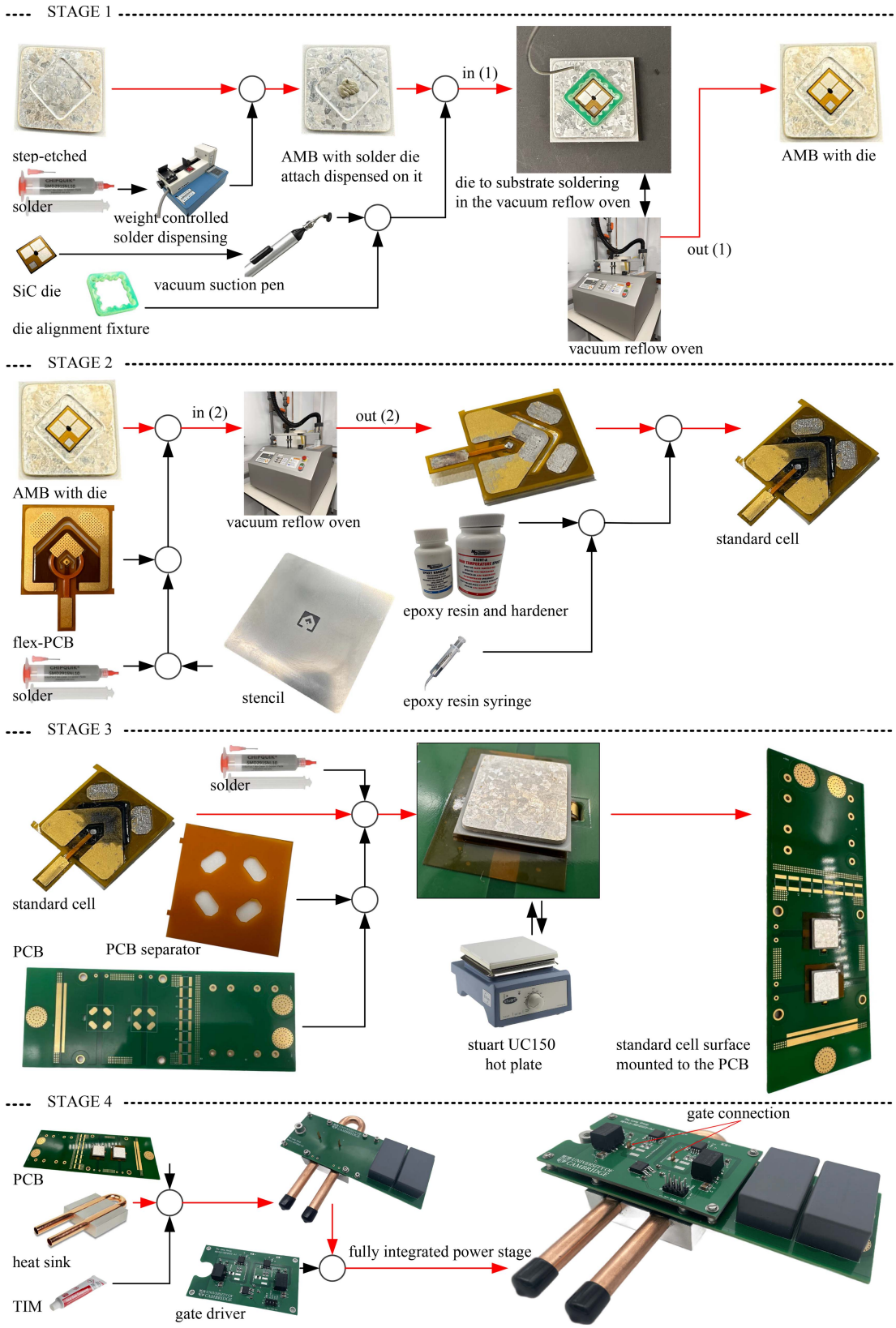


Fig. 6. Steps in the assembly of a half-bridge power stage using the standard cell.

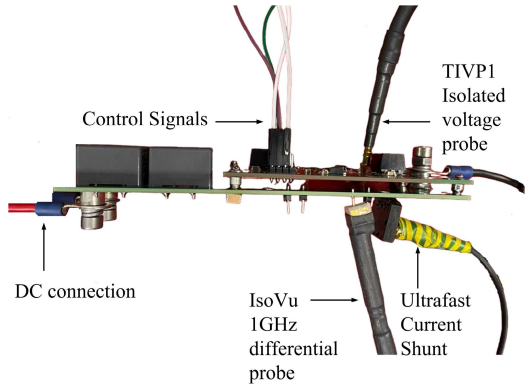
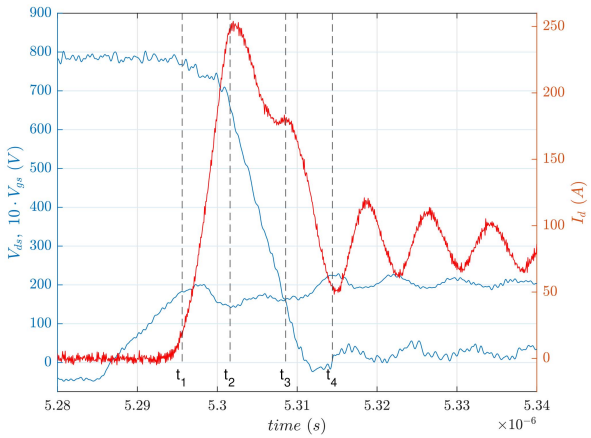
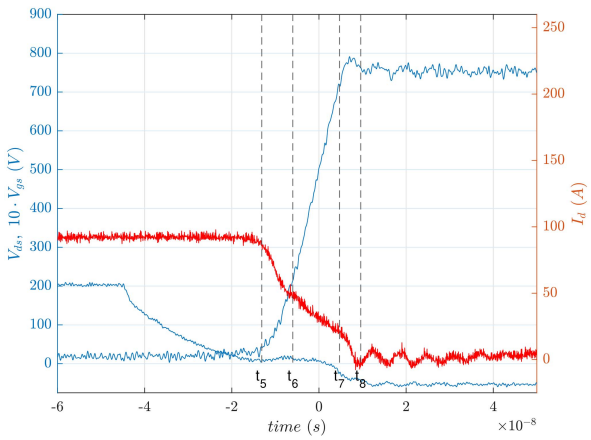


Fig. 7. Instrumentation of double pulse test: High voltage isolated probe across the lower device, low voltage isolate probe across the gate of the lower device, and the ultrafast current shunt [37] for the source current of the lower device.



(a)



(b)

Fig. 8. Zero gate resistor DPT test. (a) Turn-ON event and (b) turn-OFF event; at 800 V 100 A.

regions (t_2–t_3 and t_3–t_4) in the descent of the current, marked by a clear change in the slope of the current. This change in the slope is primarily attributed to the nonlinearity of the C_{oss}, which changes spontaneously with the change of the voltage across the devices during the switching period. This observation is consistent with the results reported in [38] and [39].

The turn-OFF event is shown in Fig. 8(b). The current slew rate is approximately 6.25 A/ns and the voltage slew rate is approximately 55 V/ns. The turn-OFF event can be divided into two main regions.

1) t_5–t_7: The first segment of the current is primarily attributed to the charging current of the lower device C_{oss}. Although this current is detected by the current shunt positioned at the source of the lower device, it does not flow through the lower device channel and thus it is not entirely responsible to the turn-OFF energy losses encountered during the turn-OFF process. The lower device C_{oss} charges as long as the V_{ds} is increasing. The change in the slope of the current between t_5–t_6 and t_6–t_7 is a result of the nonlinearity of the C_{oss} value as the V_{ds} changes.
2) t_7–t_8: The second segment of the turn-OFF current starts after the V_{ds} reaches the dc-link value. The current exhibits a faster slew rate of 9 A/ns and it passes through the device channel. The near-zero turn-OFF losses (ZTL) achieved here are consistent with the conditions described in [39] and [40].

B. Power Loop Inductance

The power loop inductance can be calculated by considering the ringing frequency at the turn-OFF event and the value of the output capacitor of the SiC MOSFET under test. However, the output capacitance as well as the additional parastic capacitance from the PCB is difficult to estimate. In this article, we use a method of taking the negative derivative of the current waveform and scaling it with the dip in the voltage during the device turn-ON in this case, the power loop inductance is sought to be approximately 1 nH.

The evidence of the extremely low power loop inductance can be seen by almost no overshoot in V_{ds} during the device turn-OFF event. Both, the low ringing and low gate loop inductance result in a clean gate voltage turn-ON and turn-OFF signals. An additional validation approach for the power loop inductance is by using the following criteria: during the turn-ON event, the current starts to increase when V_{gs} reaches the threshold voltage, while V_{ds} starts to decrease when V_{gs} reaches the Miller plateau. The voltage dip observed between these two events is solely due to the stray inductance in the power loop, and it can be calculated by using the standard inductor equation $L_{\text{stray}} = \frac{dv}{di/dt}$. Both dv, di, and dt are illustrated in the experimental results shown in Fig. 9. This gives a power loop inductance of 1 nH. It should be emphasized that this method neglects the impact of inductance across V_{ds} measurement pins. Furthermore, an additional inductance was acquired due to the presence of an extra path from the shunt current sensor [37].

C. Gate Loop Inductance

The standard cell Kelvin connection forms a gate and source electrical connection between the die and the gate driver circuit. The gate and source paths are negatively coupled by utilizing the top and bottom layers of the flex-PCB. The effectiveness

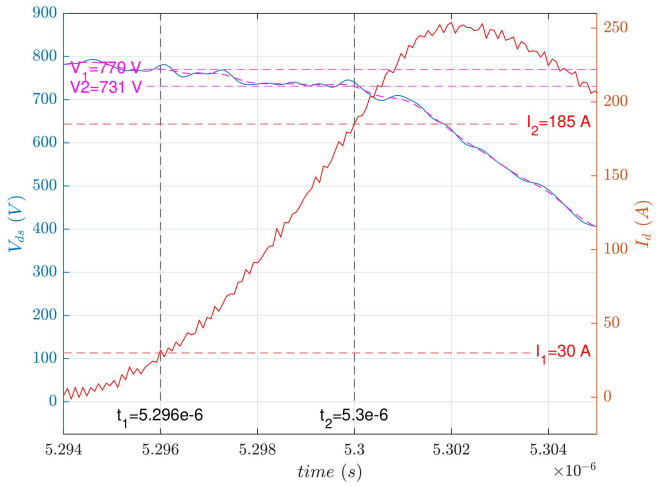


Fig. 9. Stray power loop inductance is approximated using the inductor equation, $L_{\text{stray}} = \frac{V_2 - V_1}{(I_2 - I_1)/(t_2 - t_1)} = 1$ nH.

of Kelvin connection is experimentally validated through the introduction of inductances at various points within the gate loop. The first scenario involves the inclusion of inductance in series with the gate loop, denoted as L_{insert}, as depicted in Fig. 10(a). Importantly, it is observed that the insertion of external inductance does not introduce any additional switching losses as demonstrated in Fig. 10(b).

The second scenario is evaluated by overriding the Kelvin source connection within the standard cell and establishing a direct wire connection from the gate ground plane to the source plane on the PCB, as depicted in Fig. 10(c). In this configuration, the common source inductance, denoted as L_{S-c}, is estimated to be 5 nH, a value is deemed adequate for assessing the impact of the standard cell Kelvin connection. During switching events, both the device load current and the gate current flow through the common source inductance, resulting in a voltage drop that opposes the gate driver voltage. This voltage drop effectively slows down the switching transition speed and results in elevated turn-ON and turn-OFF losses, as it is observed in the experimental result Fig. 10(d).

The experimental results presented in this study demonstrate significant energy savings attributed to the utilization of the Kelvin connection configuration in the standard cell. These findings are validated by a comprehensive analysis of energy losses in two distinct scenarios, as illustrated in Fig. 11. Specifically, we compare the energy losses in a standard cell equipped with a Kelvin connection to a standard cell without this connection. Our results reveal that the standard cell with an overridden Kelvin connection exhibits a 10% increase in switching losses when compared to the baseline standard cell. This observed increment in switching losses can be directly attributed to the presence of additional common source inductance, denoted as L_{S-c}. Furthermore, it is noteworthy that the extent of switching losses is anticipated to further increase with an increase in the value of L_{S-c}, as reported in literature [41]. These findings underscore

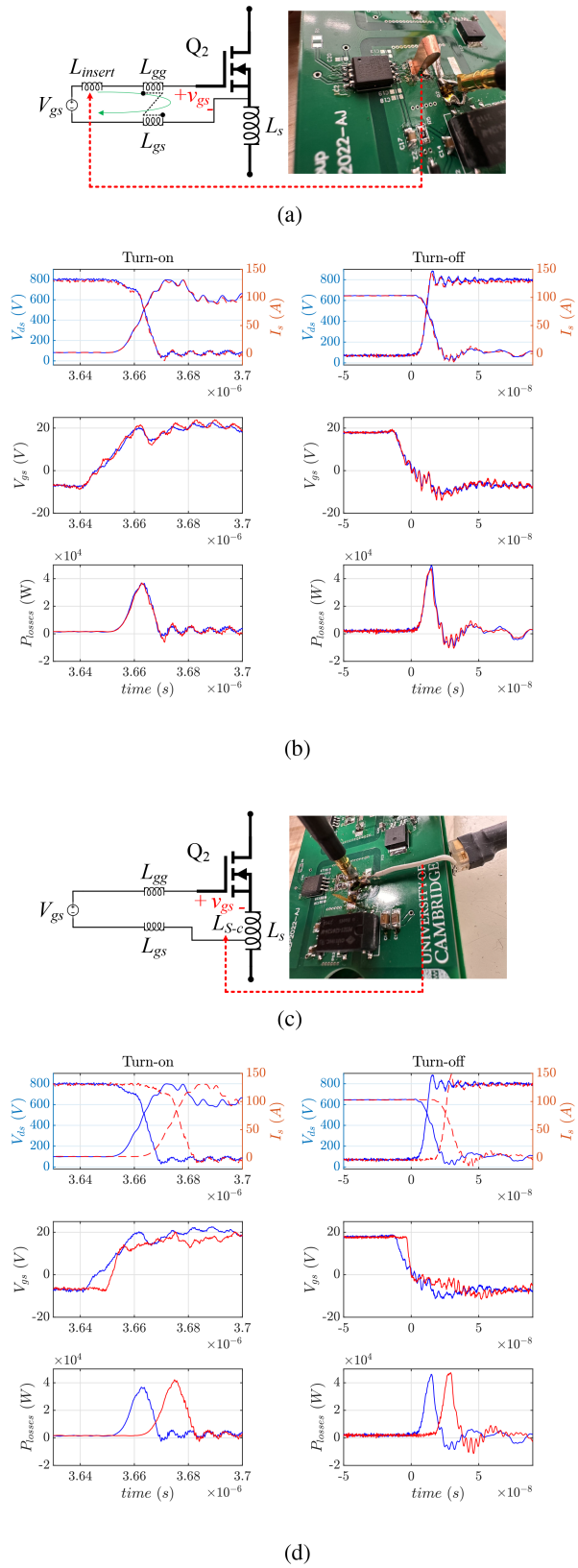


Fig. 10. Simplified circuit diagrams. (a) Gate loop with inserted inductance. (b) Comparison with baseline configuration. (c) Overriding the Kelvin connection of standard cell. (d) Comparison with baseline configuration.

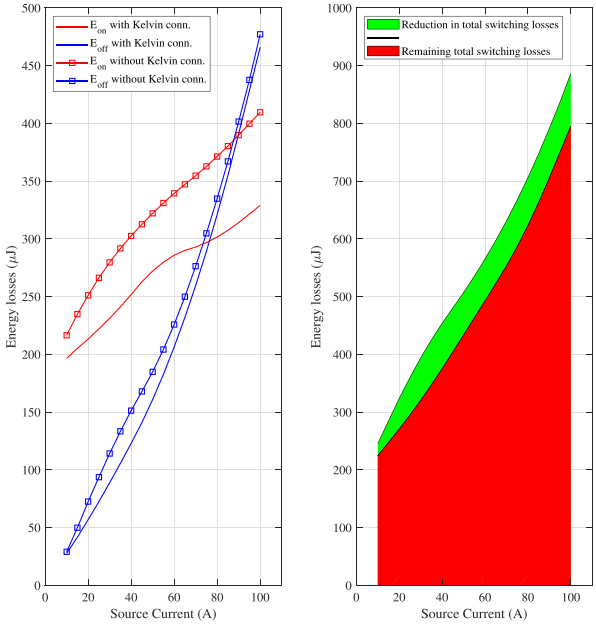


Fig. 11. Comparison of the standard cell switching losses with and without Kelvin connection.

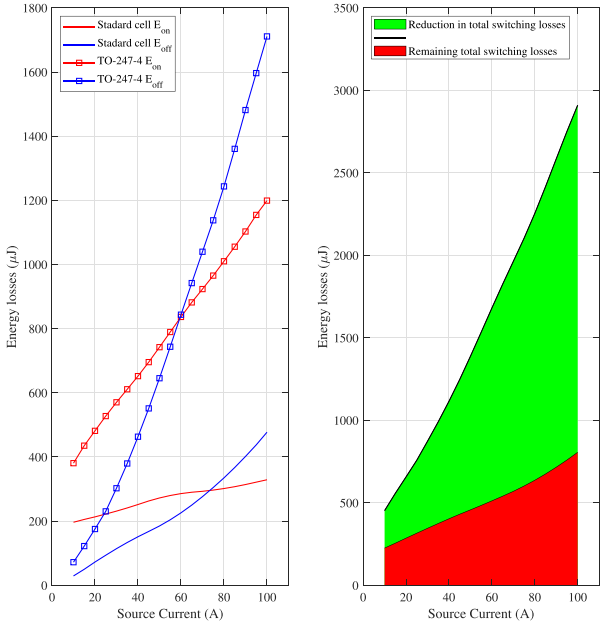


Fig. 12. Experimental comparison of switching losses between the standard cell package and the TO-247-4 package, utilizing the *SCT116N120G3DXAG* die in both packages.

the importance of careful consideration and optimization of the common source inductance in the design of the standard cell.

D. Switching Losses

In order to benchmark the reduction in switching losses with the standard cell, it is compared with manufacturer provided data of TO-247-4 package utilizing the same *SCT116N120G3DXAG* die from STMicroelectronics. The standard cell test for this comparison used a gate resistor of 4.7 Ω to match the system test conditions of the TO-247 from the manufacturer datasheet. Fig. 12 presents a comparison of the turn-ON and turn-OFF switching energies between the two packages. At a current of 100 A, the turn-ON and turn-OFF energies were reduced by 72%. Additionally, switching loss energies of the standard cell were assessed at different dc-link voltages, including 400, 600, and 800 V, as illustrated in Fig. 13.

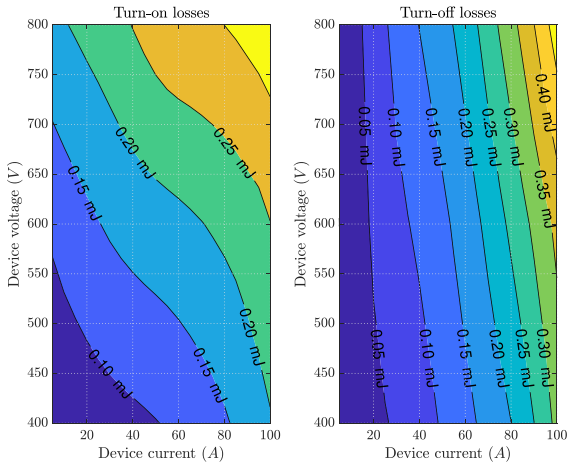


Fig. 13. Experimental comparison highlighting switching energies of the standard cell package at various DC-link voltages.

E. Continuous Testing

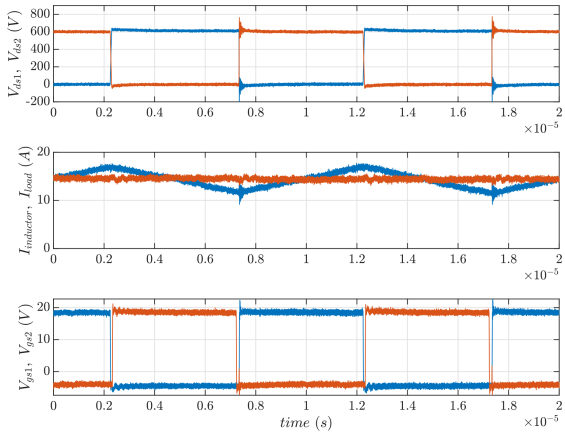
The continuous mode testing of the half-bridge using a standard cell is performed with buck converter circuit handling load currents up to 15 A, as shown in Fig. 14(a). The results of the evaluation underscore the magnitude of cross-talk observed at the gate voltage of the complementary device. Despite the presence of rapid switching transients, the utilization of a zero gate resistor effectively maintains the Miller effect below the threshold voltage as shown in Fig. 14(b).

F. Breakdown Voltage and Leakage Current Measurements

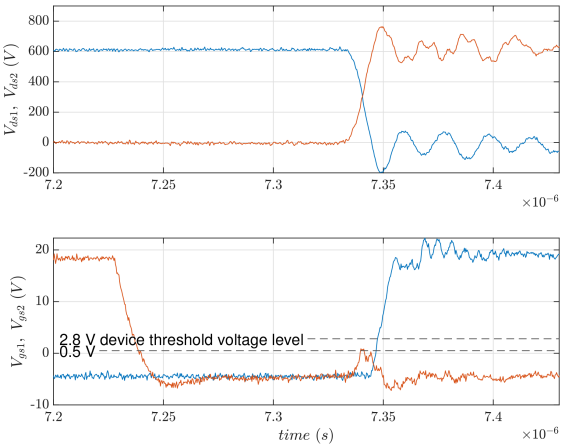
The leakage current test is conducted on the standard cell using a KEYSIGHT B1505 A curve tracer. The test criteria state that the leakage current I_{DSS} at 100% of the device rated voltage $V_{ds} = 1.2\,\text{kV}$ and gate voltage $V_{gs} = 0$ shall not exceed the nominal leakage current limit of the die set by the manufacturer, which is 10 μA. With this test, we can guarantee that the standard cell packaging successfully provides isolation between the drain and source of the die. The experimental results shown in Fig. 15 were conducted at room temperature 25 °C. It can be seen that at 1.2 kV, the leakage current is 74 nA, which is 135 times less than I_{DSS} limit.

G. Transient Thermal Impedance for the Standard Cell

The transient thermal impedance from the SiC MOSFET junction to the standard cell case, was measured using the Simcenter Micred Power Tester (T3Ster) following *JEDEC* standards. The process begins with a calibration step, utilizing the SiC MOSFET's



(a)



(b)

Fig. 14. (a) Continuous testing waveforms of Buck converter with 600 V input voltage and 15 A load current. (b) Zoom-in to the hard switching event of the upper device and the resulting cross-talk at the lower device gate voltage.

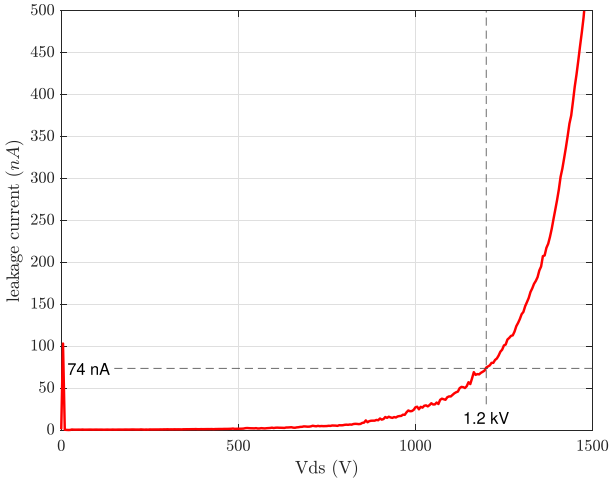
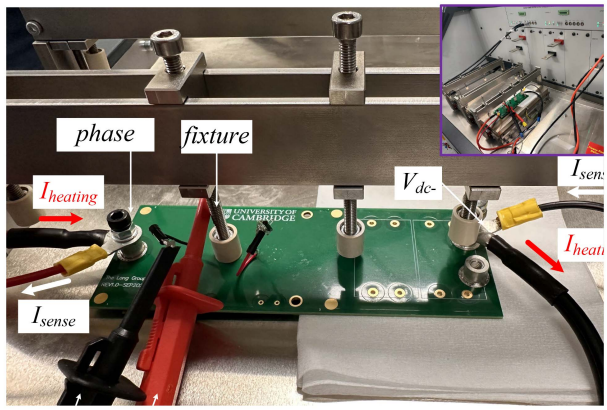
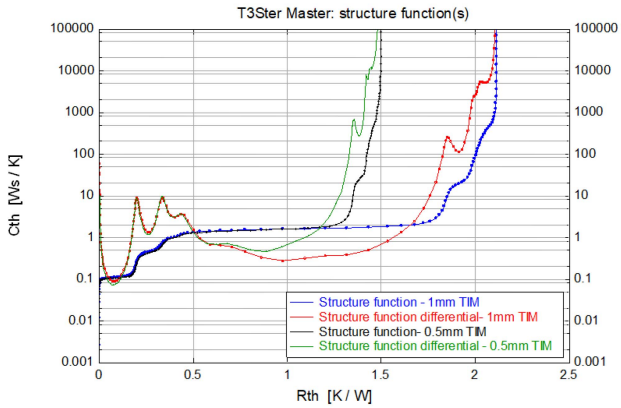


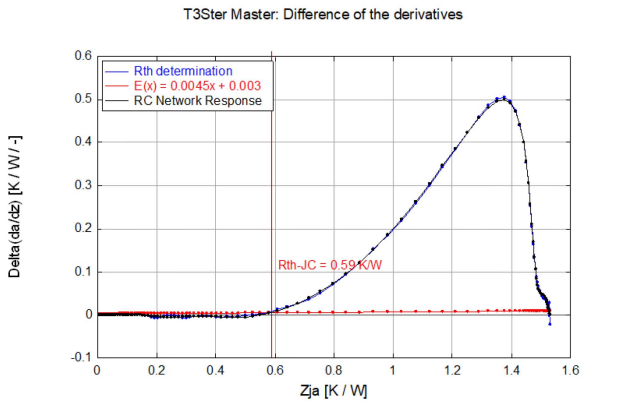
Fig. 15. Curve tracer leakage current test. The SiC die manufacturer leakage current acceptable limits is 10 μA.



(a)



(b)



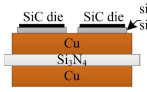
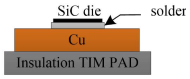
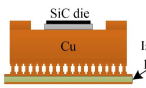
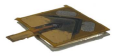
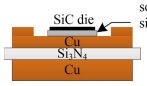
(c)

Fig. 16. (a) Transient thermal impedance test setup, (b) the structure-function for 0.5 mm TIM and 1.5 mm TIM, and (c) the difference of derivatives for $R_{\text{th}-JC}$ determination.

body diode to create a lookup table linking the diode forward voltage drop to the junction temperature.

The device calibration involves heating the device using an external temperature-controlled plate and monitoring the forward voltage of the body diode across a range of device temperatures. To ensure accurate measurements, the body diode forward

TABLE III
JUNCTION TO THE ISOLATED CASE THERMAL RESISTANCE $R_{\text{TH}-JC}$ ($\frac{K}{W}$), AND THE $FOM = R_{\text{TH}} \cdot A_{\text{DIE}}$ ($\frac{mm^2\,K}{W}$) FOR STATE-OF-THE-ART COMMERCIAL DISCRETE PACKAGES COMPARED TO THE PROPOSED STANDARD CELL

Package type	Illustration	Layers stack	R_{th-JC}	$R_{th} \cdot A_{die}$	Remarks
ST PAK/IDPAK			0.6[45]	15	-Two dies in parallel per ST PAK/IDPAK package which divides the R_{th-JC} by two. -The reported case to fluid temperature is 0.35 K/W which lead to total effective $R_{th-JA} = 0.95\ K/W$
TO-247-4L/TO247plus			1.3	32	-Non-isolated package, which required an external TIM pad. -The comparative R_{th-JC} is given considering 150 um TIM thickness with 4 W/mK. -The R_{th} of junction to the non-isolated case of the TO-247 is $0.25 - 0.33\ K/W$[46].
Embedding/p^2 Pack, ABB			0.58, 0.5[47]	17.545, 24.32	-The die size is 30.25 mm^2 whereas the die size used in the proposed standard cell is 25 mm^2. - The isolation voltage is for 48 V application. To support the 1.2 kV die, a significantly thicker insulation prepreg shall be used.
Proposed standard cell			0.59	14.75	-The low thermal resistance is due to the reduction of the AMB top copper thickness. -The thermal resistance can be further reduced to 0.47 when silver sintering is used for die attach.

current was restricted to 100 mA to mitigate any current-induced heat effects. Additionally, to ensure complete deactivation of the MOSFET channel, the gate voltage was biased to -8 V. Our methodology yielded an accuracy of $0.1\,^{\circ}$C in junction temperature estimation.

After the calibration step, the device was interfaced with the cooling plate through a thermal interface material (TIM), as depicted in Fig. 16(a). Subsequently, a heating current was passed through the MOSFET channel to induce thermal losses within the die. Typically, 60% of the rated current was applied to achieve a substantial temperature difference (ΔT) at the MOSFET junction. This significant ΔT is chosen to minimize measurement noise and enhance the accuracy of system temperature sensing. The heating current was consistently applied for a duration of 30 s to ensure that the system attained a thermal steady-state condition. This heating current was then interrupted, to allow 100 mA sensing current to pass through the body diode while recording the temperature during the cooling phase in the form of forward voltage across the body diode. The data from the cooling phase are subsequently subjected to post processing to derive the structure function of the thermal layer stack. To determine the thermal impedance from the junction to case of the standard cell, the test was repeated using two different thicknesses of thermal interface material (TIM), namely, 0.5 and 1.5 mm. The separation evident in the structure function, as depicted in Fig. 16(b), indicates the point at which thermal resistance occurred between the SiC die and the standard cell case. The accumulative structure function and its derivative curves did not exhibit a smooth separation, making it challenging to pinpoint a well defined separation point. A more precise determination of the separation point is essential to accurately estimate the junction to case thermal impedance. To achieve this, the difference in derivatives for both cases was calculated and then normalized by ΔT to yield the steady-state difference in thermal impedance. Given that the normalized difference included some noise, an exponential or *RC*-network fit was applied to estimate $R_{\text{th}-JC}$ with the minimal error. The $R_{\text{th}-JC}$ has identified as the point of intersection between the *RC*-network fitted curve and the trend line $\epsilon = 0.0045 R_{\text{th}-JC} + 0.003$, as illustrated in Fig. 16(c). Consequently, the thermal resistance from the junction to the case of the standard cell was determined to be 0.59 K/W. The detailed values of the Cauer and Foster circuit models are shown in Table IV of the appendix.

Table III shows the effective junction to case packaging thermal resistance for the standard cell compared with other conventional and competitive technologies. The table also shows a figure of merit (FOM) derived as the thermal resistance of the package multiplied by the die area. The lower the FOM the more effective the thermal layer stack in conducting the heat flux from the die to the heatsink. It is important to consider that the definition of the junction-to-case thermal resistance must specify whether the case is electrically isolated or not. A nonisolated package requires an external isolation layer, which introduces additional thermal resistance. Since the standard cell is an isolated package, the comparison in Table III includes the isolation layer as part of the overall isolated package layer stack.

VI. CONCLUSION

This article proposes a novel packaging design for SiC MOSFET, namely, the standard cell, which can be used in most of converter circuit as a surface-mounted discrete device. The design of the standard cell focuses on power loop inductance, gate loop inductance, thermal resistance, current density distribution, and isolation/electric field gradient. An experimental prototype of a half-bridge configuration is presented to validate the proposed standard cell. Double-pulse testing results show that the achieved stray power loop inductance is within 1 nH and gate loop inductance is within 1.5 nH. The turn-ON and turn-OFF energies are reduced by approximately 72% compared to the

conventional TO-247-4 L package. Furthermore, the presented standard cell is tested in continuous loading condition in a buck converter topology. The thermal impedance of the standard cell is determined using *JEDEC* standards, revealing a 0.59 k/W junction-to-case thermal resistance. Further investigation into die paralleling and optimization of transient current sharing will be reported in subsequent articles.

APPENDIX

A. Creepage and Clearance Calculation1

This section presents a step-by-step guideline for determining the required creepage and clearance distances based on *IEC-60664-1* and *IEC-60664-4* standards.

B. Cauer and Foster Network

The Cauer network, from R0 to R2 is the cumulative $R_{\text{th}-JC} = 0.59\,K/W$ which is the junction-to-case thermal resistance. This value is visible in the structure function with the derivatives graph as shown in Fig. 16(b). The junction to case thermal resistance can be designated as the point where the derivatives meet for the last time as shown in Fig. 16(a). While Cauer's model is compounding to an actual physical layer in the thermal layer stack, Foster's model does not correspond to an actual physical thermal layer stack.

TABLE IV
CAUER AND FOSTER NETWORK

.SUBCKT CAUER 1 6	.SUBCKT FOSTER 1 6
C0 1 0 0.11645901430195142	C0 1 2 0.2330343648827001
R0 1 2 0.21580486484548622	R0 1 2 0.071986499568534007
C1 2 0 0.39908388189275812	C1 2 3 0.39256839282504319
R1 2 3 0.13744627072988552	R1 2 3 0.086579035371261562
C2 3 0 0.54991663664616508	C2 3 4 0.98251866551623457
R2 3 4 0.22917511304472399	R2 3 4 0.099215425050721132
C3 4 0 0.61098220218163857	C3 4 5 1.3761631758407455
R3 4 5 0.82248817530217067	R3 4 5 1.1348323193591274
C4 5 0 303.92270253740207	C4 5 6 268.66810006389147
R4 5 6 0.089243670342240955	R4 5 6 0.10154481491486322

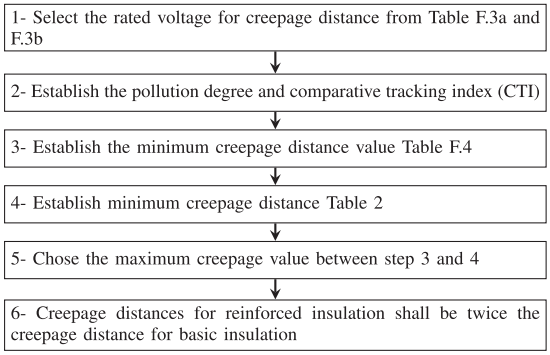


Fig. 17. Creepage calculation based on *IEC-60664-1* and *IEC-60664-4* standards, for rated voltage of 1 kV, pollution degree 1, and CTI index 1, the required creepage is 3.2 mm for the functional isolation and 6.4 mm for the reinforced isolation.

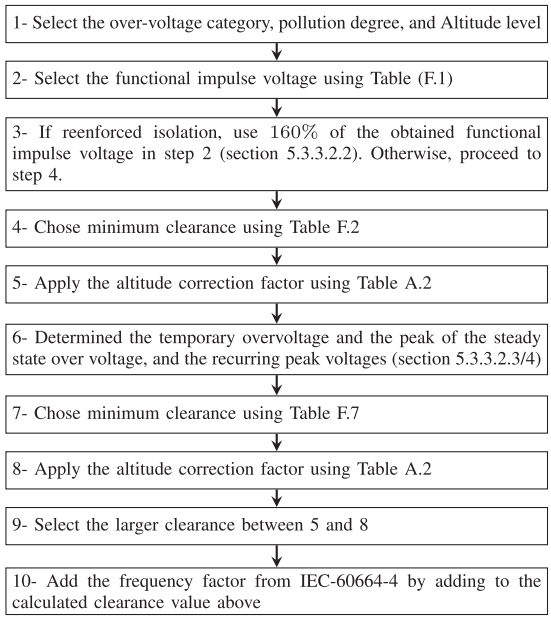


Fig. 18. Clearance calculation based on *IEC-60664-1* and *IEC-60664-4* standards. For a rated voltage of 1 kV, over-voltage category I, pollution degree 1, and altitude of 4000 m, the required clearance is 6.2 mm for the functional isolation and 11 mm for the reinforced isolation.

REFERENCES

[1] X. She, A. Q. Huang, Ó. Lucía, and B. Ozpineci, "Review of silicon carbide power devices and their applications," *IEEE Trans. Ind. Electron.*, vol. 64, no. 10, pp. 8193–8205, Oct. 2017.

[2] H. Lee, V. Smet, and R. Tummala, "A review of SiC power module packaging technologies: Challenges, advances, and emerging issues," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 1, pp. 239–255, Mar. 2020.

[3] R. Alizadeh and H. A. Mantooth, "A review of architectural design and system compatibility of power modules and their impacts on power electronics systems," *IEEE Trans. Power Electron.*, vol. 36, no. 10, pp. 11631–11646, Oct. 2021.

[4] F. Hou et al., "Review of packaging schemes for power module," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 1, pp. 223–238, Mar. 2020.

[5] Y. Yang, L. Dorn-Gomba, R. Rodriguez, C. Mak, and A. Emadi, "Automotive power module packaging: Current status and future trends," *IEEE Access*, vol. 8, pp. 160126–160144, 2020.

[6] C. Chen, F. Luo, and Y. Kang, "A review of SiC power module packaging: Layout, material system and integration," *CPSS Trans. Power Electron. Appl.*, vol. 2, no. 3, pp. 170–186, Sep. 2017.

[7] M. Ando and K. Wada, "Design of acceptable stray inductance based on scaling method for power electronics circuits," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 5, no. 1, pp. 568–575, Mar. 2017.

[8] A. D. Callegaro et al., "Bus bar design for high-power inverters," *IEEE Trans. Power Electron.*, vol. 33, no. 3, pp. 2354–2367, Mar. 2018.

[9] C. Bi, R. Lu, and H. Li, "Prediction of electromagnetic interference noise in SiC MOSFET module," *IEEE Trans. Circuits Syst. II: Express Briefs*, vol. 66, no. 5, pp. 853–857, May 2019.

[10] K. Abe, M. Ishihara, Y. Hatakenaka, K. Umetani, and E. Hiraki, "Feasibility of parasitic drain inductance design for minimizing switching loss in bridge circuits using GaN-FETs," in *Proc. IEEE 30th Int. Symp. Ind. Electron.*, 2021, pp. 1–5.

[11] P. Liu, R. Yu, A. Q. Huang, and J. Strydom, "Turn-on gate resistor optimization for paralleled SiC MOSFETs," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2020, pp. 2810–2814.

[12] X. Sun et al., "Design and evaluation of a face-down embedded SiC power module with low parasitic inductance and low thermal resistance," *IEEE Trans. Power Electron.*, vol. 38, no. 3, pp. 2799–2804, Mar. 2023.

[13] F. Hou, W. Wang, T. Lin, L. Cao, G. Q. Zhang, and J. A. Ferreira, "Characterization of PCB embedded package materials for SiC MOSFETs," *IEEE Trans. Compon. Packag. Manuf. Technol.*, vol. 9, no. 6, pp. 1054–1061, Jun. 2019.
[14] Y. Park, S. Chakraborty, and A. Khaligh, "Characterization of a bare-die SiC-Based, wirebond-less, integrated half-bridge with multi-functional bus-bars," *IEEE Trans. Transp. Electrific.*, vol. 8, no. 3, pp. 3946–3959, Sep. 2022.
[15] J. Knoll, G. Son, C. DiMarino, Q. Li, H. Stahr, and M. Morianz, "Design and analysis of a PCB-Embedded 1.2 kV SiC half-bridge module," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2021, pp. 5240–5246.
[16] J. S. Knoll, G. Son, C. DiMarino, Q. Li, H. Stahr, and M. Morianz, "A PCB-Embedded 1.2 kV SiC MOSFET half-bridge package for a 22 kW AC–DC converter," *IEEE Trans. Power Electron.*, vol. 37, no. 10, pp. 11927–11936, Oct. 2022.
[17] F. Hou et al., "Fan-out panel-level PCB-Embedded SiC power MOSFETs packaging," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 1, pp. 367–380, Mar. 2020.
[18] Y. Qian, F. Hou, J. Fan, Q. Lv, X. Fan, and G. Zhang, "Design of a fan-out panel-level SiC MOSFET power module using ant colony optimization-back propagation neural network," *IEEE Trans. Electron Devices*, vol. 68, no. 7, pp. 3460–3467, Jul. 2021.
[19] M. Montazeri et al., "Vertically stacked, flip-chip wide bandgap MOSFET co-optimized for reliability and switching performance," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 4, pp. 3904–3915, Aug. 2021.
[20] S. Seal, M. D. Glover, and H. A. Mantooth, "3 -D wire bondless switching cell using flip-chip-bonded silicon carbide power devices," *IEEE Trans. Power Electron.*, vol. 33, no. 10, pp. 8553–8564, Oct. 2018.
[21] T. Gottwald and C. Roessle, "Minimizing form factor and parasitic inductances of power electronic modules: The p2 pack technology," in *Proc. 7th Electron. Syst.-Integration Technol. Conf.*, 2018, pp. 1–7.
[22] T. Gottwald, M. Martina, C. Marczok, M. Laumen, B. Flieger, and O. Wendt, "Power embedding," in *Proc. 12th Int. Conf. Integr. Power Electron. Syst.*, 2022, pp. 1–7.
[23] Q. Huang, C. Peng, S. F. -M. Ellen, W. Zhu, and L. Wang, "A finite element analysis on the reliability of heavy bonding wire for high-power IGBT module," *IEEE Trans. Components, Packag. Manuf. Technol.*, vol. 11, no. 2, pp. 212–221, Feb. 2021.
[24] I. Ndip, A. Öz, H. Reichl, K. -D. Lang, and H. Henke, "Analytical models for calculating the inductances of bond wires in dependence on their shapes, bonding parameters, and materials," *IEEE Trans. Electromagn. Compat.*, vol. 57, no. 2, pp. 241–249, Apr. 2015.
[25] E. Dechant, N. Seliger, and R. Kennel, "Performance of a GaN half bridge switching cell with substrate integrated chips," in *Proc. PCIM Europe; Int. Exhib. Conf. Power Electron., Intell. Motion*, 2019, pp. 1–7.
[26] E. Dechant, N. Seliger, and R. Kennel, "A study of dielectric breakdown of a half-bridge switching cell with substrate integrated 650 V GaN dies," in *Proc. IEEE Int. Workshop Integr. Power Packag.*, 2019, pp. 18–23.
[27] I. Kasko, S. E. Berberich, M. Gross, P. Beckedahl, and S. Buetow, "High efficient approach to utilize SiC MOSFET potential in power modules," in *Proc. 29th Int. Symp. Power Semicond. Devices*, 2017, pp. 259–262.
[28] P. Beckedahl, I. Bogen, and J. Steger, "SiC automotive power module with laser welded, ultra low inductive terminals and up to 900Arms phase current," in *Proc. 12th Int. Conf. Integr. Power Electron. Syst.*, 2022, pp. 1–5.
[29] P. Beckedahl, M. Spang, and O. Tamm, "Breakthrough into the third dimension - sintered multi layer flex for ultra low inductance power modules," in *Proc. 8th Int. Conf. Integr. Power Electron. Syst.*, 2014, pp. 1–5.
[30] A. Miric and P. Dietrich, "Inorganic substrates for power electronics applications," *Heraeus Deutschland*, 2015. [Online]. Available: https://www.heraeus.com/media/media/het/doc_het/products_and_solutions_het_documents/metal_cermaic_substrates_documents/Inorganic_Substrates_for_Power_Electronics_2015-3_AMiric-PDietrich_V8.pdf
[31] Y. Li et al., "Application of Ag-Cu-Ti active metal composite filler in ceramic joining: A review," *Front. Mater. Sci.*, vol. 17, 2023, Art. no. 230664.
[32] F. W. Grover, *Inductance Calculations: Working Formulas and Tables*. New York, NY, USA: Dover Publications, 1946.
[33] H. Wen and W. Xiao, "Design and optimization of laminated busbar to reduce transient voltage spike," in *Proc. IEEE Int. Symp. Ind. Electron.*, 2012, pp. 1478–1483.
[34] C. Chen, Z. Huang, L. Chen, Y. Tan, Y. Kang, and F. Luo, "Flexible PCB-based 3-D integrated SiC half-bridge power module with three-sided cooling using ultralow inductive hybrid packaging structure," *IEEE Trans. Power Electron.*, vol. 34, no. 6, pp. 5579–5593, Jun. 2019.
[35] L. Yin, C. Kapusta, A. Gowda, and K. Nagarkar, "A wire-bondless packaging platform for silicon carbide power semiconductor devices," *ASME. J. Electron. Packag.*, vol. 140, Jul. 2018, Art. no. 031009.
[36] L. D. Stevanovic, R. A. Beaupre, E. C. Delgado, and A. V. Gowda, "Low inductance power module with blade connector," in *Proc. 25th Annu. IEEE Appl. Power Electron. Conf. Expo.*, Palm Springs, CA, USA, 2010, pp. 1603–1609.
[37] L. Shillaber, Y. Jiang, L. Ran, and T. Long, "Ultrafast current shunt (UFCS): A gigahertz bandwidth ultra-low-inductance current sensor," *IEEE Trans. Power Electron.*, vol. 37, no. 12, pp. 15493–15504, Dec. 2022.
[38] X. Wang, "Switching transients optimization and investigations into threshold voltage shift for SiC MOSFETs using a current-controlled gate driver," Ph.D dissertation, Newcastle University, Newcastle upon Tyne, U.K., 2022.
[39] X. Li et al., "Achieving zero switching loss in silicon carbide MOSFET," *IEEE Trans. Power Electron.*, vol. 34, no. 12, pp. 12193–12199, Dec. 2019.
[40] S. Song, H. Peng, X. Chen, Q. Xin, and Y. Kang, "Determination and implementation of SiC MOSFETs zero turn-off loss transition considering no Miller plateau," *IEEE Trans. Power Electron.*, vol. 38, no. 12, pp. 15509–15521, Dec. 2023.
[41] G. Engelmann et al., "Impact of the different parasitic inductances on the switching behavior of SiC MOSFETs," in *Proc. IEEE 18th Int. Power Electron. Motion Control Conf.*, Budapest, Hungary, 2018, pp. 918–925.
[42] JEDEC Solid State Technology Association, "Addendum no. 3 to JESD24—Thermal impedance measurements for vertical power MOSFETs (delta source-drain voltage method)," JESD24-3, Nov. 1990. [Online]. Available: https://www.jedec.org/standards-documents/docs/jesd-24-3
[43] S. Singh et al., "Effects of die-attach voids on the thermal impedance of power electronic packages," *IEEE Trans. Components, Packag. Manuf. Technol.*, vol. 7, no. 10, pp. 1608–1616, Oct. 2017.
[44] STMicroelectronics, "Automotive silicon carbide Power MOSFET 1200 V, 130 A, 14.6 mΩ," *DS14312-Rev1*, Jun. 2023.
[45] Infineon, "Automotive silicon carbide Power MOSFET 1200 V, 127 A, 14.6 mΩ," *IMW120R014M1H*, May 2023.
[46] D. Kearney, S. Kicin, E. Bianda, A. Krivda, and D. Bauman, "PCB embedded power electronics for low voltage applications," in *Proc. 9th Int. Conf. Integr. Power Electron. Syst.*, Nuremberg, Germany, 2016, pp. 1–6.

Ameer Janabi was born in Babylon, Iraq. He received the Ph.D. degree in power electronics typology and control from Michigan State University, East Lansing, MI, USA, in 2021.

He has worked for several automotive companies in Detroit, including Eaton e-mobility as a Power Electronics Specialist and Magna International as an Inverter Design Expert. He is also a consultant for FEV North America, Auburn Hills, MI, USA. He has been serving as a Research Associate in integrated power electronics with the University of Cambridge, Cambridge, U.K., since 2022, with an affiliation to Trinity College.

Luke Shillaber (Student Member, IEEE) received the B.A. and M.Eng. degrees in electrical and electronics engineering 2018 from the University of Cambridge, Cambridge, U.K., where he is currently working toward the Ph.D. degree in low inductance packaging and sensing with the Department of Engineering.

His research interests include high-speed switching of wide-bandgap semiconductors and high bandwidth power measurements.

Wucheng Ying received the honoured B.Eng. degree in electrical and electronic engineering from the University of Nottingham, Nottingham, U.K., in 2018. He is currently working toward the Ph.D. degree in engineering with the University of Cambridge, Cambridge, U.K.

His research interests include dual-active-bridge converters, magnetic component optimization and coupling techniques, ZVS techniques, power transistor characterization, etc.

Wei Mu (Graduate Student Member, IEEE) received the B.S. and the M.Sc. degrees in electrical engineering from Xi'an Jiaotong University, Xi'an, China, in 2019 and 2022, respectively. Between 2017 and 2019, he undertook a double degree program from CentraleSupélec, Université Paris-Saclay, Gif-sur-Yvette, France, where he received the engineer degree (Diplome d'Ingénieur). He is currently working toward the Ph.D. degree in power electronic packaging and reliability with Cambridge Power Electronics Laboratory, University of Cambridge, Cambridge, U.K.

. His research interests include packaging design, AI empowered reliability monitoring, thermal management of power converters, and the application and integration of wide bandgap power semiconductors.

Borong Hu (Member, IEEE) received the B.Eng. degree in electrical engineering from Chongqing University, Chongqing, China, in 2014, and the Ph.D. degree in power electronics from the University of Warwick, Coventry, U.K., in 2021.

He is currently a Postdoctoral Research Associate with the University of Cambridge, Cambridge, U.K., and the founder of PowerSense Technology Ltd., Tonbridge, U.K. His research interests include machine learning, intelligent design and operation, packaging integration, reliability, and condition monitoring of power electronic systems.

Dr. Hu was the recipient of IEEE ECCE William Portnoy Award, U.K. EPSRC Supergen ORE ECR Award, and the Cambridge Chris Abell Prize.

Yunlei Jiang (Member, IEEE) received the B.Eng. degree from Nanjing Normal University, Nanjing, China, in 2015, the M.Sc. degree from Southeast University, Nanjing, in 2018, and the Ph.D. degree from the University of Cambridge, Cambridge, U.K., under the support of Jardine-Cambridge Scholarship, in 2023, all in engineering.

He is currently a Senior Power Electronics Engineer (Starship) with SpaceX, Hawthorne, CA, USA. From 2018 to 2019, he was a Research Assistant with WEMPEC, University of Wisconsin Madison, Madison, WI, USA. In 2022, he was a Power Electronics Intern with the drive inverter team of Tesla Motor, Palo Alto, CA. His current research interests include high-reliability packaging, thermal design, and system integration of power electronics.

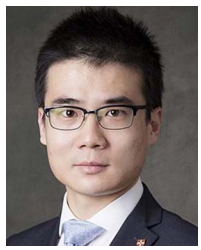
Dr. Jiang was awarded the 2023 William M. Portnoy Prize Paper Award from IEEE-IAS Power Electronics Devices and Components Committee (PEDCC).

Nikolaos Iosifidis (Graduate Student Member, IEEE) received the B.Sc. degree in physics from Aristotle University of Thessaloniki, Thessaloniki, Greece, in 2019, and the M.Sc. degree in sustainable energy technologies in 2020 from the University of Warwick, Coventry, U.K., where he is currently working toward the Ph.D. degree in packaging of power electronics.

Li Ran (Fellow, IEEE) received the Ph.D. degree in power systems engineering from Chongqing University, Chongqing, China, in 1989.

He was a Research Associate with the Universities of Aberdeen, Nottingham, and Heriot-Watt, Aberdeen, Nottingham, and Edinburgh, U.K., respectively. He became a Lecturer in Power Electronics with Northumbria University, Newcastle upon Tyne, U.K., in 1999, and was seconded to Alstom Power Conversion, Kidsgrove, U.K., from 2001 to 2003. Between 2003 and 2012, he was with Durham University, Durham, U.K., where he was promoted to a Chair in Electrical Power in 2010. He took a sabbatical leave from the Massachusetts Institute of Technology, Cambridge, MA, USA, in 2007. He joined the University of Warwick, Coventry, U.K., as a Professor in Power Electronics - Systems, in 2012. Currently, he is part time with the University of Warwick, Coventry, U.K., and Chongqing University. His research interests include reliability and packaging of power semiconductors for electric power generation, delivery, and utilization.

Dr. Ran shared, with his coauthors, prize paper awards from IEEE Power Electronics and Industry Applications Societies.



Teng Long (Member, IEEE) received the B.Eng. degree in electrical engineering from the Huazhong University of Science and Technology, Wuhan, China, the B.Eng. (first-class Hons.) degree from the University of Birmingham, Birmingham, U.K., in 2009, and the Ph.D. degree in electrical engineering from the University of Cambridge, Cambridge, U.K., in 2013.

Until 2016, he was a Power Electronics Engineer with the General Electric (GE) Power Conversion, Rugby, U.K. He is currently a Full Professor with the University of Cambridge. His research interests include power electronics, electrical machines, and machine drives.

Dr. Long is a Chartered Engineer (CEng) registered with the Engineering Council in the U.K.