# Common-Leg Coupled Inductor Configuration in a Three-Level Interleaved DC–DC Medium Voltage SiC-Based Converter

Michał Harasimczuk, *Member, IEEE*, Rafał Kopacz, *Member, IEEE*, Rafał Miśkiewicz, *Member, IEEE*, Radosław Sobieski, and Jacek Rąbkowski, *Senior Member, IEEE*

***Abstract*—The article proposes and investigates an alternative coupled inductor configuration in a three-level interleaved dc–dc converter. The new common-leg coupled inductor structure is introduced, and possible modulation methods are studied and theoretically analyzed, focusing on the impact on current ripples, power losses, and common-mode noise. The concept is validated using an MV-rated, SiC-based bidirectional converter dedicated to battery storage application in a bipolar EV charging station, tested up to 1 kV and 10 kW. Furthermore, the comparative study shows that the suggested method exhibits a smaller volume when compared to the conventional approach with several single inductors, comparable performance but with a more straightforward inductor design than the tapped inductor solution, and full section current controllability, unlike the single-inductor option. Finally, using the proposed technique, common-mode noise can be entirely limited, allowing the minimization of excess filtering. Overall, the proposed inductor configuration can be effectively and competitively used in modern SiC-based three-level dc–dc converters.**

***Index Terms*—Coupled inductor (CI), dc–dc multilevel converter, dc–dc power conversion, power electronics, SiC power MOSFETs.**

## I. Introduction

In THE midst of the transformation of the electric grid into carbon-confined grounds, the inclusion of renewable systems, EV charging applications, and battery storage systems, all enabled by well-performing power electronics is a necessity [1], [2], [3]. Furthermore, recent advances in the field of power semiconductor devices, mainly due to the introduction and development of wide bandgap components, i.e., Silicon Carbide have led to a notable improvement in efficiency, power density, and more [4], [5], [6]. Besides, as these power devices established based on SiC are characterized by higher sustainable voltages, reaching medium voltage (MV) level has become less cumbersome, and thus, many formerly low-voltage applications have their voltage range extended, as is the case with some photovoltaic and energy storage applications, e.g., rated at 1.5 kV instead of 800 or 400 V [7].

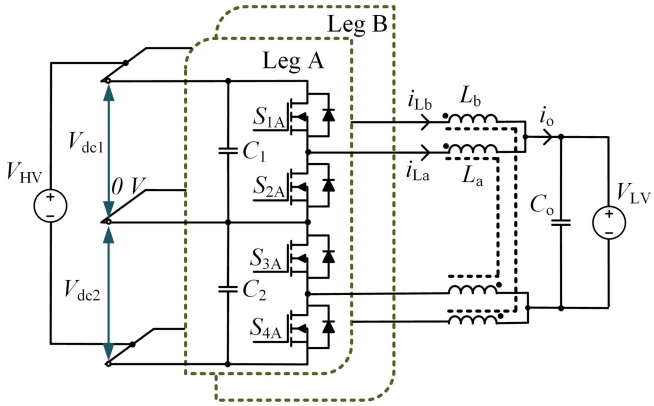



Fig. 1. Proposed bidirectional three-level buck-boost converter with common-leg CI.

Considering an application of a dc–dc converter operating at 1.5 kV, which could be employed as a battery energy storage interface in an EV charging station [8], [9], common and well-developed 1.2 kV SiC MOSFETs cannot be directly applied in a two-level topology. Thus, other solutions, such as multilevel converters, have to be taken into account [10]. Here, a three-level dc–dc, depicted in Fig. 1 is considered as it provides a simpler structure, bipolar connection capability, low transistor voltage stress, and high possible power density [8], [11], [12], [13], as well as the possibility to operate in soft-switching mode [14], [15], and is a more appropriate choice compared to conventional multilevel converters, e.g., a flying capacitor converter [16].

Moreover, interleaving is a well-known technique to reach high-power values as the current is split into several sections [17], [18], [19], [20] Simultaneously, by proper phase-shift operation of the converter legs, the effective output current frequency can be enlarged, leading to severely limited current ripples, which is crucial for battery-oriented applications.

In addition, for the three-level converter, there have been several modulation techniques proposed [21], which can further

Manuscript received 20 October 2023; revised 1 February 2024 and 27 March 2024; accepted 20 April 2024. Date of publication 2 May 2024; date of current version 20 June 2024. This work was supported by the funding from the EEA/Norway Grants 2014–2021. Recommended for publication by Associate Editor J.B. He. *(Corresponding author: Rafał Kopacz.)*

Michał Harasimczuk is with the Faculty of Electrical Engineering, Bialystok University of Technology, 15-351 Bialystok, Poland (e-mail: m.harasimczuk@pb.edu.pl).

Rafał Kopacz, Rafał Miśkiewicz, and Jacek Rąbkowski are with the Institute of Control and Industrial Electronics, Warsaw University of Technology, 00-662 Warsaw, Poland (e-mail: rafal.kopacz@pw.edu.pl; rafal.miskiewicz@pw.edu.pl; jacek.rabkowski@pw.edu.pl).

Radosław Sobieski is with the Markel sp.z.o.o., 05-500 Piaseczno, Poland (e-mail: radek.sobieski@markel.pl).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2024.3396293.

Digital Object Identifier 10.1109/TPEL.2024.3396293

improve the current ripples, e.g., the N-type, and Z-type control methods [12], [22]. However, these are not universally superior as they may lead to increased individual inductor currents or expedited power losses [12], [22]. Furthermore, some modulation techniques introduce common-mode (CM) voltage, leading to enlarged EMI generation that may require more bulky filters or supplementary slow-down of the transistor switching speed, e.g., through the gate resistance. Thus, advanced coupled inductor (CI) structures have been introduced to diminish the negative effects of the sophisticated modulation strategies, as well as to provide a higher volumetric power density, as, for a case with a two-phase interleaved converter, four single inductors (SIs) can be replaced by two tapped inductors (TIs) [12], [23]. Unfortunately, such a configuration results in circulating currents that are the source of inflated power losses. Moreover, to obtain notable performance with the CIs, the magnetics design with appropriate coupling coefficient is required, which is a challenging task [24], [25], [26].

Thus, this article introduces an alternative common-leg CI configuration based on a positive coupling coefficient with a different modulation scheme. The proposed approach forgoes the three-level operation to obtain lower volume compared to the four-inductor approach, similar ripple performance but with a notably more straightforward magnetic design when stood against the TI solution, and full current control-ability in contrast to a SI option. Moreover, the proposed solution completely eliminates the CM voltage, allowing for a more compact design with a smaller EMI filter. Overall, the proposed alternate inductor configuration is a worthy consideration for dc–dc converters, as validated based on an MV SiC-based prototype.

A similar technique to that described in this article, involving the bifurcation of the inductor windings, leading to a reduction in CM noise, has been presented in [27], and [28]. However, in [27] and [28], this was described in the context of a three-level, four-quadrant voltage step-up/step-down converter and in a single-section configuration, which constitutes a significant difference compared to the system presented in this article. Furthermore, in the considered article, even though the CM voltage is reduced, it is still apparent unlike in the proposed configuration.

The rest of this article is organized as follows. After the concise introduction, the operation principles of the converter with the proposed inductor structure and modulation scheme are depicted. Next, the experimental study is described, starting with a brief overview of the prototype and the results validating the concept. Then, a thorough comparison with other state-of-the-art approaches, founded on a theoretical and experimental analysis, is given. Finally, the article is concluded in the last Section.

## II. Three-Level Dc–Dc Converter With Common-Leg CIs

### A. Basic Operation Principles

The schematic of the proposed converter is shown in Fig. 1. In such a circuit, there are two CIs with turns ratio $n = 1$, common for each leg of the interleaved structure—this is the main difference compared to the converters in [12] and [23], where four SI, or two TIs with a low coupling coefficient in a different configuration are employed.

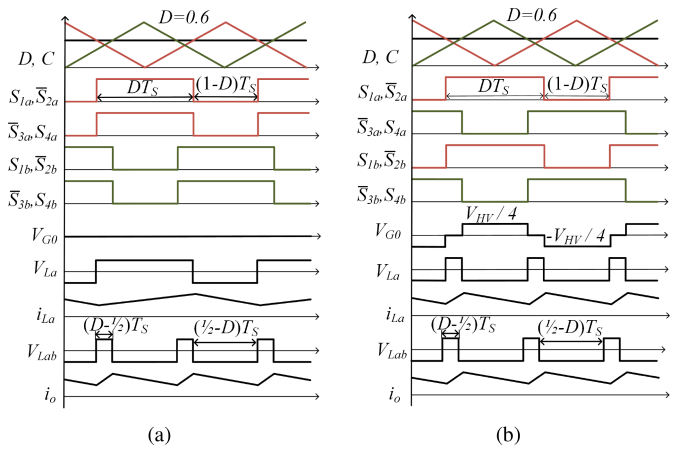



Fig. 2. Waveforms of the proposed bidirectional three-level buck boost converter with common-leg CI for different control methods: (a) two-level control (H) and (b) noninterleaving control (I). From the top: $D$ is the duty cycle, $C$ is the carrier function, $S_{xy}$ are the transistor control signals ($x = 1$, 2, 3, or 4 and $y = a$ or $b$), $V_{G0}$ is the CM voltage, $V_{La}$ and $i_{La}$ are the inductor voltage and current, $V_{Lab}$ is the equivalent inductor voltage, and $i_o$ is the output current.

Fig. 2 shows waveforms of the proposed converter under $D = 0.6$ in step-down mode for two different control methods: noninterleaving (I) and two-level (H). In both methods, the power transistors are controlled with pulse width modulation (PWM) with a constant duty ratio for each pair of transistors. Under the I-type modulation scheme, both legs are controlled in phase with each other. That results in the same phase current in each leg. Furthermore, using that control method, there is a possibility of adopting a control algorithm with capacitor $C_1$ and $C_2$ voltage balancing. In H-type control, the legs of the interleaved structure are controlled with a phase shift—current ripples in both legs have the same shape and are shifted by 180°. In the proposed inductor configuration, other control methods described in [12] and [23] cannot be used as in each operating cycle of the converter, the voltage clamped to each CI winding has to be equal for each pair ($V_{La1} = V_{La2}$, $V_{Lb1} = V_{Lb2}$), which determines the transistor states.

To simplify the converter analysis, the equivalent circuits presented in Fig. 3 were used. Furthermore, balanced voltages on capacitors $C_1, C_2$, and constant voltage on capacitors $C_1, C_2$, and $C_o$ were assumed. The power losses in all components of the converter, as well as parasitic inductances and capacitances, were omitted. Moreover, only the step-down mode is considered (when energy is transferred from source $V_{HV}$ to $V_{LV}$). For a case with the energy flowing in the opposite direction, the converter equations are akin and symmetrical, and thus not elaborated on further. Fig. 3(a) represents schematic from Fig. 1, in which instead of MOSFETs $S_{1a} - S_{4a}$ and $S_{1b} - S_{4b}$ ideal switches are used. In addition, instead of dc-link capacitors $C_1$-$C_2$, ideal voltage sources $V_{\mathrm{dc1}}$ and $V_{\mathrm{dc2.}}$ are employed. Furthermore, the model from Fig. 3(a) has been simplified and modified to the one presented in Fig. 3(b), in which ideal switches $S_{1a} - S_{4a}$ and $S_{1b} - S_{4b}$ and voltage sources $V_{\mathrm{dc1}}$ and $V_{\mathrm{dc2.}}$ have been replaced with voltage pulse sources $V_{a0}, V_{d0}, V_{b0}, V_{\mathrm{c0}}$. Those voltages pulse source can reach only two values, 0 or $V_{HV}/2$ and these depend on the state of transistor pairs: $S_{1a} - S_{2a}$, $S_{3a} - S_{4a}$, $S_{1b} - S_{2b}$, $S_{3b} - S_{4b}$, and represent the voltages between 0 and $a, b, c$, or

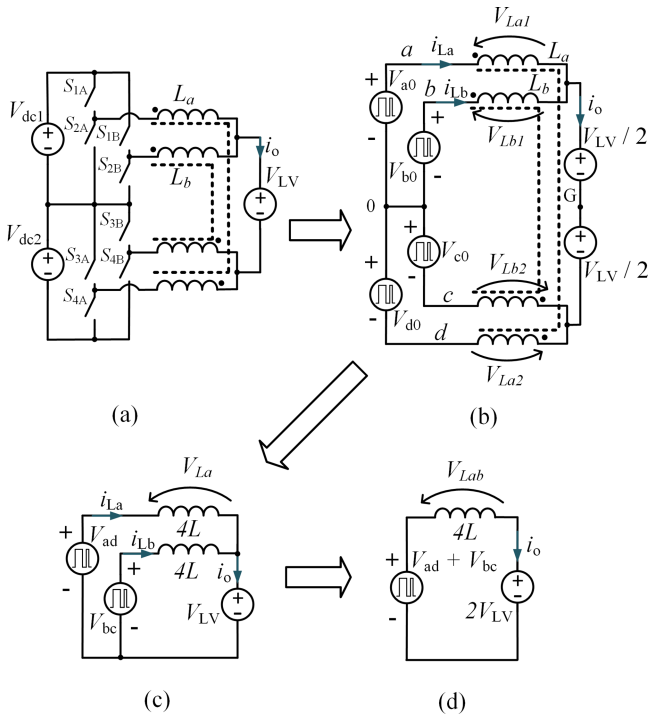



Fig. 3. Equivalent circuits of the proposed converter. (a) Basic model, (b) model with voltage pulse-sources instead of transistors, (c) model to calculate inductor current ripples, and (d) model to calculate output current ripple.

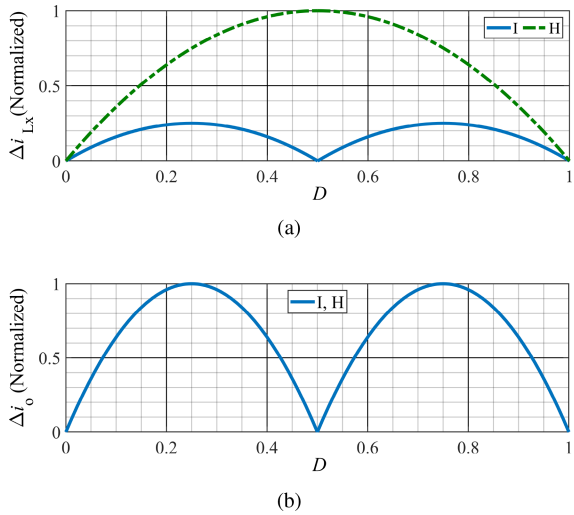



Fig. 4. Normalized currents ripples for both control methods in: (a) inductor and (b) output.

$d$ potentials. Further, assuming that the magnetizing inductances in the inductors are equal ($L_a = L_b$), their turn ratio equals one, and that the symmetrical switching of the converter transistors, according to Fig. 2, an equivalent circuit showed in Fig. 3(c) can be employed to calculate the voltage current ripple in each inductor, where $V_{ad} = V_{a0} + V_{d0}$ and $V_{bc} = V_{b0} + V_{c0}$. In that circuit, the two CIs are replaced with two SIs with an inductance four times higher than the magnetizing inductance of the CI. The proposed equivalent circuit is correct only if $V_{La1} = V_{La2}$ and $V_{Lb1} = V_{Lb2}$—which is the case when the circuit is operated with either I-type or H-type modulation scheme. To calculate the $i_o$ current ripples, the model in Fig. 3(c) was further simplified to Fig. 3(d), combining two pulse sources into one.

Analyzing the equivalent converter circuit depicted in Fig. 3 and waveforms shown in Fig. 2, the inductor current ripples can be described by (1) and (2) for the I-type control method. For the H-type technique, the inductor current ripple is given by (3). Please note that the formulated equations differ depending on $G_V$ only for the I-type approach

$$\left.\begin{array}{l}\Delta i_{Lx,I} = \frac{V_{La,I}}{4L}(D-1/2)T_S = \\ \frac{(1-G_V)(G_V-1/2)V_{HV}T_S}{4L}\end{array}\right\} \text{ for } G_V \geq 0.5 \quad (1)$$

$$\left.\begin{array}{l}\Delta i_{Lx,I} = \frac{V_{La,I}}{4L}DT_S \\ = \frac{G_V(1/2-G_V)V_{HV}T_S}{4L}\end{array}\right\} \text{ for } G_V \leq 0.5 \quad (2)$$

$$\Delta i_{Lx,H} = \frac{V_{La,H}}{4L}DT_S = \frac{G_V(1-G_V)V_{HV}T_S}{4L} \quad (3)$$

where: $G_V$ is the voltage gain ($G_V = D = V_{LV}/V_{HV}$), $L$ is the magnetizing inductance of the CIs ($L = L_a = L_b$), $T_S$ is the switching period, and $\Delta I_{Lx,Y}$ are the current ripples in all the inductors, where $Lx$ represents inductor $L_a$ or $L_b$ and $Y$ represents the control method.

The normalized inductor current ripples are showcased in Fig. 4(a). The ripples are significantly lower using the I-type control, especially for a case with a duty ratio of about $D = 0.5$. This difference is caused by the fact that in I-type modulation, voltages $V_{ad}$ and $V_{bc}$ can establish at three values – 0 and $V_{HV}/2$ for $G_V =< 0.5$, $V_{HV}/2$ and $V_{HV}$ when $G_V >= 0.5$. On the other hand, while the H-type scheme is used, voltages $V_{ad}$ and $V_{bc}$ are operated in a two-level fashion and reach either 0 or $V_{HV}$ in the whole voltage gain range. Thus, in I-type modulation, the voltage drop on the converter inductors is reduced, and so are its current ripples.

To calculate the output current ripple, the equivalent circuit depicted in Fig. 3(c) is used. The voltage drop on the equivalent inductance depends on the transistors' switching states, and voltages $V_{HV}$ and $V_{LV}$ is given by the following formula:

$$V_{Leq} = V_{ac} + V_{bd} + 2V_{LV}. \quad (4)$$

The output current ripples for both control methods are the same and can be expressed as follows:

$$\left.\begin{array}{l}\Delta i_{o,Y} = \frac{V_{Leq}}{4L}(D-1/2)T_S = \\ \frac{(1-G_V)(2G_V-1)V_{HV}T_S}{4L}\end{array}\right\} \text{ for } G_V \geq 0.5 \quad (5)$$

$$\left.\begin{array}{l}\Delta i_{o,Y} = \frac{V_{Leq}}{4L}DT_S = \\ \frac{G_V(1-2G_V)V_{HV}T_S}{4L}\end{array}\right\} \text{ for } G_V \leq 0.5 \quad (6)$$

where $\Delta i_{o,Y}$ are the output current ripples ($Y$ represents either I-type or H-type control methods).

The output current ripples for both control techniques are shown in Fig. 4(b). Minimal output current ripples occur for $D = 0.5$ ($D = 0$ and $D = 1$ are not appearing in real applications)—that means for $V_{HV}$ two times higher than $V_{LV}$—and is equal to zero. Voltage $V_{G0}$ representing the voltage between points 0 and G is a CM voltage that negatively affects the electromagnetic interference (EMI) noise. When the H-type control method is

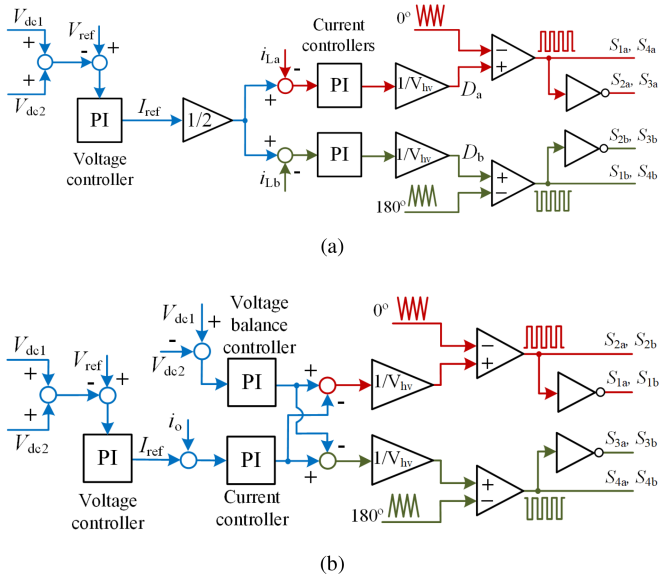



Fig. 5. Control diagram for (a) H-type modulation with separate current regulators for each section and (b) I-type modulation with voltage balancing capability. Exemplary waveforms showcasing the converter operated with this control strategy are depicted in Fig. 2.

employed, that voltage is equal to zero, which is a critical improvement compared to I-type control or other control methods with different inductor configurations [12]. Pulse voltage source $V_{G0}$ depends on the transistors' switching states, and for both analyzed modulation schemes can be described as follows:

$$V_{G0,H} = \frac{V_{a0} + V_{b0} - V_{c0} - V_{d0}}{4} = 0. \tag{7}$$

### B. Control Strategy

The employed control system is arranged in a conventional, cascaded voltage–current structure. The control loop with H-type modulation is composed of a voltage proportional–integral (PI) controller and two current PI controllers, each dedicated to a specific section of the converter, ensuring an equitable allocation of the current between the converter sections, and is shown in Fig. 5(a). The output of the voltage regulator serves as the input for the current controllers, which further determine the control duty cycles for the transistors, $D_a$ for switches in phase A, and $D_b$ for switches in phase B.

Furthermore, in I-type modulation, unlike in H-type modulation, there is a possibility of balancing the voltage between the capacitors $C_1$ and $C_2$ in the three-level structure. In case of issues with balancing this voltage, e.g., due to uneven load on the high-voltage side, an additional voltage regulator for capacitor voltage balancing can be used, as depicted in Fig. 5(b). However, this was not necessary in this work, as the voltage was balanced through a self-balance mechanism. Moreover, it is worth noting that in CI inductor configuration with I-type modulation, it is impossible to employ separate current regulators for each section. Nevertheless, considering the current self-balance mechanism, such a feature is not required.

The modulator is also structured conventionally, using PWM. The duty cycle given for each transistor pair according to the regulator is compared with a triangular carrier function at a specific phase shift depending on the modulation used: in I-type modulation the transistor pairs $S_{1a}, S_{2a}$ and $S_{1b}, S_{2b}$ are nonshifted while pairs $S_{3a}, S_{4a}$ and $S_{3b}, S_{4b}$ are shifted by 180°, whereas in H-type control the converter sections are shifted—pairs $S_{1a}, S_{2a}$ and $S_{3a}, S_{4a}$ are the reference for the phase, while pairs $S_{1b}, S_{2b}$ and $S_{3b}, S_{4b}$ are shifted by 180° (see Fig. 2).

TABLE I
CORE PARAMETERS OF THE EXPERIMENTAL PROTOTYPE OF THE THREE-LEVEL CONVERTER

| Parameter | Value |
|---|---|
| Tested high-side voltage | Up to 1 kV |
| Tested output power | Up to 10 kW |
| Switching frequency $f_S$ | 64 kHz |
| Output low-voltage side capacitance | 60 $\mu$F |
| Dc-link capacitors | $2 \times 2 \times 60\,\mu$F |
| Power transistors | $8 \times NTH4L040N120SC1$ |
| Magnetizing inductance | 185 $\mu$H |
| DSP | TMS320F28388D |

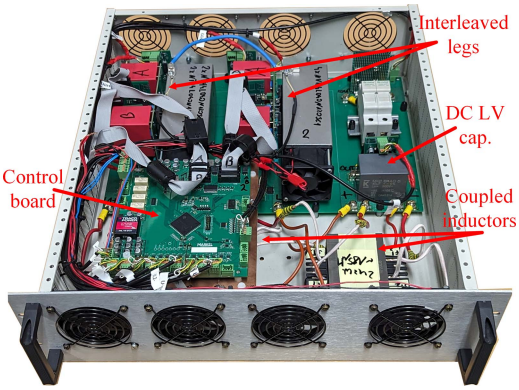



Fig. 6. Prototype of the three-level interleaved DC–DC converter with the common-leg CIs.

## III. EXPERIMENTAL STUDY

The proposed common-leg CI configuration is validated using an MV model of a nonisolated, bidirectional dc–dc converter designed to operate as a battery energy storage interface in an EV charging station [8]. The system employs two interleaved sections based on the state-of-the-art 1.2 kV SiC MOSFETs (NTH4L040N120SC1) controlled via a control board based on a DSP (TMS320F28388D) in a closed-loop system described in the previous section. The CIs are constructed using Litz wire (800 × 0.1 mm) and three MSS powder cores with distributed gap (EMS-0803820-040) pairs per inductor, and were wound with 2 × 21 turns for each CI exhibiting a magnetizing inductance of 185 $\mu$H. A more comprehensive description of the inductor design is shown further in Section IV-D, where a direct comparison with magnetics employed in other state-of-the-art converters is given. More detailed parameters of the prototype are shown in Table I, while the photograph of the prototype is depicted in Fig. 6. The interleaved legs are based on three-level modules described in Kopacz et al.'s [29] work. The whole converter is enclosed in a 3 U rack case. The tests were performed

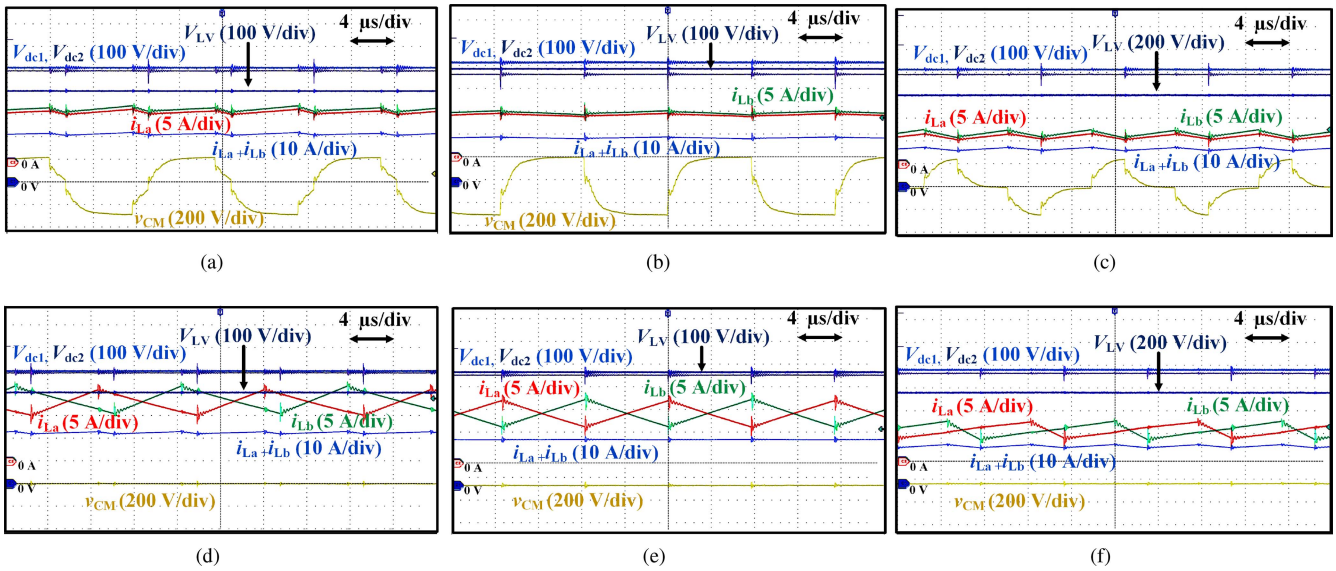



Fig. 7. Exemplary experimental results of the three-level DC–DC converter with proposed common-leg CI obtained at 10 kW of output power and 1000 V high-side voltage in step-down mode, where: $V_{\mathrm{dc1}}$ and $V_{\mathrm{dc2}}$ are the high-side DC-link voltages, $V_{\mathrm{LV}}$ is the low-side voltage, $i_{La}$ and $i_{Lb}$ are the positive-terminal inductor currents, and $v_{\mathrm{CM}}$ is the CM voltage. (a) $G_V = 0.4$, I modulation (CI). (b) $G_V = 0.5$, I modulation (CI). (c) $G_V = 0.8$, I modulation (CI). (d) $G_V = 0.4$, H modulation (CI). (e) $G_V = 0.5$, H modulation (CI). (f) $G_V = 0.8$, H modulation (CI).

at up to 1 kV and 10 kW of power for various voltage gains. For the setup, two EA PSB12000-40 units were employed as a power supply and an electronic load. The waveforms were acquired using Tektronix MSO46 oscilloscope supported by voltage probes (THDP0100 and THDP0200) and current probes TCP0030 A, while the efficiency was measured with Yokogawa WT5000 power analyzer. Exemplary results showcasing the operation of the proposed converter in both operating modes (I-type and H-type) and different voltage gains ($G_V = 0.4, 0.5,$ or 0.8) are depicted in Fig. 7. Waveforms illustrate the voltages across dc-link capacitors on high-voltage side ($V_{\mathrm{dc1}}$, $V_{\mathrm{dc2}}$), low-voltage side $V_{\mathrm{LV}}$, inductor currents $i_{La}$ and $i_{Lb}$ low-voltage side current $i_{La} + i_{Lb}$, and CM voltage $v_{\mathrm{CM}}$ (referred as $V_{G0}$ voltage in Fig. 3).

Under I-type control, the inductor and output currents are in phase, and their ripple frequency is two times higher than switching frequency $f_S$. When H-type modulation is employed, the inductor current ripple frequency is equal to the switching frequency $f_S$ and is shifted by 180°. That results in the output current frequency being two times higher than the switching frequency $f_S$. Furthermore, at voltage gain equal to 0.5, according with theoretical considerations described in Section II (see Fig. 4), the inductor and output current ripples in both control techniques are close to zero. Moreover, the important difference between the considered control techniques is the CM voltage $v_{\mathrm{CM}}$—in H-type control, that voltage is equal to zero, while for the I-type scheme, that voltage is floating between $V_H/4$ and $-V_H/4$. Fig. 8(a) and (b) shows a comparison of inductor and output current ripples for both considered control methods. The current ripples obtained in the experimental study are similar to the outcomes of the theoretical study. Thus, it is confirmed that the theoretical analysis of the converter current ripples described in Section II has been performed appropriately.

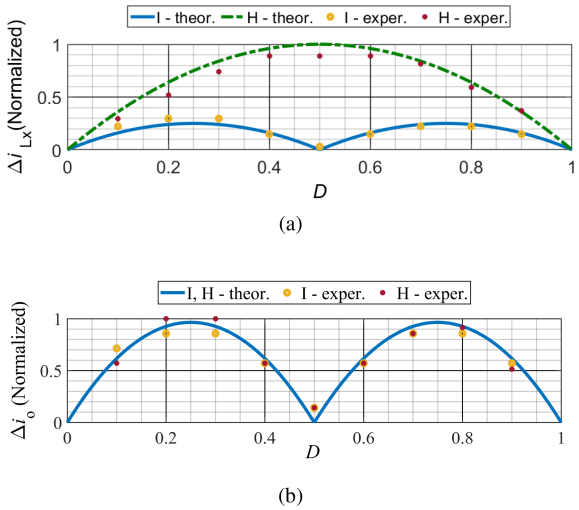



Fig. 8. Comparison of theoretical and experimental current ripples for H-type and I-type control methods in the proposed converter in: (a) inductor and (b) output.

## IV. Comparison and Discussion

In the literature, especially in [12], [23], and [30], there are described various configurations of inductors and control methods used in the three-level boost-buck converter. The possible structures of inductors are depicted in Fig. 9. The basic SI configuration shown in Fig. 9(a) consists of four SIs with equal inductances. To reduce the component count and increase power density, a structure with two TIs was proposed in [see Fig. 9(b)] [12]. The structure of a four-winding coupled inductor (4WI), as shown in 9(c), has been proposed in Qin and Lee's [30] work. This structure enables an even greater reduction in the dimensions of the inductor compared to the converter with TI.

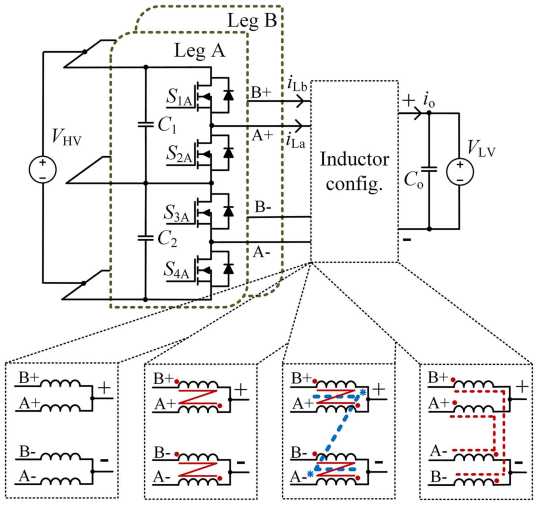



Fig. 9. Three-level bidirectional boost-buck converter with different inductor configurations: (a) four SIs (SI), (b) two tapped inductors (TI), (c) 4WI, and (d) proposed common leg CI.

Finally, Fig. 9(d) presents the configuration with CIs which is introduced in this article.

### A. Control Strategy

Fig. 10 shows five control methods that can be used in the considered converter with the different inductor configurations. The control methods are named according to the switching sequence of the power transistor control signals. Starting off, the I-type control, shown in Fig. 10(a) is the simplest, non-interleaving case, where each section is controlled in phase, with identical signals. Using this approach, the inductor current ripples are two times lower compared to the output current ripples. Another modulation scheme is depicted in Fig. 10(b)—the H-type technique. Employing this method, the voltage between points A+/B+ and A–/B– (see Fig. 9) can be either $V_{HV}$ or 0, and the system operates in a two-level fashion despite its three-level structure. This is the main difference between the other control techniques, in which the voltage can reach three values: $V_{HV}$, $V_{HV}/2$, and 0. Two-level control, employed in the H-type method, increases the inductor current ripples and hinders the use of the capacitor voltage balancing algorithm. Furthermore, X-type control technique is a basic interleaving method in which the phases are controlled with a 180° phase shift. Finally, in and N-type and Z-type modulation methods, the half-bridge structures of the converter are controlled with 0°, 90°, 180°, and 270° phase shift.

### B. Current Ripples

It should be emphasized that current ripples in the inductors and in the output are crucial, as these have a substantial impact on inductor core losses, switch rms currents, output filter capacitance, size of the cooling system—and, as a consequence—power density of the converter.

To exhibit the advantages and disadvantages of the proposed solution, inductor, and output current ripples comparison between the proposed solution and other methods described in the literature is presented. Fig. 11 shows the current ripple comparison for all considered configurations and control techniques. The comparison was made assuming the inductances in the SI structure were equal to the sum of the series connected inductors of the coupled structure in TI and CI configurations. For the TI connection, the ripples were calculated for a coupling coefficient $k = 0.8$. Furthermore, current ripples in the converter with a 4WI assume identical values and shapes as in the TI system, considering that the self-inductance of individual inductors in the considered configurations is the same. Moreover, the mutual inductance $M_x$ represents the positive coupling between the four windings of 4WI inductor is twice as large as the mutual inductances $M$ of the inductors in the TI configuration [12], [30]. When the proposed CI structure is used, the coupling coefficient has no practical impact on output and inductor current ripples.

At first, in Fig. 11(a), the output current ripple is considered. As can be seen, the best results are achieved for the SI configuration, most notably with N-type and Z-type modulations. However, the requirement of four individual inductors is not favorable in terms of compact converter design. On the other hand, TI exhibits only two CIs but with a cost of enlarged ripples, especially for I-type, X-type, and H-type control schemes. The proposed CI configuration establishes a middle ground between the two conventional solutions—despite using only two CIs, akin to the TI setup, the output current ripples are lower than the counter-option in most of the operating range (except for $G_V = 0.25$ and $G_V = 0.75$).

Moreover, the lowest current ripples in the inductors occur in the I-type control technique. In TI configuration, X-type and I-type modulations are characterized by the highest inductor current ripples. In the proposed solution, using the H-type control technique, the inductor current ripples are similar to TI employing Z-type and N-type control techniques. However, to achieve proper operation using the TI-Z and TI-N approaches, the CI should exhibit a low coupling coefficient; thus, designing the inductor is not a simple task. Furthermore, despite using a CI with low $k$, the inductor current ripple is still higher than in the SI structure. The impact of the coupling coefficient on the current ripples is shown in Fig. 11(c)—for $k = 0.98$, the inductor current ripples are even three times higher than for $k = 0.9$ and five times higher than for $k = 0.8$. As can be seen, without the appropriate, complex design of the TIs, the applicability of the TI approach is questionable.

### C. Experimental Study

To compare the proposed CI configuration with conventional SI approach, experiments with I-type, N-type, and Z-type modulation have been performed. Exemplary results obtained at 1000 V high-side voltage and with low-side voltage at 400 V transferring 10 kW for the conventional four SI configurations are depicted in Fig. 12.

Fig. 13 presents the measured efficiency of the laboratory model of the analyzed converter for two different inductor configurations: with four individual inductors [see Fig. 9(a)] and with the proposed configuration using two CIs [see Fig. 9(d)]. The tests were conducted for two different voltage gains ($G_V = 0.4$ and $G_V = 0.8$) and three control methods in the SI configuration, as well as two in the proposed CI configuration. For the CI configuration, the efficiency measurements

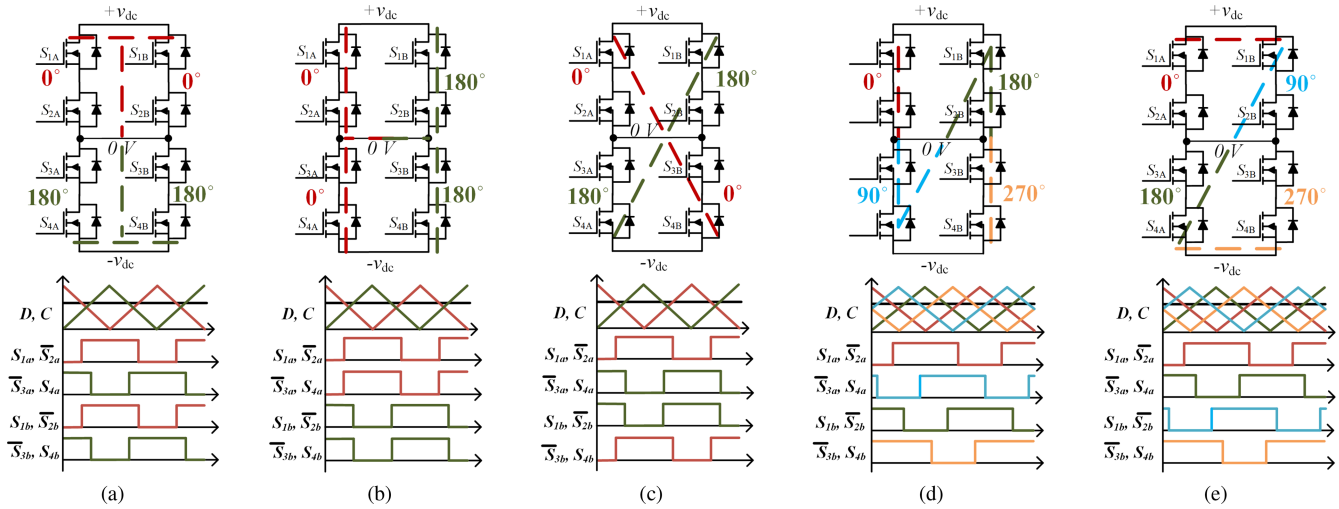



Fig. 10. Sequence of the modulations schemes for the different control methods applicable in a three-level DC–DC converter with exempary waveforms for the switching signals: (a) I-type, (b) H-type, (c) X-type, (d) N-type, and (e) Z-type.

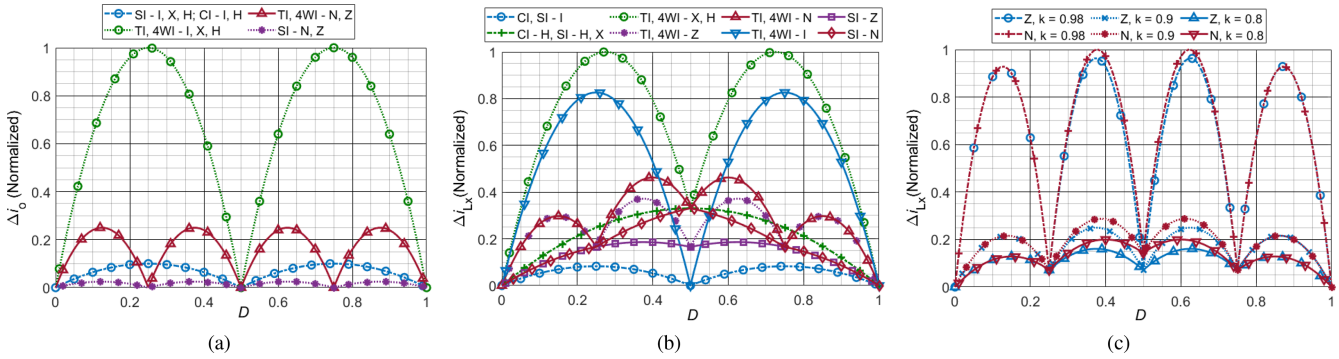



Fig. 11. Current ripples comparison for different inductor configurations and modulation strategies: (a) output current ripples, (b) inductor current ripples, and (c) inductor current ripples in TI configuration considering various coupling coefficients $k$.

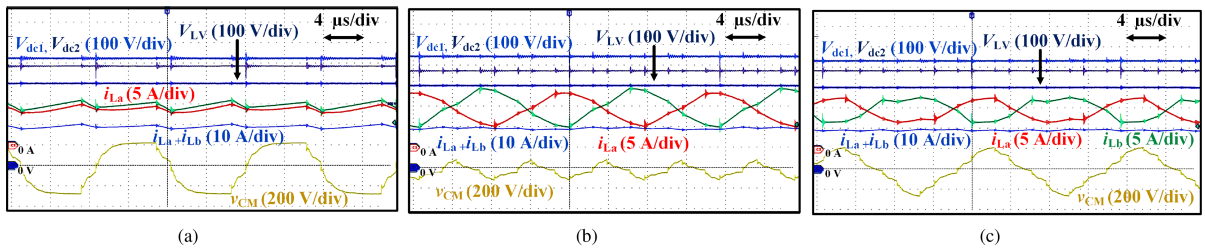



Fig. 12. Exemplary experimental results obtained for the three-level DC–DC converter with conventional SI configuration at 10 kW of output power and 1000 V high-side voltage in step-down mode, where: $V_{\mathrm{dc1}}$ and $V_{\mathrm{dc2}}$ are the high-side DC-link voltages, $V_{\mathrm{LV}}$ is the low-side voltage, $i_{La}$ and $i_{Lb}$ are the positive-terminal inductor currents, and $v_{\mathrm{CM}}$ is the CM voltage. (a) $G_V = 0.4$, I modulation (SI). (b) $G_V = 0.4$, N modulation (SI). (c) $G_V = 0.4$, Z modulation (SI).

were conducted using inductors described in Section III. In the SI configuration, four off-the-shelf inductors from Ferryster (DEMS-65X54/0,15/37) were used, made from four cores (EMS-0653327-040) and inductance of roughly 150 $\mu$H each. The total volume of the inductors in the CI configuration was 1330 cm$^3$, compared to 1576 cm$^3$ in the SI configuration. Please note that despite the lower volume, the inductors in CI option were characterized by higher inductance, leading to lower current ripples. As can be seen in Fig. 13, the efficiency increases with output power and voltage gain $G_V$ for both analyzed inductor configurations and all control methods. The efficiency reaches a maximum value of approximately 99.2% for the maximum output power and the proposed CI solution with H modulation. The efficiency for I modulation and for all investigated modulations in the SI configuration is comparable, being only about 0.1% lower for the maximum output power and $V_{\mathrm{LV}} = 800$ V. The lowest efficiency is obtained for the minimum measured output power, around 2 kW, and $V_{\mathrm{LV}} = 400$ V, but it is

TABLE II
COMPARISON BETWEEN THE INDUCTOR STRUCTURE AND MODULATION SCHEME CONFIGURATIONS SHOWCASING CRUCIAL PARAMETERS OF THE THREE-LEVEL DC–DC CONVERTER

| Inductor setup and control strategy | No. of inductors | Inductors current ripples | Output current ripple | Inductor design complexity | CM noise | Voltage balancing capability | Ref. |
|---|---|---|---|---|---|---|---|
| SI-I | 4 | v.low | low | simple | high | yes | [12, 23] |
| SI-X | 4 | medium | low | simple | none | yes | [23] |
| SI-N | 4 | low | v. low | simple | low | yes | [12] |
| SI-Z | 4 | low | v. low | simple | medium | yes | [12] |
| TI-I | 2 | high | high | complex | high | yes | [12, 23] |
| TI-X | 2 | medium | high | complex | none | yes | [23] |
| TI-N | 2 | medium | medium | complex | low | yes | [12] |
| TI-Z | 2 | medium | medium | complex | medium | yes | [12] |
| 4WI-I | 1 | high | high | v. complex | high | yes | [30] |
| 4WI-X | 1 | medium | high | v. complex | none | yes | [30] |
| 4WI-N | 1 | medium | medium | v. complex | low | yes | [30] |
| 4WI-Z | 1 | medium | medium | v. complex | medium | yes | [30] |
| CI-I | 2 | v.low | low | simple | high | yes | proposed |
| CI-H | 2 | medium | low | simple | none | no | proposed |

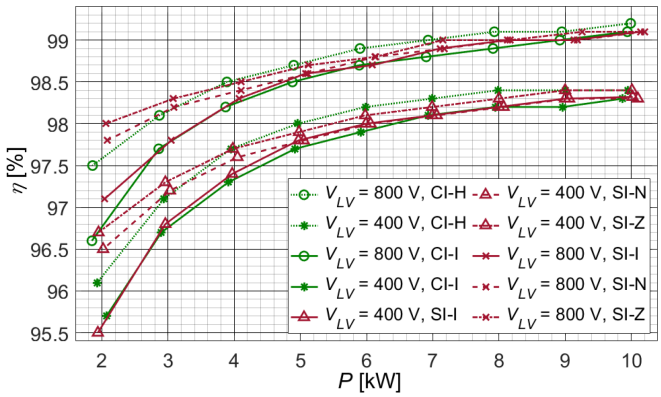



Fig. 13. Efficiency of the three-level DC–DC converter with the proposed common-leg CI compared with conventional SI system.

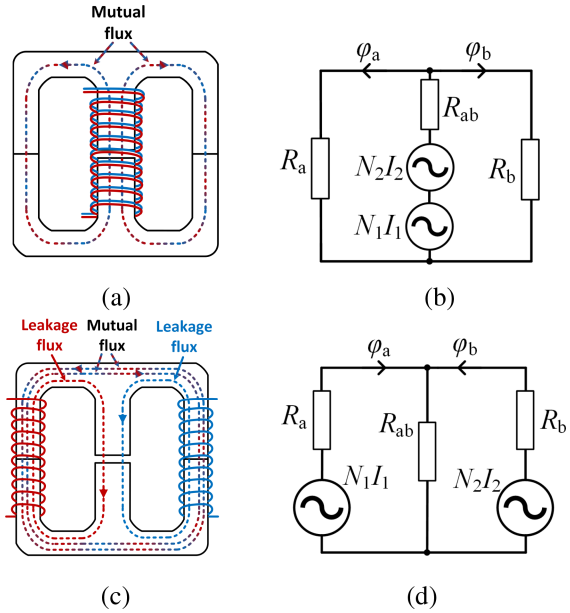



Fig. 14. Proposed (a) coupled and (c) tapped [12], [23] inductors and its models (b) and (d), respectively.

still higher than 95.5%. Overall, the efficiency remains at a high level for the two analyzed inductor configurations, indicating that the use of two CIs instead of four individual inductors (SI) has a positive but modest impact on efficiency.

### D. Inductor Design

An interesting solution described in the papers [30] is the use of a single 4WI instead of two two-winding CIs or four individual ones, as shown in the Table II. This inductor, in its operation and current distribution across its windings, resembles converters with a TI described in [12] and [23], allowing a significant increase in the power density of the inductive components and, consequently, the power density of the entire converter. However, this configuration requires the construction of a complex inductive element and modulation control I, N, or Z. Controlling the system with a four-winding inductor in H modulation results in significant current ripples in its windings, which increase its rms currents and it makes practical implementation of this solution difficult. As a consequence, this system, like other interleaved three-level buck-boost converters described in the scientific literature so far, is characterized by substantial CM voltage values, which is a significant drawback compared to the proposed converter. Furthermore, in addition to the potential for increased power density by replacing two TI inductors with a single four-winding inductor, the utilization of this configuration does not differ significantly from the TI configuration. This is because the current waveforms and control methods are the same in both configurations.

As mentioned earlier, in the proposed solution, the inductor can be conventionally designed, meaning both windings of the CI can be placed on the same part of core, as shown in Fig. 14(a). This design ensures that the generation of a small leakage flux, and inductor of this type are characterized by a high coupling coefficient. This is a key difference compared to systems [12], [23] where the magnetic coupling coefficient should be low to counteract high current ripple [see Fig. 11(c)] leading to circulating currents [23] in inductor windings and thus induce additional losses in the converter components. A TI with a

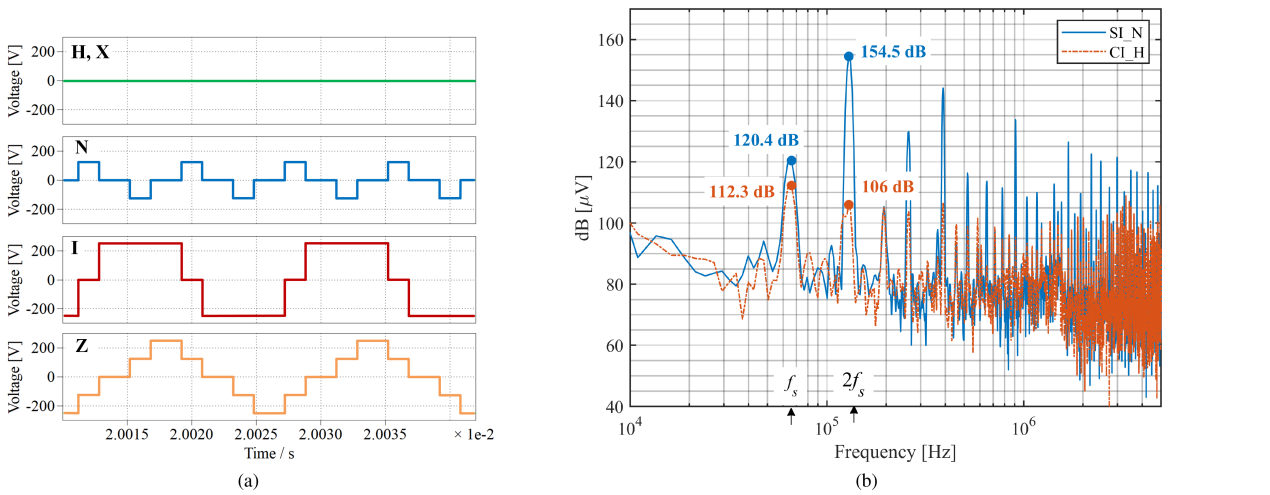



Fig. 15. CM noise comparison for different inductor structures and control methods $V_{HV} = 1$ kV and a duty ratio $D = 0.4$: (a) on the basis of Plecs simulations and (b) on the basis of experimental results (depicted for the two most prominent methods to limit the CM voltage in CI and SI configurations).

low coupling coefficient can be implemented by placing both windings of the inductor on different part of core [see Fig. 14(c)]. The low coupling coefficient is achieved by directing the major portion of the magnetic flux through the central leg of the core, as illustrated in Fig. 14(c). The magnetic models of both analyzed chokes are depicted in Fig. 14(b) and (d). Based on these models, mutual and leakage inductances of the considered inductors can be determined. These inductances have been calculated and described in [23] and [31]. Assuming that the outer legs of the TI [see Fig. 14(a) and (b)] do not have an air gap (as powder core is employed), in contrast to the inner leg, it can be assumed that $R_a << R_{ab}$. In addition, assuming $N = N_1 = N_2$, the leaked and mutual inductances of the TI can be expressed by

$$L_{Lk(\mathrm{TI})} = \frac{N^2}{2R_{ab} + R_a} \tag{8}$$

$$M_{(\mathrm{TI})} = \frac{N^2 R_{ab}}{2R_{ab}R_a + R_a^2}. \tag{9}$$

Similarly, based on Fig. 14(b), the mutual inductance of the CI from Fig. 14(a) can be determined. Assuming that the entire magnetic flux will be concentrated in the inductor core, this inductance can be calculated according to the equation

$$M_{(\mathrm{CI})} = \frac{(2N)^2}{\left(R_{ab} + \frac{R_a R_b}{R_a + R_b}\right)} \approx \frac{(2N)^2}{R_{ab}}. \tag{10}$$

In accordance with (8)–(10) and Fig. 14, the execution processes of the TI and CI inductors must differ. In the CI system, the magnetic coupling coefficient does not affect the nature of currents in the inductor windings, and their fluxes sum up in each operating cycle. In the TI system, a low magnetic coupling coefficient and its impact on current ripples require a careful approach to inductor design which makes it much more difficult.

### E. CM Voltage Noise

In addition to the inductors and output current ripples, CM voltage noise is also crucial. Fig. 15(a) illustrates the voltages between points G and 0 for various control strategies. $V_{GO}$ is directly associated with CM noise. This voltage does not depend on the CI configuration; it is determined solely by the modulation method. The waveforms were obtained using PLECS simulation software, assuming $V_{HV} = 1$ kV and a duty ratio $D = 0.4$. According to the provided waveforms, in the proposed inductor configuration with H modulation, the CM voltage is theoretically reduced to zero. In practice, there is a small voltage due to voltage spikes on parasitic inductances during transistor switching (see Fig. 7). Fig. 15(b) compares the CM voltage spectrum obtained from the experimental studies. This spectrum was determined using an oscilloscope based on the waveforms shown in Figs. 7(d) and 12(b). The lowest CM voltage among the considered control methods is a characteristic of N modulation, which can be utilized in SI and TI inductor configurations. Therefore, the comparison was conducted between the proposed CI inductor configuration with H modulation and the SI inductor configuration with N modulation. As assumed, the CM voltage level for the proposed solution is significantly lower, for example, at a switching frequency ($f_s = 64$ kHz), and doubled switching frequency, the CM voltage level in H modulation is lower by 8.1 and 47.5 dB, respectively. In the proposed method, utilizing the H-type control strategy, CM noise is almost completely eliminated. Consequently, the CM filter can be omitted, or at least substantially reduced, providing a substantial positive impact on the power density of the converter.

### F. Discussion

To summarize the advantages and disadvantages of the proposed CI structure compared to SI and TI, a Table II is given. The main advantages of the novel CI structure are lower output current ripples and CM noise using H-type control compared to the TI inductor structure operating employing any of the control strategies. Moreover, considering the impact of the coupling coefficient, the CI design is also more straightforward. Furthermore, when standing against the SI option, the proposed solution allows for lower number of magnetic components. Thus, even though the ripples are higher, the proposed approach is still worthy of consideration. On the other hand, a main disadvantage

of the proposed solution is the impossibility of using voltage balancing of high-voltage side capacitors $C_1$ and $C_1$ under H modulation. However, the self-balancing mechanism is still present [32], and additional control is not needed in most applications, as it is the case of the considered system where another converter controls the voltage [9]. It should be noted that the proposed converter is designed to collaborate with other converters connected to a common three-level dc voltage bus, such as a three-level ac–dc converter. In such a scenario, the inverter may be responsible for implementing the voltage balancing algorithm and stabilizing the dc-link. Thus, voltage balancing capability of the dc–dc converter is not required. Furthermore, balancing can easily be introduced with I-type modulation. Thus, the proposed converter could be effectively employed in various dc–dc applications and stands competitively among its peers.

## V. Conclusion

An alternative common-leg CI for the three-level dc–dc converters is proposed in this article. The new structure can be effectively employed as a worthy counterpart to other state-of-the-art approaches, as shown in Table II summarizing the outcomes of the comparison. As can be seen, the proposed alternate common-leg CI configuration with H-type control shows favorable characteristics, as it allows for a lower number of components than the SI option, decent individual current ripples and low output current ripples, while maintaining a simple magnetic design compared to other CI-based options, and vastly reduced CM noise. Thus, the proposed solution of the common-leg CI applied in a three-level dc–dc converter based on SiC power devices is a noteworthy option for dc–dc power conversion in the MV range, especially for applications concerning battery energy storage, photovoltaics, and EV charging stations.

## References


[1] S. Chang, J. Cho, J. Heo, J. Kang, and T. Kobashi, "Energy infrastructure transitions with PV and EV combined systems using techno-economic analyses for decarbonization in cities," *Appl. Energy*, vol. 319, Aug. 2022, Art. no. 119254. [Online]. Available: https://linkinghub.elsevier.com/retrieve/pii/S0306261922006122

[2] G. Wang et al., "A review of power electronics for grid connection of utility-scale battery energy storage systems," *IEEE Trans. Sustain. Energy*, vol. 7, no. 4, pp. 1778–1790, Oct. 2016. [Online]. Available: https://ieeexplore.ieee.org/document/7506096/

[3] A. Hussain, V.-H. Bui, J.-W. Baek, and H.-M. Kim, "Stationary energy storage system for fast EV charging stations: Simultaneous sizing of battery and converter," *Energies*, vol. 12, no. 23, Nov. 2019, Art. no. 4516. [Online]. Available: https://www.mdpi.com/1996-1073/12/23/4516

[4] X. She, A. Q. Huang, O. Lucia, and B. Ozpineci, "Review of silicon carbide power devices and their applications," *IEEE Trans. Ind. Electron.*, vol. 64, no. 10, pp. 8193–8205, Oct. 2017. [Online]. Available: https://ieeexplore.ieee.org/document/7815312/

[5] G. Iannaccone, C. Sbrana, I. Morelli, and S. Strangio, "Power electronics based on wide-bandgap semiconductors: Opportunities and challenges," *IEEE Access*, vol. 9, pp. 139446–139456, 2021. [Online]. Available: https://ieeexplore.ieee.org/document/9565934/

[6] J. Biela, M. Schweizer, S. Waffler, and J. W. Kolar, "SiC versus Si–Evaluation of potentials for performance improvement of inverter and DC–DC converter systems by SiC power semiconductors," *IEEE Trans. Ind. Electron.*, vol. 58, no. 7, pp. 2872–2882, Jul. 2011. [Online]. Available: https://ieeexplore.ieee.org/document/5560803/

[7] C. Jung, "Power up with 800-V systems: The benefits of upgrading voltage power for battery-electric passenger vehicles," *IEEE Electrific. Mag.*, vol. 5, no. 1, pp. 53–58, Mar. 2017. [Online]. Available: https://ieeexplore.ieee.org/document/7873375/

[8] R. Kopacz, M. Harasimczuk, J. Rabkowski, and R. Sobieski, "Three-level interleaved non-isolated DC/DC converter as a battery interface in an EV charging system with bipolar DC-Link," *PRZEGLĄD ELEKTROTECHNICZNY*, vol. 1, no. 5, pp. 204–208, May 2023. [Online]. Available: https://sigma-not.pl/publikacja-143224-2023-5.html

[9] J. Rąbkowski et al., "Advanced charging system with bipolar DC-link and energy storage," in *Proc. Prog. Appl. Elect. Eng.*, 2022, pp. 1–6. [Online]. Available: https://ieeexplore.ieee.org/document/9966572/

[10] T. Meynard and H. Foch, "Multi-level conversion: High voltage choppers and voltage-source inverters," in *Proc. PESC '92 Record. 23 rd Annu. IEEE Power Electron. Specialists Conf.*, 1992, pp. 397–403. [Online]. Available: https://ieeexplore.ieee.org/document/254717/

[11] M. Zhang, Y. Jiang, F. Lee, and M. Jovanovic, "Single-phase three-level boost power factor correction converter," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 1995, pp. 434–439. [Online]. Available: https://ieeexplore.ieee.org/document/468984/

[12] S. Lu, M. Mu, Y. Jiao, F. C. Lee, and Z. Zhao, "Coupled inductors in interleaved multiphase three-level DC–DC converter for high-power applications," *IEEE Trans. Power Electron.*, vol. 31, no. 1, pp. 120–134, Jan. 2016. [Online]. Available: https://ieeexplore.ieee.org/document/7027864/

[13] S. Kim, H. Cha, and H.-G. Kim, "High-Efficiency voltage balancer having DC–DC converter function for EV charging station," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 1, pp. 812–821, Feb. 2021. [Online]. Available: https://ieeexplore.ieee.org/document/8945328/

[14] M. Mohamadi and S. K. Mazumder, "Confluence of integrated magnetics and TCM for a ZVS based higher order differential-mode rectifier," *IEEE Trans. Power Electron.*, vol. 38, no. 7, pp. 8624–8642, Jul. 2023. [Online]. Available: https://ieeexplore.ieee.org/document/10093933/

[15] Z. Yao and S. Lu, "Voltage self-balance mechanism based on zero-voltage switching for three-level DC–DC converter," *IEEE Trans. Power Electron.*, vol. 35, no. 10, pp. 10078–10087, Oct. 2020. [Online]. Available: https://ieeexplore.ieee.org/document/9020048/

[16] C. Chen, Z. Chen, H. S. Rizi, and A. Q. Huang, "Comparative study of 100 kW three-level bidirectional DC-DC converters for battery storage integration with 1500 V PV inverter," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2023, pp. 3061–3068. [Online]. Available: https://ieeexplore.ieee.org/document/10131202/

[17] K. Bi, Y. Lu, Y. Zhuang, Y. Zhu, and Q. Fan, "Decoupling power balancing strategy with reduced current sensors for two-phase interleaved neutral point clamped DC/DC converter applied in energy storage system," *IEEE Trans. Energy Convers.*, vol. 38, no. 1, pp. 147–157, Mar. 2023. [Online]. Available: https://ieeexplore.ieee.org/document/9829319/

[18] R. Zhou, Y. Xuan, F. Liu, M. H. Patmal, and P. Yang, "Research on control strategies of interleaved three-level bidirectional buck/boost converter for energy storage system," in *Proc. IEEE 6th Int. Elect. Energy Conf.*, 2023, pp. 3519–3524.

[19] P.-E. Velazquez-Elizondo, I. Araujo-Vargas, I. Cervantes, K. Cano-Pulido, and M.-A. Hernandez-Nochebuena, "A 32 kW power-dense six-phase dual-interleaved DC–DC buck-boost converter with three interphase transformer," *IEEE Access*, vol. 10, pp. 130880–130893, 2022. [Online]. Available: https://ieeexplore.ieee.org/document/9987487/

[20] N. Nupur and S. Nath, "Minimizing ripples of inductor currents in coupled SIDO boost converter by shift of gate pulses," *IEEE Trans. Power Electron.*, vol. 35, no. 2, pp. 1217–1226, Feb. 2020. [Online]. Available: https://ieeexplore.ieee.org/document/8767986/

[21] H.-I. Kim, S.-H. Kim, S.-W. Baek, H.-W. Kim, K.-Y. Cho, and G.-D. Kim, "Comparison of interleaving methods of parallel connected three-level bidirectional converters," *Energies*, vol. 15, no. 1, (6), Dec. 2021, pp. 1–19. [Online]. Available: https://www.mdpi.com/1996-1073/15/1/6

[22] R. Kopacz, M. Harasimczuk, J. Rąbkowski, and R. Sobieski, "Experimental evaluation of inductor configurations and modulation techniques in an interleaved three-level DC/DC SiC-based converter," in *Proc. IEEE 17th Int. Conf. Compatibility, Power Electron. Power Eng.*, 2023, pp. 1–6. [Online]. Available: https://ieeexplore.ieee.org/document/10227393/

[23] L. Tan, N. Zhu, and B. Wu, "An integrated inductor for eliminating circulating current of parallel three-level DC–DC converter-based EV fast charger," *IEEE Trans. Ind. Electron.*, vol. 63, no. 3, pp. 1362–1371, Mar. 2016. [Online]. Available: https://ieeexplore.ieee.org/document/7314924/

[24] Y.-C. Liu, C. Chen, Y.-C. Chung, M.-C. Tsai, and K. A. Katherine, "Integrated magnetics design for an interleaved three-phase buck converter," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2020, pp. 4533–4538. [Online]. Available: https://ieeexplore.ieee.org/document/9235677/

[25] T. Kang, A. Gandomkar, J. Lee, and Y. Suh, "Design of optimized coupling factor for minimum inductor current ripple in DC-DC converter using multiwinding coupled inductor," *IEEE Trans. Ind. Appl.*, vol. 57, no. 4, pp. 3978–3989, Jul./Aug. 2021. [Online]. Available: https://ieeexplore.ieee.org/document/9428523/

[26] Y. Yang, T. Guan, S. Zhang, W. Jiang, and W. Huang, "More symmetric four-phase inverse coupled inductor for low current ripples & high-efficiency interleaved bidirectional buck/boost converter," *IEEE Trans. Power Electron.*, vol. 33, no. 3, pp. 1952–1966, Mar. 2018. [Online]. Available: https://ieeexplore.ieee.org/document/8023781/

[27] Y. Cao et al., "Common-mode noise reduction and capacitor voltage autobalance using bridged midpoints and coupled inductor in a 3-L buck-boost converter," *IEEE Trans. Power Electron.*, vol. 38, no. 10, pp. 12365–12369, Oct. 2023.

[28] Y. Cao et al., "A three-level buck–boost converter with planar coupled inductor and common-mode noise suppression," *IEEE Trans. Power Electron.*, vol. 38, no. 9, pp. 10483–10500, Sep. 2023.

[29] R. Kopacz, M. Harasimczuk, B. Lasek, R. Miśkiewicz, and J. Rąbkowski, "All-SiC ANPC submodule for an advanced 1.5 kV EV charging system under various modulation methods," *Energies*, vol. 14, no. 17, 2021, Art. no. 5580.

[30] R. Qin and F. C. Lee, "Modeling and design for integrated coupled inductors in interleaved three-level dc/dc converters," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2017, pp. 498–503.

[31] P.-L. Wong, P. Xu, P. Yang, and F. C. Lee, "Performance improvements of interleaving VRMs with coupling inductors," *IEEE Trans. Power Electron.*, vol. 16, no. 4, pp. 499–507, Jul. 2001.

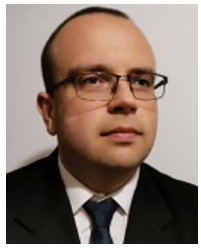
[32] F. Z. Peng, "A generalized multilevel inverter topology with self voltage balancing," *IEEE Trans. Ind. Appl.*, vol. 37, no. 2, pp. 611–618, Mar./Apr. 2001.

**Michał Harasimczuk** (Member, IEEE) was born in Białystok, Poland. He received the M.Sc. and Ph.D. degrees in electrical engineering from the Bialystok University of Technology, Bialystok, Poland, in 2013 and 2019, respectively.

He is currently with the Faculty of Electrical Engineering, Bialystok University of Technology. From 2020 to 2023, he was with the Warsaw University of Technology, Warsaw, Poland. His research interests include power electronics, namely, dc/dc soft-switching converters, multilevel converters, SiC-based converters, and ac/dc converters.

**Rafał Kopacz** (Member, IEEE) received the B.Sc., M.Sc., and Ph.D. degrees in electrical engineering from the Warsaw University of Technology, Warsaw, Poland, in 2018, 2019, and 2024, respectively.

He is currently an Assistant Professor with the Institute of Control and Industrial Electronics, Warsaw University of Technology. He was a Visiting Researcher with SINTEF Energy and Norwegian University of Science and Technology, Trondheim, Norway, in 2019, where he was working on reliability issues of SiC power devices, as well as Power Electronics Systems Laboratory, Swiss Federal Institute of Technology Zurich, Zurich, Switzerland, in 2023, where he was investigating novel concepts for solid-state transformers. His research interests include SiC-based power electronics, energy conversion in medium voltage range, especially using series connection and multilevel topologies, as well as power converters for EV fast charging stations, traction applications, and renewable energy sources.



**Rafał Miśkiewicz** (Member, IEEE) was born in Warsaw, Poland. He received the M.Sc. degree in electrical engineering from the Warsaw University of Technology, Warsaw, Poland, in 2008, and the Ph.D. degree in electrical engineering from the Institute of Electrical Engineering, Warsaw, Poland, in 2017.

He is currently an Employee of the Institute of Control and Industrial Electronics, Warsaw University of Technology. He was with the Institute of Electrical Engineering, now the Łukasiewicz Research Network—Institute of Electrical Engineering. His research interests include inductive wireless power transfer systems, isolated and nonisolated dc/dc converters based on resonant circuits.

**Radosław Sobieski** received the M.Sc. and Ph.D. degrees from the Warsaw University of Technology, Poland, in 2010 and 2023, respectively, both in electrical engineering.

He is currently a Director of R&D in the Markel Sp. z o. o., Piaseczno, Poland. His research interests include SiC-based power converters in MV range, dc/dc and ac/dc converters for BESS and renewable energy sources. Moreover, he also works in area of conversion for EV fast charging and power supply for electric traction.

**Jacek Rąbkowski** (Senior Member, IEEE) received the M.Sc. and Ph.D. degrees from the Warsaw University of Technology, Warsaw, Poland, in 2000 and 2005, respectively, both in electrical engineering.

In 2004, he joined the Institute of Control and Industrial Electronics, Warsaw University of Technology, where he is currently a Professor in power electronics. From 2010 to 2013, he was with the Laboratory of Electrical Energy Conversion, KTH Royal Institute of Technology, Stockholm, Sweden. From 2015 to 2016, he was with the Power Electronics Group, Tallin University of Technology, Tallin, Estonia. He has coauthored more than 190 scientific papers and two books. His research interests include power converters based on wide bandgap devices: topologies, design aspects, pulsewidth modulation techniques, and, especially, gate, and base drivers. Moreover, he also works in area of medium-voltage power conversion and, recently, on power converters for EV charging.

Dr. Rąbkowski is a Member of the European Power Electronics and Drives Association, involved with the International Scientific Committee. He was the Chairman of the Joint Industrial Electronics Society/Power Electronics Society Chapter in the frame of the IEEE Poland Section. Since 2015, he has been an Associate Editor for IEEE TRANSACTIONS ON POWER ELECTRONICS.