A High-Efficient Single-Switch, Soft-Switching High Step-Up DC–DC Converter With a Simple Structure and Continuous Input Current for Renewable Energy Integration

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***Abstract*—This article presents a novel single-switch soft-switching high step-up dc–dc boost converter. By utilizing a coupled inductor and series capacitors in the output stage, the converter achieves soft switching performance for the power switch during turn-ON and turn-OFF, along with a high step-up voltage gain. The design of the coupled inductors enables the simultaneous achievement of soft switching and high voltage gain without the need for additional auxiliary circuits, ensuring circuit simplicity and high efficiency. Furthermore, the converter maintains continuous input current, similar to a boost converter, improving battery lifespan and renewable input power source operation. The proposed converter addresses diode reverse recovery issues and incorporates a common ground between input and output stages, simplifying the feedback circuit. Comparative analysis with similar high-efficiency high step-up boost converters is performed, and a 200-W laboratory prototype is implemented.**

***Index Terms*—Coupled-inductors, dc–dc power converters, high-efficiency boost converter, high voltage gain, soft switching.**

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I. Introduction

In RECENT decades, an ongoing demand for high step-up dc–dc converters, which are applicable in a plethora of applications, has increased.

For applications with a considerable discrepancy between the input and output voltage stage, high step-up converters can play a critical role in boosting up the low input voltage level required by the ac inverter. Renewable energy-based systems, consisting of solar panels and fuel cells, are some examples of such applications [1] and [2]. As shown in Fig. 1, the main sections for a grid-connected solar system are dc–dc converters, solar inverters, and a storage system. In this application, the inverter should inject a sinusoidal current into the grid, and the dc link should be adjusted in a specific voltage range. Therefore, there is no need to have a precise voltage regulation.

DC–DC converters are divided into two categories based on isolation: isolated and nonisolated converters. In the isolated converters, the whole power is transferred through a magnetic field, whereas in the nonisolated converters, the whole or a part of power is transmitted electrically. One of the monumental advantages of nonisolated converters over isolated ones is higher efficiency and lower volume. Therefore, when galvanic isolation is not required, nonisolated dc–dc converters are preferred over isolated ones [3]. A traditional boost converter is a fundamental step-up topology among nonisolated converters, which is utilized to boost the voltage. The classical boost converter suffers from low voltage gain, violent diode reverse recovery problems, high voltage stress across the main switch, and hard switching performance. To address the serious hurdles, diverse topologies have been proposed in the literature [4]. In [5] and [6], to increase voltage gain, coupled inductor and switched capacitor techniques have been introduced. However, for the converter in [6], all semiconductors operate under a hard switching manner and leakage inductance of the coupled inductors causes a spike across the main switch which results in extra electromagnetic interference. These obstacles can be overcome by using clamp and snubber circuits [7]. In [8], a converter is suggested, in which by employing a multiplier cell and a voltage doubler, ultra-high voltage gain is obtained. Nonetheless, hard switching

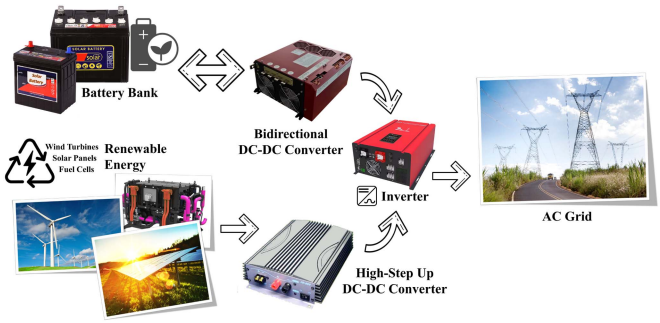

Fig. 1. Block diagram of a grid-connected renewable energy system.

performance and utilizing manifold semiconductor devices are considerable disadvantages of this method, resulting in high loss and low efficiency. The combination of these techniques has recently obtained a lot of broad interest due to the capability of increasing high voltage gain by a modest duty cycle. However, complexity is the conspicuous drawback of this method yielding additional cost [9].

The substantial fluctuations in input current pose a significant challenge to the accurate tracking of the maximum power point in PV panels, potentially reducing the lifespan of the input capacitor. Conversely, low input current ripple can improve the reliability and dynamic response of the system. Thus, maintaining a continuous input current is a highly desirable feature for solar applications [10], [11], [12], [13], [14], [15].

In studies [11], [12], [13], high step-up converters are examined, leveraging high voltage gain and continuous input current. However, it is noteworthy that the efficiency of these converters is impacted by switching losses. Among these converters, the structure of the one presented in [13] is comparatively simpler. The circuit topology presented in [12] and [14] are quadratic converters that take advantage of continuous input current, high voltage gain, and low voltage stress across the switch. Despite having these advantages, these converters operate in a hard switching manner and efficiency in these converters is relatively low.

In conjunction with high voltage gain and continuous input current, taking advantage of soft switching performance is another outstanding feature, which simultaneously has been craving for dc–dc converters. To provide greater clarity on the matter, it is important to note that losses and efficiency are closely linked; especially, to achieve high efficiency, it is necessary to minimize both switching and conduction losses. By doing so, the amount of wasted energy is reduced, resulting in a more efficient system. The most important approach to reduce switching loss is to use soft switching techniques, such as passive lossless snubber [16], [17], [18], [19], active clamp [20], [21], [22], [23], [24], [25], [26], and zero voltage transition (ZVT) techniques [27], [28], [29], [30], [31]. Active clamp and ZVT techniques employ an additional switch to provide soft switching. Conversely, the passive lossless snubber technique eliminates the need for an extra switch but typically necessitates a larger number of passive components, such as diodes, capacitors, and inductors. The active clamp and ZVT techniques provide zero voltage switching conditions at the expense of an extra active switch, whereas in the passive lossless snubber technique, the main switch turns ON under ZCS condition and E_{oss} losses might limit the switching frequency of the converter in [16] and [18].

In [23] and [24], high step-up boost converters are proposed, in which, by using an active clamp technique, a soft switching condition is obtained. Also, in this converter, by utilizing coupled inductor technique and voltage multiplier cells, high voltage gain is achieved. However, this converter suffers from some disadvantages including losing soft switching performance at the light load, discontinuous input current, and having floating switch which makes control circuit complex. The circuit topology presented in [27] is a soft switched high step-up boost converter. In this converter, to achieve soft switching manner on the whole range of output power, a ZVT based auxiliary circuit is used. In addition, not only, by employing several multiplier cells and coupled inductor technique, ultra-high voltage gain is obtained but also continuous input current is another excellent merit of this topology resulting in declining size of input filter. On the negative side, obtaining several advantages simultaneously develops at the expense of circuit complexity.

In the converter presented in [28], a quasi-Z-source high step up is introduced in which soft switching performance, continuous input current, and high voltage gain are achieved. However, due to lack of auxiliary diode in ZVT cells, current stress of auxiliary switch is high and also because of conduction loss of input diode, loss is high and efficiency is low.

In [29], a proper high step-up converter based on impedance source is introduced. Simplicity is one of the main merits of this converter so only a single magnetic core and just two diodes and switches are used. Furthermore, continuous input current, high voltage gain, soft switching conditions in a wide range of output power, and common ground are other advantages of this converter. Despite excellent advantages, to obtain soft switching performance, an extra switch is needed resulting in higher cost and low power density. Also, at light loads, the freewheeling loss of this converter is high yielding to low efficiency. Compared to other converters, the one proposed in [26] stands out with its high efficiency achieved by utilizing a low number of diodes in both the main and auxiliary circuits and having a simple structure. However, like the converter in [29], this converter also requires extra switches. In [30] and [31], soft-switching converters are introduced which enables solid transitions between constant current mode and constant voltage mode without the need for frequency switching and relays so that this feature contributes to improving system stability. Nevertheless, complexity is the main disadvantage of this topology.

In this article, we introduce a high step-up converter with soft switching using a single switch and a minimal number of components. By employing only one power switch, the circuit achieves a low cost and reduced complexity. To enhance the limited voltage gain of the conventional boost converter while maintaining continuous input current ripple, we integrate coupled inductors in series with the output stage. These coupled inductors are designed to facilitate zero voltage switching (ZVS) at turn-ON for the power switch and ZVS turn-OFF with the assistance of the snubber capacitor. Moreover, the combination

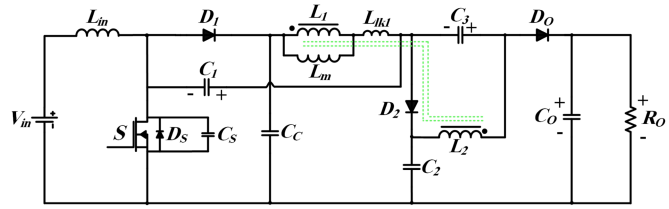

Fig. 2. Proposed soft-switched, single-switched high step-up converter.

of coupled inductors and multiplier cell techniques significantly increases the voltage gain while decreasing the voltage stress across the power switch. The leakage inductance of the coupled inductors is utilized to mitigate the reverse recovery problem of the output diode. The continuous input current ensures minimal input current ripple, resulting in improved performance of the renewable power source and eliminating the need for a bulky input filter capacitor to compensate for the large current ripple. Another notable advantage of the proposed converter is the shared ground between the input and output stages, which simplifies the feedback circuit.

The rest of this article is as follows. Section II presents the proposed circuit, including its structure and operating principles. Section III covers the steady-state analysis and provides design guidelines. In Section IV, we present the experimental results and compare the performance of the proposed converter with other counterparts. Finally, Section V concludes this article.

II. Operating Principle

The schematic and theoretical key waveforms of the proposed single switch soft switching high step-up converter can be seen in Figs. 2 and 3, respectively. The proposed converter is basically a boost converter in which coupled inductors with turn ratio $n = n_2/n_1$ and multiplier capacitors are utilized to extend the voltage gain. The voltage multiplier cell includes three switched capacitors C_1, C_2, and C_3 as well as a feed-forward diode D_2. A diode and a capacitor are added to absorb the leakage energy of the coupled inductors and to clamp the voltage across the power switch. This leakage energy is then transferred to the output and helps increase the voltage gain. S is the power switch, and L_{in} is the boost inductor. As can be seen in Fig. 4, the coupled inductors are modeled by an ideal transformer with primary and secondary windings L_1 and L_2, a magnetizing inductance L_m, and equivalent leakage inductance L_{lk}. C_C is the clamp capacitor and the output capacitor of the input boost converter is applied to provide voltage–second balance for the secondary coupled inductor, D_1 also acts as the output diode of the boost converter. D_O and C_O are the output diode and output capacitor of the converter, respectively. At a steady state, there are six operating modes during a switching period. To simplify the analysis, it is assumed that all components are ideal, and the voltage drop across semiconducting elements can be neglected. Also, capacitors are large enough so that their voltages are constant during a switching period. Fig. 4 illustrates the equivalent schematic of the proposed converter working in different operating intervals.

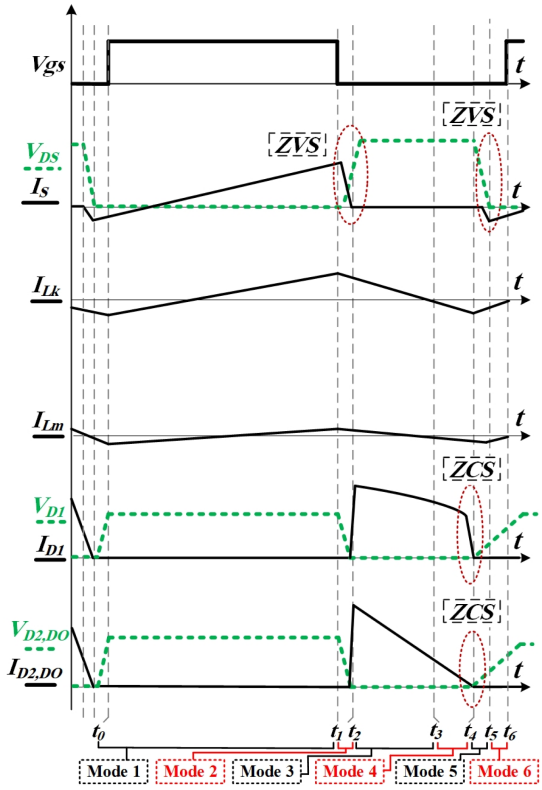

Fig. 3. Key waveforms of the proposed converter.

Mode 1 [t_0–t_1] [see Fig. 4(a)]: In this mode, S is ON, diodes D_1, D_2, and D_O are reverse biased and L_{in} is charged by the input voltage source. Also, the magnetizing inductance L_m and L_{k1} are charged, respectively, by $(V_{C1} + V_{C3} - V_{C2}) \times \frac{n_1}{n_2}$ and $(2V_{C1} + V_{C3} - V_{C2} - Vcc)$ voltage. The output load is fed by the output capacitor C_o.

$$i_{L\text{in}}(t) = i_{L\text{in}}(t_0) + \frac{V_{\text{in}}}{L_{\text{in}}}(t - t_0) \tag{1}$$

$$i_{Lm}(t) = i_{Lm}(t_0) + \frac{V_{C1} + V_{C3} - V_{C2}}{L_m}(t - t_0) \tag{2}$$

$$i_{L\text{lk}}(t) = \frac{2V_{C1} + V_{C3} - V_{C2} - V_{CC}}{L_{\text{lk}}}(t - t_0). \tag{3}$$

Mode 2 [t_1–t_2] [see Fig. 4(b)]: At the commencing of this mode, the switch turns OFF and the snubber capacitor starts to charge. The summation of L_{in} and L_{K1} currents pass through C_S and increase V_{CS} linearly. This mode ends when V_{CS} reaches the voltage of the clamp capacitor.

$$V_{CS}(t) = \frac{I_{L\text{in}} + I_{L\text{lk}1}}{C_S}(t - t_1) \tag{4}$$

$$\Delta t_2 = t_2 - t_1 = \frac{V_{CC}}{I_{L\text{in}} + I_{L\text{lk}1}} C_S. \tag{5}$$

Mode 3 [t_2–t_3] [see Fig. 4(c)]: When V_{CS} is equal to V_{CC} at t_2, D_1, D_2, and D_O conduct. The capacitor voltage V_{C3} is applied across the inductor L_2 and I_{Lm} is decreasing with $\frac{V_{C3}}{nL_m}$ slop. Also, $(V_{C1} + \frac{V_{C3}}{n})$ is applied across the leakage inductance $L_{\text{lk}1}$ so that $I_{\text{lk}1}$ is also reducing. In this interval,

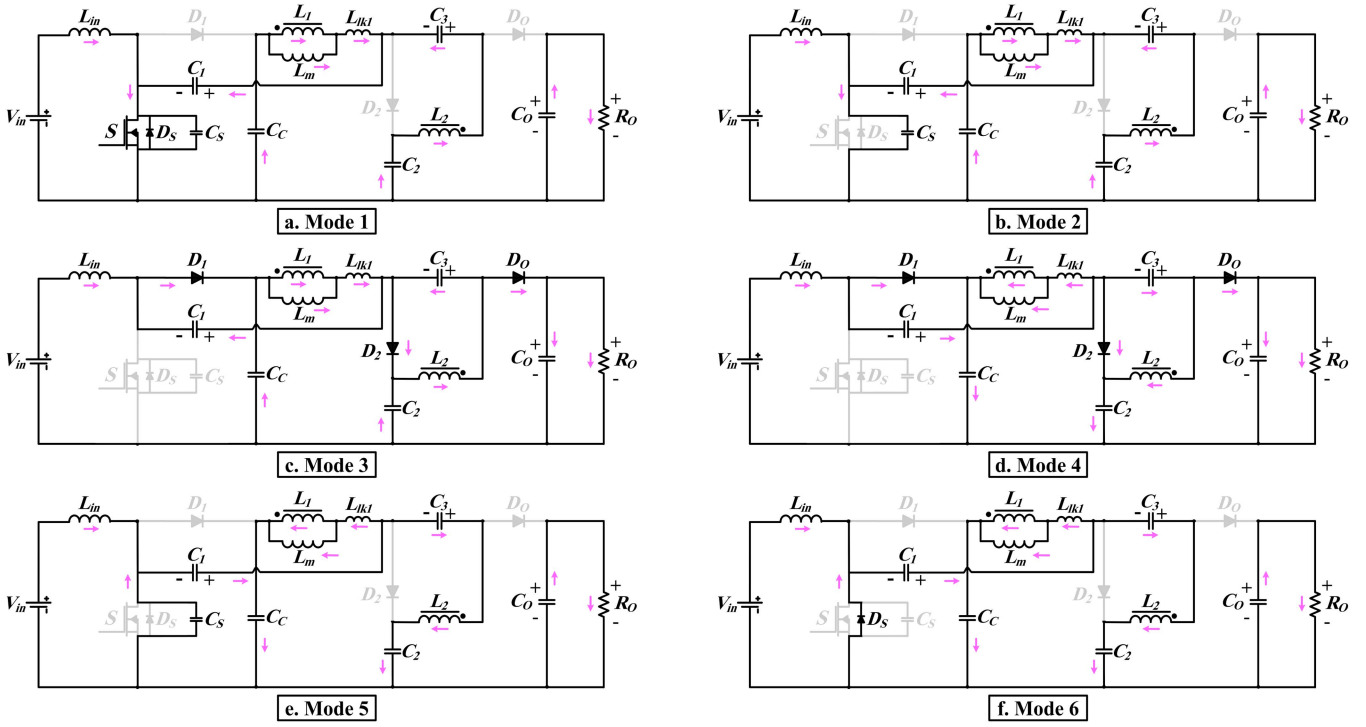

Fig. 4. Equivalent circuits of converter operating modes.

the input inductor current equals $I_{DO} - I_{C2} - I_{CC}$, where the input inductor current is constant and the output diode current increases so that the currents of capacitors decrease. This mode ends when I_{lk1} reaches zero (C_C and C_2 currents reach zero).

$$i_{\text{Llk1}}(t) = i_{\text{Llk1}}(t_2) - \frac{\frac{V_{C3}}{n} + V_{C1}}{L_{\text{lk1}}}(t - t_2) \tag{6}$$

$$i_{\text{Llk1}}(t_2) = i_{\text{Llk-max}} \tag{7}$$

$$i_{Do}(t) = i_{Do\_\text{peak}} - \frac{\frac{V_{C3}}{n} + V_{C1}}{L_{\text{lk1}}}(t - t_2) \tag{8}$$

$$i_{\text{Do\_peak}} = \frac{2I_o}{1-D} = \frac{P_o}{DV_o} \tag{9}$$

$$\Delta t_3 = t_3 - t_2 = \frac{i_{\text{Llk-max}}}{\frac{V_{C3}}{n} + V_{C1}} L_{\text{lk1}}. \tag{10}$$

Mode 4 [t_3–t_4] [see Fig. 4(d)]: During this period, I_{C1}, I_{C2}, and I_{CC} have positive direction and charge the capacitors. Also, I_{L2}, I_{Llk1}, and I_{Lm} reach zero and then increase in a negative direction. In this interval, the input inductor current equals $I_{DO} + I_{C2} + I_{CC}$. As the input inductor current is constant and the output diode current is declining, the currents of capacitors are increasing. This mode ends when I_{DO} reach and diodes D_o, D_1, and D_2 turn OFF under ZCS conditions.

$$i_{\text{Llk1}}(t) = -\frac{\frac{V_{C3}}{n} + V_{C1}}{L_{\text{lk1}}}(t - t_3). \tag{11}$$

Since the equation for D_o in this mode is the same as in the previous mode, the sum of the duration of modes 3 and 4 is achieved by

$$\Delta t_{42} = t_4 - t_2 = \frac{i_{Do_{\text{peak}}}}{\frac{V_{C3}}{n} + V_{C1}} L_{\text{lk1}} \tag{12}$$

where

$$i_{Do-\text{peak}} = \frac{2I_O}{1 - D_{\text{eff}}}. \tag{13}$$

Mode 5 [t_4–t_5] [see Fig. 4(e)]: As diode D_1 turns OFF at the start of this mode and I_{L1} along with I_{L2} are increasing, the snubber capacitor starts to discharge until its voltage reaches zero and then is reversed. So, the antiparallel diode of the power switch conducts.

$$V_{CS}(t) = V_{CC} - \frac{I_{L_{\text{in}}} + \frac{(n+1)}{n} I_{\text{lk1}} - \frac{I_{Lm}}{n}}{C_S}(t - t_4) \tag{14}$$

$$\Delta t_5 = t_5 - t_4 = \frac{V_{CC}}{I_{L_{\text{in}}} + \frac{(n+1)}{n} I_{\text{lk1}} - \frac{I_{Lm}}{n}} C_S. \tag{15}$$

Mode 6 [t_5–t_6] [see Fig. 4(f)]: When the capacitor voltage is negated at the start of this period, the antiparallel diode of the power switch conducts, and the current is transferred from the capacitor to the antiparallel diode. In this mode, because of $V_{C1} - V_{CC}$ voltage applied across inductor L_1, I_{L1}, and I_{L2} currents are declining. In this mode, before I_{L1} reaches half of the input inductor current and the antiparallel diode turns OFF, the power switch can be turned ON under ZVS conditions.

$$i_{Lm}(t) = i_{Lm}(t_5) + \frac{V_{C1} + V_{C3} - V_{C2}}{L_m}(t - t_5) \tag{16}$$

$$i_{\text{Llk}}(t) = i_{\text{Llk}}(t_5) - \frac{V_{CC} - V_{Lm} - V_{C1}}{L_{\text{lk1}}}(t - t_5) \tag{17}$$

$$t_{65} = \frac{\left(i_{\text{Lk}}\left(t_5\right) - \frac{i_{Lin}}{2}\right) L_{k1}}{V_{cc} - V_{Lm} - V_{C1}} \tag{18}$$

$$D_{\text{eff}} = D - t_{65}. \tag{19}$$

According to (19), the duration of this mode can affect the effective duty cycle (D_{eff}) and the voltage gain of the converter, which is discussed in the next section.

III. Analysis and Design of the Proposed Converter

In this section, the proposed converter is analyzed in a steady-state condition, and the equations for the voltage gain by considering the impact of the leakage inductance (L_{k1}) and voltage stress across elements, along with the design procedure of the passive elements, are provided. Moreover, a comparison is provided between the proposed converter and its counterparts.

A. Voltage Gain of the Proposed Converter

To determine the voltage gain of the proposed converter, it is necessary to measure the voltage across capacitors C_C, C_1, C_2, and C_3. By applying voltage-second balance to L_{in}, V_{Cc} is achieved. When the switch S is conducting, V_{in} voltage is applied across L_{in}, and when S is turned OFF, $V_{\text{in}} - V_{cc}$ is applied across L_{in}. Therefore, C_C voltage can be obtained as follows:

$$V_{CC} = \frac{V_{\text{in}}}{1 - D}. \tag{20}$$

To measure the voltage across capacitors C_1, C_2, and C_3, we must establish the volt–second balance relations of the L_m inductor, which involves calculating its voltage when the switch is both ON and OFF.

During the first mode when switch S is ON, accounting for the leakage inductance, the voltage across L_m can be expressed as follows:

$$V_{\text{lm\_}S(\text{on})} = V_{CC} - V_{C1} - L_{\text{lk1}} \frac{n_2}{n_1} \frac{2I_O}{D^2T}. \tag{21}$$

By substituting V_{CC} from (20) in (21), V_{lm} is as follows:

$$V_{\text{lm\_}S(\text{on})} = \frac{V_{\text{in}}}{1 - D} - V_{C1} - L_{lk1} \frac{n_2}{n_1} \frac{2I_O}{D^2T}. \tag{22}$$

On the other hand, the voltage across the magnetizing inductance during the third mode in which the power switch is OFF is equal to

$$V_{\text{lm\_}S(\text{off})} = \frac{V_{C3}}{n}. \tag{23}$$

Using (22) and (23), the volt–second balance of L_m inductor is

$$\left(\frac{V_{c3}}{n}\right)(1 - D) + \left(\frac{V_{\text{in}}}{1 - D} - V_{C1} - L_{\text{lk1}} \frac{n_2}{n_1} \frac{2I_O}{D^2T}\right) D = 0. \tag{24}$$

Finally, V_{C3} is given by

$$V_{C3} = \frac{nD}{1 - D} \left[V_{C1} + L_{\text{lk1}} \frac{n_2}{n_1} \frac{2I_O}{D^2T} - \frac{V_{\text{in}}}{1 - D}\right]. \tag{25}$$

Also, we can calculate the volt–second balance relation of L_{lk1} inductor

$$(n + D) V_{C1} - DV_{C2} - nD \frac{V_{\text{in}}}{1 - D} + V_{C3} = 0. \tag{26}$$

From mode (3) V_{C2} is equal to

$$V_{C2} = V_{C1} + \frac{V_{\text{in}}}{1 - D}. \tag{27}$$

Substituting V_{C3} and V_{C2} from (25) and (27) in (26), the voltage of C_1 capacitor is achieved as follows:

$$V_{C1} = DV_{\text{in}} \left(\frac{n + 1}{n}\right) + \frac{D}{1 - D} V_{\text{in}} - \frac{2nL_{\text{lk1}} I_O}{DT}. \tag{28}$$

By substituting V_{C1} from (28) in (25) and (27), V_{C3} and V_{C2} are calculated as

$$V_{C2} = V_{\text{in}} \left[\frac{1 + D}{1 - D} + D\left(\frac{n + 1}{n}\right) + \frac{D}{1 - D}\right] - \frac{2nL_{\text{lk1}} I_O}{DT} \tag{29}$$

$$\begin{aligned} V_{C3} = {} & \left(\frac{nD}{1 - D}\right) \\ & \times \left[\left[DV_{\text{in}} \left(\frac{n + 1}{n}\right) + \frac{DV_{\text{in}}}{1 - D} - \left(\frac{2nL_{\text{lk1}} I_O}{DT}\right)\right] \right. \\ & \left. + \left(\frac{2nL_{\text{lk1}} I_O}{D^2T}\right) - \left(\frac{V_{\text{in}}}{1 - D}\right)\right] \end{aligned} \tag{30}$$

$$\begin{aligned} V_O = {} & \frac{V_{\text{in}}}{1 - D} \left[D + \left(\frac{nD^2}{1 - D}\right)\right] \\ & + DV_{\text{in}} \left(\frac{n + 1}{n}\right) \left[1 + \left(\frac{nD}{1 - D}\right)\right] \\ & - L_{\text{lk1}} \left[\frac{2nI_O}{DT} \left(1 + \left(\frac{nD}{1 - D}\right)\right) + \left(\frac{2nI_O}{D^2T}\right)\right]. \end{aligned} \tag{31}$$

According to mode (3), $V_O = V_{C2} + V_{C3}$ and using (29) and (30), the output voltage of the converter considering leakage inductance is obtained as below. In addition, the voltage gain comparison of the proposed converter versus other converters is shown in Fig. 5. The last term in (31) represents the impact of leakage inductance on the voltage gain ratio of the converter.

To analyze this effect, we employed MATLAB software and (31) to plot the relationship between duty cycle and output current for two different values of turn ratio "n" ($n = 1$ and 2), as shown in Fig. 6. The parameters specified in Table I were utilized for generating Fig. 7. According to this figure, the duty cycle of the switch experiences minimal changes for light loads ($I_o = 50$ mA, equivalent to 10% of the nominal load). This indicates that the converter operates with duty cycles above 0.5 across a wide range of loads, and the duty cycles remain almost constant throughout the entire range of the output power. Note that this analysis does not consider the variations in losses of the semiconductors under different load conditions because these variations typically have a minimal impact on the converter's gain and duty cycle changes. To explain more details on the

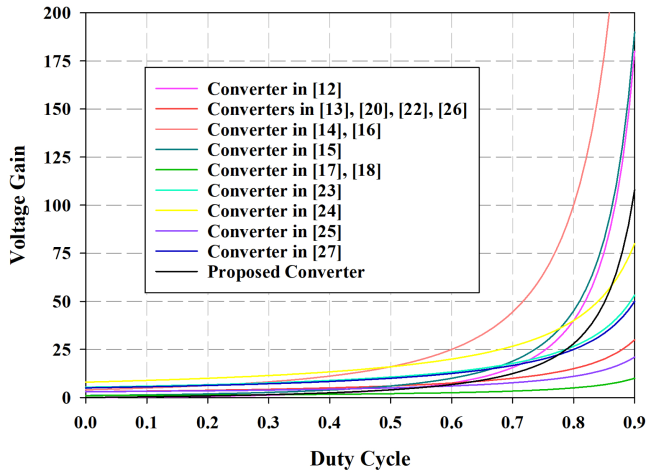

Fig. 5. Comparison of voltage gain: proposed converter versus other converters in [12], [13], [14], [15], [16], [17], [18], [20], [22], [23], [24], [25], [26], and [27] ($n = 1$ and coupling factor (k) $= 1$).

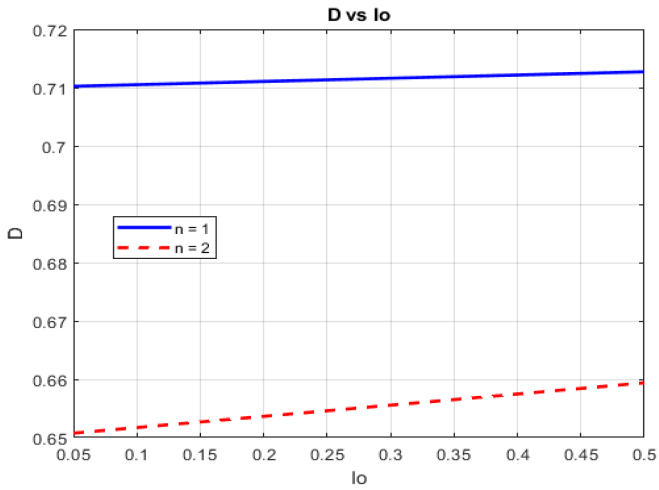

Fig. 6. Duty cycle versus output current for different turn ratios (n). Equation (28) is used to plot this graph, analyzing the effect of leakage inductance (L_{lk1}) when the output load changes.

TABLE I
IMPORTANT PARAMETERS OF THE IMPLEMENTED PROTOTYPE

Parameter/ Component	Value	Component	Value
Input voltage (V_{in})	30 V	C_1	4.7 µF/160 V
Output voltage (V_O)	400 V	C_2	4.7 µF/250 V
Output power (P_O)	200 W	C_3	4.7 µF/250 V
Frequency (f_{sw})	100 kHz	C_O	22 µF/450 V
Experimental Efficiency	%97.5	S	IRF150P221
C_C	4.7 µF/160 V	D_2, D_O	MUR1520
C_S	4.7 nF/200 V	D_1	BYV32-200
$L_{m1} = L_{m2}$	500 µH	L_{in}	300 µH
L_{lk1}	17 µH	n	1

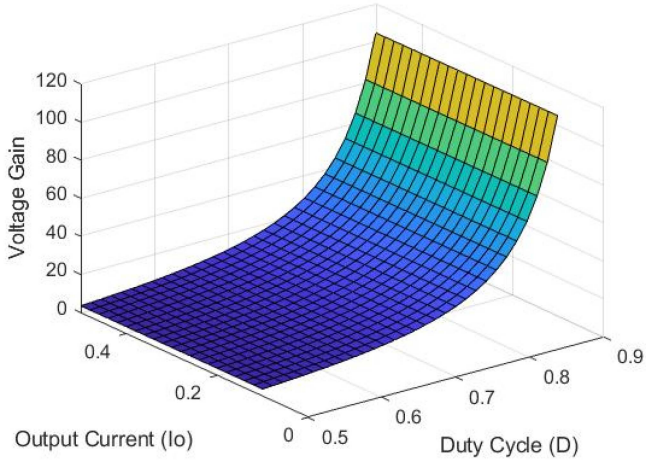

Fig. 7. Voltage gain ratio of the converter versus I_o and duty cycle (D) based on (31).

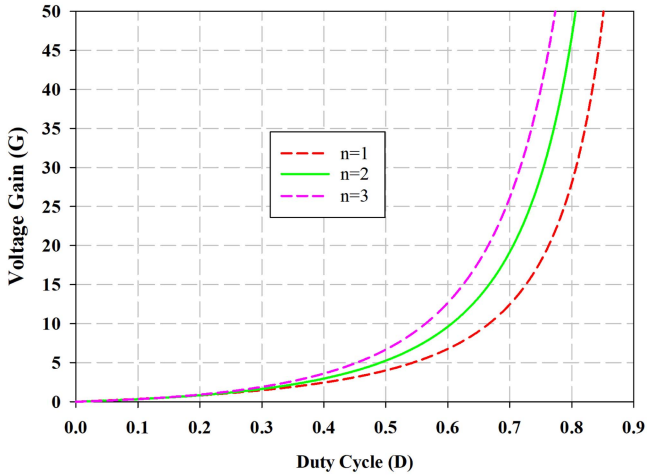

Fig. 8. Voltage gain ratio versus duty cycle for different turn ratios (n), without leakage inductance (L_{lk1}) (32).

voltage gain ratio, a 3-D plot of voltage gain versus duty cycle and output current is illustrated in Fig. 7.

In addition, by omitting the influence of leakage inductance (L_{lk1}) in (31) and simplifying the equation, we arrive at the following equation, which represents the voltage gain ratio G:

$$G = \frac{V_o}{V_{in}} = \frac{[2n+1]\,D + 2\left[n^2 - n - 1\right]D^2 + \left[1 - n^2\right]D^3}{n(1-D)^2}. \tag{32}$$

Considering $n = 1$, the gain is given by $\frac{V_o}{V_{in}} = \frac{D(3-2D)}{(1-D)^2}$. However, in accordance with mode 6 and taking into account the effective duty cycle (D_{eff}), it is more accurate to utilize the equation $\frac{V_o}{V_{in}} = \frac{D_{eff}(3-2D_{eff})}{(1-D_{eff})^2}$.

Fig. 8 illustrates the voltage gain plot of the proposed converter based on (32) for various values of the transformer turn ratio (n). By increasing the turn ratio of the coupled inductors, the desired output voltage can be achieved at lower duty cycles.

TABLE II
CURRENT AND VOLTAGE STRESS OF SEMICONDUCTOR ELEMENTS

COMPONENTS	CURRENT STRESS	VOLTAGE STRESS
SWITCH S_1	$\frac{P_o}{V_{in}}+\frac{V_{in}}{L_{in}}DT+\left(\frac{D^2(2D-n)T}{(1-D)^2}\right)\frac{V_{in}}{L_{lk}}$	$\frac{V_{in}}{1-D}$
DIODE D_1	$\frac{P_o}{V_{in}}+\frac{V_{in}}{L_{in}}DT$	$\frac{V_{in}}{1-D}$
DIODE D_2	$\frac{(n+2)V_{in}-V_o(1-D)}{L_{k1}}T_{sw}$	$\frac{V_{in}(1+\mathrm{D})}{1-D}$
DIODE D_o	$\frac{I_o}{1-D}$	$\frac{V_{in}(1+\mathrm{D})}{1-D}$

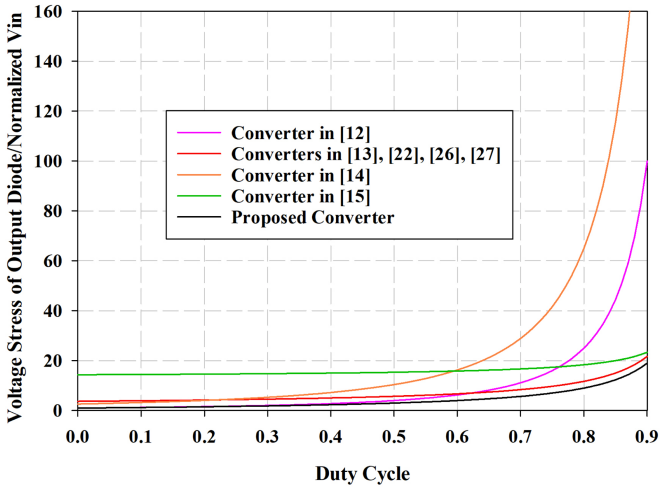

Fig. 9. Comparison of output diode voltage stress: proposed converter versus converters in [12], [13], [14], [15], [22], [26], and [27].

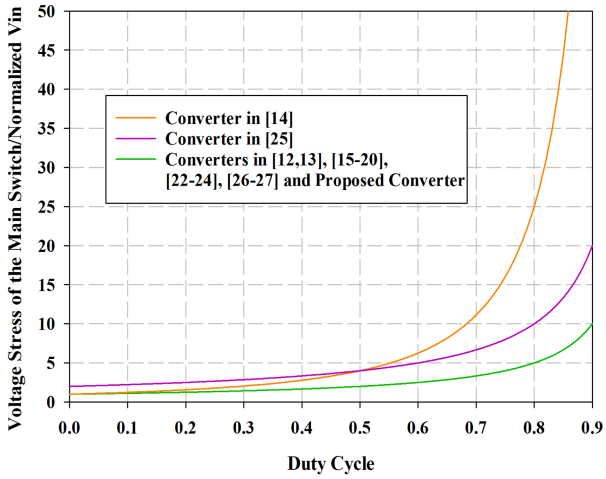

Fig. 10. Comparison of main switch voltage stress: proposed converter versus converters in [12], [13], [14], [15], [16], [17], [18], [19], [20], [22], [23], [24], [25], [26], and [27].

TABLE III
WINDING PARAMETERS OF THE COUPLED INDUCTORS

Parameter	Proposed Converter		
	Lin	L1	L2
Number of wires turns	71	25	25
Wire length [cm]	497	410	410
Wire cross section [mm]	1.5	1	1
DC resistance [Ω]	10 mΩ	20 mΩ	20 mΩ

B. Voltage Stress of the Semiconductor Elements

Table II presents the voltage and current stress values for different semiconductor components. We can determine the voltage stress of the main switch S_1 and diode D_1 by applying mode 1 and mode 3, respectively, which results in a voltage stress equal to V_{CC}. Equation (20) can be used to calculate these voltage stress values. Similarly, the voltage stress values for diodes D_2 and D_O can be determined using mode 2 and mode 1, respectively, resulting in stress values of V_{C2}-V_{C1} and V_O-V_{C3}-V_{C1}. These values can be calculated using (28)–(31).

Moving on to the current stress, the highest current for switch S_a is equal to the summation of input current and i_{lk} during mode 2. Using (1) and (3) and substituting the values of V_{c1}, V_{c2}, V_{c3}, and V_{cc} from (28), (29), (30) and (20), the current stress of the switch can be calculated. Also, the output diode and switch voltage stress comparison of the proposed converter versus other converters are shown in Figs. 9 and 10.

C. Design of Magnetic Components

The magnetic components of this circuit are the input inductor Lin and the coupled inductors L_1 and L_2. To design L_{in}, we need to take into account the desired ripple and the V_{in} voltage that is applied across L_{in} when the switch is ON. We can use (33) to calculate L_{in}

$$L_{\text{in}}=\frac{V_{\text{in}}.D}{\Delta I.f_{\text{sw}}}. \tag{33}$$

For designing the coupled inductors, we need to determine the turn ratio (n) and the magnetizing inductance L_m. The turn ratio affects the voltage stress on the main switch, and a higher turn ratio results in a smaller duty cycle and lower voltage stress on the switch. However, a lower turn ratio and larger duty cycle will reduce the amount of power processed magnetically through the coupled inductors.

To design the magnetizing inductance (L_m), we need to consider the voltage ($V_{CC}-V_{C1}$) applied across L_m when the switch is on [as per (22)]. It is important to note that an effective duty cycle should be considered for the turn-ON duration of the switch. In this converter, as the magnetizing inductance current flows in both directions, the peak current of L_m changes between positive and negative values, consistently operating under continuous conduction mode (CCM) conditions. The specifications of the inductors are presented in Tables III and IV

$$L_m=\frac{\left(1+D_{\text{eff}}\left(\frac{n+1}{n}\right)\right)V_{\text{in}}-\frac{4nI_o}{D_{\text{eff}}^2T}L_{lk1}}{\Delta I_{Lm}f}\,D.T. \tag{34}$$

TABLE IV
PARAMETERS OF THE MAGNETIC CORES

Parameter	Input Inductor	Coupled Inductor
Core	EI 33-29	EE 42-42
Core size	33 × 29 × 13 mm	42 × 42 × 15 mm
Cross-sectional area	119 mm^2	182 mm^2

D. Design of Capacitors

When the switch is on, C_C is discharged by the magnetizing inductance current and C_1 is charged by this current. Thus, their voltage ripples are equal. The capacitors are designed based on the desired voltage ripple as follows:

$$C_1 = \frac{I_{L\text{in}}\,(1-D)}{f\Delta V_{C1}} \tag{35}$$

$$C_C = \frac{I_{LM}D}{f.\Delta V_{CC}} \tag{36}$$

$$C_2 = C_3 = \frac{(1-D)\,I_{Lm}}{f\,(n+1)*\Delta V_o}. \tag{37}$$

Also, the snubber capacitors are achieved by

$$C_{s1}, C_{s2} > \frac{i_{\text{sw}} * t_f}{2V_{\text{sw}}} \tag{38}$$

where V_{sw} is the maximum voltage of the switch, i_{Sw} denotes the switch current, and t_r and t_f are rise and fall times, respectively.

E. Soft Switching Criteria

According to modes 3 and 4 as well as (12), the D_O diode must turn OFF before entering mode 5. This implies that Δt_{42} duration must be shorter than the OFF time of the switch which is $(1-D)T$. Consequently, prior to commencing mode 5, D_o turns OFF, allowing for the discharge of the C_s capacitor.

$$\Delta t_{42} + \Delta t_{54} < (1-D)\,T. \tag{39}$$

Replacing (12) and (15) in (39)

$$\frac{V_{CC}}{I_{L_{\text{in}}} + \frac{(n+1)}{n} I_{\text{lk1}} - \frac{I_{Lm}}{n}} C_S + \frac{i_{DO-\text{peak}}}{\frac{V_{C3}}{n} + V_{C1}} L_{\text{lk1}} < (1-D)\,T. \tag{40}$$

Simplifying the above equation, the maximum value for C_s is achieved based on L_{k1}, which can guarantee soft switching. Also, the maximum snubber capacitor to achieve ZVS as a function of duty cycle and output current is shown in Fig. 11.

$$C_S < \left(\frac{nI_{L_{\text{in}}} + (n+1)\,I_{\text{lk1}} - I_{Lm}}{nV_{CC}}\right) \times \left((1-D)\,T - \frac{2n.L_{\text{lk1}}I_o}{(1-D_{\text{eff}})\,(V_{C3}+nV_{C1})}\right). \tag{41}$$

To analyze soft switching under light loads, it is important to consider the slight variations in the duty cycle of the switch as the load changes (refer to Fig. 5). By appropriately selecting a value for C_S in (41) under full load conditions, the inequality in (40) can be satisfied for light loads. As the load decreases, the term in (40) containing I_O also decreases, whereas the duty cycle remains nearly constant. This ensures that the inequality remains valid even at light loads. As a result, diode D_O turns OFF before entering mode 5, guaranteeing the achievement of soft switching regardless of the load condition, as long as the input inductor current operates in CCM. To demonstrate this and ensure soft switching, (41) is used to plot the maximum C_S value versus I_O and D, guaranteeing soft switching. This demonstrates that when I_O reduces, the maximum possible capacitor to provide soft switching will increase. Therefore, by considering full load conditions when choosing the value of the C_S capacitor, soft switching at light loads is also guaranteed.

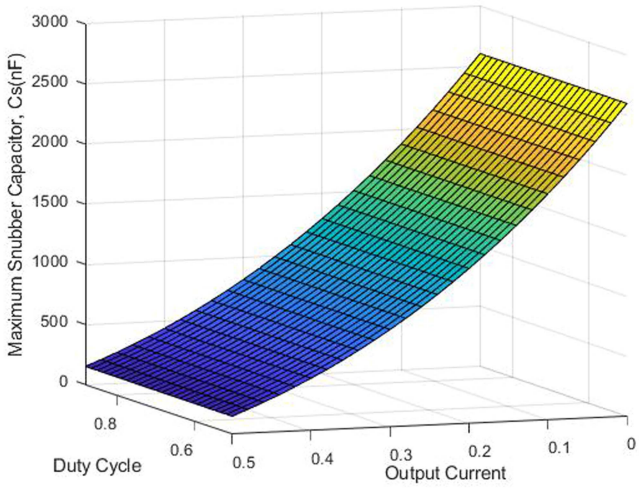

Fig. 11. Maximum snubber capacitor to achieve ZVS as a function of duty cycle and output current.

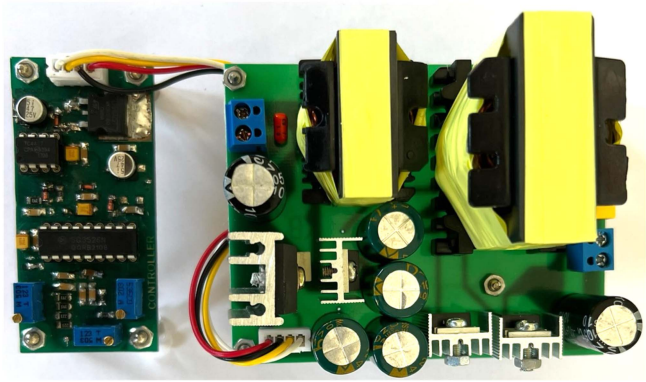

Fig. 12. Power and control prototype of the proposed converter.

IV. RESULTS AND COMPARISONS

A. Experimental Results

To prove the effectiveness of the proposed converter in real conditions, a laboratory prototype of the proposed converter is implemented and shown in Fig. 12. The full specifications of the implemented circuit are listed in Table I. The experimental waveforms are provided in Fig. 13. Fig. 14(a) represents the

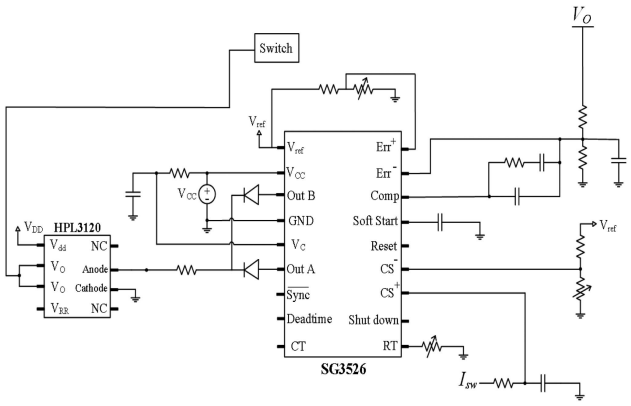

Fig. 13. Control circuit of the proposed converter.

voltage and current of the switch S. As can be seen in Fig. 14(a), the ZVS condition is achieved for the power switch at turn on and turn OFF. Also, Fig. 14(a) shows that the voltage stress of the switch is much lower than the converter output resulting in using a low voltage-rated switch with lower $R_{ds}(\text{on})$. This can reduce conduction losses of the switch. The voltage and current waveforms of D_2, D_O are shown in Fig. 14(b). As can be observed, D_2 and D_O turn OFF under ZCS condition. The voltage stress across D_O is less than the output voltage, and the existence of the leakage inductance leads to lower reverse recovery losses. The voltage and current of the clamp diodes D_1 are illustrated in Fig. 14(c). A considerably lower voltage than the output voltage is applied across this diode, this diode also has ZCS turn-OFF performance and does not impose reverse recovery losses. The input current waveform is shown in Fig. 14(d) in which the input current is continuous thanks to the input inductor. Low rippled and continuous input current is an important advantage of the proposed structure compared with coupled-inductor-based step-up counterparts which makes it a good candidate for renewable and battery-based applications. The proposed converter has also been tested at 50% of nominal load to evaluate its performance. Fig. 14(e) illustrates the soft switching operation of the switches at light loads. The voltage of C_2, C_3, and C_C capacitors, along with the current of input inductors, and L_1 and L_2 are respectively, shown in Figs. 14(f)–(h) and 9(i).

The control block diagram of the presented converter and its 3-D prototype are shown in Fig. 14. A simple voltage control circuit using SG3526 is utilized to regulate the output voltage.

B. Comparison Results

In this section, a comprehensive comparison is presented between the proposed high step-up boost converter and other high step-up topologies. The comparison is based on various key parameters including voltage gain, switch voltage stress, soft switching performance, continuous input current, common ground, floating switch, and component count. The results of the comparison are summarized in Table V.

From a soft-switching perspective, most converters except for [8], [13], [14], and [15] exhibit a soft-switching condition. However, it is important to note that the voltage gain ratio and voltage stress across the main switch in converters presented in [17] and [18] are identical to those of a conventional boost converter. This characteristic makes them unsuitable for high step-up applications.

Among the converters presented in Table V, it is noteworthy that the voltage gain ratio and voltage stress across the main switch in converters presented in [17] and [18] mirror those of a conventional boost converter. This characteristic renders them unsuitable for high step-up applications. Also, converters in [28] and [29] are Z-source and quasi-Z-source converters that inherently just operate with duty cycles under 0.5. From a soft-switching perspective, it is observed that most converters, except for [12], [14], and [15], demonstrate a soft-switching condition.

Among the converters listed in Table V, the proposed converter stands out with its high voltage gain, enabling lower duty ratios. The soft-switched converters with higher or equal voltage gain are found in [21], [23], [24], and [27]. However, they employ a higher number of components, including an extra auxiliary circuit and switch to reduce switching losses. This adversely affects both power density and efficiency when compared to the proposed converter. Converters presented in [17] and [18] have a relatively low number of total components but utilize an extra auxiliary switch for soft switching and have a low voltage gain ratio similar to the boost converter.

In addition to its high voltage gain and soft-switching capability, the proposed converter also features continuous input current, which proves advantageous for renewable energy applications, allowing for smaller input filter capacitors. Conversely, converters presented in [17], [21], [23], [24], and [26] suffer from pulsating input current, which reduces the reliability of the system and the lifespan of input sources such as fuel cells. These converters also require larger input filters when connected to solar panels. In addition, converters presented in [12], [20], [21], [23], and [24] lack a common ground between the input and output voltages, thereby introducing complexity to the control circuit.

Zheng et al. [22] discussed a converter that shares similarities with the proposed converter, including continuous input current and common ground while maintaining the same component count. However, it has a lower voltage gain and utilizes an additional floating switch, which reduces power density. Furthermore, this converter relies on an active clamp technique for achieving soft switching, which is load-dependent and lacks soft switching at light loads.

Another comparable converter with a low component count is described in [26]. However, it incorporates an additional switch with a floating gate driver, which negatively impacts both the power density and cost of the circuit. Moreover, it suffers from pulsating input current as mentioned earlier, necessitating larger input filters for connecting to solar panels.

The results depicted in Fig. 16 demonstrate the impressive performance of the proposed converter in terms of efficiency. Theoretical calculations indicate an efficiency of 98.4%, which closely aligns with the experimental efficiency of 97.5% achieved under full load conditions. The small discrepancy between the theoretical and experimental results can be attributed to losses that were not accounted for simulation.

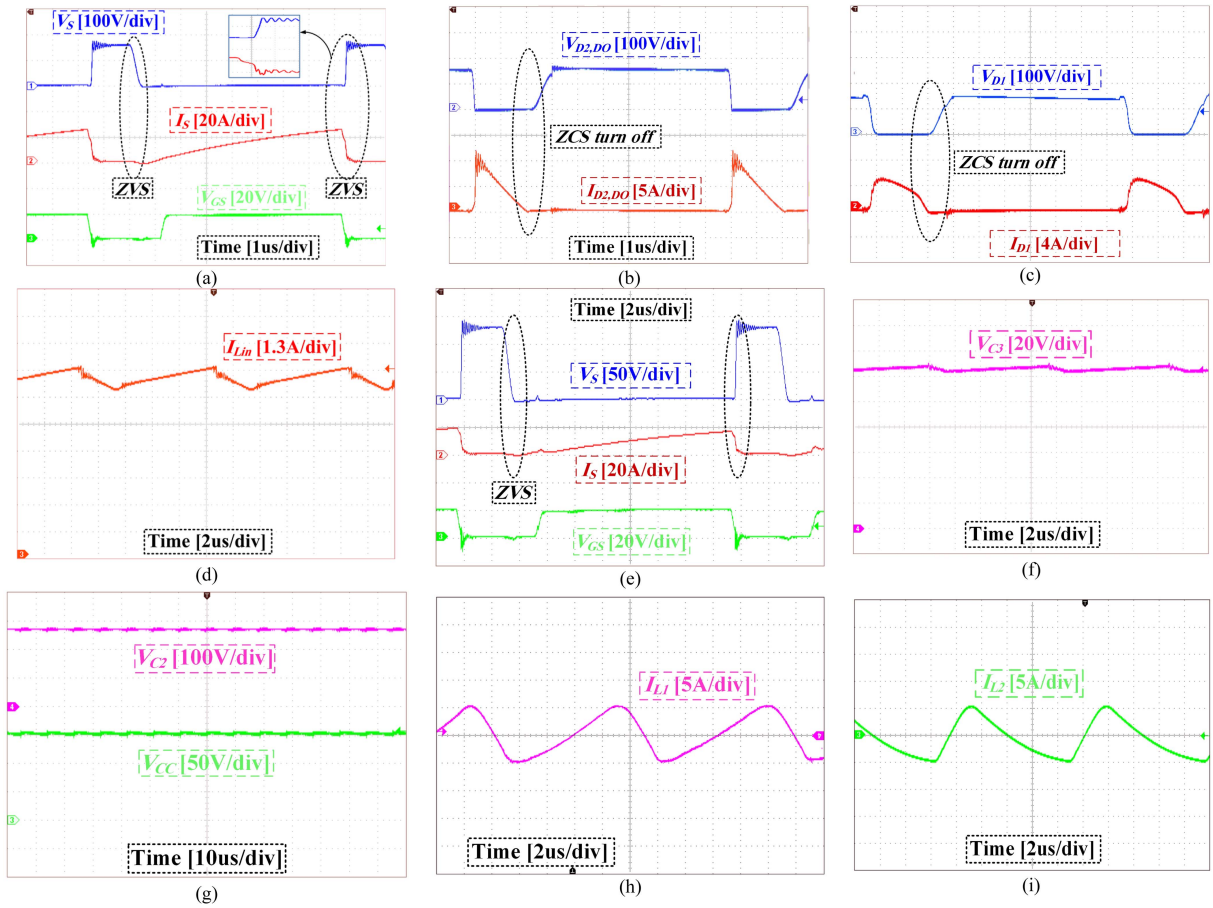

Fig. 14. Experimental waveforms of the implemented prototype. (a) V_{DS} and I_{DS}. (b) $V_{D2,DO}$ and $I_{D2,DO}$. (c) V_{D1} and I_{D1}. (d) I_{Lin}. (e) V_{DS} and I_{DS} at light load. (f) Voltage of C_3 capacitor. (g) Voltage of C_2 and C_C capacitor. (h) Current of input inductor L_1. (i) Current of input inductor L_2.

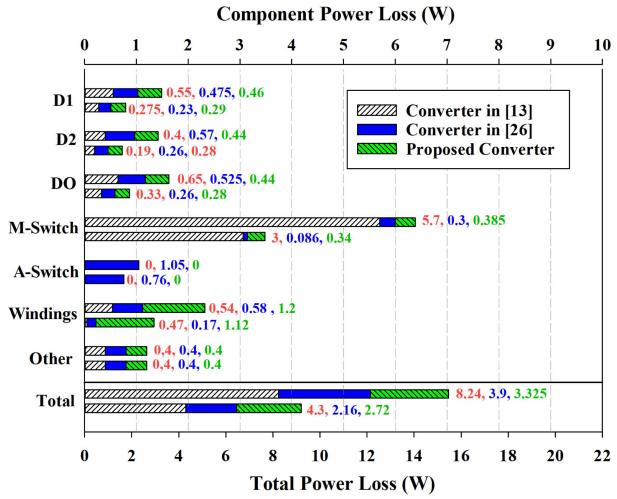

Fig. 15. Losses breakdown of the proposed converter and converters in [13] and [26].

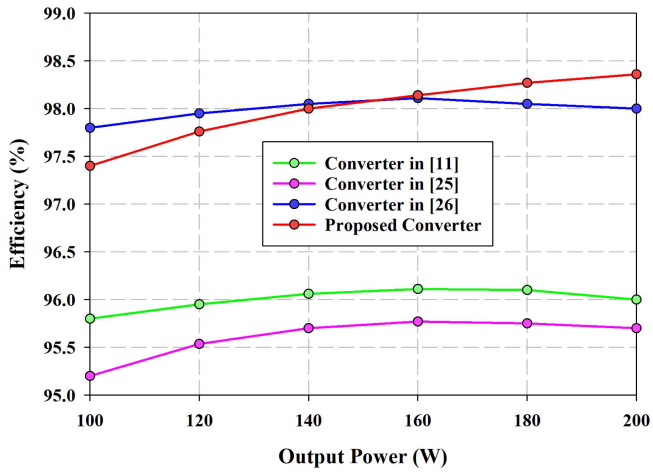

Fig. 16. Efficiency of the proposed converter in comparison with converters in [13], [26], and [29].

Fig. 16 also reveals that both the proposed converter and the converter discussed in [26] exhibit the highest efficiencies at full load. Notably, the proposed converter surpasses the efficiency of the converter in [26], achieving a slightly higher efficiency of 98.4% compared to 98% at an output power of 200 W. It is worth highlighting that both converters maintain impressive efficiency levels even at light load conditions. The converter in [26] achieves a light load efficiency of approximately 97.8%, whereas the proposed converter achieves an efficiency of around 97.4% at light loads.

TABLE V
COMPARISON OF THE PROPOSED CONVERTER WITH OTHER STEP-UP BOOST CONVERTERS

Converters	Voltage gain (G)	Duty cycle with n=1 and G=18	No extra auxiliary switches	Switch voltage stress	Soft switching turn ON/OFF	CIC*	C-G*	No floating switch	Number of components				
									MOS*	D*	Cap*	MC*	T*
Ref. [12]	$\frac{2D+n-1}{(1-D)^2}$	0.718	✘	$\frac{(1-D)V_O}{2D+n-1}$	✘	✓	✘	✘	2	4	4	2	12
Ref. [13]	$\frac{2+n}{(1-D)}$	0.833	✓	$\frac{V_O}{2+n}$	ZCS/✘	✓	✓	✓	1	3	4	2	10
Ref. [14]	$\frac{2+(n+m)+mD}{(1-D)^2}$	0.5	✓	$\frac{V_O}{2+(n+m)+mD}$	✘	✓	✘	✓	1	6	4	2	13
Ref. [15]	$\frac{1+nD}{(1-D)^2}$	0.694	✓	$\frac{V_O}{1+D}$	ZCS/✘	✓	✓	✓	1	6	4	3	14
Ref. [16]	$\frac{4}{(1-D)^2}$	0.55	✘	$\frac{V_O}{4}$	✘	✓	✓	✓	4	7	5	5	21
Ref. [17]	$\frac{1-nD}{1-D}$	0.94	✓	V_O	ZCS/ZVS	✘	✓	✓	1	4	2	1	8
Ref. [18]	$\frac{1}{1-D}$	0.94	✓	V_O	ZCS/ZVS	✓	✓	✓	1	3	3	2	9
Ref. [20]	$\frac{D(n-1)+n+2}{(1-D)}$	0.833	✘	$\frac{V_O}{D(n+1)+n+2}$	ZVS//ZVS	✓	✓	✘	2	3	5	2	12
Ref. [21]	$\frac{n(2-D)+(1-D)^2}{(1-2D)^2}$	0.331	✘	$\frac{V_O(1-D)}{n(2-D)+(1-D)^2}$	ZVS//ZVS	✘	✘	✘	4	4	5	2	15
Ref. [22]	$\frac{n+2}{(1-D)}$	0.833	✘	$\frac{V_O}{n+2}$	ZVS//ZVS	✓	✓	✘	2	2	4	2	10
Ref. [23]	G [23] *	0.65	✘	Vsw [23] *	ZVS//ZVS	✘	✓	✘	2	3	5	2	12
Ref. [24]	$\frac{2N(n+1)+4}{(1-D)}$	0.56	✘	$\frac{V_O}{2N(n+1)+4}$	ZVS//ZVS	✘	✓	✘	4	2	4	3	13
Ref. [25]	$\frac{3-D}{(1-D)}$	0.882	✘	$\frac{V_O}{3-D}$	ZVS//ZVS	✓	✓	✓	2	5	3	3	13
Ref [26]	$\frac{n+2}{(1-D)}$	0.833	✘	$\frac{V_O}{n+2}$	ZVS/ZVS	✘	✓	✘	2	3	4	1	10
Ref. [27]	$\frac{3+2n}{(1-D)}$	0.722	✘	$\frac{V_O}{3+2n}$	ZVS//ZVS	✓	✓	✓	2	6	6	2	16
Ref. [28]	$\frac{2+n-D}{(1-2D)}$	0.428	✘	$\frac{V_O}{2+n-D}$	ZVS//ZVS	✓	✓	✓	2	4	4	2	12
Ref [29]	$\frac{2n+1}{(1-2D)}$	0.416	✘	$\frac{V_O}{2n+1}$	ZVS/ZVS	✓	✓	✘	2	5	5	1	13
Proposed Converter	G in (29)	0.75	✓	$\frac{V_O}{(1-D)G}$	ZVS//ZVS	✓	✓	✓	1	3	4	2	10

CIC: continuous input current; C-G: common ground, MOS: MOSFET; D: diode; Cap: capacitor; MC: magnetic components; T: total.
* G [23] = $\frac{2+m+n+mn+D(1+m)}{(1-D)}$ and Vsw [23] = $\frac{V_O}{2+m+n+mn+D(1+m)}$

C. Loss Distribution

In this section, a detailed power loss analysis is presented to gain a better understanding of the power dissipation of each component individually. The analysis is conducted on the proposed converter and two of its counterparts from previous works [13] and [26] for comparative purposes. The converter in [13] is identical to the proposed converter in terms of the passive and active components and the converter in [26] has the same total number of components. The results of the analysis are depicted in Fig. 15 and Table VI, which shows that D_1, D_2, and D_O are common to all three converters. M-Switch refers to the main power switch, whereas A-Switch represents the auxiliary switch of the converter presented in [26]. The losses associated with the ESR of the capacitors and gate drivers are combined and labeled as "Other" in the chart. The power loss calculations are performed using OrCAD PSPICE software simulation for both half-load and full-load conditions.

Based on the analysis, it is expected that the converted presented in [13] will have the highest switch losses due to its hard switching performance. Meanwhile, the converted presented in [26] has lower main switch losses than the proposed converter, but it requires an additional auxiliary switch, resulting in higher total switch losses when considering the summation of A-Switch and M-Switch losses for the converter presented in [26]. The diode losses are almost the same for all three converters. Furthermore, the proposed converter has the highest winding losses due to the operation of its coupled inductors.

Upon examining the total power loss, the converter in [13] shows the highest power dissipation despite using the same components as the proposed converter. Under full-load conditions, the proposed converter achieves lower power loss and higher

TABLE VI
IMPORTANT PARAMETERS OF THE IMPLEMENTED PROTOTYPE

Component	Resistance [Ω]	RMS Current [A]	Power Loss [W]
Main switch	0.0036	10.34	0.385
Inductor L_{in}	0.010	6.55	0.44
Inductor $L_{1,2}$	0.020	4.4	2*0.38
Component	**Forward Voltage [V]**	**Average Current [A]**	**Power Loss [W]**
Diode D_1	0.95	0.49	0.46
Diode D_2	0.9	0.49	0.44
Diode D_O	0.9	0.49	0.44
Total			2.925

efficiency compared to the converter presented in [26]. However, under half-load conditions, the proposed converter experiences higher power dissipation. Nevertheless, the proposed converter's notable advantage lies in its use of one fewer switch compared to the converter presented in [26], enabling soft switching, high efficiency, and continuous input current.

V. CONCLUSION

In this article, we have introduced a single soft-switched high step-up boost converter that utilizes coupled inductors and a multiplier cell technique to achieve extended voltage gain, soft switching performance, and reduced voltage stress on semiconductor elements. The design of the coupled inductors enables soft switching operation for the power switch without the need for additional circuits. The leakage inductance of the coupled inductors also addresses the reverse recovery problem of diodes. The converter benefits from continuous input current, facilitated by the input inductor, which is particularly advantageous in renewable energy applications and allows for smaller input filter capacitors. With its simple structure, low cost, and high efficiency, the proposed converter is well-suited for low to medium-power applications with limited input voltage levels. The implementation of a 200 W, 30–400 V laboratory prototype demonstrated excellent performance, achieving full load efficiency of 97.5%.

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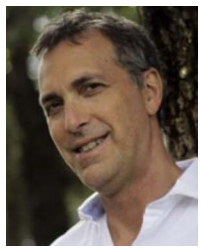

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