Letters

Liquid Metal Fluidic Connection and Floating Die Structure for Ultralow Thermomechanical Stress of SiC Power Electronics Packaging

Wei Mu, *Graduate Student Member, IEEE*, Ameer Janabi, Borong Hu, *Member, IEEE*, Luke Shillaber, and Teng Long, *Member, IEEE*

***Abstract*—Coefficients of thermal expansion (CTE) of various materials in packaging structure layers vary largely, causing significant thermomechanical stress in power electronic packages during operation. For wirebondless SiC modules, the stress is even larger due to the structure's rigidity and the high Young's modulus of SiC crystals. This letter takes a flexible printed circuit board (FPCB)/die/active metal brazed (AMB) packaging stack as an example to prove the feasibility of floating die structure enabled by liquid metal (LM) fluidic connection. The CTE mismatch among the die, printed circuit board, and AMB substrate is decoupled by the LM layer without compromise of thermal and electrical conduction. The finite-element analysis demonstrates a 56% reduction in von Mises stress of the device and more than 99% shear stress reduction at the FPCB-AMB interface, compared with a conventional rigid solder connection. Testing results show that LM-based packaging has a similar thermal and electrical conduction and higher breakdown voltage when compared with the soldered counterpart. Accelerated thermal cycling aging tests validate the stability of the insulation ring for LM-based packaging, especially under high-temperature conditions. The feasibility of using LM fluidic interconnections for a floating die structure of SiC packaging is validated.**

***Index Terms*—Liquid metal (LM), printed circuit board (PCB)/direct bond copper (DBC) hybrid packaging, reliability, SiC packaging, thermomechanical stress.**

I. Introduction

POWER electronics' packages involve layers of materials with different coefficients of thermal expansion (CTE), leading to thermomechanical stress during operation. Currently, to improve the thermal and electrical performance of power modules, bond wires are replaced by copper clip, printed circuit board (PCB), or ceramic substrate, which also increase the rigidity of the structure. The CTE mismatch between the materials of additional packaging layers can cause significant stress and lead to failures after long-term operation. This problem is more pronounced for SiC devices due to their high Young's modulus

Manuscript received 1 December 2023; revised 3 February 2024 and 4 March 2024; accepted 9 March 2024. Date of publication 27 March 2024; date of current version 16 May 2024. *(Corresponding author: Teng Long.)*

The authors are with the Department of Engineering, University of Cambridge, Cambridge CB2 1PZ, U.K. (e-mail: TL322@cam.ac.uk).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2024.3379121.

Digital Object Identifier 10.1109/TPEL.2024.3379121

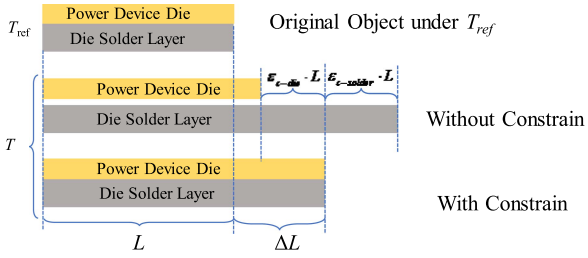

Fig. 1. Illustration of constrained strain and thermal stress.

[1]. Furthermore, the small footprint of SiC MOSFET die can increase the heat flux density significantly, causing higher thermal stress due to a high-temperature gradient [2]. It is reported in [3] that the number of cycles to failure is inversely correlated to the maximum von Mises stress in the solder layer. Therefore, reducing thermal stress is crucial for power modules.

Studies on mitigating thermomechanical stress often focus on double-sided cooled modules [3], [4], [5], [6], [7], [8], [9]. These methods are based on low CTE/Young's modulus materials or stress-relieving structures. The application of low CTE materials includes molybdenum buffer [4], porous sintered silver interposer [5], and die attach [6]. Examples of stress-relieving structures include trenched copper plates [7], geometrically modified spacers [3], fuzzy buttons [8], and additional direct bonded copper plate as stress relaxation [9].

This letter proposes a novel "floating die" as a stress-relieving structure realized by liquid metal (LM) fluidic material. A flexible PCB (FPCB)/die/active metal brazed (AMB) substrate hybrid module is designed to demonstrate the feasibility of LM fluidic connection and floating die structure. PCB/die/ceramic substrate has been an attractive solution for power electronics packaging because it can combine the advantages of electrical integration of the PCB and heat dissipation of the ceramic substrate [10]. Moreover, the performance of PCB/ceramic hybrid design can be further exploited by combining it with double-sided cooling [11], embedded die structure [12], and nano-silver sintering [13]. However, previous studies on hybrid packaging solutions mainly focus on the design and optimization of thermal and electrical performance. Meanwhile, the high thermomechanical stress, resulting from both the increased number of layers and the diversity of materials used, has not been adequately investigated.

Therefore, this letter takes an FPCB/die/AMB packaging stack as an example of implementing LM fluidic connection and floating die structure while maintaining its superior thermal and electrical performance.

The 3-D finite-element analysis (FEA) is used to model the thermomechanical stress incurred in the device package in Section III. To give an intuitive explanation of the cause of the stress in the device package, we can consider a simplified 1-D model of a power device die and its die-attach solder, which is commonly used in packaging for electrical and thermal interconnection, as shown in Fig. 1.

Assume that the die and solder are stress free at the initial reference temperature T_{ref}. When temperature T rises to higher values, the die is under tension and the solder is under compression, resulting in constrained strain that is expressed as follows:

$$\varepsilon_c = \alpha\,(T - T_{\text{ref}}) - \frac{\Delta L}{L}. \tag{1}$$

According to Newton's third law, the stress of the die and solder layer is equal and the directions are opposite; the constrained strain of the die and solder can be, respectively, solved. The resulting thermal stress is expressed as follows:

$$\begin{aligned}\sigma_{\text{solder}} = \sigma_{\text{die}} &= E_{\text{solder}} \cdot \varepsilon_{c-\text{solder}} = E_{\text{die}} \cdot \varepsilon_{c-\text{die}} \\ &= \frac{(\alpha_{\text{solder}} - \alpha_{\text{die}}) \cdot (T - T_{\text{ref}})}{1/E_{\text{die}} + 1/E_{\text{solder}}}\end{aligned} \tag{2}$$

where $\varepsilon_{c-\text{solder}}$ and $\varepsilon_{c-\text{die}}$ are the constrained strains of the die and solder, respectively, as shown in Fig. 1, which is the direct cause of thermal stress. $\alpha_{\text{solder}} - \alpha_{\text{die}}$ is the CTE mismatch and E is Young's modulus. As shown in (2), because the SiC material has higher Young's modules, the resulting thermal stress is also high. Instead of solder, interconnecting materials with a lower Young's modulus or similar CTE of the SiC die can reduce the thermal stress. LMs can be considered to have zero Young's modulus since liquids do not exhibit elastic behavior with an infinite capacity to deform under any applied stress without exhibiting a restoring force.

This work eliminates constrained strains by decoupling the thermal strain of the SiC die from the AMB substrate using a floating die structure. This structure is formed by the frictional contact using LM for interconnection, instead of the conventional rigid connection.

LMs are types of alloys that keep in the liquid phase at room temperature. This nature, along with its high thermal and electrical conductivity, makes LMs receive increasing attention in soft electronics, robotics, and biomaterials [14]. Unlike the soldering or sintering process, which exposes devices to high temperatures and rigidly bonds them, LM can achieve interconnection at room temperature with a fluidic approach [15]. For power electronics, bismuth-based LM has been used to reduce the thermal resistance of a press-pack insulated gate bipolar transistor (IGBT) module [16], while liquid gallium was used as the top-side interconnection for a diode [17]. This letter fully utilizes the advantages of LMs with an embedded floating die structure. The SiC MOSFET is floating on a layer of LM, which acts as the die attach instead of using rigid interconnection methods.

TABLE I
COMPARISON OF DIFFERENT LMS AND SOLDER

Material	Key material properties		
	Melting point (°C)	Electrical Conductivity (S/m)	Thermal Conductivity (W/(mike))
GaInAg	8	5.0×10^6	75
$Ga_{68}In_{22}Sn_{10}$	−17	3.46×10^6	16.5
$In_{51}Bi_{32.5}Sn_{16.5}$	53	4.9×10^6	70
Mercury	−39	1.04×10^6	8.34
Solder (SAC305)	217	7.6×10^6	58.7

The fluidic nature of LM can decouple the thermal strain of two different materials at the interface with an uncompromised electric and thermal conduction capability. The LM layer not only eliminates the thermomechanical stress of the die-attach layer but also reduces the shear stress between AMB and FPCB.

The rest of this letter is organized as follows. Section II presents the selection of LMs and the structure of the LM-based SiC packaging. Section III evaluates and compares the thermal stress of the LM-based packaging with its soldered counterpart. Section IV describes the fabrication process and experimental results. Finally, Section V concludes this letter.

II. PROPERTIES OF LMS AND DESIGN OF LM-BASED SIC PACKAGING

Desirable LM should have relatively high electrical and thermal conductivities. A low melting temperature is preferable for keeping the floating structure. Table I compares the properties of different LMs. Mercury and Galinstan ($Ga_{68}In_{22}Sn_{10}$) have low melting points but less conductive and the toxicity of mercury is also problematic. $In_{51}Bi_{32.5}Sn_{16.5}$ has decent conductivities but the melting temperature (53 °C) is impractical. In this letter, an LM material composed of silver, indium, and gallium (GaInAg) is used. It has competitive thermal and electrical properties [thermal conductivity of 75 W/(mK) and electrical conductivity of 5×10^6 S/m] compared with SAC 305 solder. In addition, GaInAg is a nontoxic material with a relatively low melting point of 8 °C making it a feasible interconnection material at room temperature.

The selection of GaInAg also considers die metallization and the coating of AMB substrate used in this study. The drain of the SiC MOSFET (SCT116N120G3DXAG, 1200 V, 130 A) from STMicroelectronics is Ti/Ni/Ag, which exhibits chemical stability when in contact with gallium in the GaInAg LM. Also, this drain metallization is commonly used for power electronic devices. The AMB substrate is plated with silver. This ensures good wettability with the silver-based GaInAg-LM, allowing effortless LM printing on the surface of AMB and die metallization, and reducing the thermal and electrical resistance at the interface.

Due to the strong cohesive force of metallic bonds among atoms, LMs have high surface tension with a surface tension coefficient γ >500 mN/m [18], which is six times higher than

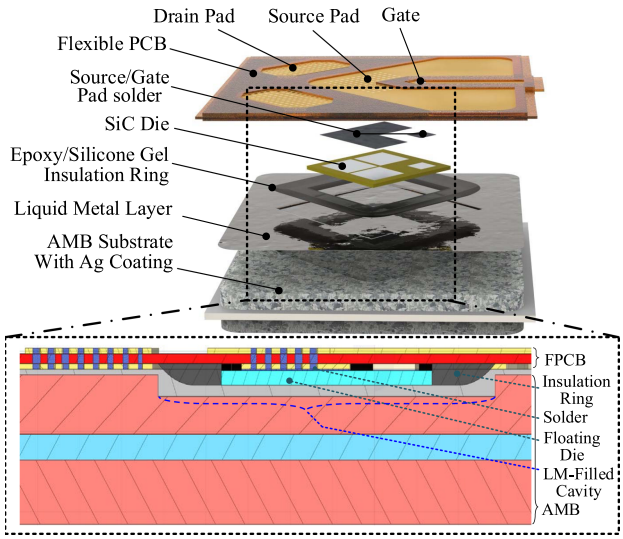

Fig. 2. Structure of the LM-based PCB/die/AMB hybrid SiC packaging.

water. In the proposed packaging, the total perimeter L of the contact interface between AMB and FPCB wetted by LM is 54.3 mm. The minimum force $F = 2\gamma L$ needed to overcome surface tension and separate two surfaces is calculated as 54.3 mN, indicating that the surface tension of LM can support the total weight of the package (28.6 mN). Furthermore, the extremely high surface tension ensures the printed LM stays between the interface without random flow.

Fig. 2 illustrates the structure of the proposed GaInAg-LM packaging. The design is to decouple the thermal strain of the AMB substrate from both the FPCB and the SiC device using LM and an embedded floating die structure. The top surface of the AMB is covered by GaInAg-LM to replace the conventional drain-side die-attach layer. The source and gate of the SiC MOSFET die are soldered underneath the FPCB. The die chip is embedded inside the cavity of the top copper of the AMB, allowing the die to float on the LM layer. As a result, rigid connections are replaced by a frictional contact between the FPCB and the AMB, and a fluidic connection between the die and the AMB. For comparison, a soldered counterpart where both the die drain side and the FPCB are soldered to the AMB substrate is also considered in this study. Both packaging designs utilize the same FPCB, and their AMB substrates are essentially the same, with the only difference being the depth of the cavity.

The FPCB consists of a 0.29-mm-thin layer of polyimide core with two Oz copper layers at both sides. SAC 305 solder is used between the die and the FPCB by connecting the source and gate, giving precise connections to the top side of the die and keeping the die floating around the center of the cavity. Unlike the die attach between the die and the AMB substrate, the solder layer between the FPCB and the die does not experience high thermal stress, owing to the low Young's modulus and low thickness of FPCB. In addition, the thin FPCB structure also enables a small power loop that effectively reduces parasitic inductance and resistance.

The AMB has thick Cu layers of 0.8 mm, which can improve the current carrying and heat spreading capability. A cavity of 7 mm × 7 mm in the middle of the top copper layer of the AMB is designed to embed the die inside the AMB copper layer and keep the source–gate surface level with the copper top surface for FPCB connection. The cavity is rotated by 45° relative to the substrate to achieve a uniform current density distribution and keep symmetry at system level for simpler integration. The cavity is created by a chemical etching process using $FeCl_3$ solution, which is widely adopted to etch the copper on PCB [19]. The cavity depth is controlled by etching time. For the soldered module, the cavity depth is 290 μm, while the thickness of the die is approximately 180 μm. This leaves a gap of approximately 110 μm for the solder to reflow during the vacuum reflow process. For the LM packaging, the cavity depth has been reduced to 210 μm, creating a thinner gap between the bottom of the die and the AMB being filled with the LM. Therefore, the embedded die is fluidically touched to the AMB top copper layer via a fluidic LM layer. A shallower cavity can reduce the amount of LM needed, avoiding random spilling and reducing thermal resistance. Detailed dimensions of the designs can be found in Table II.

TABLE II
DIMENSIONS OF THE PROPOSED DESIGN

Parameters	Values
AMB size (L)×(W) ×(H)	15 mm×15 mm ×1.92 mm
AMB Cu thickness	0.8 mm
AMB Si3N4 Ceramic thickness	0.32 mm
SiC die size (L)×(W) ×(H)	5.1 mm×5.1 mm×0.18mm
Cavity size (L)×(W)	7 mm×7 mm
AMB cavity depth for LM packaging	210 μm
AMB cavity depth for solder packaging	290 μm
Die solder thickness of solder packaging	50 μm
AMB surface Ag metallization thickness	450 nm
FPCB polyimide core thickness	290 μm
FPCB Cu thickness	70 μm

III. THERMOMECHANICAL STRESS EVALUATION

FEA is used to evaluate and compare the thermomechanical behavior of the LM-based packaging and solder-based packaging. For thermal modeling, a loss of 100 W from the die is set as the heat source. The bottom side of the AMB is set to a heat transfer coefficient of 7500 W/(m^{2}K), representing the cooling capability provided by the liquid cooling plate in the experiment. All other boundaries are adiabatic. For mechanical modeling, the Coulomb friction model is utilized for the contact interface between the FPCB and AMB with a friction coefficient of 0.5. For the LM-based packaging, the top side of FPCB is subject to a 20 N downward force, which is insignificant for common mechanical clamping. For the solder-based packaging, no external force is exerted.

As shown in Fig. 3, the thermomechanical stress on the SiC die in the LM packaging is significantly lower than in the soldered packaging. This improves reliability because high stress within the die chip can result in cracks in the device [20]. The stress of the LM packaging is mainly distributed near the source pad where it is soldered to the FPCB. However, the FPCB is thin

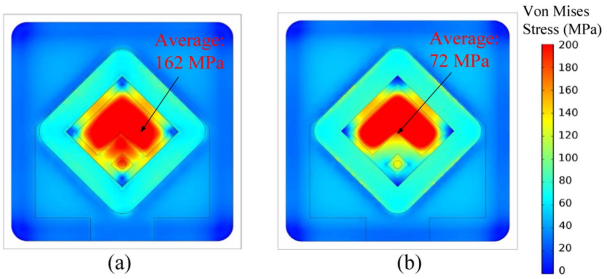

Fig. 3. Thermomechanical stress comparison of the die and the AMB. (a) Solder-based packaging. (b) LM-based packaging.

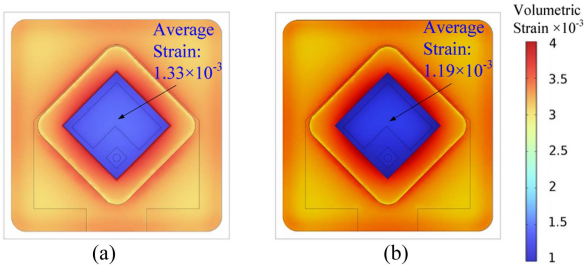

Fig. 4. Comparison of volumetric thermal strain of the die and AMB. (a) Solder-based packaging. (b) LM-based packaging.

and the polyimide has a lower Young's modulus. Therefore, the small solder connection for the die to the FPCB does not cause high stress. By contrast, for the solder-based packaging, both the top and bottom sides of the die are soldered to the FPCB and AMB, respectively. The rigid connection to the thick copper of the AMB substrate results in significant stress. Therefore, the average von Mises stress of the die in the solder packaging is 2.25 times higher than that of the LM-based design.

As it is shown in Fig. 4, because the die has a lower CTE than AMB, it has a lower thermal strain. For the LM-based packaging, the difference in thermal strain between the AMB and die is not problematic because it is decoupled by the LM and the floating die structure. Therefore, compared with the solder-based package, the LM package's die has a lower strain and its AMB has a higher strain. For the solder-based packaging, the rigid connection makes the SiC die under tension and the AMB is under compression, causing significant shear stress among die, solder, and AMB. The shear stress of the AMB is illustrated in Fig. 5. For the solder-based packaging, the average shear stress inside the cavity reaches 16.6 MPa. However, for the LM packaging, the average shear stress inside the cavity is only 106 kPa, which is a 99.4% reduction. This near elimination of sheer stress is due to the decoupling of strain of the die chip and AMB by interfacing with fluidic LM. It is noteworthy that the shear stress outside the cavity is also reduced. In Fig. 5(a), high shear stress between the FPCB and the AMB is due to the rigid connection via solder. This stress is nearly eliminated by joining the FPCB and AMB via fluidic LM, as shown in Fig. 5(b).

The shear stress at the bottom copper layer of the FPCB is also compared in Fig. 6. The average surface shear stress of the solder packaging reached 3.95 MPa, whereas that of the LM packaging

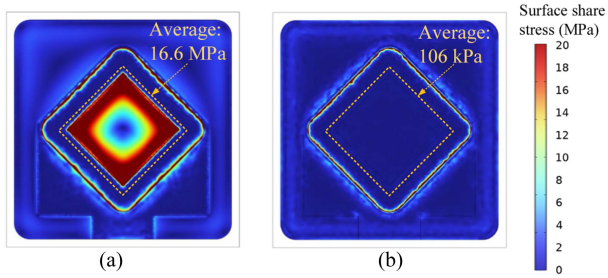

Fig. 5. Comparison of shear stress on the top copper of AMB substrate. (a) Solder-based packaging. (b) LM-based packaging.

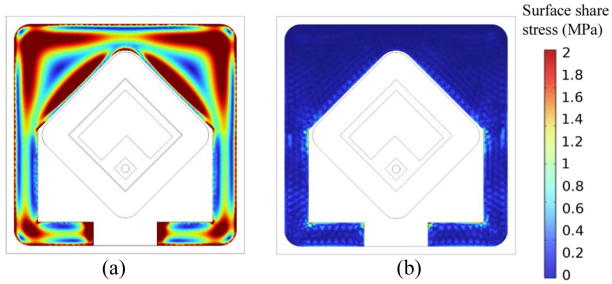

Fig. 6. Comparison of shear stress of the bottom Cu layer of the FPCB. (a) Solder-based packaging. (b) LM-based packaging.

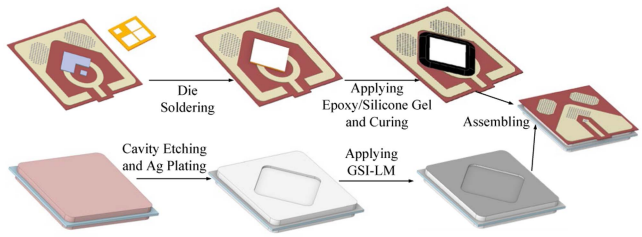

Fig. 7. Fabrication process of the GaInAg-LM FPCB/AMB hybrid packaging.

is only 0.74 MPa. This is because the rigid connection of the solder-based packaging is changed into a fluidic connection in the LM-based packaging, and the force on the surface of the copper becomes frictional, resulting in significantly lower shear stress from the mismatched CTE. A lower shear force on the Cu layer can reduce the possibility of delamination of the FPCB for improved reliability.

IV. Fabrication of the LM-Based Packaging and Experiment

Samples of LM-based packaging are made using the process, as shown in Fig. 7. After applying solder paste using stencil, the source and gate of the die are soldered to the FPCB. Then, the epoxy or silicone gel is applied to form an insulation ring around four sides of the die. This can form a dam to stop the LM from leaking to the source and gate and provide sufficient protection from voltage breakdown. The AMB is etched, plated with silver, and then covered with GaInAg-LM. Finally, the FPCB with die is touched to the AMB via GaInAg-LM. The high surface tension

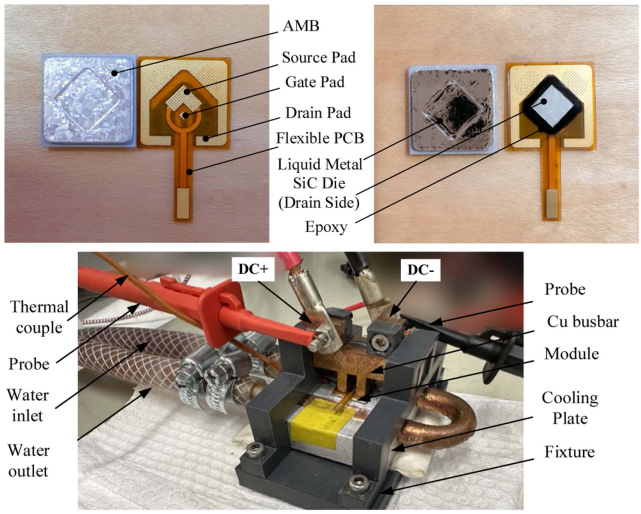

Fig. 8. Prototype of LM-based packaging and experimental setup.

of GaInAg-LM adheres the FPCB and AMB. For comparison, solder-based packaging using the same die and FPCB is also fabricated.

As shown in the upper half of Fig. 8, the top metallization of the AMB substrate is entirely wetted by the GaInAg-LM. The surface tension well holds the LM on the Ag-plated Cu surface and constrains LM from randomly flowing and dripping. A fixture is designed to accommodate the device under test (DUT), Cu busbar, and cooling plate. A downward clamping force is applied to DUT by the fixture through Cu busbar.

The experimental setup for the comparison of thermal resistance under different power dissipation is shown in the lower half of Fig. 8. To ensure a fair comparison, we used the same cooling conditions for both packaging types, including an identical cooling plate with the same coolant temperature (11.6 °C) and flow rate (16 L/min). We also applied thermal interface material for better thermal conductivity and used a torque screwdriver to uniformly tighten the fixture screws, reducing variability in thermal contact resistance. Additionally, we set the thermal camera to capture the highest temperature on the source soldering pad, ensuring that any potential error would be systematically applied to both sets of measurements. This consistency in testing conditions is crucial for a valid comparison, as it minimizes external influences and reveals the inherent thermal performance differences between the two packaging approaches. It is shown in Fig. 9 that the thermal resistance of the LM packaging slightly increases with its power dissipation, from 0.92 to 1.04 K/W. This is because, under high power losses, the high temperature increases the scattering of free electrons inside LM, reducing its thermal conductivity. However, the average thermal resistance for the LM packaging is only 5% larger than that of the soldered counterpart.

By replacing the cold plate with a load cell, the downward force (clamping force) applied to the DUT can be measured. The electric characteristics of the LM packaging have been tested under different clamping forces. The result from the B1505A curve tracer is demonstrated in Fig. 10. When the force applied

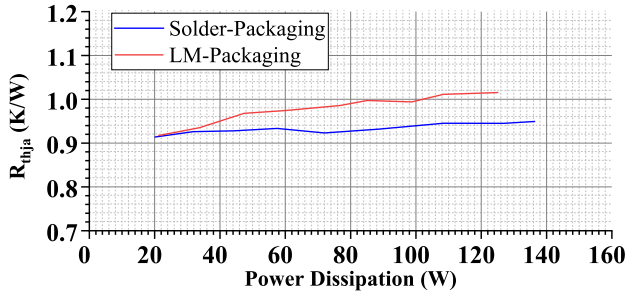

Fig. 9. Junction to coolant thermal resistance comparison.

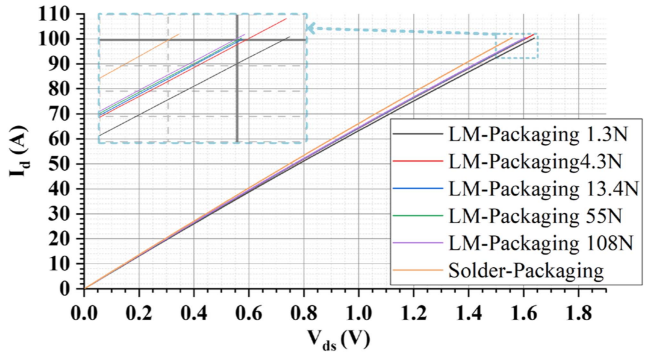

Fig. 10. Output characteristics comparison between solder packaging and LM packaging under different pressures ($V_{gs} = 18$ V).

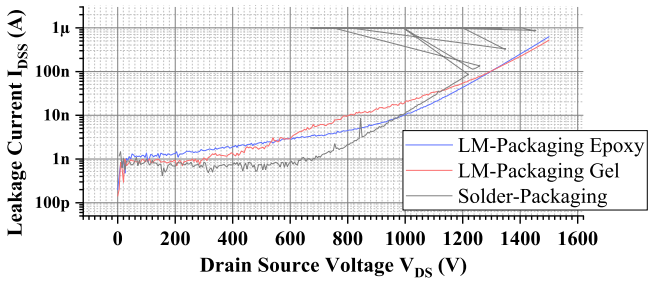

Fig. 11. Leakage current measurement result for LM packaging ($V_{gs} = 0$ V).

to the FPCB exceeds 4.3 N, its influence on on-state resistance is negligible. This means that the LM-based packaging design requires very low clamping force to achieve good electric contact among FPCB, die, and AMB. In real applications, this pressure is lower than the pressure required for a power module to be attached to a heatsink. The R_{dson} for the solder packaging and LM packaging is 15.53 mΩ and 15.98 mΩ, respectively, which are very close.

To validate the voltage-blocking capability of the proposed LM packaging, the leakage current is measured, as shown in Fig. 11. The LM-based packages with epoxy or silicone gel insulation ring are tested and compared with the soldered design. The measurement stops when the voltage exceeds 1.5 kV, or the leakage current exceeds 1 μA. Both LM-based designs have a leakage less than 1 μA at 1.5 kV, which is beyond the rated voltage of the SiC MOSFET. This proves that the GaInAg-LM

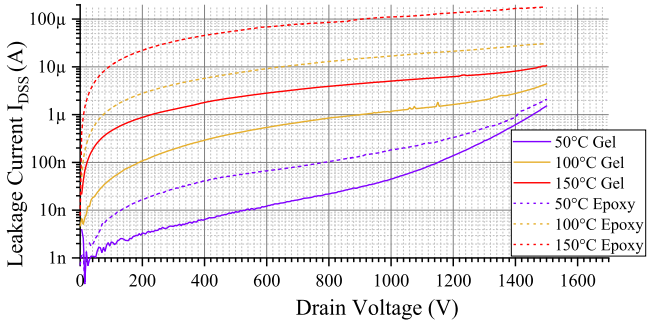

Fig. 12. Leakage current of LM package at higher junction temperatures.

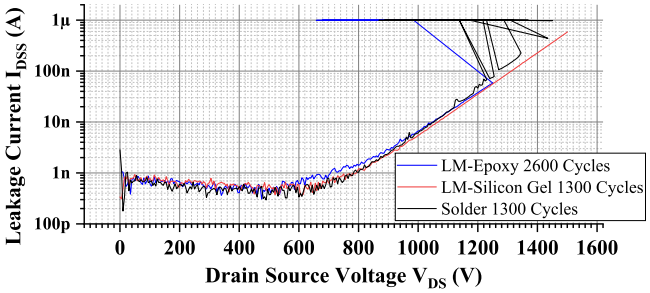

Fig. 13. Leakage current of comparison after thermal cycling.

packaging does not affect the voltage-blocking capability of the device.

For the soldered design, the implementation of epoxy or silicone gel to the assembly needs to be after the soldering process by injecting because the soldering temperature is too high for epoxy or silicone gel to withstand. The injecting process is prone to void, which could be the cause of an earlier breakdown at 1220 V of the soldered design, as shown in Fig. 11. By contrast, the fluidic approach using LM at the room temperature to join parts, thus, the insulation epoxy or silicone gel, can be applied to the die sides and protect the die before applying the LM. The fabrication process becomes simpler and more reliable.

Leakage current measurements were extended to higher junction temperatures, revealing an expected increase in leakage current with temperature, a characteristic inherent to semiconductor devices. As shown in Fig. 12, both the epoxy and silicone gel can withstand the high voltage and high junction temperature without signs of breakdown. In this test, silicone gel exhibits better insulation capability, especially at high-temperature ranges.

A preliminary reliability assessment on the LM packaging is carried out through accelerated thermal cycling tests using a harsh temperature profile. The environment temperature T_a cycles are between 52 and 217 °C with $\Delta T_a = 165$ °C and 4 min per cycle. The measured temperature at the top of the package varies between 52 and 180 °C with $\Delta T = 128$ °C. The leakage current after temperature cycling is shown in Fig. 13. The LM package with silicone gel insulation ring had no degradation of insulation after 1300 cycles.

The microscopic image of the silicone gel insulation ring after 2600 thermal cycles in Fig. 14 also showed no damage caused

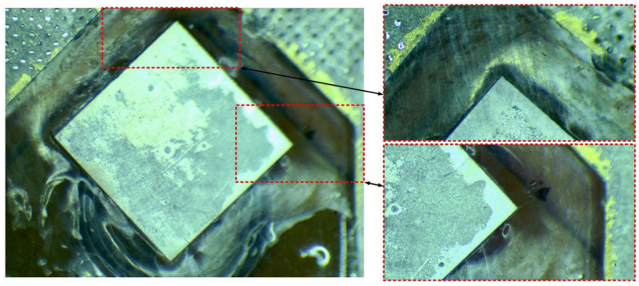

Fig. 14. Microscopic image of silicone gel insulation ring with no signs of damage after 2600 thermal cycles.

by repeated temperature cycles. However, this sample had a gate failure due to high temperature. This LM sample would have been able to pass the insulation test after 2600 cycles if the gate of the MOSFET had not been damaged. The soldered module experienced 2600 cycles failed due to solder crack. Therefore, the leakage of the soldered package that experienced 1300 cycles is demonstrated, which breaks down at 1230 V. The module with epoxy insulation has a breakdown voltage of 1250 V after 2600 cycles, which is higher than the soldered module that experienced fewer temperature cycles.

V. Conclusion

This letter presents a power electronics packaging solution based on the floating die structure and LM fluidic connection for ultralow thermomechanical stress. Instead of using rigid connections, such as solder joints and nano-silver sintering with excessive thermal stress, the GaInAg-LM layer is adopted to decouple the thermal strain while maintaining thermal and electrical connections. The FEM simulation has demonstrated a 56% reduction in the von Mises stress of the die and a 99% reduction in shear stress. Prototypes of both the LM-based packaging and solder-based packaging of a hybrid FPCB and AMB structure example are fabricated and compared in the experiment. The GaInAg-LM can provide similar electrical and thermal conduction to the solder. High-temperature leakage measurement and thermal cycling aging test validate the uncompromised voltage-blocking capability of the LM-based packaging. This letter demonstrates the feasibility of using LM material for a fluidic structure of power device packages. This new packaging technology has uncompromised thermal and electrical conduction. The fabrication of such packaging can be completed at the room temperature without large pressure, which increases the reliability of the die chip. The fluidic structure and room temperature fabrication process enabled by LM can also inspire more high-performance and low-thermal-stress packaging designs.

Acknowledgment

The authors would like to thank the Henry Royce Institute for providing access to their testing facilities, Dr. N. Udugampola for his assistance with the measurements, and STMicroelectronics for supplying us with their high-quality SiC power device.

REFERENCES

[1] B. Hu et al., "Failure and reliability analysis of a SiC power module based on stress comparison to a Si device," *IEEE Trans. Device Mater. Rel.*, vol. 17, no. 4, pp. 727–737, Dec. 2017.

[2] W. Mu et al., "Direct integration of optimized phase-change heat spreaders into SiC power module for thermal performance improvements under high heat flux," *IEEE Trans. Power Electron.*, vol. 37, no. 5, pp. 5398–5410, May 2022.

[3] J. Jeon, J. Seong, J. Lim, M. K. Kim, T. Kim, and S. W. Yoon, "Finite element and experimental analysis of spacer designs for reducing the thermomechanical stress in double-sided cooling power modules," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 4, pp. 3883–3891, Aug. 2021.

[4] M. Wang et al., "Reliability improvement of a double-sided IGBT module by lowering stress gradient using molybdenum buffers," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 7, no. 3, pp. 1637–1648, Sep. 2019.

[5] C. Ding, H. Liu, K. D. T. Ngo, R. Burgos, and G.-Q. Lu, "A double-side cooled SiC MOSFET power module with sintered-silver interposers: I-design, simulation, fabrication, and performance characterization," *IEEE Trans. Power Electron.*, vol. 36, no. 10, pp. 11672–11680, Oct. 2021, doi: 10.1109/TPEL.2021.3070326.

[6] H. Ren et al., "Thermal stress reduction strategy for high-temperature power electronics with Ag sintering," *Microelectronics Rel.*, vol. 127, Dec. 2021, Art. no. 114379.

[7] X. Cao, G.-Q. Lu, and K. D. T. Ngo, "Planar power module with low thermal impedance and low thermomechanical stress," *IEEE Trans. Compon., Packag. Manuf. Technol.*, vol. 2, no. 8, pp. 1247–1259, Aug. 2012.

[8] A. I. Emon, Y. Wu, Y. Li, A. B. Mirza, S. Deng, and F. Luo, "A double-sided cooled split-phase SiC power module with fuzz button interposer," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 11, no. 5, pp. 4918–4928, Oct. 2023, doi: 10.1109/JESTPE.2023.3294932.

[9] K. Sugiura et al., "Reliability evaluation of SiC power module with sintered Ag die attach and stress-relaxation structure," *IEEE Trans. Compon., Packag. Manuf. Technol.*, vol. 9, no. 4, pp. 609–615, Apr. 2019.

[10] A. B. Jørgensen, S. Bęczkowski, C. Uhrenfeldt, N. H. Petersen, S. Jørgensen, and S. Munk-Nielsen, "A fast-switching integrated full-bridge power module based on GaN eHEMT devices," *IEEE Trans. Power Electron.*, vol. 34, no. 3, pp. 2494–2504, Mar. 2019.

[11] A. I. Emon et al., "Design and optimization of gate driver integrated multichip 3-D GaN power module," *IEEE Trans. Transp. Electrific.*, vol. 8, no. 4, pp. 4391–4407, Dec. 2022.

[12] X. Tian et al., "PCB-on-DBC GaN power module design with high-density integration and double-sided cooling," *IEEE Trans. Power Electron.*, vol. 39, no. 1, pp. 507–516, Jan. 2024, doi: 10.1109/TPEL.2023.3311440.

[13] S. Lu, T. Zhao, Z. Zhang, K. D. T. Ngo, R. Burgos, and G.-Q. Lu, "Low parasitic-inductance packaging of a 650 V/150 a half-bridge module using enhancement-mode gallium-nitride high electron mobility transistors," *IEEE Trans. Ind. Electron.*, vol. 70, no. 1, pp. 344–351, Jan. 2023.

[14] W. Babatain, M. S. Kim, and M. M. Hussain, "From droplets to devices: Recent advances in liquid metal droplet enabled electronics," *Adv. Funct. Mater.*, 2023, Art. no. 2308116.

[15] P. Ralston, M. Oliver, K. Vummidi, and S. Raman, "Liquid metal vertical interconnects for flip-chip assembly of GaAs C-band power amplifiers onto micro-rectangular coaxial transmission lines," in *Proc. IEEE Compound Semicond. Integr. Circuit Symp.*, 2011, pp. 1–4.

[16] X. Wang et al., "Thermal contact resistance optimization of press-pack IGBT device based on liquid metal thermal interface material," *IEEE Trans. Power Electron.*, vol. 37, no. 5, pp. 5411–5421, May 2022.

[17] Z. Sun et al., "Thermal characteristics of liquid metal interconnects for power semiconductors," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2023, pp. 1135–1140.

[18] M. Song, K. E. Daniels, A. Kiani, S. Rashid-Nadimi, and M. D. Dickey, "Interfacial tension modulation of liquid metal via electrochemical oxidation," *Adv. Intell. Syst.*, vol. 3, May 2021, Art. no. 2100024.

[19] O. Sisso, S. Dor, D. Eliyahu, E. Sabatani, and N. Eliaz, "Corrosion inhibition of copper in ferric chloride solutions with organic inhibitors," *npj Mater. Degradation*, vol. 4, no. 1, 2020, Art. no. 38.

[20] K. Yao, H. Yano, H. Tadano, and N. Iwamuro, "Investigations of SiC MOSFET short-circuit failure mechanisms using electrical, thermal, and mechanical stress analyses," *IEEE Trans. Electron Devices*, vol. 67, no. 10, pp. 4328–4334, Oct. 2020.