Multisampling Digital Pulse-Width Modulator Based on Asymmetric Dual-Edge Carrier

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***Abstract*—In the domain of digital control systems, significant phase delays stem from various factors, such as analog-to-digital conversion, finite sampling frequency values, algorithm computation time, and the digital pulsewidth modulator (DPWM). Typically, the delay introduced by DPWMs has a more substantial impact than the preceding factors. While numerous approaches have been proposed to mitigate or eliminate such delays, multisampling stands out as one of the most commonly employed methods. However, recent innovative architectures, particularly those based on the asymmetric dual-edge (ADE) carrier, have demonstrated that digital pulsewidth modulation (PWM) with zero phase delay, or even positive phase gain, can be effectively implemented. This suggests the possibility of further enhancing dynamic performance by increasing the number of samples per cycle. Unfortunately, the potential benefits of multisampling may be compromised by the operating point dependence issues inherent in ADE-DPWM. This article introduces a comprehensive architecture and a conclusive design approach for multisampling ADE-DPWM, facilitating the harnessing of multisampling benefits without encountering operating point issues. The experimental verification includes assessments of small-signal responses and robustness against operating point variations. Additional experimental tests are conducted to emphasize the improved dynamic performance compared to state-of-the-art trailing-triangle edge carrier-based modulators.**

***Index Terms*—Asymmetric dual-edge (ADE) pulsewidth modulator, digital control, fast dynamic response, high frequency phase boost, multisampling.**

I. Introduction

DIGITAL controls have progressively replaced analog counterparts across various power electronics applications. This transition is driven by multiple factors, including enhanced safety and monitoring functionalities, resilience against parameter fluctuations and component degradation, greater versatility, and programmability. Furthermore, the essential components of digital architectures, such as microcontrollers and field programmable gate arrays (FPGAs), have become more rapid and cost-effective. These considerations, along with related factors, have spurred the widespread adoption of digital controls over analog ones in numerous industrial contexts [1]. In power electronics, a typical control system involves the regulation of voltages and currents of state variables (e.g., inductor currents, capacitor voltages). Such regulation necessitates closed-loop architectures, which invariably impact the stability properties of the overall system. For instance, in multiloop controllers with inner-current and outer-voltage controls, regulators are designed to ensure a specific *phase margin*. Generally, closed-loop properties are contingent on the operating point, value, and nature of the load. Analog systems struggle to guarantee high performance across large variations of these values unless one resorts to work arounds that significantly escalate system cost and complexity. In contrast, digital control systems are programmable and configurable, enabling the implementation of architectures that are challenging or even impossible to realize in the analog domain [2], [3], [4]. Analog controls, notably, persist in high-dynamic performance custom applications (e.g., state-of-the-art voltage regulation modules for graphics processing units (GPUs)/central processing units (CPUs) [5], [6], [7]). This persistence is primarily attributed to the aforementioned delays that can impede dynamic performances [8], [9], [10] or cause stability issues [11].

A common strategy to mitigate such delays includes the multisampling approach (i.e., increasing the number of samples per period). Double-sampling DPWMs based on trailing-triangle edge (TTE) carriers are prominent solutions. Higher oversampling factors introduce nonlinearities that impair controlled system operation. These phenomena concern [12], [13], [14], [15] the amplification of noise injected into the control system, zero-gain and infinite-gain zones, vertical crossings, double vertical crossings [16], etc. By changing the controlling architectures, additional strategies to enhance digital control performance can be exploited. Some remarkable solutions include hysteretic-based controls [17], [18], mixed-signal approaches [19], [20], and predictive controls [21], [22], [23], [24], [25]. These strategies, although leading to significant benefits in appropriate contexts, do not solve the delay issues and require deep changes in the architecture with respect to the pulsewidth modulator-based control system. Furthermore, in many applications, due to strict noise requirements, costs, implementation issues, or simply mere conventions, these strategies cannot be adopted, and PWM-based controls still represent one of the most

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common solutions. Thus, the field of research concerning novel PWM architectures is still relevant today.

Recent publications [26], [27], [28] have shifted the traditional perspective on DPWM-based control systems. Indeed, they introduced *fully-digital* PWM systems with either *zero phase delay* or *positive phase gain*. To better understand the operating principle of the developed modulator, consider the naturally sampled PWM (NS-PWM) proposed in [29] as a starting point. This analog PWM introduces an additional degree of freedom compared to conventional PWMs: the modulating period is dynamically changed during transients, and this variation is exploited to create small-signal behavior similar to that of a derivative action. A similar NS-PWM based on this operation is presented in [30]. In [31], a hysteretic modulator based on the current ripple synthesis is proposed and analyzed. The architectures in [29], [30], and [31] are somewhat close in terms of dynamic performance improvement. Based on the properties of such analog systems, enhanced *digital* pulsewidth modulators have been recently introduced.

The developed architecture proposed in this article significantly advances digital control strategies in power electronics by enhancing our theoretical understanding of *variable-frequency* digital PWM and offering practical solutions for implementation challenges. The key contributions and the article's organization are summarized as follows.

1) A comprehensive comparison of the proposed *multisampling* ADE-DPWM and the state-of-the-art trailing-triangle-edge carrier-based DPWM (TTE-DPWM). This comparison, detailed in Section II, helps to identify the ADE-DPWM benefits, clarifying the reasons behind the achieved improvements.
2) The study introduces an improved multisampling architecture building upon prior work [26], [27], [28]. The final *multisampling* architecture presented in Section III addresses operating point issues while maintaining phase gain improvement as the oversampling factor increases.
3) Another contribution of this work is the generalized small-signal model, detailed in Section IV. This model, based on the *DF* method, provides precise insights into the ADE-DPWM behavior across all operating points. The model of the final architecture facilitates accurate predictions under varying conditions, guiding design, and tuning processes effectively.
4) An essential contribution comes from the sensitivity-study approach to designing the system parameters. This approach enhances adaptability to varying operational conditions and bridges theoretical understanding with practical application, revealing the complex parameter interactions influencing system behavior.
5) The article includes extensive experimental validation of the small-signal transfer function. To this end, Section V collects more than 1000 experimental tests. This article delves into an entire family of DPWM architectures with limitless applications. To showcase the potential of the final structure, two notable examples are discussed. The first example maximizes phase advance by essentially eliminating the need to incorporate derivative actions in the control chain for the relevant target applications. The second example pertains to a digital modulator that competes admirably with the high-performance *purely* analog NS-PWM proposed in [29].
6) Laboratory assessments encompass two prevalent scenarios employing DPWM systems. Those tests are discussed in Section VI. Such laboratory experiments directly compare the developed architectures against the state-of-the-art trailing triangle-edge carrier-based DPWM. The final results distinctly demonstrate the enhanced dynamic response capabilities of the developed systems.

II. ADE DPWM vs State-of-The-Art Trailing-Triangle-Edge DPWM

This manuscript proposes a *multisampling* DPWM architecture based on the *ADE* carrier that eliminates typical delays found in traditional structures. To provide readers with an understanding of the fundamental operation of the ADE carrier-based modulator and its key differences with respect to the state-of-the-art TTE carrier-based DPWM, this article starts with a direct comparison. This outlines the basic functioning of the ADE-DPWM and highlights its primary distinctions from the leading DPWM method, the TTE-DPWM. This scenario necessarily encompasses two or more samples per modulation cycle. Indeed, as proved in [26], the *single-sampling* ADE-DPWM yields a pulsewidth modulator with a fixed sampling period, introducing a delay similar to the conventional TTE-based methodologies. The advantages of the ADE-DPWM become evident when considering two or more samples per modulation cycle, resulting in DPWM with either *zero delay* or with *positive phase delay*.

Fig. 1(a) compares the operation of the state-of-the-art *double-sampling* TTE-DPWM and the *double-sampling* ADE-DPWM. The y-axis is normalized with respect to the available full-scale range and therefore TTEC and ADEC values $\in [0, 1]$. The main differences between the two architectures can be summarized as follows. When the modulating signal increases (i.e., the difference between the current and previous samples is positive), DPWM systems react by increases the ON-phase while decreasing the OFF-phase. In TTE-DPWM, once fixed $d[i] = \frac{T_{\text{on-TTE}}[i]}{T_s}$, the OFF-phase is imposed by the relation $T_{\text{on-TTE}}[i] + T_{\text{off-TTE}}[i] = T_s = \text{constant}$. On the other hand, in ADE-DPWM one obtains independent changes in both ON and OFFphases. With a positive variation of the modulating signal, the modulation period decreases (i.e., $T_s[i] < T_s$), and therefore $x_{on}[i] = \frac{T_{\text{on-ADE}}[i]}{T_s[i]} > \frac{T_{\text{on-ADE}}[i]}{T_s}$. Furthermore, as shown in Fig. 1(a), $T_{\text{on-ADE}}[i] > T_{\text{on-TTE}}[i]$ and therefore $x_{on}[i] > d[i]$. Having reduced the modulation period, one also obtains $T_{\text{off-ADE}}[i] = T_{\text{s-ADE}}[i] - T_{\text{on-ADE}}[i] < T_s - T_{\text{on-TTE}}[i]$. Similar considerations hold for negative variations in the modulating signal. Thus, for the same modulating signal variation, the ADE-DPWM reacts with more pronounced and *independent* variations of ON and OFFphases with respect to the state-of-the-art TTE-DPWM.

This qualitative analysis can be proved analytically. Indeed, from Fig. 1(a), one has

$$\text{ADE-DPWM} \rightarrow \begin{cases} \Delta x_{on}[i] & = \Delta M_{on}[i] \\ \Delta x_{off}[i] & = -\Delta M_{off}[i] \\ \Delta x_{s_{ADE}}[i] & = \Delta x_{on}[i] + \Delta x_{off}[i] \end{cases} \tag{1}$$

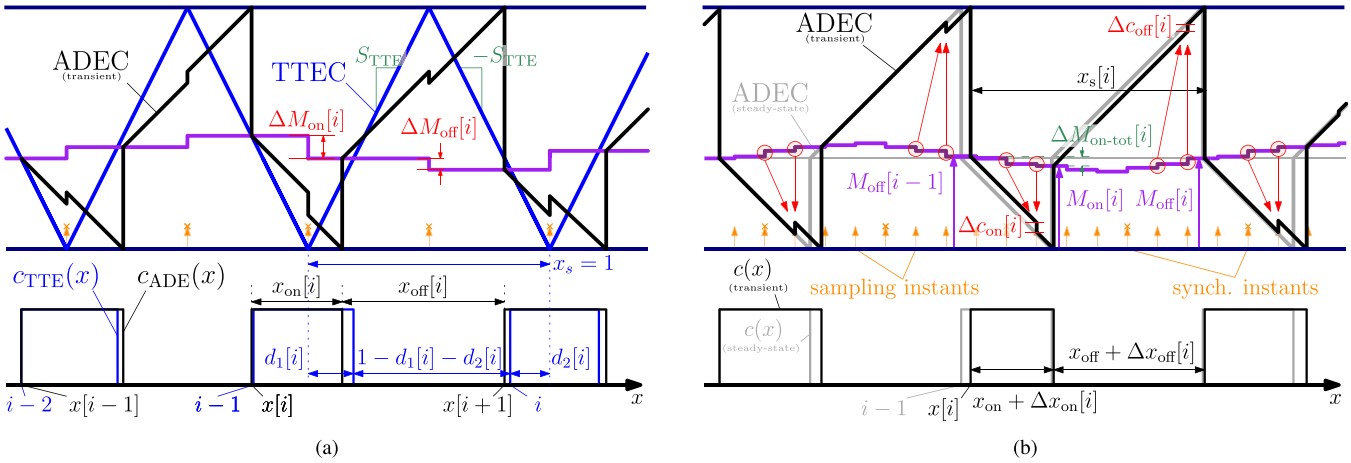


Fig. 1. (a) Exemplified time operation of (blue lines) TTEC and (black lines) ADEC-based *double-sampling* DPWMs and corresponding control signals (bottom). (b) Exemplified time operation of the *multisampling* ADE-DPWM for $N_{\text{smpl}} = 8$. Gray lines represent the steady-state operation.

$$\text{TTE-DPWM} \rightarrow \begin{cases} \Delta d[i] & = \frac{\Delta M_{\text{on}}[i] + \Delta M_{\text{off}}[i]}{2} \\ \Delta d'[i] & = -\frac{\Delta M_{\text{on}}[i] + \Delta M_{\text{off}}[i]}{2} \\ \Delta x_{\text{s}_{\text{TTE}}}[i] & = 0. \end{cases} \tag{2}$$

with

$$\Delta x_{\text{s}_{\text{ADE}}}[i] \triangleq \frac{T_{\text{s}_{\text{ADE}}}[i] - T_{\text{s}}}{T_{\text{s}}}, \quad \Delta x_{\text{s}_{\text{TTE}}}[i] \triangleq \frac{T_{\text{s}_{\text{TTE}}}[i] - T_{\text{s}}}{T_{\text{s}}} \tag{3}$$

while $\Delta d[i]$ and $\Delta d'[i]$ are the normalized variation of the ON and OFFphases for the TTE-DPWM.

Expressions in (1) can be founded in [26] or, in a more general form, in [27]. The expression for the TTE-DPWM can be obtained as follows. For the ith modulating cycle, $\Delta d[i]$ is defined as the difference between the current duty cycle (i.e., $d[i]$) and the steady-state one (i.e., D). Therefore, one has $\Delta d[i] = d[i] - D$. In Fig. 1(a), $d[i]$ is divided in two parts

$$d[i] = d_1[i] + d_2[i]. \tag{4}$$

By naming the TTE carrier slope as S_{TTE}, however D is chosen, one obtains

$$\begin{aligned} d_1[i] &= \Delta M_{\text{on}}[i]/S_{\text{TTE}} \\ d_2[i] &= \Delta M_{\text{off}}[i]/S_{\text{TTE}}. \end{aligned} \tag{5}$$

By defining $d'[i] \triangleq 1 - d[i]$ one immediately obtains

$$\Delta d'[i] = -\Delta d[i]. \tag{6}$$

Please note that, with the chosen normalization one has $S_{\text{TTE}} = 2$. Using this in (5) and (6) and substituting (4) one obtains (2). Comparing (1) and (2) reveals that in the ADE-DPWM, changes in ON and OFF phases are directly proportional to the difference between the current and previous samples. Precisely, these changes correspond to the *discrete derivative* of the modulating signal. Conversely, in TTE-DPWM, due to the relationship between the ON and OFF phase duration (i.e., $T_{\text{on-TTE}} + T_{\text{off-TTE}} = T_{\text{s}} = \text{constant}$), the TTE modulator cannot achieve this. Understanding and leveraging these differences is paramount for optimizing digital control strategies and enhancing the performance of power electronics systems.

III. Multisampling Asymmetric Dual-Edge DPWM

Once the operation of the *double-sampling* ADE-DPWM is clarified, the analysis of the modulator is conducted when the number of samples, denoted as N_{smpl}, exceeds two. These cases are studied separately due to the absence of the operating point dependency of the *double-sampling* ADE-DPWM, while the *multisampling* version with $N_{\text{smpl}} > 2$ demonstrates notable operating-point dependency. Indeed, in the worst-case scenario, its transfer function introduces zero phase-delay, akin to the *double-sampling* version, thereby nullifying the contributions of additional samples. This consideration has motivated the contribution submitted in [28] in which an ADE carrier-based modulator with $N_{\text{smpl}} = 4$ is analyzed and the current manuscript that introduces the final *multisampling* ADE-DPWM architecture and a design procedure valid for generic values of N_{smpl}.

Fig. 1(b) exemplifies the transient operation of the *multisampling* ADE-DPWM proposed in [28] for $N_{\text{smpl}} = 8$. The multisampling factor is formally defined as $N_{\text{smpl}} \triangleq f_{\text{smpl}}/f_s$, where f_{smpl} and f_{s} are the sampling and the switching frequencies, respectively. Please note that time axes in Fig. 1 are normalized with respect to the steady-state switching period (i.e., $x = t/T_{\text{s}}$).

The difference between DPWMs in [28] and [26] lies in the use of the acquired samples. Indeed, the architecture proposed in [28] uses the information coming from the *last* and but also from the *second to last* sample to mitigate the operating point dependence. Those values are furthermore multiplied by the *weight function* $f_p(M)$.

For the ith modulating cycle, the variations of ON and OFF phases can be defined as the difference with respect to their steady state values x_{on} and x_{off}, i.e.,

$$\begin{aligned} \Delta x_{\text{on}}[i] &\triangleq x_{\text{on}}[i] - x_{\text{on}} \\ \Delta x_{\text{off}}[i] &\triangleq x_{\text{off}}[i] - x_{\text{off}}. \end{aligned} \tag{7}$$

For the architecture proposed in [28], those variation can be written as follows:

$$\Delta x_{\text{on}}[i] = \Delta M_{\text{on-tot}}[i] + f_p(M)\left(M_{\text{on-}\nu_{\text{n}}}[i] - M_{\text{on-}\nu_{\text{n}}-1}[i]\right)$$

$$-\Delta x_{\text{off}}[i] = \Delta M_{\text{off-tot}}[i] + f_p(M)\left(M_{\text{off-}\nu_\text{f}}[i] - M_{\text{off-}\nu_\text{f}-1}[i]\right). \tag{8}$$

The integers ν_n and ν_f represent the number of samples acquired during the ON and the OFF phases, respectively.[1] The quantities $M_{\text{on-}\nu_\text{n}}[i]$ and $M_{\text{off-}\nu_\text{f}}[i]$ are the last samples acquired during the ON and OFF phases and $\Delta M_{\text{on-tot}}[i]$ and $\Delta M_{\text{off-tot}}[i]$ represent the overall modulating signal variations during the ith ON and OFF phases, respectively. The latter, can be expressed as follows:

$$\begin{aligned}\Delta M_{\text{on-tot}}[i] &\triangleq \Delta M_{\text{off}}[i-1] + \sum_{\tau=1}^{\nu_\text{n}} \Delta m_\tau[i] \\ \Delta M_{\text{off-tot}}[i] &\triangleq \Delta M_{\text{on}}[i] + \sum_{\tau=\nu_\text{n}+1}^{N_\text{smpl}} \Delta m_\tau[i],\end{aligned} \tag{9}$$

where $\Delta m_\tau[i]$ is the τth variation of the modulating signal during the ith cycle.

The time-domain evolution described by (8), is now modified to obtain an enhanced *multisampling* ADE-DPWM architecture capable of improving the dynamic performances further reducing the operating point dependence. This facilitates an efficient and comprehensive design of ADE-DPWM modulators, enabling the near-complete elimination or substantial reduction of operational point dependency while keeping the advantages coming from the multisampling approach. The following paragraph summarizes the underlying motivation for this contribution.

A. Problem Statement and Proposed Solution

The solution presented in [28] addresses the operating point issue in *multisampling* ADE-DPWM for $N_\text{smpl} = 4$. Nevertheless, the ultimate dynamic performances do not deviate significantly from those provided by the adapted *double-sampling* architecture proposed in [27]. This is primarily because the proposed modification aims to minimize the variation concerning the operating point, with no substantial impact on the final small-signal phase gain. Moreover, when $N_\text{smpl} \geq 8$, the dependence on the operating point becomes more pronounced, irrespective of the chosen *weight functions*, while the associated benefits in terms of phase gain become increasingly marginal.

The proposed solution comes from the following basic idea. In dual-edge analog NS-PWM, the modulating signal is *sampled* at the beginning and at the end of the ON (or OFF) phase. In other words, at the points where the modulating signal intersects the carrier. In ADE-DPWM modulators already present in literature, the modulating signal variation responsible for modulating the rising and falling edges of the control signal $c(x)$ is the last one the system registers in each phase, as shown in Fig. 1(b). The solution to the problem of operating point dependency or lack of performance increase is solved in this article by using the two types of sampling. In fact, the equation of the time evolution of the control signal (i.e., (8)) is modified by introducing two additional terms representing the variation of the modulating signal across an entire ON-phase (or OFF-phase). For very large oversampling factors, these samples approximate those that an analog modulator would acquire. This insight forms the basis idea of the modifications introduced in (8) and which represent the final version of the *multisampling* ADE-DPWM architecture proposed in this manuscript.

Thus the final architecture must includes two additional terms proportional to the difference between the first sample acquired in the current phase (i.e., ON or OFF phases) and the one acquired at the end of the previous phase (i.e., previous OFF or ON phases).

In accordance with this intuition, using two further *generic* weight functions depending on the operating point (i.e, $k_\text{sn}(M)$ and $k_\text{sf}(M)$), (8) is therefore modified as follows:

$$\begin{aligned}\Delta x_{\text{on}}[i] = {} & \Delta M_{\text{on-tot}}[i] + f_p(M)\left(M_{\text{on}}[i] - M_{\text{on-}\nu_\text{n}-1}[i]\right) + \\ & + k_\text{sn}(M)\left(M_{\text{on}}[i] - M_{\text{off}}[i-1]\right) \\ -\Delta x_{\text{off}}[i] = {} & \Delta M_{\text{off-tot}}[i] + f_p(M)\left(M_{\text{off}}[i] - M_{\text{off}\nu_\text{f}-1}[i]\right) + \\ & + k_\text{sf}(M)\left(M_{\text{off}}[i] - M_{\text{on}}[i]\right).\end{aligned} \tag{10}$$

It is crucial to emphasize that the architecture identified by (10) is entirely generic. The fundamental concept involves the introduction of *two additional parameters* into the system, facilitating a more precise and accurate modification of the frequency response. However, it is important to note that the inclusion of these two terms is not arbitrary. Upon analyzing the frequency behavior of the individual variations in the modulating signal outlined in (8), it becomes evident that their trends do not undergo drastic alterations with increasing distances between collected samples. By incorporating terms with analogous trends and appropriately weighting the various contributions, it becomes feasible to achieve operative point-independent behavior while optimizing the system's dynamic performance. This is simply not attainable with the architecture introduced in [28], as the weight function $f_p(M)$ is designed to mitigate dependence on the operating point, and there are no additional parameters to act upon.

Clearly, the effectiveness of these modifications remains uncertain. It becomes imperative to compute the *new* small-signal model for the proposed architecture outlined in (10). Subsequently, through careful selection of the generic functions $k_\text{sn}(M)$ and $k_\text{sf}(M)$, it can be determined whether the desired objectives are attainable. Although the small-signal model is very complex to study, since the functions involved are only dependent on M, it is possible to derive the transfer function by reusing the expressions derived in [27] and [28].

Fig. 2(b) summarizes the evolution of *multisampling* ADE-DPWM architectures. As is made clear later in the manuscript, this generic architecture makes it possible to solve the problem of the operating point dependency, but also to increase the performance of the modulator as the oversampling factor increases.

IV. Small-Signal Analysis

The describing function (DF) method is used to derive the small signal model of the proposed DPWM architecture. On this purpose, a small-sinusoidal perturbation $\hat{u}(x)$ is superimposed to a constant modulating signal value M at the modulator's input,

[1] Therefore, one has $\nu_\text{n} + \nu_\text{f} = N_\text{smpl}$.

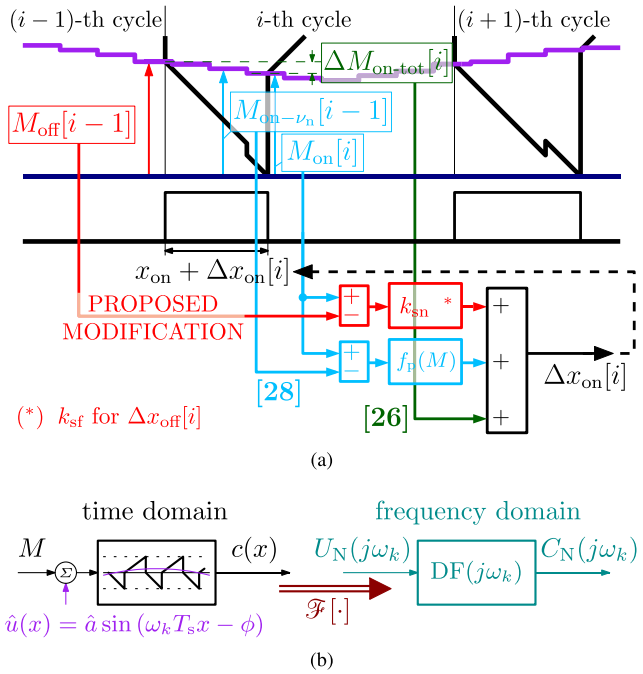


Fig. 2. (a) Evolution of *multisampling* ADE-DPWM architectures. The green patch represents the structure in [26], the light-blue path the modification introduced in [28]. The red one represents the additional path proposed in this manuscript. (b) Graphical representation and notation for the small signal analysis of the ADE-DPWM.

i.e., $M(x)=M+\hat{u}(x)$ with

$$\hat{u}(x)=\hat{a}\sin(\omega_k T_s x-\phi)\,,\quad(\hat{a}\ll M)\,. \tag{11}$$

Fig. 2(a) summarizes the input and output configuration while introducing the corresponding notation in the frequency domain. The symbol $\mathscr{F}[\cdot]$ denotes the Fourier Transform operator.

According with this representation, the small signal model of the proposed DPWM architecture is obtained by computing the ratio between the Fourier Transform of the modulator's output and input signals (i.e., respectively $C_{\text{N}}(j\omega_k)$ and $U_{\text{N}}(j\omega_k)$) evaluated at the perturbation frequency ω_k [i.e., $\text{DF}(j\omega_k)\triangleq C_{\text{N}}(j\omega_k)/U_{\text{N}}(j\omega_k)$].

The explicit calculation of the Fourier Transform of $c(x)$ corresponding to the perturbed steady-state in quite long and complex but can be avoided by using the main results of the frequency analysis proposed in [27] and [28]. Indeed, regardless their explicit expressions, the generic functions $k_{\text{sn}}(M)$ and $k_{\text{sf}}(M)$ depend only on the operating point and can be treated as constants in the computation of the frequency response.[2] Thus, the small-signal transfer function of the proposed *multisampling* ADE-DPWM architecture can be written as follows:

$$\text{DF}(s)=\frac{D_{\text{n}}(s)-D_{\text{f}}(s)}{1-e^{sT_s}}(1-e^{-sT_s x_{\text{on}}})+\ D_{\text{n}}(s)e^{-sT_s x_{\text{on}}} \tag{12}$$

[2]The analytical derivation is omitted because it is long and complex. It also offers no interesting insights with respect to the objectives of this manuscript.

where $D_{\text{n}}(s)$ and $D_{\text{f}}(s)$ are defined as follows:

$$\begin{aligned}
D_{\text{n}}(s)\ \triangleq\ & e^{sT_s\left(\frac{x_{\text{on}}}{2}+\frac{\nu_{\text{n}}-1}{2N}\right)}+\\
&+f_p\left(e^{s\frac{T_{\text{smpl}}}{2}}-e^{-s\frac{T_{\text{smpl}}}{2}}\right)e^{sT_s\left(\frac{x_{\text{on}}}{2}+\frac{\nu_{\text{n}}-2}{2N}\right)}+\\
&+k_{\text{sn}}\left(e^{s\frac{T_{\text{smpl}}}{2}\frac{N+\nu_{\text{n}}-\nu_{\text{f}}}{2}}-e^{-s\frac{T_{\text{smpl}}}{2}\frac{N+\nu_{\text{n}}-\nu_{\text{f}}}{2}}\right)e^{sT_s\left(\frac{x_{\text{on}}}{2}-\frac{1}{2N}\right)}
\end{aligned} \tag{13}$$

$$\begin{aligned}
D_{\text{f}}(s)\ \triangleq\ & e^{sT_s\left(1-\frac{x_{\text{off}}}{2}+\frac{\nu_{\text{f}}-1}{2N}\right)}+\\
&+f_p\left(e^{s\frac{T_{\text{smpl}}}{2}}-e^{-s\frac{T_{\text{smpl}}}{2}}\right)e^{sT_s\left(1-\frac{x_{\text{off}}}{2}+\frac{\nu_{\text{f}}-2}{2N}\right)}+\\
&+k_{\text{sf}}\left(e^{s\frac{T_{\text{smpl}}}{2}\frac{N+\nu_{\text{f}}-\nu_{\text{n}}}{2}}-e^{-s\frac{T_{\text{smpl}}}{2}\frac{N+\nu_{\text{f}}-\nu_{\text{n}}}{2}}\right)e^{sT_s\left(1-\frac{x_{\text{off}}}{2}-\frac{1}{2N}\right)}.
\end{aligned} \tag{14}$$

The first terms of $D_{\text{n}}(s)$ and $D_{\text{f}}(s)$ constitute the *multisampling* ADE-DPWM architecture disclosed in [26]; adding the terms multiplied by $f_p(M)$, one obtains the architecture in [28]. Finally, the with the terms multiplied by the generic functions $k_{\text{sn}}(M)$ and $k_{\text{sf}}(M)$ one has the *final* architecture proposed in this manuscript.

A. Operative Design

The design procedure is detailed by using two remarkable examples. In the first one is assumed to maximize phase gain around $f_s/2$ and reduce operating point dependence as much as possible. In the second example, a small-signal transfer function that maximize the phase gain around f_s while maintaining flat the gain curve is obtained. The purpose of this procedure is clearly to individuate proper shapes of the generic functions $k_{\text{sn}}(M)$ and $k_{\text{sf}}(M)$ in a way that satisfies these objectives. Proper weight functions lead to a small-signal behaviors that are, respectively, identified by $\text{DF}_d(s)$ and $\text{DF}_a(s)$. As mentioned earlier, these are just two examples. Indeed, the proposed general multisampling architecture allows the designing of ADE-DPWM with different frequency responses.

The main analytical tool involved in this procedure is the *sensitive function* defined as follows:

$$S_{\text{DF}(j\omega_x)/M}=\frac{\partial\text{DF}(j\omega_x)}{\text{DF}(j\omega_x)}\Big/\frac{\partial M}{M}. \tag{15}$$

Fig. 3 shows the sensitivity versus $M\in(\frac{2}{8},\frac{4}{8})$ of (12), respectively, for $f_p(M)=k_{\text{sn}}(M)=k_{\text{sf}}(M)=0$ (that results in the architecture developed in [26]) and $f_p(M)=\frac{1}{2}+|M-\frac{1}{2}|$ and $k_{\text{sn}}(M)=k_{\text{sf}}(M)=0$ (that results in the architecture developed in [28]). These transfer functions are referred to as $\text{DF}_1(s)$ and $\text{DF}_{\text{mod1}}(s)$, respectively.

The curves in Fig. 3 are obtained by imposing $\omega_x=2\pi f_s/2$. In the range of frequencies of interest, this specific value is chosen because it is the one for which the dependence on the operating point is most pronounced. The sensitivity functions corresponding to $\text{DF}_1(s)$ and $\text{DF}_{\text{mod1}}(s)$ are indicated as $S_1(M)\triangleq S_{\text{DF}_1(j\omega_x)/M}$ and $S_m(M)\triangleq S_{\text{DF}_{\text{mod1}}(j\omega_x)/M}$.

From Fig. 3 is immediate to observe that the use of the weight function $f_p(M)$ strongly reduces the operating point dependence of the *multisampling* ADE-DPWM. However, this

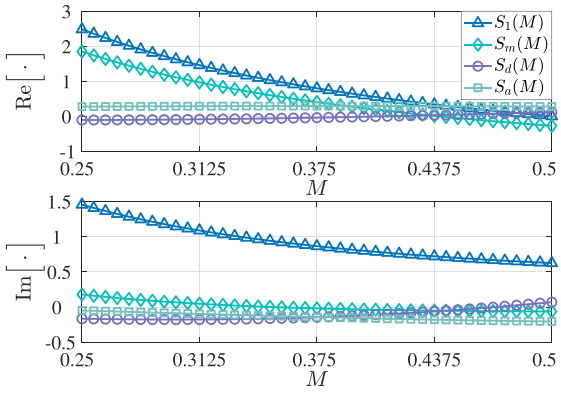


Fig. 3. Real and imaginary part of $S_1(M)$, $S_m(M)$, $S_d(M)$ and $S_a(M)$ for $\omega_x = 2\pi f_s/2$ and $M \in (\frac{2}{8}, \frac{4}{8})$.

strategy fails when higher values of the oversampling factor are considered. The following proves that using appropriate values for $k_{\text{sn}}(M)$ and $k_{\text{sf}}(M)$, better results can be obtained especially for $N_{\text{smpl}} > 4$.

As stated at the beginning of this section, to showcase the effectiveness of the proposed methodology and underscore the properties of the proposed multisampling architecture, two noteworthy implementation examples are analyzed: the *derivative* and the *simil-analog* ADE-DPWMs, respectively, individuated by $\text{DF}_d(s)$ and $\text{DF}_a(s)$. These use, respectively, the following set of parameters:

$$\begin{aligned} f_{P1}(M) &= c_1 M^2 - c_2 M + c_3, \quad k_{\text{sn}} = 1.5, \quad k_{\text{sf}} = 1.5 \\ f_{P2}(M) &= c_4 + c_5 \left| M - \frac{1}{2} \right|, \quad k_{\text{sn}} = -1.5, \quad k_{\text{sf}} = 0.4. \end{aligned} \tag{16}$$

with $c_1 = c_2 = 28$, $c_3 = 8$, $c_4 = 4$ and $c_5 = 1/c_4$.

The corresponding sensitivity functions evaluated for $\omega_x = 2\pi f_s/2$ are indicated with $S_d(M) \triangleq S_{\text{DF}_d(j\omega_x)/M}$ and $S_a(M) \triangleq S_{\text{DF}_a(j\omega_x)/M}$. The plots in Fig. 3 show that $S_d(M)$ and $S_a(M)$ are always smaller than $S_{\text{mod1}}(M)$. This analysis must be repeated for all operational points. To simplify the approach one can divide the operating point range into a finite number of intervals and perform the sensitivity analysis only for points in the middle of these intervals.

In summary, the operating procedure is as follows.

1) In accordance with the theory developed in [28] one choose the weight function $f_p(M)$ [i.e., $f_{P1}(M)$ or $f_{P2}(M)$].
2) The operating point range $M \in [M_{\text{min}}, M_{\text{max}}] \in [0, 1]$ is divided in K subintervals (i.e., $[M_{\text{min}}, M_{\text{max}}] = [M_0, M_1] \cup [M_1, M_2] \cup \ldots [M_{\text{K-1}}, M_{\text{K}}]$). For each subinterval one choose its midpoint $M_{m\text{-i}} = \frac{M_{\text{i}} + M_{\text{i-1}}}{2}$.
3) In the range of interest, the frequency f_x at which the dependence on the operating point is more pronounced must be identified.
4) The sensitivity analysis is therefore performed at the frequency f_x, around to all K operating points $M_{m\text{-i}}$, $i = 1, 2, \ldots \text{K}$.
5) For each subinterval, the values $k_{\text{sn}}(M_{m\text{-i}})$ and $k_{\text{sf}}(M_{m\text{-i}})$ are chosen in order to achieve a specific goal (e.g., maximize phase gain around f_x while maintaining a weak operative point dependence).
6) When $k_{\text{sn}}(M_{m\text{-i}})$ and $k_{\text{sf}}(M_{m\text{-i}})$ vary slightly, one can approximate them with constant values. Alternatively, one can use simple functions with a symmetrical shape with respect to the operating point $M = \frac{1}{2}$.[3]

B. Discussion

The Bode plots of $\text{DF}_1(s)$ and $\text{DF}_{\text{mod1}}(s)$ are reported in Fig. 4(a) and (b). The dependence on the operating point is very pronounced for $\text{DF}_1(s)$, confirming the trend of $S_1(M)$ in Fig. 3. One can also notice that for $N_{\text{smpl}} = 8$ the operating point dependence is noticeable also for $\text{DF}_{\text{mod1}}(s)$.

The transfer function in Fig. 4(c) is designed to guarantee high phase-boost around $\omega_x = 2\pi f_s/2$. The resulting small-signal behavior is similar to a discrete derivative action. Compared to $\text{DF}_{\text{mod1}}(s)$, the phase boost is more pronounced and the dependence on the operating point almost completely eliminated.

The architecture described by $\text{DF}_a(s)$, shown in Fig. 4(d), is designed to have a flatter response up to the switching frequency similar to the analog NS-PWM proposed in [29]. This is an outstanding result not only because the operating point dependence is almost completely eliminated, but also considering that an analog modulator is compared to a digital one which provides similar performance in terms of phase delay and frequency response modulus.

C. Consideration on the Physical Realization

This section provides the basic description of the hardware operations required to implement the proposed architecture. Even if $k_{\text{sn}}(M)$ e $k_{\text{sf}}(M)$ may be constants, in this section having to consider the maximum architecture complexity, the two terms are supposed functions of the operating point. The expressions in (10) describe the time domain evolution of the control signal $c(x)$ (i.e., the modulator's output). In the physical implementation, these can be rearranged in order to minimize the architecture's complexity. A first, intuitive choice is obtained by rearranging the terms in (9).

Using Fig. 1(b) as a reference, the term $\Delta M_{\text{on-tot}}[i]$ in (9) can be rewritten as follows:

$$\Delta M_{\text{on-tot}}[i] = \Delta M_{\text{off}}[i-1] - \Delta M_{\text{on}}[i]. \tag{17}$$

Using (17) in the first equations of (10), for $\Delta x_{\text{on}}[i]$ one has

$$\begin{aligned} \Delta x_{\text{on}}[i] = {} & \Delta M_{\text{off}}[i-1] - \Delta M_{\text{on}}[i] \\ & + f_p(M)\left(+M - M + M_{\text{on}}[i] - M_{\text{on-}\nu_{\text{n}}-1}[i]\right) \\ & + k_{\text{sn}}(M)\left(+M - M + M_{\text{on}}[i] - M_{\text{off}}[i-1]\right) \\ = {} & \Delta M_{\text{off}}[i-1]\left(1 - k_{\text{sn}}(M)\right) - \Delta M_{\text{on}}[i]\left(1 - k_{\text{sn}}(M)\right) \\ & + f_p(M)\left(\Delta M_{\text{on}}[i] - \Delta M_{\text{on-}\nu_{\text{n}}-1}[i]\right) \end{aligned}$$

[3] As emphasized in the section and as proved in [26] the dependence on the operating point is symmetrical with respect to this value.

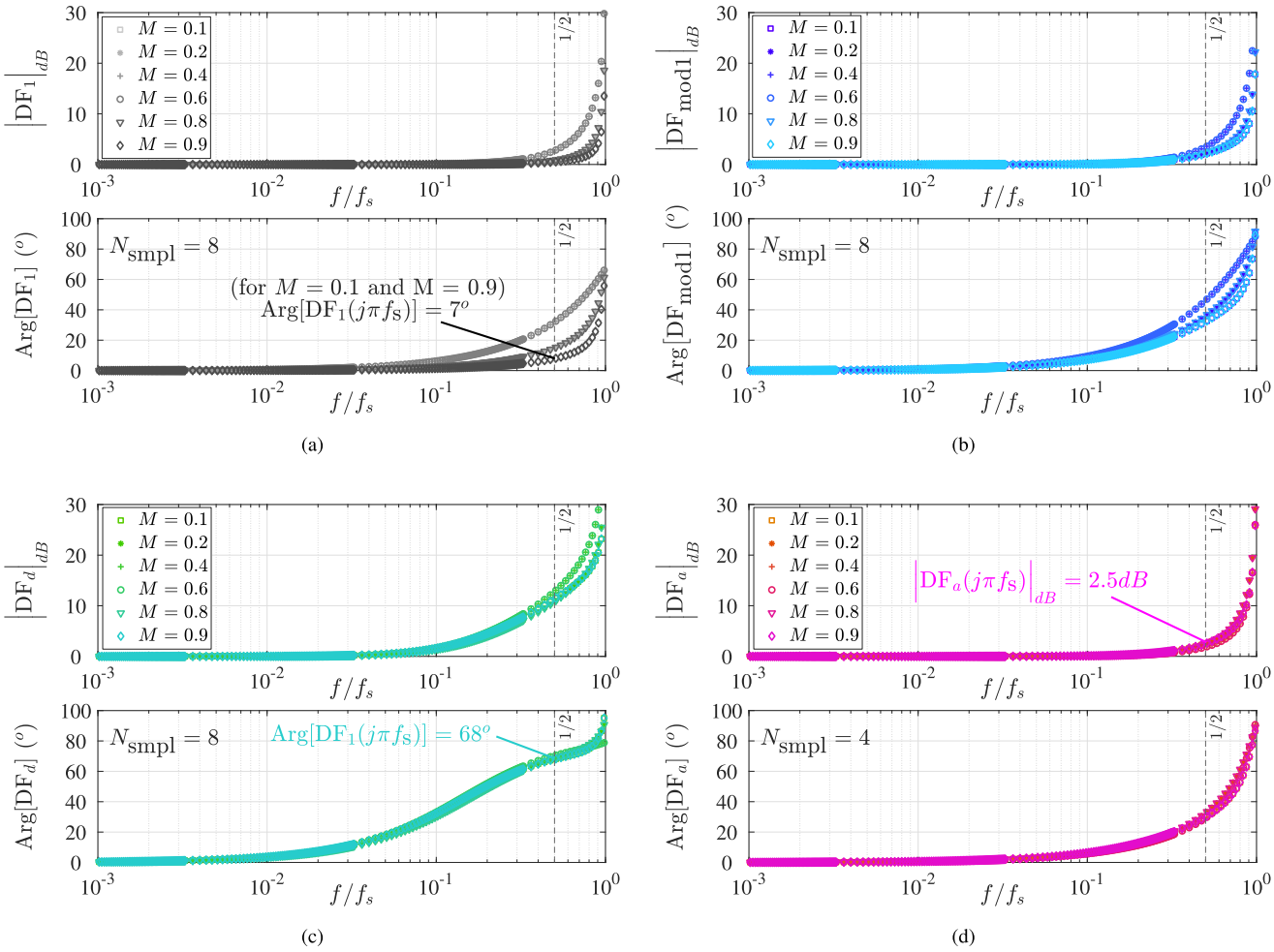


Fig. 4. Bode plot of the analytical small-signal models of (a) $\mathrm{DF}_1(s)$ and (b) $\mathrm{DF}_{\mathrm{mod1}}(s)$ proposed, respectively, in [26] and [28] for $N_{\mathrm{smpl}} = 8$, and Bode plot of (c) $\mathrm{DF}_d(s)$ ($N_{\mathrm{smpl}} = 8$) and (d) $\mathrm{DF}_a(s)$ ($N_{\mathrm{smpl}} = 4$).

$$= \underbrace{(\Delta M_{\mathrm{off}}[i-1] - \Delta M_{\mathrm{on}}[i])\,(1 - k_{\mathrm{sn}}(M))}_{\text{term 1}} + \underbrace{(\Delta M_{\mathrm{on}}[i] - \Delta M_{\text{on-}\nu_{\mathrm{n}}-1}[i])\,f_p(M)}_{\text{term 2}}. \tag{18}$$

In (18) one can individuate two modulating signal variations and two functions used to weigh them. Precisely, *term 1* in (18) represents the change in the modulating signal throughout the whole *on-phase* while *term 2* the variation calculated between the last and second-to-last samples acquired. For brevity, these contributions may be generically referred to as $\Delta M_{\text{on-L}}[i]$ and $\Delta M_{\text{on-S}}[i]$. By defining $k'_{\mathrm{sn}}(M) \triangleq 1 - k_{\mathrm{sn}}(M)$, (18) can be rewritten as follows:

$$\Delta x_{\mathrm{on}}[i] = \Delta M_{\text{on-L}}[i]\; k'_{\mathrm{sn}}(M) + \Delta M_{\text{on-S}}[i]\; f_p(M). \tag{19}$$

Using identical considerations one has

$$\Delta x_{\mathrm{off}}[i] = \Delta M_{\text{off-L}}[i]\; k'_{\mathrm{sf}}(M) + \Delta M_{\text{off-S}}[i]\; f_p(M). \tag{20}$$

Regardless the value of N_{smpl}, since $f_p(M)$, $k'_{\mathrm{sn}}(M)$ and $k'_{\mathrm{sf}}(M)$ are evaluated, to implement (19) and (20) six algebraic sums and four products are required.

All three functions $f_p(M)$, $k'_{\mathrm{sn}}(M)$, and $k'_{\mathrm{sf}}(M)$ exhibit, at most, a dependency on the operating point. In the practical applications addressed in this article, the control is aware of the operating point, and it undergoes variations at a slower rate than the switching/modulation period. Consequently, the values of $f_p(M)$, $k'_{\mathrm{sn}}(M)$, and $k'_{\mathrm{sf}}(M)$ can be treated as constants over multiple cycles. Importantly, their assessment remains unaffected by the oversampling factor. It is noteworthy to stress that when employing a quadratic $f_p(M)$ functions, the functions k_{sn} and k_{sf} can be reasonably approximated as constant values, thereby contributing to a reduction in system complexity.

As the oversampling factor changes, the primary factor subject to change is the frequency at which the calculation of the four terms in (19) and (20) is updated. Indeed, to ensure the proper functioning of the architecture, it is essential to update these four terms at each $T_{\mathrm{smpl}} = T_{\mathrm{s}}/N_{\mathrm{smpl}}$. However, the computations involved are relatively straightforward and can be implemented without difficulty in custom logic or systems utilizing FPGAs.

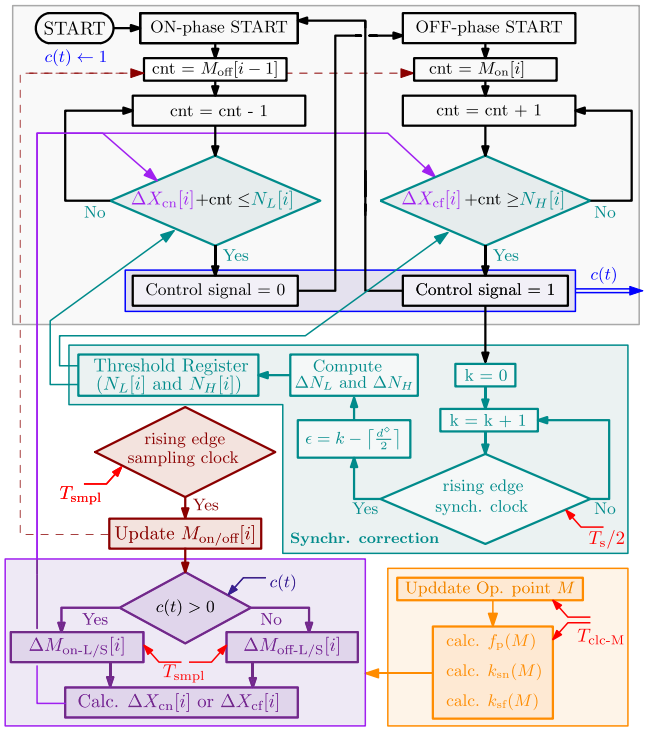


Fig. 5. Organization of the proposed *multisampling* ADE-DPWM architecture.

To better describe the complexity of the developed *multisampling* ADE-DPWM architecture, Fig. 5 reports a qualitative representation of its final implementation. The block in gray represent basic components that are required to build any DPWM (i.e., those components are required also to build the TTE-based DWPM). The block in dark-cyan represent the synchronism correction. The orange and the purple block represent the additional components required to implement the proposed architecture. In the counters on top of the diagram are used the following condition to determine the duration of the ON and OFF phases:

$$\begin{aligned} \Delta X_{\text{cn}}[i] + \text{cnt} &\leq N_{\text{L}}[i] \\ \Delta X_{\text{cf}}[i] + \text{cnt} &\geq N_{\text{H}}[i]. \end{aligned} \tag{21}$$

The terms $\Delta X_{\text{cn}}[i]$ and $\Delta X_{\text{cn}}[i]$ are used to generate the variations $\Delta x_{\text{on}}[i]$ and $\Delta x_{\text{off}}[i]$.[4] These additional variables are computed to the usual implementation of conventional DPWM (i.e., the variations in the *on* and *off* phases are determined by comparing the carrier values with the modulating signal). The ultimate equations for $\Delta X_{\text{cn}}[i]$ and $\Delta X_{\text{cf}}[i]$ exhibit equivalent computational complexity to the expressions provided in (19) and (20). The scaling coefficients employed in the hardware implementation depend on the resolution and numerical representation of the involved variables.

The synchronization mechanism used in the proposed architecture uses a slow correction to keep the center of ON and OFF phases of $c(x)$ synchronized with a specific clock signal. In Fig. 5, the synchronization clock is $T_{\text{synch}} = T_{\text{s}}/2$. This is coherent with the representation in Fig. 1(b) (where the synchronization instants are highlighted with $\times$). Hence, regardless of N_{smpl}, the synchronization error is computed concerning these instants. This aligns with a practical application scenario wherein those instants are generally used to sample the average inductor current (e.g., when the modulator is used within a digital average current-mode control for synchronous Buck converters). The operation of the synchronization mechanism is detailed in [26]. No changes are required to implement the final architecture discussed in this manuscript.

Finally, in the orange block, the calculation of the operating point M is assumed to be repeated every ν modulating cycles (i.e., $T_{\text{clc-M}} = \nu T_{\text{s}} = \nu N_{\text{smpl}} T_{\text{smpl}}$). Formulating a universally applicable strategy for this computation proves challenging without contextualizing it within the confines of a specific application. The description presented in Fig. 5 and discussed in this section is of a general nature. Customization and enhancements are advisable when tailoring the approach to a particular application.

For instance, one may start from an initial value, presuming that the register containing the operating point undergoes updates as samples related to changes in the modulating signal accumulate. Consequently, the update of that register could transpire at each T_{smpl}, following a phase (either ON or OFF), or even upon the culmination of an entire modulation cycle (i.e., $c(x) = 1 \to 0 \to 1$, at f_{s} rate). Another simple alternative is to calculate M by averaging the last $m \in \mathbb{N}$ acquired samples. The optimal strategy is contingent upon the specific requirements of the application and the desired performance.

D. Design of $k_{sn}(M)$, $k_{sf}(M)$, and $f_p(M)$

Fig. 4(a) shows the transfer function $\text{DF}_1(s)$ of the simplest *multisampling* ADE-DPWM architecture. This does not include any mechanism to compensate the operative point dependence. One can notice that the dependence on the operating point M is symmetrical with respect to $M = \frac{1}{2}$. Precisely one has $\text{DF}_1(s)\big|_{M=z} = \text{DF}_1(s)\big|_{M=1-z}$, $z \in [0, 1] \subset \mathbb{R}$.

Once the symmetry is known, one can manipulate the dynamic evolution of $c(x)$ by incorporating two supplementary components that, when appropriately weighted, can alleviate the operating point dependence. This is show on Fig. 4(b). In the frequency domain, the two additions (i.e., $f_p(M)(M_{\text{on}}[i] - M_{\text{on-}\nu_{\text{n}}-1}[i])$ and $f_p(M)(M_{\text{off}}[i] - M_{\text{off}\nu_{\text{f}}-1}[i])$) exhibit a comparable trajectory to the initial transfer function $\text{DF}_1(s)$. Therefore, through suitable weighting, it becomes feasible to nullify the operating point dependence by shaping $f_p(M)$. This holds for architectures characterized by low oversampling factors (i.e., $N_{\text{smpl}} \leq 4$). Nevertheless, the utilization of $f_p(M)$ does not afford an enhancement in dynamic performance with an increase in the oversampling factor. To fix this issue, the dynamic evolution of $c(x)$ is further modified by introducing the terms $k_{\text{sn}}(M)(M_{\text{on}}[i] - M_{\text{off}}[i-1])$ and $k_{\text{sf}}(M)(M_{\text{off}}[i] - M_{\text{on}}[i])$. These, can be used as additional knobs to reshape the modulator transfer function. To design those functions one can use the approach proposed at the end of Section IV-A.

[4] According to the representation on Fig. 5 $N_{\text{L}}[i]$ and $N_{\text{H}}[i]$ are the numerical values of the upper and lower thresholds used set and reset the carrier's counter.

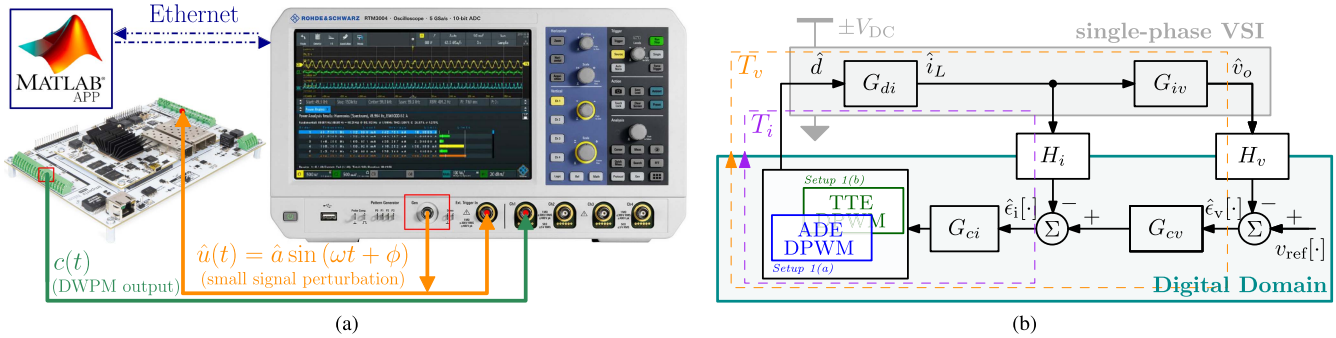


Fig. 6. (a) Experimental setup for the small-signal transfer function measurements. (b) Block diagram representation of the selected case-study.

In the examples discussed in Section IV-B, the functions $k_{sn}(M)$ and $k_{sf}(M)$ have been replaced by constant values. Evidently, this is not the sole conceivable approach. Indeed, as proved with the experimental tests reported in the next sections, nonconstant functions can be employed for $k_{sn}(M)$ and $k_{sf}(M)$. These functions, due to the symmetry mentioned of the modulator transfer function, must be selected from families that ensure symmetry with respect the operating point $M = \frac{1}{2}$.

Although the possibilities are infinite, for simplicity of implementation, only the following family of functions are taken into account:

$$k_{pw}(M) = \begin{cases} c_0 & \frac{1}{2} - \alpha < M < \frac{1}{2} + \alpha \\ c_1 + c_2 \left| M - \frac{1}{2} \right| & \text{elsewhere} \end{cases}. \tag{22}$$

In the following sections, $k_{pw}(M) = k_{sn}(M) = k_{sf}(M)$ is used to build an implementation of the proposed *multisampling* ADE-DPWM architecture. This approach avoids the use of quadratic functions for the weight function $f_p(M)$ contributing to lightening the final architecture's complexity.

V. Experimental Validation

The proposed architectures are extensively tested via MATLAB/Simulink simulation and experimentally. Experimental tests validated behavior matching perfectly the MATLAB/Simulink simulation and the theoretical curves. Therefore, only experimental results are presented to avoid redundancy.

Experimental measurements of the small-signal transfer functions are obtained by superimposing small sinusoidal perturbations to constant steady-state modulating signal values. Fig. 6 shows the organization of the experimental setup. The *multisampling* ADE-DPWM is coded in VHDL using the Imperix B Board Pro (BB-pro), equipped with a Xilinx XC7Z030-3FBG676E FPGA. The small sinusoidal perturbation $\hat{u}(t)$ is generated by the internal signal generator of the Rohde & Schwarz RTM3004 oscilloscope. This perturbation is then injected into the analog input of the BB-pro. The final modulating signal processed by the modulator is the numerical representation of $M(t) = M + \hat{u}(t) = M + \hat{a}\sin(\omega t + \phi)$, whit $\hat{a} \ll M$. The Fourier analysis of the modulator's output is done whit the RTM3004. The resultant data are transmitted via Ethernet to a PC and collected using a custom MATLAB app. This app also changes the value of the injected frequency once the previous measurement is completed.

To validate the developed small-signal transfer function models, the frequency responses for each operating point and each modulator are experimentally verified. In total 72 frequency values are employed for each operating point. Two distinct ADE-DPWM architectures are tested (i.e., the *simil-analog* ADE-DPWM with $N_{smpl} = 4$ and the *derivative* ADE-DPWM with $N_{smpl} = 8$). Seven operating points are tested for each architecture. Fig. 7 summarizes the results of $72 \times 2 \times 7 = 1008$ experimental tests.

For the *simil-analog* ADE-DPWM shown on Fig. 7(a), the parameter set in (16) is used. For the *derivative* ADE-DPWM shown on Fig. 7(b) the following parameters are adopted $[k(M) = k_{sn}(M) = k_{sf}(M)]$

$$f_p(M) = \frac{1}{3} + 3\left| M - \frac{1}{2} \right|$$

$$k(M) = \begin{cases} 0.5 & 0.4 < M < 0.6 \\ \frac{3}{11} + \frac{11}{4}\left| M - \frac{1}{2} \right| & \text{elsewhere.} \end{cases} \tag{23}$$

As mentioned in Section IV-D, instead of a quadratic $f_p(M)$ and constant values k_{sn} and k_{sf}, an equivalent solution with piecewise-linear functions for $f_p(M)$ and $k_{sn}(M) = k_{sf}(M)$ is used.

A. Discussion

The worst-case phase-variation of the *simil-analog* modulator is approximately $4°$, while for the derivative version, it is around $7.5°$. The phase degradation near to f_s is due to the synchronization mechanism. This mechanism is essential where synchronism between specific points of the inductor current (e.g., the point at which the average value is located) and specific points of the control signal (e.g., the midpoint of the $c(x)$ pulse) is necessary. Nonetheless, the performance of the developed modulators remains nearly unaffected up to $f \approx 0.8 f_s$.

It should be noted that such performance levels for digital modulators *have never been* reported in the literature. The ADE-DPWM architectures are valid and more performative alternatives to the TTEC-based structures, even in cases where

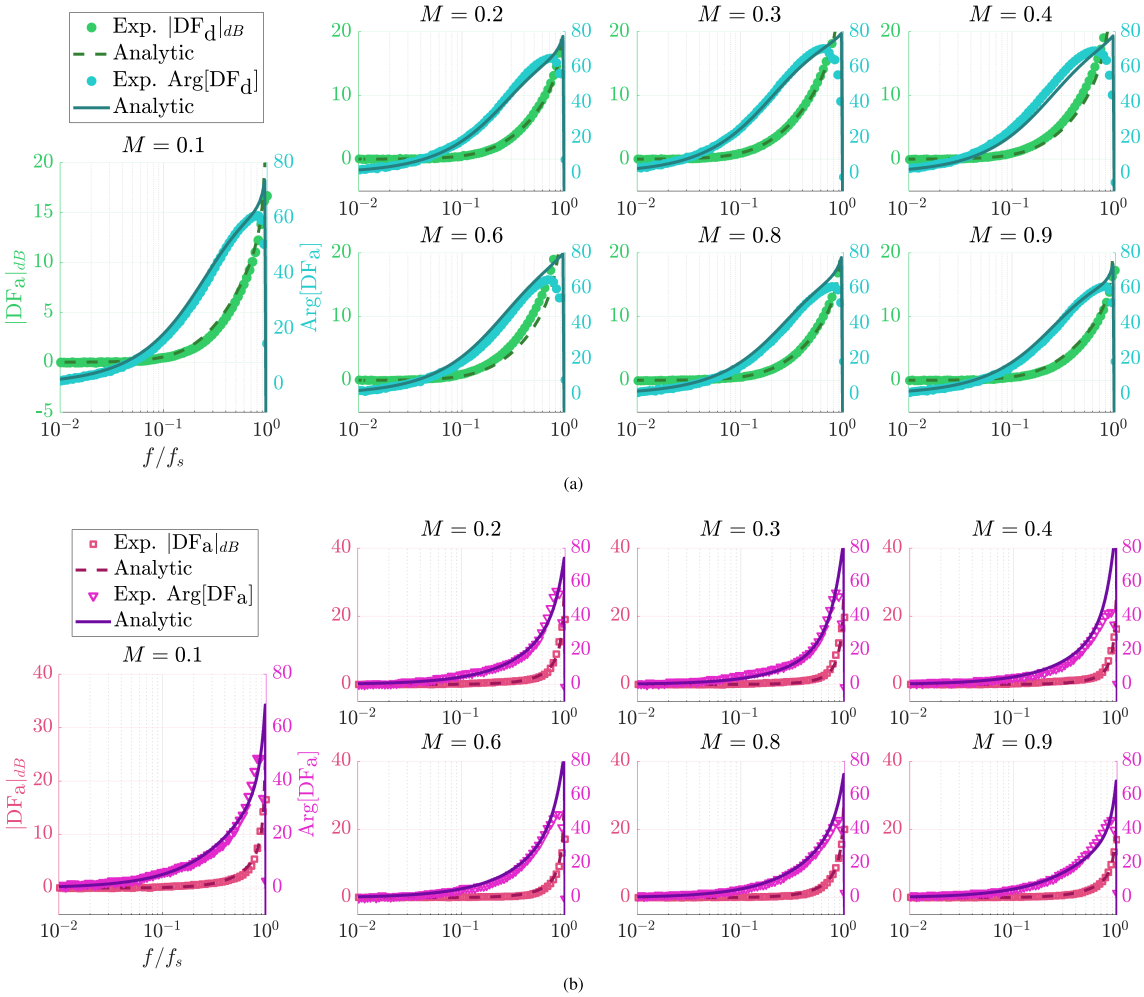


Fig. 7. Bode-plot comparison of (a) $\mathrm{DF}_d(s)$ and (b) $\mathrm{DF}_a(s)$ *versus* the corresponding experimental transfer function measurements.

multisampling is adopted. By almost eliminating the operational point dependency, the resulting ADE-DPWMs can be used to compensate for the phase degradation introduced by the signal acquisition and conversion chain. The final phase-gain is programmable and can be used to avoid specific numeric derivative actions in closed-loop controllers (e.g., like in the PID compensator).

B. Experimental Small-Signal Comparison of ADE-DPWM versus TTE-DPWM

The differences between the proposed *multisampling* architectures and the *multisampling* TTE-DPWM are even more pronounced when their small-signal models are directly compared. Fig. 8(a)[5] shows the comparison between the experimental phase response of the *simil-analog* ADE-DPWM and the TTE-DPWM for $N_{\mathrm{smpl}} = 4$. For the TTE-DPWM, the phase *delay* increases as the frequency increases. Instead, for the proposed modulator the phase *advance* increases with increasing frequency. Digital PWMs capable of providing phase advance instead of phase delay *have never been proposed in the literature* and their introduction stems from the contribution submitted in [26]. The vertical line in Fig. 8 denotes the crossing frequency chosen for the inner current-loop treated in Section VI. There is a distinct difference between the phase of the proposed modulator and the traditional one. This phase advance can be used to extend the bandwidth of the control system, but also to avoid introducing numerical derivatives into the compensator. Indeed, discrete derivatives and high oversampling factors lead to several noise issues [32] and must be avoided or properly treated. Moreover, as shown in [11], such modulators can be adopted to improve the passivity region in grid-connected converters, dramatically improving the stability properties. Similar considerations, with even more evident phase gain, can be made by examining Fig. 8(b).

[5]Here only the phase response is considered. However, other interesting properties come from the gain response of the *simil-analog* ADE-DPWM. In fact, it remains rather flat over a wide frequency range, greatly containing the degradation of the gain margin in closed-loop systems. For reasons of space this aspect is not further discussed.

VI. Applications in Typical Industrial Scenarios

In Section III, two instances of ADE-DPWM implementation rooted in the proposed general *multisampling* architecture are

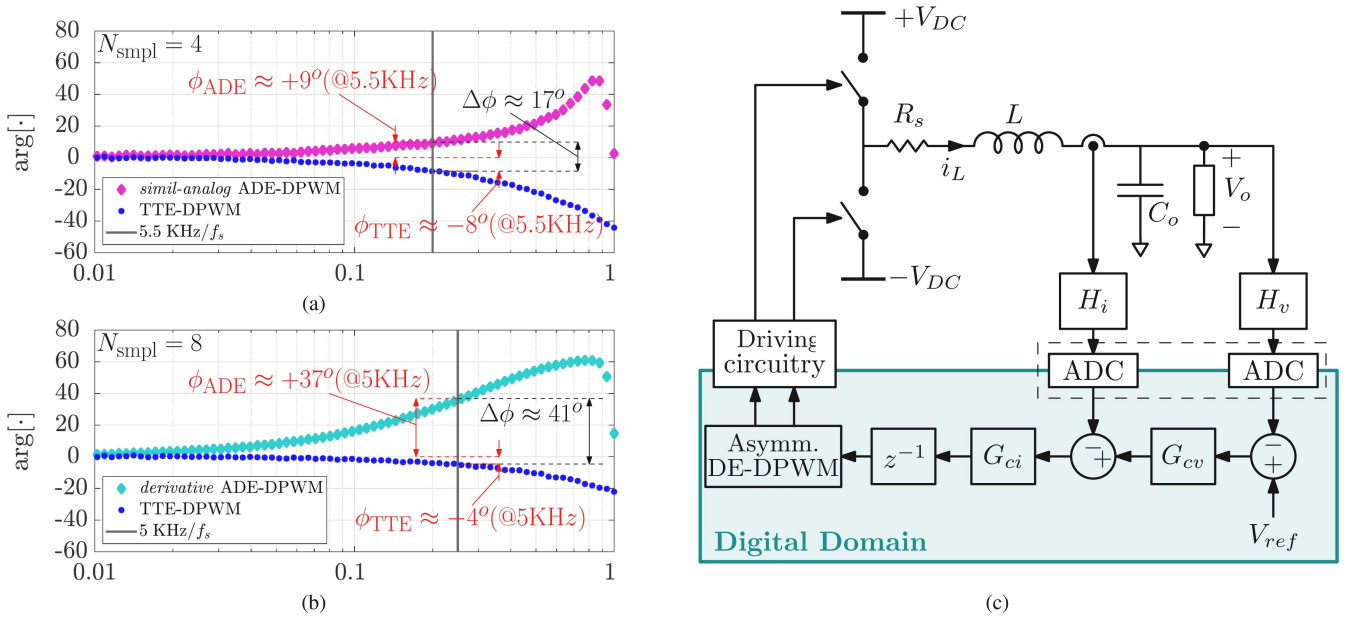


Fig. 8. Comparison between the experimental phase response of (a) the *simil-analog* ADE-DPWM ($N_{\text{smpl}} = 4$) *versus* the TTE-DPWM ($N_{\text{smpl}} = 4$) and (b) the *derivative* ADE-DPWM ($N_{\text{smpl}} = 8$) *versus* the TTE-DPWM ($N_{\text{smpl}} = 8$). Horizontal axes represent the normalized frequency (i.e., f/f_s). (c) Circuit and block diagram representation of the output voltage controlled single-phase voltage-source inverter used in the experimental measurements in Section VI.

TABLE I
EXPERIMENTAL SETUPS

TOPOLOGY	DPWM architecture	NAME
Single-phase VSI	*simil-analog* ADE-DPWM ($N_{\text{smpl}} = 4$)	*Setup 1(a)*
Single-phase VSI	TTE-DPWM ($N_{\text{smpl}} = 4$)	*Setup 1(b)*
Synchronous Buck	*derivative* ADE-DPWM ($N_{\text{smpl}} = 8$)	*Setup 2(a)*
Synchronous Buck	TTE-DPWM ($N_{\text{smpl}} = 8$)	*Setup 2(b)*

TABLE II
MAIN PARAMETERS OF THE MULTILOOP VOLTAGE CONTROLLED SINGLE-PHASE VOLTAGE SOURCE INVERTER

Output Power	1 kW
DC-Link Voltage	200 V
Output Voltage	110 Vrms (VSI), 130 V (Buck)
Output Capacitance	25 µF
Nominal output Load	13.5 Ω (VSI), 16 Ω (Buck)
Output Frequency	50 Hz (VSI)
Inductance	120 µH
Inductance ESR	15 mΩ
Multi-Sampling Factor	$N_{\text{smpl}} = 4$ (VSI), 8 (Buck)
Inner Current-Loop Phase-Margin	51° (VSI), 51° (Buck)
Inner Current-Loop Bandwidth (ADE)	6 kHz (VSI), 5.5 kHz (Buck)
Inner Current-Loop Bandwidth (TTE)	5.5 kHz (VSI), 5 kHz (Buck)
Outer Voltage-Loop Phase-Margin	42° (VSI), 46° (Buck)
Outer Voltage-Loop Gain-Margin	8 dB (VSI), 8.5 dB (Buck)
Outer Voltage-Loop Bandwidth (ADE)	2.6 kHz (VSI), 2.9 kHz (Buck)
Outer Voltage-Loop Bandwidth (TTE)	1.9 kHz (VSI), 1.9 kHz (Buck)

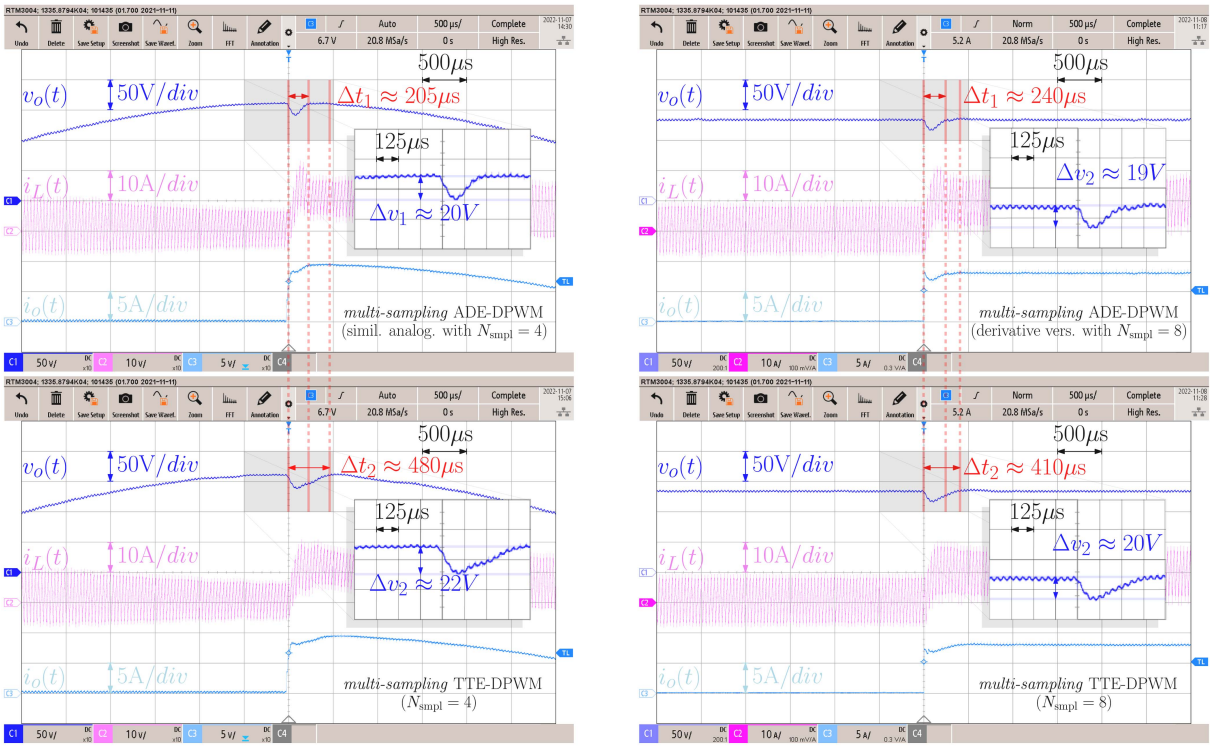
showcased. These examples provide a glimpse of the numerous possible implementations that can be derived from the proposed *general multisampling* architecture following the disclosed design approach.

The primary aim of these illustrations is to prove the effectiveness in shaping the frequency response of *multisampling* ADE-DPWMs. This shift in perspective transforms the role of DPWM from a component responsible for generating control signals–that introduces *phase deterioration* in closed-loop control setups–into a central tool that *enhances* a system's dynamic performance by increasing the available phase margin or the achievable bandwidth.

In this section, examples disclosed in Section III, namely *derivative* and *simil-analog* multisampling ADE-DPWMs, are employed in multiloop output voltage controls for a single-phase voltage source inverter (VSI) and a dc–dc Buck converter. The four laboratory configurations considered in this section are summarized in Table I; the main converter's parameters are detailed in Table II.

A. Multiloop Output Voltage Controlled Single-Phase Voltage Source Inverter

The topology's circuit of *Setup 1* and the block diagram of digital control are sketched in Fig. 8(c). The corresponding small-signal model is depicted in Fig. 6(b). Constants H_v and



(a) (b)

Fig. 9. (a) No-load-to-13.5 Ω load-step variation of the output voltage controlled VSI. On top there is the response of the system involving the proposed *simil-analog* ADE-DPWM, while on the bottom the one with the TTE-DPWM ($N_{\text{smpl}} = 4$). (b) Load step variation no-load-to-16 Ω of the output voltage controlled Buck converter. On top the systems using the proposed *derivative* ADE-DPWM, on bottom the one using the TTE-DPWM ($N_{\text{smpl}} = 8$).

H_i represent the overall gain of the sensing circuitry, which include the analog-to-digital converters transfer functions and the numerical full-scales. The small-signal expressions for $G_{di}(s)$ and $G_{iv}(s)$ in Fig. 6(b) can be found in [2]. Expressions for $G_{ci}(s)$ and $G_{cv}(s)$ denote the inner current-loop and the outer voltage-loop frequency compensators, respectively.

A target phase margin of $\phi_m = 50°$ is chosen for the inner-current loop. This value aligns with the typically utilized values for commercial VSIs, ensuring stable operation and adequate damping during transients. It is noteworthy that higher phase margin values (i.e., $\phi_m > 60$) would favor the ADEC-based architectures disclosed in this manuscript; however, they would not provide a realistic and fair comparison. A similar rationale applies to the selection of the crossover frequency (i.e., $\omega_{ci} = 2\pi f_{ci}$). Consequently, the chosen design criteria is to maximize the dynamic performance of *Setup 1(b)* and to ascertain whether, given identical converter parameters and phase margins, the proposed ADE-DPWM deliver superior dynamic performance or not. Indeed, as highlighted in Fig. 6(b), the difference between *Setup 1(a)* and *Setup 1(b)* lies in the pulsewidth modulator architectures. The following procedure details the compensators' desgin for *Setup 1(a)* and *Setup 1(b)*.

Whit reference to Fig. 6(b), the uncompensated inner-current loop gain can be written as follows:

$$T_{\text{iu}}(s) = G_{di}(s)\ H_i(s)\ G_{\text{DPWM}}(s). \tag{24}$$

Now, $T_{\text{iu}}(s)$ is mapped in the discrete frequency domain (or z-domain) by applying a discretization method like *Zero-order hold* map or a *Bilinear* (also called Tustin or prewarp) map. Once the method is chosen, a one-to-one correspondence is established between the continuous and discrete frequency domains. The corresponding discrete frequency domain version of (24) is denoted to as $T_{\text{iu-d}}(p)$ while p_{ci} is used to individuates the corresponding of f_{ci}. The target values for f_{ci} and ϕ_m are reported in Table II. From this, by defining $G_{ci} = k_p + T_{\text{s}} \frac{k_i}{1-z^{-1}}$, one can solve the following system with respect to k_p and k_i

$$\begin{cases} \left|G_{ci}(p_{ci})\ T_{\text{iu-d}}(p_{ci})\right| & = 1 \\ \arg\left[G_{ci}(p_{ci})\ T_{\text{iu-d}}(p_{ci})\right] & = \phi_m - \pi. \end{cases} \tag{25}$$

Now, chosen the gain and phase margin values for the outer-voltage loop, the same procedure is repeated to design $G_{cv}(z)$.

In this specific scenario, the notable benefit provided by the proposed modulators stems from the fact that, while maintaining an equal phase margin, the loop gain of *Setup 1(a)* encompasses a broader available bandwidth. This outcome arises due to the phase gain introduced by the ADE-DPWM modulator. Notably, the TTE-DPWM modulator introduces a $\approx -8°$ delay at the relevant frequency, whereas the proposed modulator introduces an $\approx +9°$ advance [see Fig. 8(a)]. Therefore, the phase gain of the inner loop obtained by replacing only the DPWM modulator between *Setup 1(a)* and *Setup 1(b)* is about $\Delta\phi \approx 17°$. As a result, the *simil-analog* multisampling ADE-DPWM systems

can effectively operate at higher crossover frequencies while maintaining the same *target* phase-margins.

For both systems [i.e., *Setup 1(a)* and *Setup 1(b)*], the multisampling DPWM architectures and the other digital parts are realized with the BB-Pro.

The load-step response for *Setup 1(a)* and *Setup 1(b)* are shown in Fig. 9(a). The digital control system using the proposed modulator is able to react faster also ensuring a lower undershoot. Specifically, the load-step response for *Setup 1(b)* (top of Fig. 9) exhausts the transient in $\Delta t_1 \approx 205\,\mu\,\mathrm{sec}$, while the system using the TTE carrier-based modulator (bottom of Fig. 9) takes about *twice* as long. Furthermore, experimental tests show that the system using proposed *multisampling* ADE-DPWM does not exhibit any closed-loop issues either during steady state or transient operations. This shows how an effective design of the synchronization mechanism makes it possible to retain most of the advantages of the introduced architectures without introducing any instability phenomena into the controlled systems.

B. Multiloop Output Voltage Control for a Dc–Dc Buck Converter

The block diagram in Fig. 6(b) can be also used to describe the small-signal operation of a synchronous dc-dc Buck converter by replacing $V_{\mathrm{IN}} = \pm V_{\mathrm{DC}}$ with a unipolar voltage and using the appropriate transfer functions for each block [4]. In this case, the proposed *derivative multisampling* ADE-DPWM is tested. The inner-current and outer-voltage loops for both setups are designed to reach the same phase margins. The design of G_{ci} and G_{cv} follows the same procedure discussed in Section VI-A. The *derivative* multisampling ADE-DPWM, taking advantage of the intrinsic programmable phase gain, allowed for a bandwidth extension. As the oversampling factor increases, one would anticipate improved dynamic performance, which tends to plateau as the value of N_{smpl} continues to rise. However, in this instance, it is evident that a significant difference in dynamic performance between the two architectures still exists. Indeed, as shown on Fig. 9(b), *Setup 2(a)* takes approximately half the time to restore the output voltage with respect to *Setup 2(b)*. In this case, the phase gain of the inner loop obtained by replacing the TTE-DPWM with the proposed one is about $\Delta\phi \approx 41^\circ$ [see Fig. 8(b)].

Also in the experimental test in Fig. 8(b), no oscillation phenomena are observed due to the presence of the synchronization mechanism, confirming the possibility of using ADEC-based modulators in real applicative contexts.

VII. Conclusion

This article proposes the final multisampling ADE carrier-based DPWM architecture and its accurate small-signal model. The general architecture together with the proposed design approach addresses the issue of operating-point dependence while introducing additional parameters to shape the small-signal transfer function. Preliminary *multisampling* architectures in [26] and [28] struggled to maintain negligible operating-point dependence, especially as the number of samples per period increases. Differently, the general model and the methodology developed in this manuscript allow for precise design and fine-tuning of operating point dependence across generic N_{smpl} values.

The small-signal behavior is validated through several experimental measurements. This validation highlights the remarkable accuracy of the proposed models even in the presence of synchronization mechanisms. The developed architecture significantly diminishes operating-point dependence, offering a multisampling DPWM that consistently ensures a high-frequency phase boost. To demonstrate this, experimental load-step variations are analyzed on laboratory prototypes of a multiloop voltage-controlled dc-ac single-phase voltage-source inverter and dc–dc synchronous Buck converter. The final results demonstrate that the developed architectures deliver superior dynamic performance compared to state-of-the-art *multisampling* DPWMs based on trailing triangle edge carriers.

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