Mini-LEGO CPU Voltage Regulator

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***Abstract*—This article presents the design and optimization of a miniaturized 48-V-to-1-V, 240-A linear-extendable group operated point-of-load (LEGO-PoL) CPU voltage regulator module (VRM)—*Mini-LEGO*—with a volume of 30 mm × 11.2 mm × 8.4 mm. The Mini-LEGO converter provides vertical power delivery, and it achieves a peak efficiency of 87.1%, a full load efficiency of 84.1%, and a power density of 1390 W/in^3 when stepping down a 48 V input voltage to an output voltage of 1 V. The Mini-LEGO offers compact device implementation, simple gate drive circuitry, and a fast regulation-stage switching frequency of 1.5 MHz. The 9-mm-by-9-mm, 4-phase, 20-A-per-phase vertical coupled inductor has a per-phase transient inductance of 10.3 nH, with its coupling reducing the ripple by a factor of six, and a height of 2.5 mm. This vertical coupled inductor structure is designed following a systematic approach to minimizing its height while achieving significant current ripple reduction and maintaining sufficient saturation margin. Thermal simulations are performed to verify the cooling feasibility. A measurement characterization method for vertical coupled inductor structures is introduced and used to characterize the designed vertical coupled inductor.**

***Index Terms*—Coupled inductor, dc–dc power conversion, point-of-load, switched-capacitor (SC), vertical power delivery, voltage regulator module (VRM).**

I. Introduction

AS THE energy consumption of microprocessors continues to grow, increased attention has been placed on designing efficient and dense voltage regulator modules (VRMs) to provide power to these loads. The microprocessor industry, driven by Moore's Law, has continued to exponentially increase the transistor count on individual chips. In recent years, however, efforts have been shifted to multicore processors with increasing power consumption as Dennard scaling has broken down (see Fig. 1). These trends have placed stringent requirements on VRMs to deliver lower voltages ($\leq$1 V) and higher currents ($\geq$100 A) from a higher input voltage supply (40–60 V) [3], [4], [5].

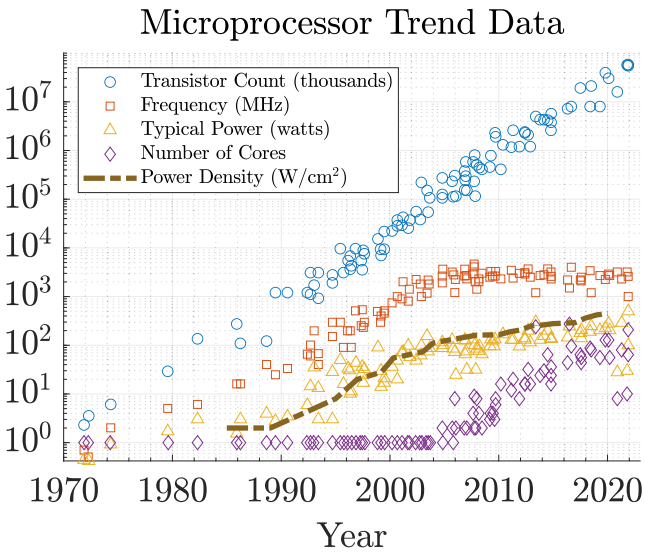

Fig. 1. Microprocessor trend data over the past 50 years (reproduced with data from [6], [7]). The transistor count per area doubles every 18 months (Moore's Law). As Dennard scaling has broken down, microprocessors have shifted to multicore systems to keep increasing transistor count year after year [8]. The increased power consumption per square centimeter of microprocessors requires dense and efficient voltage regulators.

Vertical power delivery is an attractive option to meet the power density targets for future computing systems [9], [10], [11], [12]. It is critical to minimize the height of voltage regulation modules (VRMs) to enable ultra-compact packaging and reduce interconnect lengths. The linear extendable group operated point-of-load (LEGO-PoL) architecture, and its implementation presented in [13], performs vertical power delivery for 48-V-to-1-V and achieved a current density of 1 A/mm^2 and a power density of 1000 W/in^3 for 48-V-to-1-V conversion with liquid cooling and without including the gate drive circuitry and its associated losses. Its height is 16.65 mm, which needs to be reduced to be packaged vertically with the CPU land-grid array

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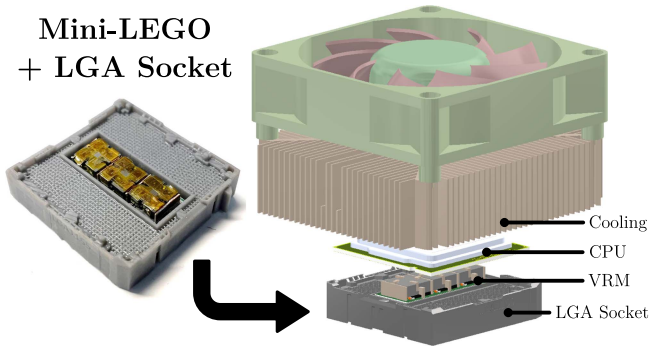

Fig. 2. VRM placed within a modified LGA socket (Intel LGA1155) for CPUs. Copackaging the VRM inside the LGA socket can leverage the cooling resources of the CPU and perform point-of-load power delivery. The VRM must have small enough area and thin enough height.

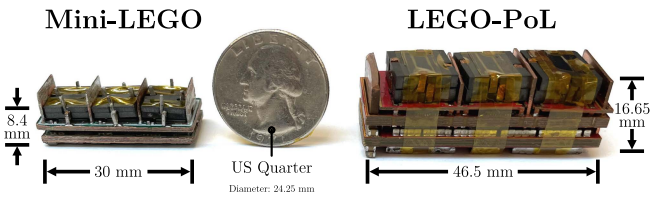

Fig. 3. Side-by-side comparison of the Mini-LEGO prototype presented in this article (developed in 2023), the vertical stacked LEGO-PoL prototype presented in [13] (developed in 2021), and a United States quarter. The volume of the 240 A Mini-LEGO is 22.5% of the 450 A LEGO-PoL. The height is reduced from 16.65 to 8.4 mm, and the area is reduced from 767 to 336 mm^2. It took 24 months to increase the power density two times.

(LGA) packaging, as illustrated in Fig. 2. This article presents a new 48-V VRM design—Mini-LEGO—which is significantly smaller and thinner than the LEGO-PoL implementation (see Fig. 3). The significantly reduced size is enabled by 1) improved device implementation, 2) optimized gate drive circuitry, 3) optimized magnetics, 4) higher switching frequency, and 5) compact packaging. Note the LEGO-PoL architecture can also be used for lateral power delivery, and vertical power delivery can be implemented with many other architectures. The vertical coupled magnetics design presented in [1] and the inductor thickness optimization method introduced in this article makes the LEGO-PoL architecture a good candidate for vertical power delivery.

Miniaturization of power electronics, driven by semiconductor devices that can switch at high switching frequencies and by high capacitor energy densities, is limited due to the rapidly increasing core losses at higher frequencies. One way to reduce the overall size and volume of magnetic components is by combining the functionality of multiple discrete inductors using a single magnetic core [14]. Leveraging this magnetic coupling by using coupled inductors can improve system efficiency, improve transient response, and better utilize magnetic energy storage. A novel coupled inductor geometry is presented and optimized for the Mini-LEGO converter, capable of performing vertical power delivery and enabling significant system height reduction.

As illustrated in Fig. 3, the Mini-LEGO reduces the height of the 48-V VRM from 16.65 to 8.4 mm as compared to the LEGO-PoL design. It has a current area density of 0.71 A/mm^2 and achieves a power density of 1390 W/in^3, including all gate drive circuitry, achieves 87.1% peak efficiency, does not require liquid cooling, and is thin enough for highly compact system packaging. The multiphase buck regulation stage switches at 1.5 MHz. Mini-LEGO tradesoff energy efficiency to realize improvements in power density and control bandwidth. The miniaturized size and thickness allows the VRM to be packaged much closer to the microprocessor where abundant cooling resources are available, mitigating the challenges of thermal management due to lower efficiency.

This article presents the optimal design of a new hardware implementation of the LEGO-PoL architecture—the Mini-LEGO converter—to demonstrate its capability at a higher switching frequency for extreme performance. The operation principles of the architecture are reviewed in Section II, and the design methodology of the Mini-LEGO converter is presented in Section III. The operation of the simplified gate driver circuit is explained in Section IV. A novel coupled magnetics geometry is introduced, suitable for vertical power delivery, with parameters that enable the tradeoff between core losses and winding losses while reducing inductor height. A loss-based optimization method is presented and the design of a four-phase coupled inductor is discussed in Section V. This inductor was characterized with a measurement procedure that can be applicable to most vertical multiphase inductor structures, with customized fixtures that include the current return path for accurate leakage induction characterization, discussed in the Appendix. The experimental results, as well as thermal simulations and analysis, are provided in Section VI. Finally, Section VII concludes this article.

II. LEGO-PoL Architecture

Fig. 4 shows the schematic of the 48-V-to-1-V 240-A Mini-LEGO converter with three series-stacked 2:1 switched-capacitor (SC) units and three parallel connected four-phase buck units with coupled inductors. The operation principles and key advantages of the LEGO-PoL architecture have been explained in detail in [13]. The LEGO-PoL architecture decouples the voltage stress, current stress, and dynamic requirements and addresses these design challenges separately with SC and coupled inductor techniques.

The input voltage is stepped down to a virtual intermediate bus voltage by a set of series-stacked 2:1 SC submodules. In the Mini-LEGO design, three stacked 2:1 SC submodules step the 48 V input voltage down to 8 V. Each submodule has its own virtual intermediate bus voltage [15]. This virtual intermediate bus voltage has an average of 8 V, but may have significant ripple depending on the effective capacitance of the flying capacitors (C_1–C_5 in Fig. 4), the operating power, and the switching frequency. This virtual intermediate bus voltage serves as the input voltage for the multiphase buck submodules, which are connected in parallel at the output. This design has three four-phase buck submodules, with each of the 12 phases delivering a maximum current of 20 A with a regulated output voltage.

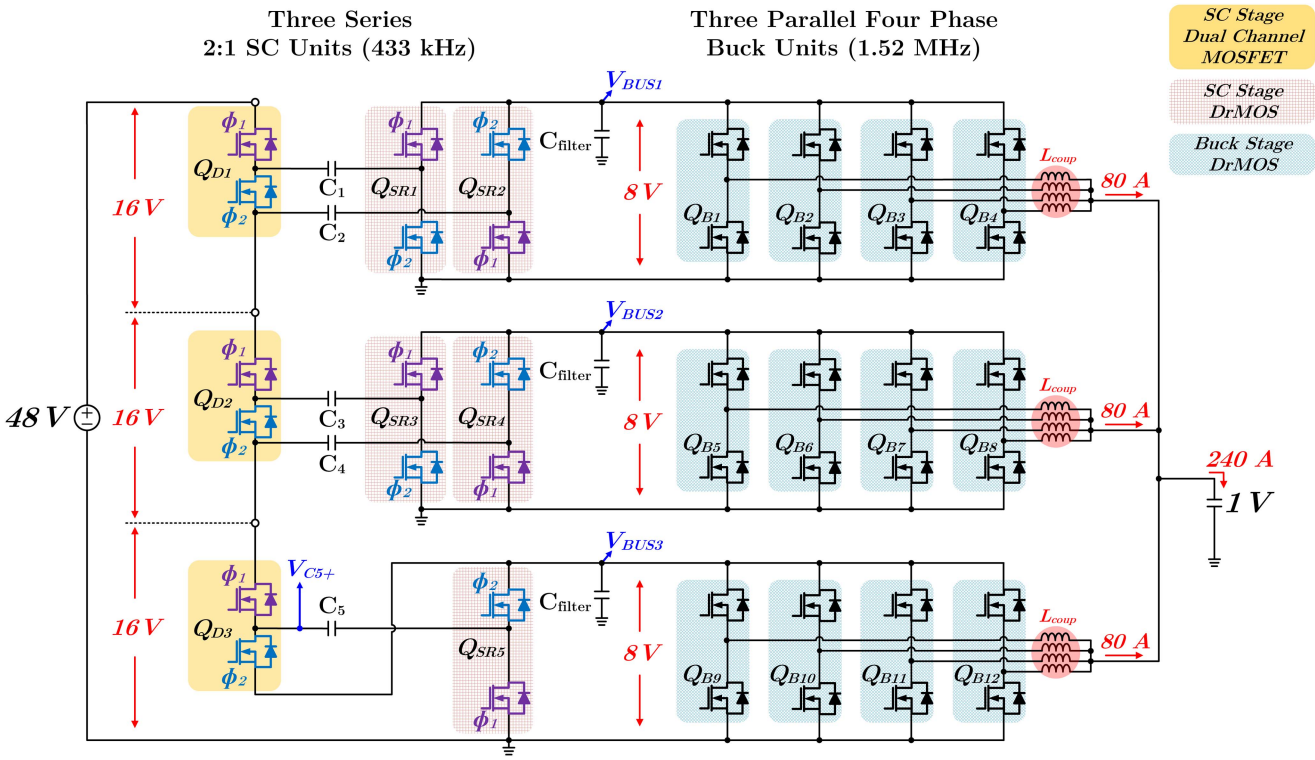

Fig. 4. Circuit topology and implementation of the 48-V-to-1-V, 240-A mini-LEGO design. Each buck phase delivers 20 A of peak current. The floating switches in the SC stage are implemented as dual-channel silicon MOSFETs, and the SC synchronous rectifier switches as well as the buck stage switches are implemented as DrMOS (integrated driver and two power MOSFETs). Three dual-channel MOSFETs, five rectification DrMOS devices, and 12 buck DrMOS devices are used, totaling 20 devices by discrete component count.

The operation of the two stages is merged. Instead of a large decoupling capacitor between the two stages, as commonly exists in intermediate-bus two-stage architectures, a small capacitance (for reference, 1.03 μF is used for the Mini-LEGO design) is used instead to filter the high-frequency ripple generated by the second stage. This allows the inductors in the multiphase buck stage to act as a current source, charging, and discharging the flying capacitors to achieve soft charging. This soft charging mechanism enables usage of much lower flying capacitor values while maintaining high efficiency [16]. The multiphase buck stage operates at a higher switching frequency than the SC stage. In addition, the LEGO-PoL architecture provides automatic current sharing and voltage balancing between submodules, as capacitors C_2 and C_4 must maintain charge balance.

The following list summarizes the advantages of the LEGO-PoL architecture, and compares the features of this architecture over other commonly used VRM solutions.

1) Different from a traditional intermediate bus converter (IBC) architecture with a transformer-based first stage [17], the front-end of the LEGO-PoL architecture leverages the advantages of SC-based solutions over transformer-based solutions [18]. It scales well to high-frequency operation and is not limited by the availability of high-performance magnetic materials in the MHz range.
2) Compared to other SC or resonant-SC two-stage solutions [19], the LEGO-PoL architecture can greatly reduce the size of the capacitance required in the first stage and the intermediate bus capacitance and offers automatic voltage balancing and current sharing as needed in high power applications, as investigated in [13] and [20].
3) Compared to other single-stage or merged-two-stage solutions with a SC front-end followed by a buck-derived unit, where all switches are synchronously operated with one common clock [21], [22], [23], the LEGO-PoL architecture allows for different SC units to operate at different frequencies to better balance the tradeoff between device utilization, efficiency, and control bandwidth.

The key contributions of this article include the following.

1) The Mini-LEGO implementation, designed to fully exploit the potential of the LEGO-PoL architecture. This architecture represents a family of novel high-conversion-ratio hybrid circuit topologies combining many SC circuits and switched-coupled-magnetic circuits to achieve multiple goals—efficiency, density, and control bandwidth. The SC front-end can be implemented using various SC circuits [24]. Other switched-coupled-magnetic circuits, such as the series-capacitor buck converter [15], [25] or the three-level buck converter [26], can be used as the second stage.
2) The multiphase vertical coupled magnetics structure, the design methodology presented in this article, and the resulting 2.5 mm-tall four-phase coupled inductor. This coupled magnetics geometry has significant synergy with vertical power delivery. The magnetic structure, core shape,

TABLE I
MINI-LEGO FLYING CAPACITORS VALUES, IMPLEMENTED WITH 4.7 μF CAPACITORS IN PARALLEL

Symbol	Bias Voltage	Number of 4.7 μF Capacitors	Effective Capacitance
C_1	40 V	16	12.8 μF
C_2	32 V	15	15.8 μF
C_3	24 V	15	21.5 μF
C_4	16 V	15	35.6 μF
C_5	8 V	15	56.8 μF

and winding configurations presented in this article can be used to enhance the magnetics design in other vertical power delivery implementations beyond the LEGO-PoL architecture [27].

3) The coupled inductor characterization method, the customized fixtures, the thermal simulation platform, and the gate drive implementation presented in this article. These contributions are critical for achieving high performance with the LEGO-PoL and other similar hybrid architectures.

III. MINI-LEGO CONVERTER DESIGN

The primary design targets for the Mini-LEGO converter are high power density and low height, which guides the design philosophy and component selection. Fig. 5(a) shows the top side layout of the SC stage, where all switches are placed. Instead of implementing the 10 ground-referenced synchronous rectifier switches as discrete MOSFETs with separate gate driver integrated circuits (ICs), we implement them as DrMOS devices, which comprise of an integrated driver and two power MOSFETs (highlighted in Fig. 4). The footprint of the DrMOS devices chosen (onsemi FDMF3039) is 3.5 mm $\times$ 4.5 mm. For the floating switches, dual-channel symmetric MOSFETs (onsemi NTTFD2D8N03P1E), configured as half-bridges, are used. Two power MOSFETs are integrated in one package within the standard footprint area of 3.3 mm $\times$ 3.3 mm. The gate drive circuitry for the floating switches is placed in the remaining area.

The bottom side layout of the SC stage is shown in Fig. 5(b). Each of the five flying capacitors consists of fifteen 50 V, 4.7 μF, 0805 MLCCs. Each flying capacitor has a different dc bias voltage, resulting in a different effective capacitance as shown in Table I. A row of input capacitors is placed on the bottom side as well.

Fig. 5(c) shows the layout of the multiphase buck stage. The top and bottom sides are identical in terms of component placement. The board is divided into three submodules. Four DrMOS devices, capable of handling up to 45 A, are used per submodule (Reed Semiconductor RS86900). Copper rods from the SC stage vertically deliver power to the multiphase buck stage. Four pads are present per submodule to connect to the windings of the vertical coupled inductor, which sits directly on top of the DrMOS devices. This allows for an interposer-less connection between the inductors and the multiphase buck board, which further reduces the system height compared to the original LEGO-PoL

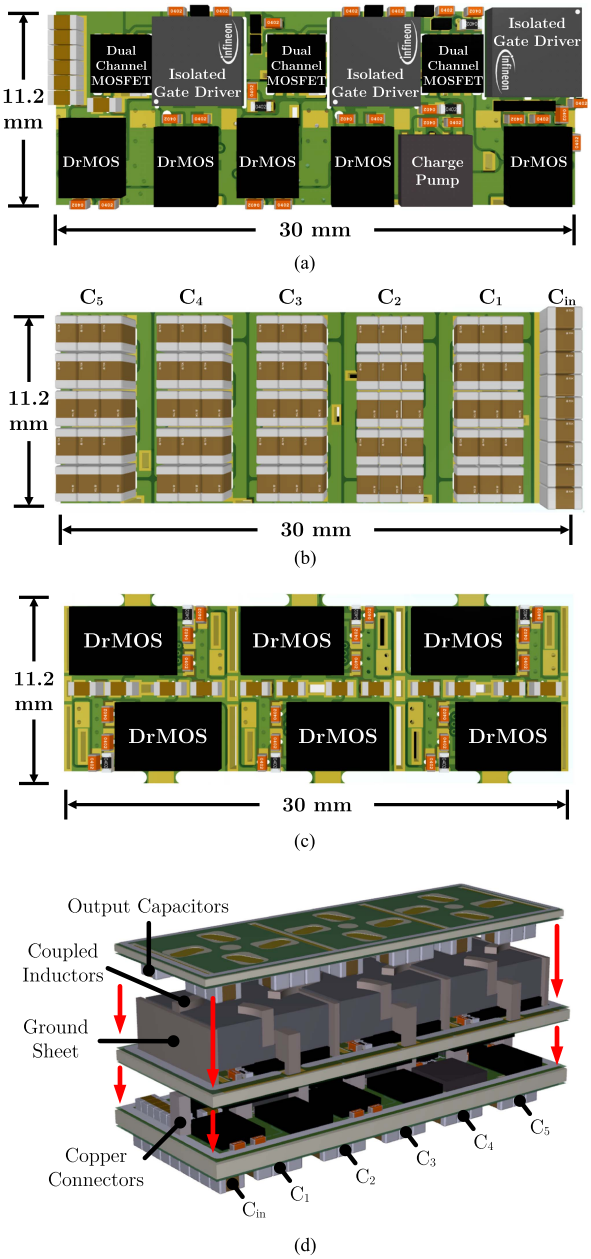

Fig. 5. (a) PCB layout of the top side of the SC stage. The power stage and all gate-drive circuitry is included within an area of 336 mm^2. (b) PCB layout of the bottom side of the SC stage, containing the flying capacitors and input capacitors. (c) PCB layout of the top side of the multiphase buck board. The bottom side has identical component placement. Four pads are present on the top side to connect to the four-phase coupled inductor. (d) Altium 3-D rendering of multiboard assembly process.

design with an interposer. The interstage filter capacitors are placed between the vertical copper connectors, resulting in a short parasitic inductance loop between the two stages [13]. Eight 0603 X7R 25 V MLCCs are used per submodule, and the derated filter capacitance value for each submodule is 1.03 μF.

Fig. 5(d) shows an Altium 3-D rendering of the full power stage assembly. Ground sheet connectors are used for the current return path. The full assembly uses four copper ground sheets,

TABLE II
KEY COMPONENTS OF THE MINI-LEGO PROTOTYPE

Switched-Capacitor Stage	
Symbol	**Component**
$Q_{D1} - Q_{D3}$	onsemi NTTFD2D8N03P1E (30 V)
$Q_{SR1} - Q_{SR5}$	onsemi FDMF3039 DrMOS (30 A)
Isolated Gate Driver	Infineon 2EDF7275K
Charge Pump	Texas Instruments UCC27212
Capacitor Used for $C_1 - C_5$	TDK 4.7 μF, 0805 X7R (50 V)
C_{in}	9 $\times$ Murata 2.2μF, 0805 X7T (100 V) 6 $\times$ Taiyo Yuden 220 nF, 0603 X7S (100 V)

Buck Stage	
Symbol	**Component**
$Q_{B1} - Q_{B12}$	Reed Semiconductor RS86900 Smart Power Stage (45 A TDC, 90 A max)
C_{filter}	1 $\times$ Kemet 1 μF, 0603 X7R (25 V) 4 $\times$ Kemet 100 nF, 0603 X7R (25 V) 3 $\times$ Kemet 22 nF, 0603 X7R (25 V)

with three coupled inductors in between them. The output capacitors are placed vertically above the coupled inductors on a separate board, embedding them within the overall converter package. The key component specifications are summarized in Table II.

IV. ULTRA-COMPACT GATE DRIVER CIRCUITRY

The LEGO-PoL architecture has 40 switches, of which 34 switches are driven as ground-referenced half-bridge pairs with integrated gate drivers in the DrMOS devices. The remaining six switches are floating and require a floating gate driver circuit. The power density of the previous LEGO-PoL design is much lower when it is calculated, including the floating gate circuitry in the overall volume than when it is calculated only including hardware in the power path.

Various techniques for implementing gate drive circuits for SC circuits and flying capacitor multilevel converters have been explored [28], [29]. In the switched-tank converter, which uses a resonant Dickson SC topology, a charge-pump gate drive circuit is used to generate the bias power for each gate driver IC [19]. The SC stage in Mini-LEGO is a Dickson SC nonresonant topology, and a similar gate driving method can be adapted. This section explains the detailed operation of the proposed gate driver circuit for Mini-LEGO and presents its simplified implementation as compared to other solutions.

Fig. 6(a) shows the power stage and gate drive circuit implementation for the SC stage floating switches. The gate drive circuit implementation is highlighted specifically in Fig. 6(b). A bootstrapping circuit is used to provide a power supply to the floating gate driver ICs. The gate drive circuit comprises a charge pump implemented with a half-bridge gate driver (4 mm $\times$ 4 mm) and three isolated gate driver ICs (5 mm $\times$ 5 mm), and is highly modular and scalable.

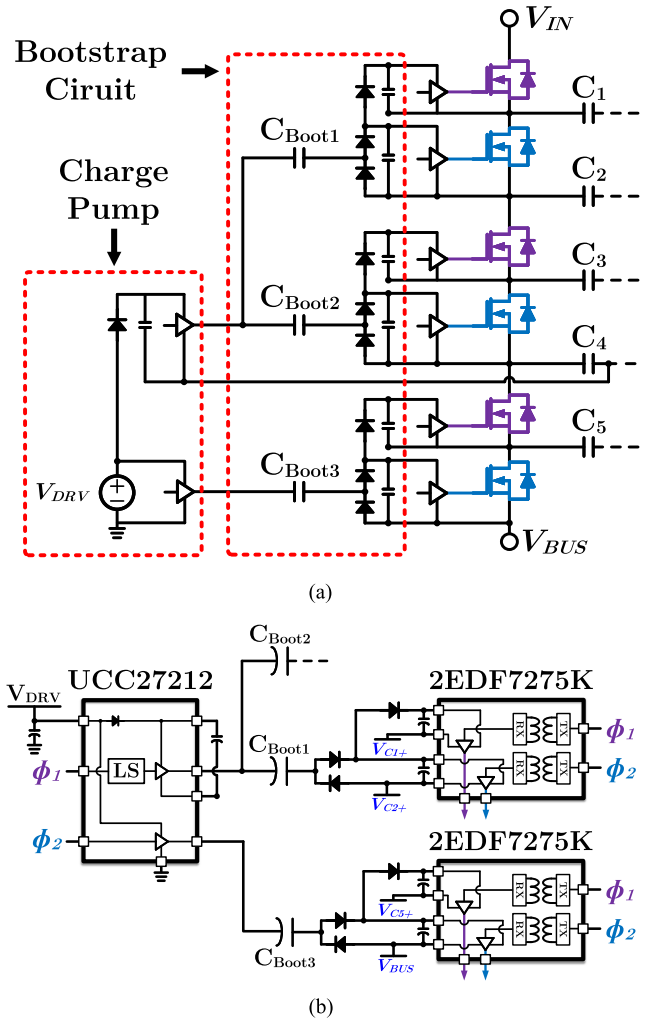

Fig. 6. (a) Circuit schematic of the gate drive for the floating switches of the SC stage. (b) Implementation of the charge pump, bootstrapping circuit, and gate drivers. An isolated gate driver IC (2EDF7275 K from Infineon) is used to drive each of the floating dual-channel MOSFETs.

Fig. 7 illustrates the operation principles of the gate drive circuitry, including the charging process of the bootstrap capacitors. Focusing on C_{Boot_1} as an example, the operation principles of the bootstrap circuit during periodic steady-state include the following:

1) During phase 1 (Φ_1), C_{Boot_1} charges the V_{DD} capacitor of the low side channel of the gate driver IC, denoted $C_{V_{\text{DD,low}}}$. The low side channel is OFFduring Φ_1.
2) During phase 2 (Φ_2), the bootstrap capacitor is charged by the flying capacitor C_2 until $V_{\text{C}_{\text{Boot}_1}} = V_{\text{C}_2}$.
3) During Φ_2, as the bootstrap capacitor is being charged, $C_{V_{\text{DD,low}}}$ charges up $C_{V_{\text{DD,high}}}$.

This charging mechanism holds for C_{Boot_2} as well. The last of the six floating switches has its drain connected to the positive terminal of C_5 (as denoted in Fig. 4) and its source connected to V_{BUS}. Thus, C_{Boot_3} has a slightly different charging mechanism, and charges during Φ_1 through the filter capacitors present across V_{BUS} and ground. The low-side channel of the charge pump is driven by Φ_2, used to charge C_{Boot_3}, and the high-side channel,

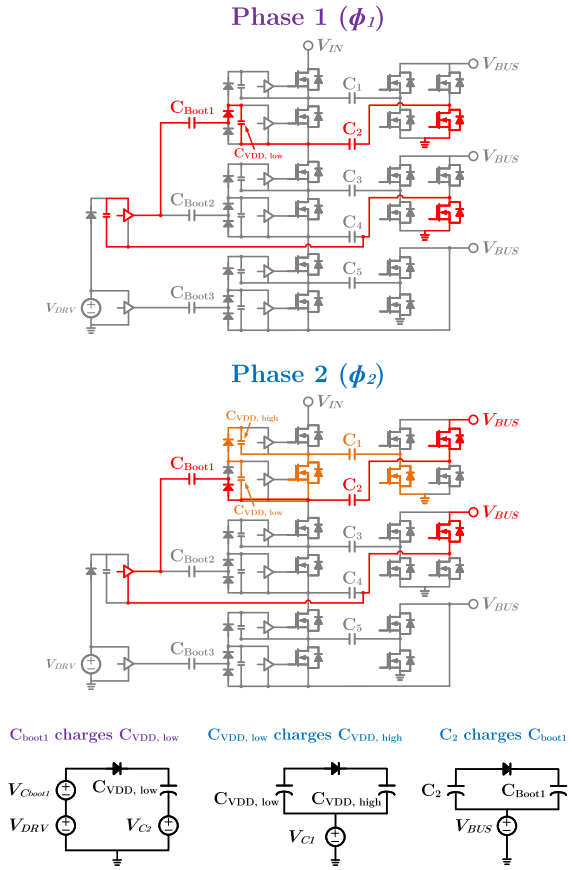

Fig. 7. Charging mechanism of the bootstrap capacitor and isolated gate driver power supply capacitors highlighted for the first submodule of the SC stage. The equivalent subcircuits shown below demonstrate how the bootstrap capacitor charges the low side channel power supply capacitor $C_{VDD,low}$ during phase ϕ_1, which then charges the high side power supply capacitor $C_{VDD,high}$ during phase ϕ_2. The flying capacitor C_2 charges the bootstrap capacitor during phase ϕ_2.

which is used to charge the bootstrap capacitors the other two submodules, is driven by Φ_1. This gate drive strategy is widely applicable to other switched-tank or Dickson-derived circuits.

Because we use an isolated gate driver IC (Infineon 2EDF7275 K), a separate level shifter is not needed for the PWM control signals. The isolated gate driver ICs are placed directly adjacent to the dual channel MOSFETs that they drive. The charge pump is placed next to the ground referenced DrMOS devices, and close to C_4, as V_{SS} for the high-side channel of the charge pump is V_{C4-} [labeled in Fig. 6(a)]. The gate drive circuitry occupies approximately 111 mm^2 of the area on the SC board, roughly 13 of the overall area.

V. Vertical Coupled Inductor Design Methods

Interleaving the individual phases of a multiphase buck converter can reduce the overall output current ripple. This current ripple reduction, however, does not extend to the individual phases themselves. If the inductors are coupled, the current ripple cancellation achieved at the output can be extended into the individual phases themselves [30]. This offers efficiency benefits in reducing the ac rms current through the copper traces

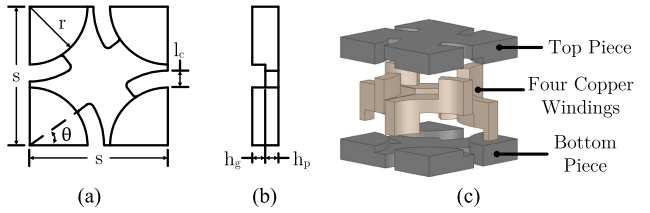

Fig. 8. (a) Top view and (b) side view of the vertical coupled inductor structure highlighting the geometric parameters used for optimization. (c) Vertical coupled inductor two-piece assembly, illustrating the copper winding positioning between the top and bottom magnetic core pieces.

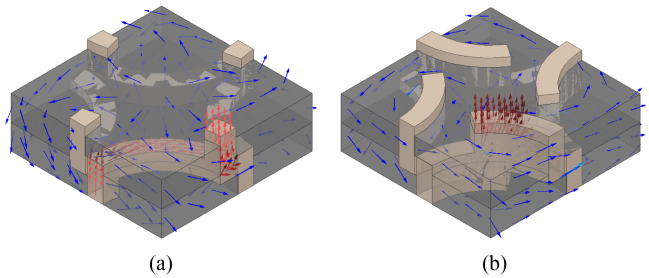

Fig. 9. Demonstration, using ANSYS Maxwell 3D, of how varying θ impacts the current and flux distribution for (a) $\theta = 15°$ and (b) $\theta = 57°$. The blue arrows on the magnetic core pieces show the flux density, and the red arrows on the winding show the current density.

and semiconductor devices. In addition, as this ripple reduction is achieved through coupling, a lower transient inductance is needed when compared to using discrete inductors, resulting in faster transient response for the same per-phase current ripple. The Mini-LEGO converter design uses coupled inductors and leverages their advantages to improve overall system density. The height of the coupled inductor in the LEGO-PoL design was 5.25 mm. The Mini-LEGO implementation reduces its height by over half to 2.5 mm through a systematic design and optimization method for vertical coupled inductors.

A. Coupled Inductor Geometry

Fig. 8(a) and (b) shows the novel fully parameterized four-phase vertical coupled inductor structure designed for the Mini-LEGO converter. The structure is designed to be a two-piece assembly, with the windings placed in between the two core pieces as demonstrated in Fig. 8(c). For the four-phase design examined in this article, the inductor can be either square or rectangular in shape, with outer legs on each of the four corners. This design can be extended to higher number of phases by changing the shape of the overall inductor.

The parameter θ, which is defined as the angle between the edge of the core and the radial cutout in which the winding is inserted, enables designs that can tradeoff between winding resistance and core losses. Fig. 9 shows the effect of different values of θ. For small values of θ, the winding makes a quarter-turn around the core leg post, while the flux traverses from the center of the bottom core piece through the individual legs and up to the top core piece. As θ increases beyond 45°, the current

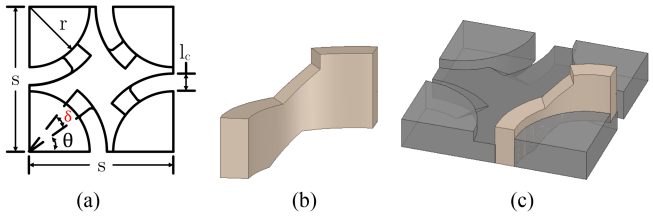

Fig. 10. (a) Top view of vertical coupled inductor structure with the addition of δ. (b) Winding design, with angled copper for continuous conduction path. (c) Winding placement within the magnetic core.

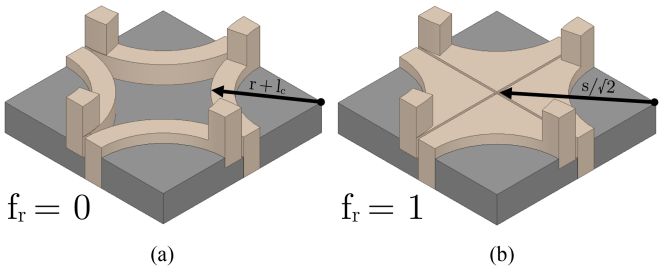

Fig. 11. Winding fill factor parameter f_r at (a) its minimum condition of $f_r = 0$ and (b) its maximum condition at $f_r = 1$. The fill factor parameter is independent of the core geometry and can be used to further fine tune the per-phase transient inductance and DC resistance of the coupled inductor after the core is manufactured.

travels vertically through the winding, while the magnetic core "wraps" around it. Higher values of θ can substantially reduce the dc resistance of the windings. With a fixed cutout size, such as in the coupled inductor design presented in [1] used for the initial LEGO-PoL vertical design, the primary way to reduce the dc resistance is to increase height between the top and bottom core plates, denoted as h_g in Fig. 8(b). Adding a parameter in θ to effectively shorten the overall winding path increases design flexibility and enables another way to reduce the dc resistance without directly contributing to overall inductor height.

An additional parameter, denoted as δ, can be introduced as well to further influence the winding design. Fig. 10 illustrates this parameter and the effect it can have on the winding design. This parameter defines a chamfer in the cutout, from the bottom to the top of the magnetic core piece (with a height of h_p), starting at the end of the cutout and ending at an angle of $\theta + \delta$. This results in an angled winding design that removes the sharp 90° corners and improves the current density distribution throughout the winding. For the inductors used in the Mini-LEGO converter, this parameter was excluded.

Another parameter, denoted as f_r, or the fill factor ratio, is independent of the magnetic geometry and is a function of the copper winding geometry. Copper blocks the passage of ac flux, and in this geometry, where the copper is placed in the air gap between the top and bottom plates, the presence or absence of copper can confine the ac flux to a certain area. Fig. 11 illustrates this concept. A fill factor ratio of 0 means the winding does not exceed the radius of $r + l_c$, when measured from the corner of the magnetic core. A fill factor ratio of 1 means the winding fills in the remaining area. This parameter can be adjusted after the

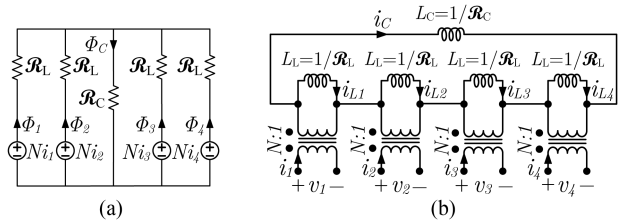

Fig. 12. (a) Reluctance model for the four-phase coupled inductor geometry presented in Fig. 8. $\mathcal{R}_L$ represents the reluctance of the path the flux takes through the bottom plate, post, and top plate, for one of the phases. $\mathcal{R}_C$ represents the leakage path through the air gap in between the top and bottom plates. (b) Inductance dual model representation of the reluctance model, obtained by taking the topological dual.

design is completed to further tune the transient inductance to its desired value.

B. Coupled Inductor Modeling

Fig. 12(a) shows the reluctance model for the proposed magnetic geometry. Each winding is represented as an MMF source. $\mathcal{R}_L$ represents the lumped reluctance of the flux path for each phase, including the corner post of the core and the parts of the top and bottom plates connecting to the middle section. The flux from each of the phases combines in the middle part of the core, and $\mathcal{R}_C$ represents the reluctance through the air gap between the top and bottom plates. The topological dual of this reluctance model results in the inductance dual model shown in Fig. 12(b) [30]. This model directly translates the magnetic geometry into the electrical circuit domain and can be evaluated using circuit simulation tools to see the electrical performance for a given coupled inductor geometry.

The transient inductance, which limits the speed at which the inductor current can slew from one level to another (di/dt), as well as the current ripple during steady-state operation, are of particular importance. The inductance dual model formulation allows for quick calculation of these values using only geometric parameters of the core. The equation used to calculate the per-phase transient inductance is

$$L_{\text{ptr}} = \frac{N^2}{\mathcal{R}_L + M\mathcal{R}_C} \tag{1}$$

where N is the number of turns and M is the number of phases. Through coupling, the ripple current during steady state is reduced when compared to the ripple current of a discrete inductor with inductance equal to L_{ptr}. The ripple reduction factor γ is a function of the strength of magnetic coupling as well as the ripple reduction achieved at the output due to interleaving (Γ), and can be expressed as follows:

$$\gamma = \frac{1 + \frac{M\mathcal{R}_C}{\mathcal{R}_L} \times \Gamma}{1 + \frac{M\mathcal{R}_C}{\mathcal{R}_L}} \tag{2}$$

where

$$\Gamma = \frac{(k + 1 - \text{DM})(\text{DM} - k)}{(1 - D)\text{DM}^2}. \tag{3}$$

D is the duty cycle and k is an integer index such that $\frac{k}{M} < D < \frac{k+1}{M}$. The per-phase ripple current during steady-state is equal to the ripple current of an uncoupled inductor with an inductance equal to L_{ptr}/γ.

C. Design Optimization

The tradeoffs between core loss, winding loss, power density, and transient response of a coupled inductor are all highly correlated. A systematic optimization for the geometric parameters can help minimize the losses, maximize the power density, and maintain the desired transient response [31].

The two major types of losses in the coupled inductor are winding loss and magnetic core loss. Both the dc and ac resistances of the windings are considered when calculating the winding loss following: $P_w = I_{\text{dc}}^2 R_{\text{dc}} + I_{\text{ac,rms}}^2 R_{\text{ac}}$, where R_{dc} and R_{ac} are the calculated dc and ac resistance of the windings, respectively. Due to the skin effect and the proximity effect, the ac current will flow on the outer edge of the winding, away from the magnetic material. Fig. 14(a) shows how this is modeled. The ac resistance is calculated based on the skin depth for only the outer region of the winding. Fig. 14(b) shows the current density from an Eddy Current simulation in ANSYS Maxwell 3D of the coupled inductor with each winding excited with a 2 A peak-to-peak sinusoidal ac current at 1.5 MHz. The current is concentrated primarily on the surface of the winding that is not interfacing with the magnetic material.

The power loss per unit volume (in units of kW/m^3) in the core is typically calculated using Steinmetz's Equation ($P_v = kf^\alpha \hat{B}^\beta$), where f is the frequency of the excitation (in kHz), $\hat{B}$ is the peak flux density (in T), and k, α, and β are constants referred to as the Steinmetz coefficients, often provided by the material manufacturer. In coupled inductors, where the current waveforms are irregular piece-wise-linear waveforms, the Steinmetz equation cannot be directly used. The "improved Generalized Steinmetz Equation" (iGSE) is used to estimate the core loss [32]. The only input parameters needed are the Steinmetz coefficients. For each linear time segment, the power loss per unit volume can be calculated as

$$\overline{P_v} = \frac{k_i (\Delta B)^{\beta-\alpha}}{T} \sum_m \left| \frac{B_{m+1} - B_m}{t_{m+1} - t_m} \right|^\alpha (t_{m+1} - t_m) \quad (4)$$

where

$$k_i = \frac{k}{(2\pi)^{\alpha-1} \int_0^{2\pi} |\cos\theta|^\alpha 2^{\beta-\alpha} d\theta}. \quad (5)$$

The parameters for the design are summarized in Table III. DMR53, a MnZn ferrite from Hengdian Group DMEGC Magnetics Company, is used as the magnetic material for this inductor design. The key material parameters are listed in Table IV. The provided parameters at 100 °C are used for the optimization procedure. Given these fixed parameters, the optimal values for the remaining free parameters can be determined to minimize the inductor loss. Parameters are constrained to ensure the finalized design meets the specified targets. Constraints on the x and y dimensions are dictated by the converter layout, which limits both to a maximum of 9 mm. Adding a constraint on the maximum total height h of the inductor of 2.5 mm, or no more than 30% of the overall system height, restricts the design space to include inductors with a volume no larger than 203 mm^3. Constraints can also be added to the electrical properties of the coupled inductor, such as the maximum tolerable phase current ripple or output current ripple as well as the maximum tolerable transient inductance. A constraint was added to this design, which sets the maximum allowable per-phase leakage inductance to 12 nH and the maximum allowable per-phase current ripple to 10 A.

TABLE III
CONVERTER PARAMETERS AND CONSTRAINTS

Parameter	Symbol	Value
Input Voltage	V_{in}	8 V
Output Voltage	V_{out}	1 V
Phase Current	I_{p}	20 A
Number of Phases	M	4
Switching Frequency	f	1.5 MHz
Maximum Length	x_{max}	9 mm
Maximum Width	y_{max}	9 mm
Maximum Height	h_{max}	2.5 mm

TABLE IV
PERFORMANCE METRICS OF DMR53 MATERIAL

Parameter	Symbol	Value
Relative Permeability	μ_r	900
Saturation Flux Density (100°C)	B_{sat}	460 mT
Core Loss Constant	k	2.07×10^{-10}
Frequency Exponent	α	2.31
Flux Density Exponent	β	2.68
Constant for Eq. (4)	k_i	4.856×10^{-12}

The phase current at which the core is optimized for greatly impacts the optimal design. If performance at lighter loads is more significant, inputting a phase current to the optimization routine that is around 30% of the targeted full load current will steer the optimization to reduce the core losses at the expense of dc resistance, which leads to higher winding losses at full load. As the Mini-LEGO converter is designed with a primary target of achieving high full load power density, a dc current of 20 A per phase is used to calculate the winding loss, as this is the thermal design point (TDP) of the Mini-LEGO converter. For designs in which the output current varies significantly during normal operation, one can consider using a weighted average cost function for the winding loss across the entire load range, or adding additional constraints to ensure that any selected design meets the targeted performance at specified load currents for thermal considerations.

The optimization routine framework is summarized in Fig. 13. The inductor loss, ripple current, and transient inductance can be calculated to obtain a design with minimized loss subject to specified constraints. As mentioned previously, the iGSE is used in this article, however, other core loss calculation methods are also applicable.

With the converter parameters and constraints set, a nonlinear optimization (*fmincon* in MATLAB) is conducted to minimize the total inductor loss. A saturation check is placed to ensure

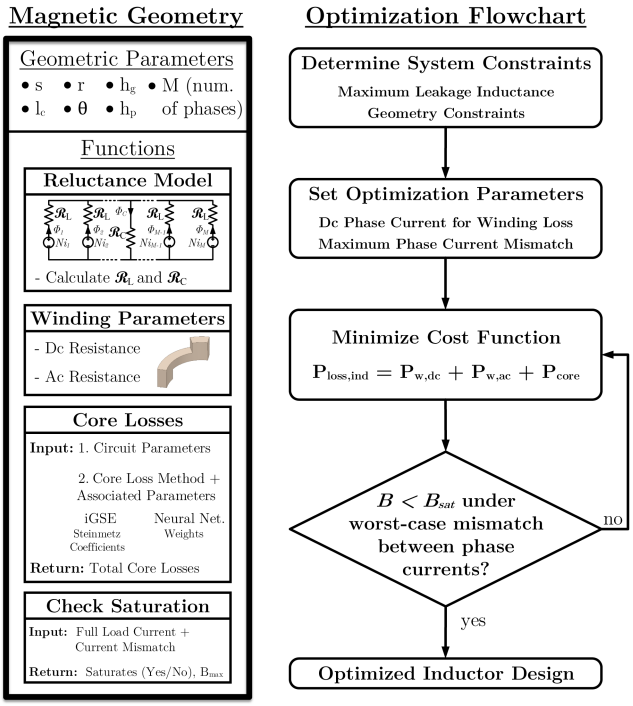

Fig. 13. Structure and flowchart for the vertical coupled inductor optimization routine. The design of the inductor is constrained by the maximum leakage inductance and the dimension. The optimization goal is the winding loss, core loss, and the core saturation margin against phase current imbalance.

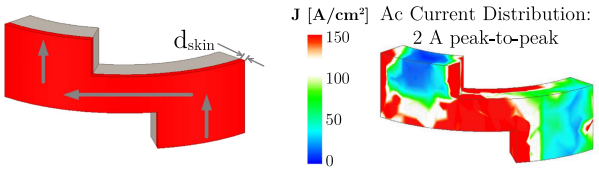

Fig. 14. (a) Approximation of the ac winding resistance for the vertical coupled inductor structure in Fig. 16 used in the optimization to compute the ac winding loss. It is assumed that the ac current only flows through the outer surface of the conductor. (b) ANSYS Maxwell 3D Eddy Current simulation of the current density distribution of one of the windings. Each winding is excited with a sinusoidal ac current of 2 A peak-to-peak at a frequency of 1.5 MHz.

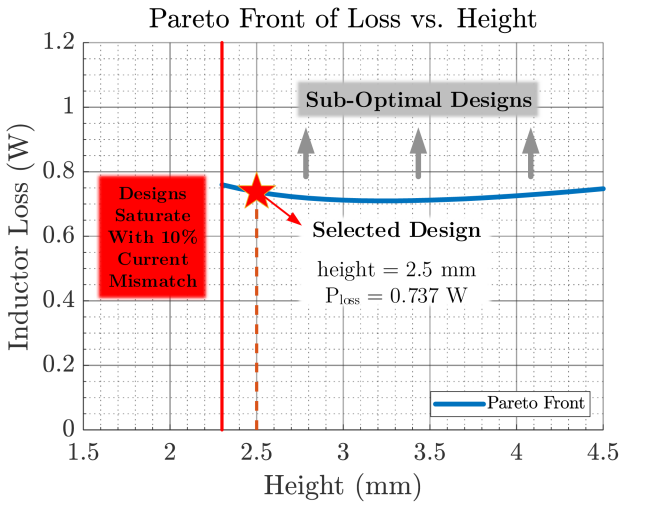

Fig. 15. Results of the optimization routine for the vertical coupled inductor showing the Pareto front of the inductor loss versus its height. The optimization is performed at a dc current of 20 A per phase and a switching frequency of 1.5 MHz. The selected height of the vertical coupled inductor for Mini-LEGO is 2.5 mm, resulting in an estimated loss of 0.737 W at full load.

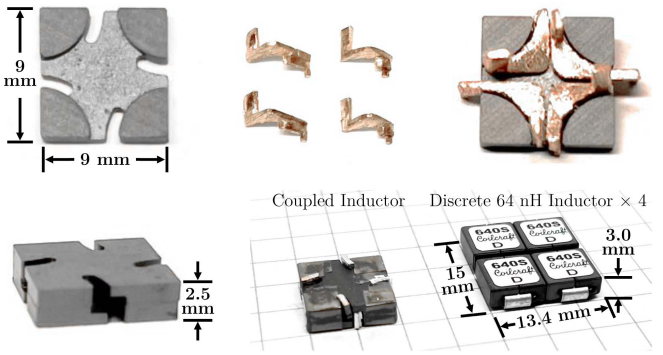

Fig. 16. Pictures of the designed vertical coupled inductor along with the four copper windings. The windings were milled with a fill factor ratio $f_r = 1$ (top right), and then later adjusted to the desired fill factor ratio $f_r = 0$ (top middle). The coupled inductor is pictured next to four discrete 64 nH inductors. For a similar per-phase ripple current, the volume of the coupled inductor is 34% of the volume and has 0.5 mm less height than the four discrete inductors. The coupled inductor has a per-phase transient inductance of 10.3 nH, over six times lower than 64 nH.

that the selected core design does not exhibit saturation under the full load operating condition, setting an upper bound on the maximum tolerable flux equal to 80% of the B_{sat} value provided by the manufacturer at 100 °C to avoid any reduction in the permeability.

Fig. 15 shows the Pareto front of the coupled inductor loss against the total height of the inductor. The optimization is conducted using a dc current of 20 A per phase. Below a height of 2.3 mm, no designs satisfy the constraint of avoiding saturation in the core under a maximum 10% dc current mismatch. At lower heights, the optimization routine attempts to decrease θ to reduce the core loss, however, reduced cross-sectional areas throughout the core causes larger core losses and larger overall losses. The minimum loss occurs when the height is 3.2 mm. A height of 2.5 mm was selected as a point that reduces the height, while only marginally increasing the overall inductor loss when compared to the loss at 3.2 mm. As the height increases, the winding path increases, and the optimization routine increases θ to compensate and reduce the winding resistance. This leads to the loss slightly increasing as the height is further increased.

D. Selected Inductor Design

Fig. 16 shows the selected vertical coupled inductor design after optimization. The parameters and dimensions of the inductor are summarized in Table V. Four copper windings are CNC milled and designed to connect with the multiphase buck board for an interposer-less design, with the coupled inductor resting directly on top of the top-side components. The windings were milled with a fill factor ratio $f_r = 1$ (as shown in the top right

TABLE V
PARAMETERS OF VERTICAL COUPLED INDUCTOR

Geometric Parameters (per Figs. 8 and 11)

Parameter	Symbol	Value
Length/Width	s	9 mm
Post Radius	r	3.5 mm
Cutout Length	l_c	0.95 mm
Plate Height	h_p	0.75 mm
Post Height	h_g	0.5 mm
Cutout Angle	θ	33°
Fill Factor	f_r	0

Size Compared to Set of Four Discrete Inductors

Parameter	Symbol	Value	
		Coupled	Discrete
Length	l	9 mm	13.4 mm
Width	w	9 mm	15 mm
Height	h	2.5 mm	3.0 mm
Volume	V	203 mm^3	603 mm^3

Per-Phase Circuit Parameters vs. Discrete Inductors †

Parameter	Symbol	Value	
		Coupled	Discrete
Ripple Current Inductance ‡	L_{ptr}/γ	63 nH	64 nH
Transient Inductance	L_{ptr}	10.3 nH	64 nH
Dc Resistance	R_{dc}	0.185 mΩ	0.123 mΩ

† Coilcraft SLC7530S-640, pictured in Fig. 16.
‡ The ripple current inductance for the coupled inductor depends on duty cycle (Eqn. 2 and 3) and is presented for $D = V_{out}/V_{in} = 0.125$.

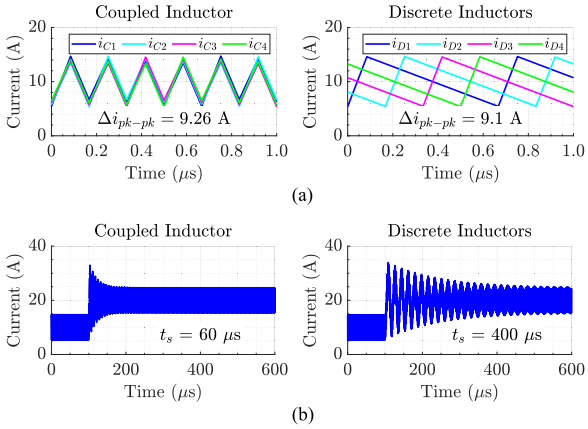

Fig. 17. Simulation waveforms of the coupled inductor using measured values (the measurement procedure is detailed in the Appendix) compared with discrete 64 nH inductors. A four-phase buck converter was simulated in open loop with $V_{in} = 8$ V, $V_{out} = 1$ V, $I_{out} = 40$ A, $f_s = 1.5$ MHz, and $C_{out} = 500\,\mu$F. (a) Steady-state phase-current waveforms for the coupled inductor (left) and the discrete inductors (right). The phase-current ripple is similar. (b) One phase-current waveform of the coupled inductor (left) and discrete inductors (right) in response to a load current transient from 40 to 80 A at $t = 100\,\mu$s, which corresponds to a 50% to 100% load transient.

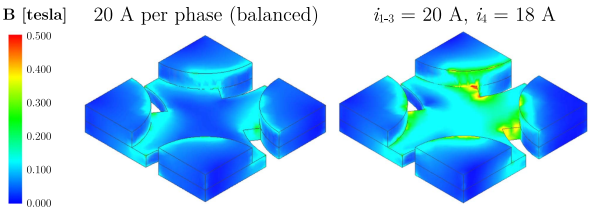

Fig. 18. Magnetostatic finite-element simulation (ANSYS Maxwell 3D) of the designed coupled inductor. The simulation was conducted both under balanced DC phase currents equal to 20 A per-phase (left) and a phase current imbalance of 10% (right) where three phases are carrying 20 A of current, while the fourth is carrying 18 A. The peak flux density of the core is 190 mT in the balanced condition and 390 mT in the imbalanced condition.

of Fig. 16), and then later adjusted to the desired fill factor ratio $f_r = 0$.

The coupled inductor was characterized to measure key inductance values when operating in the full system. Details on the measurement setup as well as extended measurement results are presented in the Appendix. The coupled inductor has a per-phase transient inductance (L_{ptr}) of 10.3 nH and has the same per-phase current ripple as a 63 nH uncoupled inductor, achieving a ripple reduction factor ($1/\gamma$) of over six.

Fig. 17(a) shows the simulated phase-current waveforms of the designed coupled inductor using the measured parameters compared with the discrete 64 nH inductors. The multiphase buck stage was simulated with $V_{\text{in}} = 8$ V, $V_{\text{out}} = 1$ V, $I_{\text{out}} = 40$ A, $f_s = 1.5$ MHz, and $C_{\text{out}} = 500\,\mu$F. The coupled inductor has a phase current ripple of 9.26 A and the discrete inductors have a ripple of 9.1 A during steady-state operation.

A load current transient from 40 to 80 A was simulated during open-loop operation, and the phase current transient is plotted in Fig. 17(b). The coupled inductor phase currents settle to within 2% of their new value in approximately 60 μs, around six times faster than the discrete inductors which take approximately 400 μs. The designed coupled inductor achieves similar per-phase steady-state ripple as the 64 nH discrete inductors, while reducing the transient inductance by more than a factor of six and occupying only one-third of the volume of four 64 nH discrete inductors.

A magnetotstatic finite-element simulation was performed to assess the flux distribution in the coupled inductor core, using ANSYS Maxwell 3D. Fig. 18 shows the dc flux density distribution during a magnetostatic simulation of the coupled inductor with equal phase currents as well as during a phase current imbalance. During the balanced operation simulation, each winding conducts 20 A, representing the full load operating condition. The maximum flux density in the core is 190 mT, well below the saturation flux density of the DMR53 material (460 mT at 100 °C). When a 10% phase current mismatch is introduced, which is the imbalance that the inductor was designed to handle, the maximum flux density in the core increases to 390 mT. This high flux density is only present in a small volume of the core, and results in a 3% decrease in magnetizing inductance.

VI. EXPERIMENTAL VERIFICATION

The Mini-LEGO prototype was assembled and tested at an input voltage of 48 V up to a maximum output current of 240 A. The assembly procedure is shown in detail in pictured in Fig. 19, along with an overall system height breakdown and

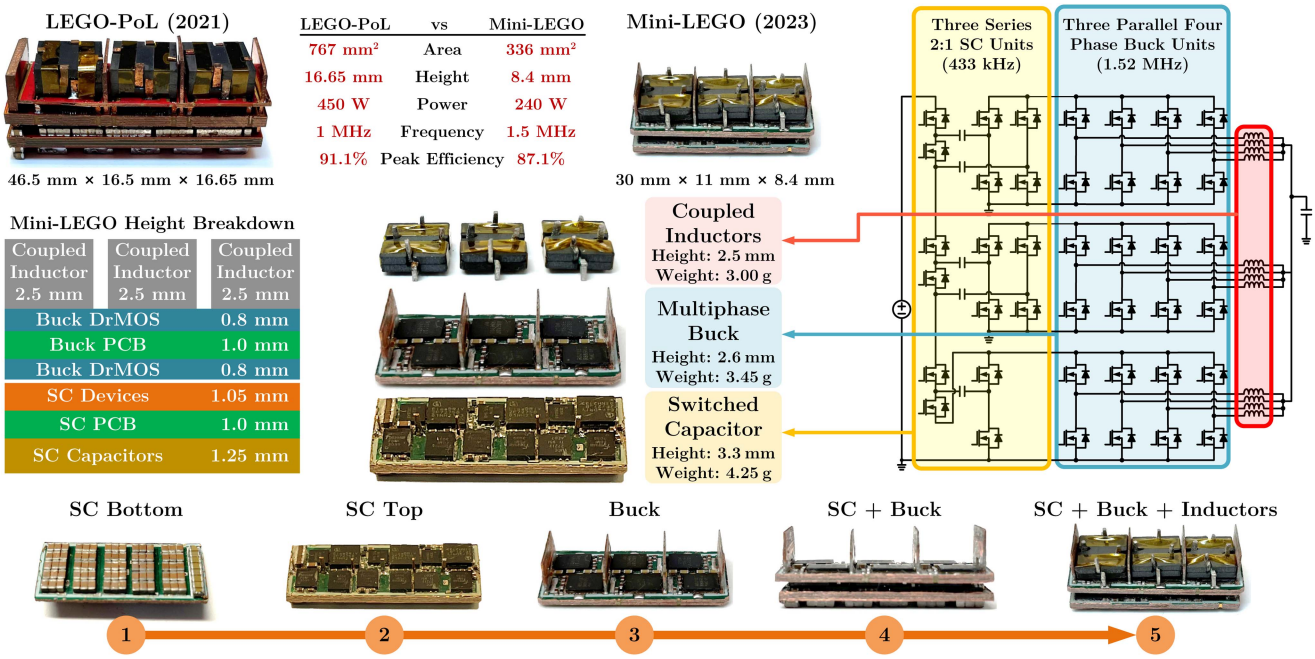

Fig. 19. Assembly procedure of the Mini-LEGO converter (bottom); simplified schematic highlighting the SC stage, buck stage, and coupled inductors (right); zoomed-in images of each stage and inductors (middle); height breakdown of the Mini-LEGO prototype (left); comparison between the Mini-LEGO converter and the LEGO-PoL converter presented in [13] (top). The power stage area of the Mini-LEGO prototype is 30 mm × 11.2 mm = 336 mm^2. The height of the prototype is 8.4 mm. The current density is 0.71 A/mm^2 at 240 A and the power density is 1390 W/in^3 at 1 V and 240 A.

a comparison to the initial LEGO-PoL prototype from [13]. Fig. 20 shows the experimental setup and test bench. Digital multimeters are used to take automated efficiency measurements. A microcontroller is programmed to generate all of the PWM signals. The Mini-LEGO converter is mounted on an output and control motherboard that interfaces with the input power source, electronic loads, and the microcontroller.

A. Steady-State Operation

Fig. 21 shows the key waveforms of the SC stage at an output voltage of 1 V and an output current of 240 A. The flying capacitors $C_1 - C_5$ charge up to 40, 32, 24, 16, and 8 V, respectively. The ac coupled waveforms of the voltage across C_2 and C_4 show that, since C_2 is biased at a higher dc voltage, the lower effective capacitance results in a higher ripple. The triangular shape of the voltage ripple show that the capacitors are being soft-charged by the coupled inductors in the multiphase buck stage.

The SC stage outputs three virtual intermediate bus voltages that are automatically balanced to a dc voltage level of 8 V, as can be seen in Fig. 22. V_{BUS1} has the highest ripple voltage as C_1 has the lowest effective capacitance. At the full load current of 240 A, the peak-to-peak ripple voltage is 2.4 V. The ripple frequency of the virtual intermediate bus voltages is 865.8 kHz, twice the switching frequency of the SC stage (432.9 kHz).

Fig. 23 shows the four switch node voltages from the second multiphase buck submodule. Each phase switches at 1.515 MHz. The four phases are interleaved, with a 90° phase shift between each of the phases. The envelope of the switch node voltages approximately follows V_{BUS2}, which is the input voltage for the second multiphase buck submodule.

B. Transient Operation

Two transient tests were performed on the Mini-LEGO converter. The first, shown in Fig. 24, was an open-loop duty cycle transient, where the duty cycle of the twelve PWM signals of the multiphase buck stage were stepped from 15% to 20%. The output voltage settles to its new voltage level within 12 μs. During the transient, the ripple on the virtual intermediate bus voltages increase as the output capacitors are being charged. The speed at which the output voltage changes to its new level depends on the output LC filter. Using a coupled inductor greatly reduces the effective inductance seen during a transient as compared to a discrete inductor with the same steady-state ripple current.

A voltage-mode control method was implemented using a TMS320F28388D microcontroller to test the system under closed-loop operation. While demonstrating transient performance in response to an extreme load current transient ($\geq$ 1 A/ns) is beyond the scope of this paper, a load current transient from 50 to 200 to 50 A (a jump of 150 A, equal to 62.5% of the full load current) was performed. Fig. 25(a) shows the intermediate bus voltages, which remain stable, with increased ripple as the load current increases. Fig. 25(b) shows the output voltage, which exhibits a 100 mV voltage spike as the load current steps down at a slew rate of 5 A/μs. More advanced control techniques, such

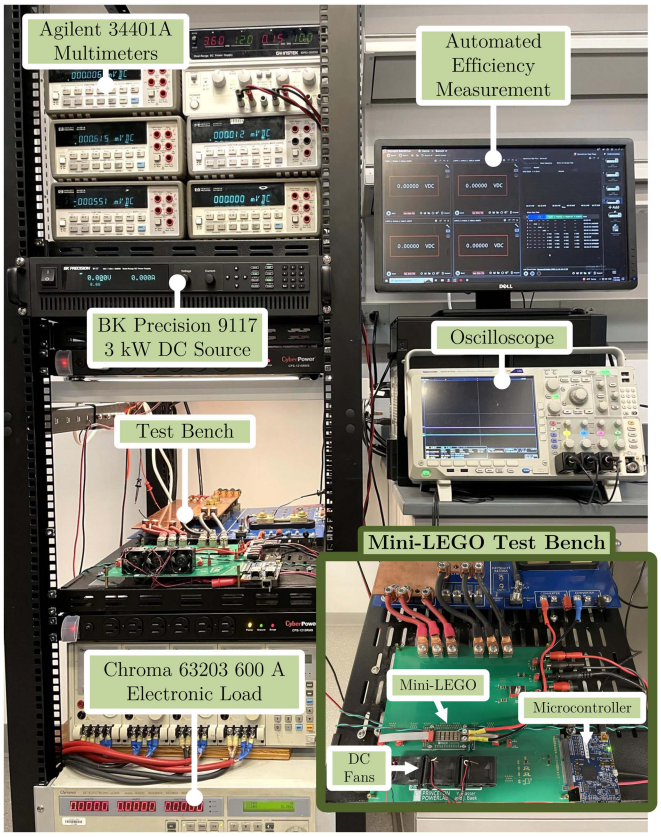

Fig. 20. Experimental test setup for characterizing converter performance. The Mini-LEGO converter is connected to an output motherboard that hosts the fans and interfaces with a DC source, microcontroller, and electronic load.

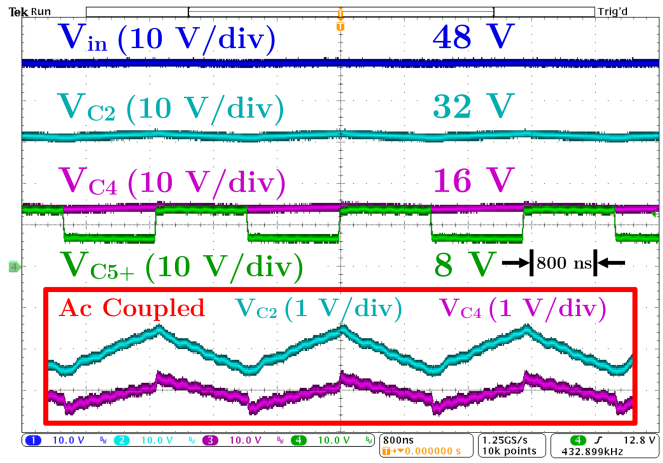

Fig. 21. Measured waveforms of the input voltage, differential voltages across C_2 and C_4, and switch node voltage V_{C5+} (labeled on Fig. 4) during 48 to 1 V operation at an output current of 240 A. The SC stage is switching at 432.9 kHz. The AC coupled waveforms of V_{C2} and V_{C4} highlight that the flying capacitors are being soft-charged by the inductor current in the multiphase buck stage.

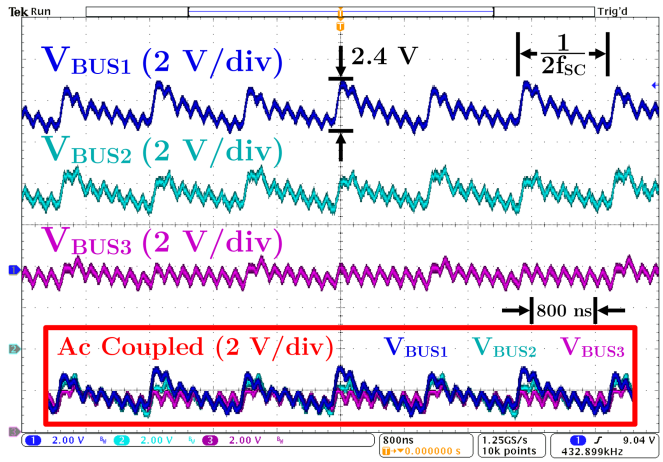

Fig. 22. Measured waveforms of the three virtual intermediate bus voltages during 48 to 1 V operation at an output current of 240 A. V_{BUS1} has the highest peak-to-peak voltage ripple at 2.4 V, since flying capacitors C_1 and C_2 have the lowest effective capacitance. The ripple frequency of the intermediate bus voltage is equal to twice the switching frequency of the SC stage (432.9 kHz). All three intermediate bus voltages are balanced at 8 V.

as current-mode control, can be used to improve the closed-loop control bandwidth and improve the transient performance [33].

C. Efficiency Measurement

Fig. 26 summarizes the efficiency of the Mini-LEGO converter with 48 V input and output voltages of 0.8, 1.0, and 1.2 V, with the SC stage switching at 432.9 kHz, and the multiphase buck stage switching at 1.515 MHz. The efficiency is presented with and without the gate drive losses included. Gate drive losses consist of the power consumed by the SC isolated gate drivers for the floating switches, powered by an auxiliary 10 V supply, and the power consumed by the SC and multiphase-buck DrMOS devices, powered by an auxiliary 5 V supply. The input voltage and output voltage were measured across the input and output capacitors. The data were measured in 10 A intervals. For the 1.0 and 1.2 V tests, the full load current was determined by the point at which the multiphase buck stage DrMOS junction temperatures were less than or equal to 100 °C. For the 0.8 V curve, the data stops at 210 A due to the voltage drop between the converter and the electronic load used which limits the amount of current from the electronic load. At an output voltage of 1.0 V, the converter achieves a peak efficiency of 87.1% at 120 A, and a full load efficiency of 84.1% at 240 A, without the gate driving losses. Including the buck stage gate driving losses of 4.5 W and the SC stage gate driving losses of 1.4 W, the peak efficiency at 1.0 V is 84.1% at 170 A and the full load efficiency is 82.3% at 240 A.

D. Thermal Analysis

To understand the cooling mechanisms of the Mini-LEGO converter prototype, thermal simulations were conducted to determine what the target power density of the converter would be based on the cooling resources available. For the experimental setup presented in Fig. 20, the decision to use forced air cooling was made, using an output motherboard that was sized to interface with all of the measurement equipment. These two factors—cooling and interface—impact the thermal performance of a converter designed for vertical power delivery and must be considered during the overall system design. The

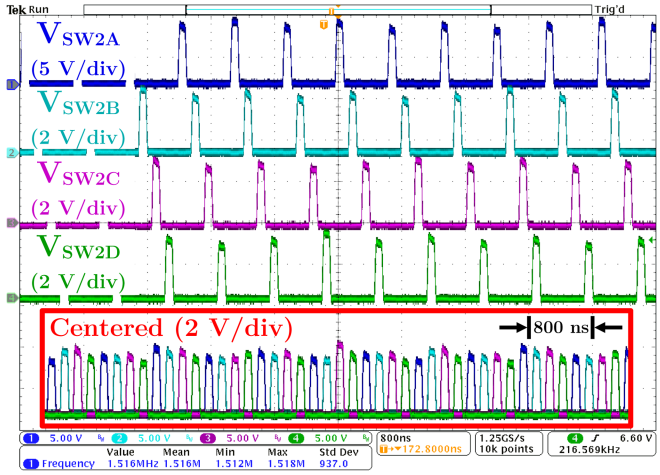

Fig. 23. Measured waveforms of the switch node voltages in the second submodule of the multiphase buck stage ($f_s = 1.515$ MHz) during 48 to 1 V operation at an output current of 240 A. The input voltage of the second submodule of the multiphase buck stage is equal to V_{BUS2}.

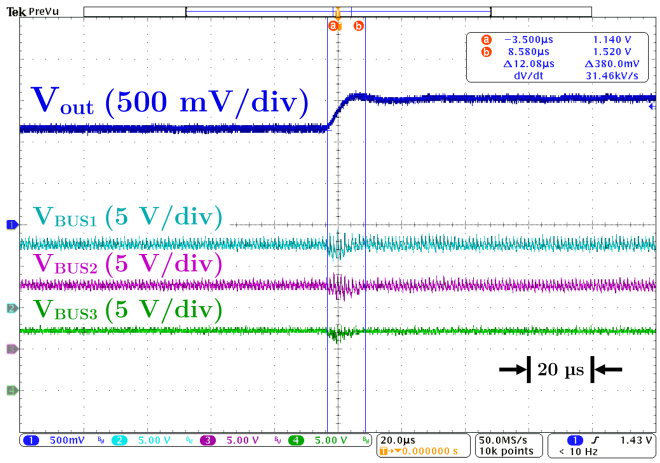

Fig. 24. Measured waveforms of the output voltage and three virtual intermediate bus voltages in response to an open-loop duty cycle transient from 15% to 20% during 48 to 1 V operation at an output current of 120 A. The output voltage changes from 1.14 V to within 2% of the new output voltage of 1.5 V within 12 μs. The output capacitance is 2.5 mF.

availability of liquid cooling resources, or the heat dissipation of loads that are placed directly on the same motherboard as the converter, will change the design considerations required for optimal thermal performance.

Fig. 27 shows the results of a thermal simulation using ANSYS Icepak 3-D, which was performed at full load ($V_{\text{out}} = 1$ V, $I_{\text{out}} = 240$ A, and $P_{\text{loss}} = 45$ W) for the Mini-LEGO converter in the experimental setup of Fig. 20. The DrMOS devices in the buck stage, DrMOS devices in the SC stage, and dual-channel MOSFETs in the SC stage are modeled as a two-resistor thermal network, using the values provided in the datasheets for junction-to-case resistance (R_{jc}) and junction-to-board resistance (R_{jb}). The temperature distribution is shown, with an expected buck stage DrMOS temperature of 95.4 °C. A second simulation using

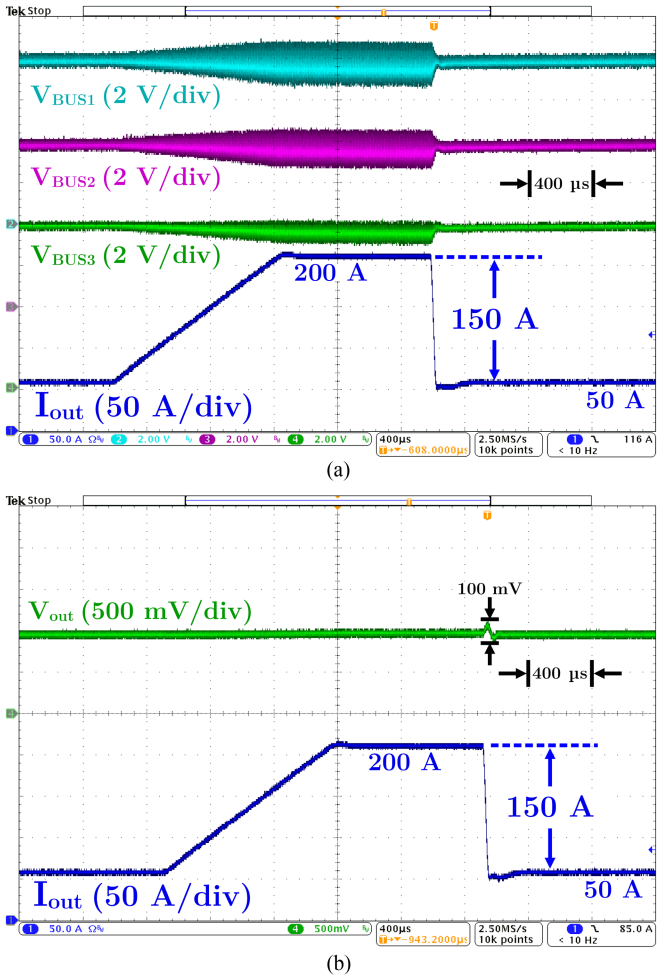

Fig. 25. Measured waveforms during a load current transient from 50 to 200 A to 50 A (62.5% load step) of (a) the three intermediate bus voltages, and (b) the output voltage during 48 to 1 V operation. A voltage-mode control method was implemented using a TMS320F28388D microcontroller. The output capacitance is 2.5 mF.

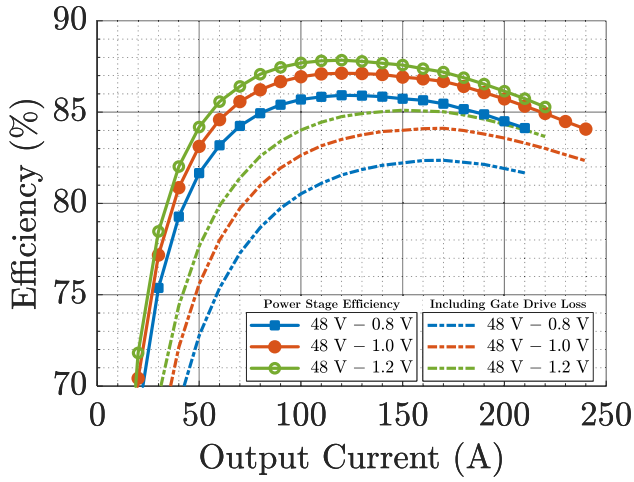

Fig. 26. Measured efficiency of the Mini-LEGO converter with and without gate driving losses during 48 to 0.8 V, 1.0 V, and 1.2 V conversion. For 48 to 1 V, without the gate driving losses, the Mini-LEGO converter achieves a peak efficiency of 87.1% at 120 A and a full load efficiency of 84.1% at 240 A.

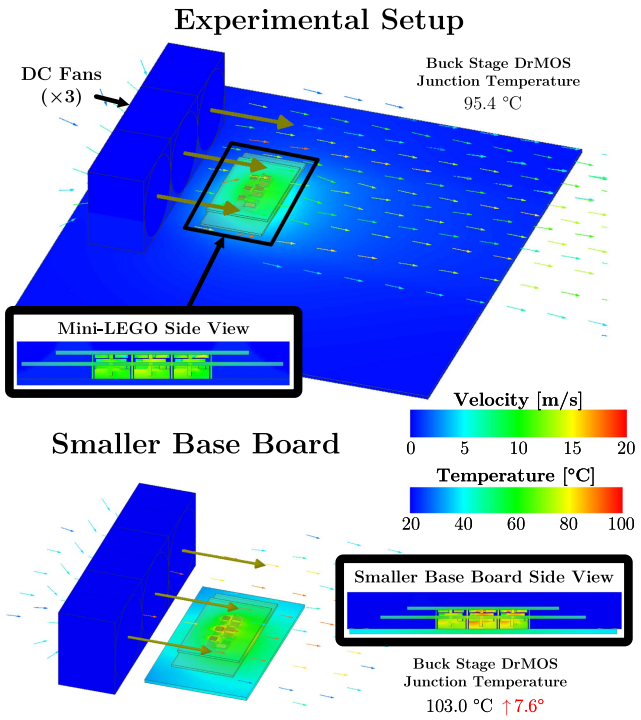

Fig. 27. ANSYS Icepak 3-D thermal simulation of the Mini-LEGO converter connected to the output motherboard shown in Fig. 20 (top) and a smaller output motherboard (bottom). The thermal simulation is done for the Mini-LEGO operating at an output voltage of 1 V and output current of 240 A, with 45 W of loss. The buck stage DrMOS junction temperature is 95.4 °C with the larger output motherboard and increases to 103 °C with the smaller output motherboard. The enlarged PCB for carrying high current also behaves as a cooling channel for removing heat.

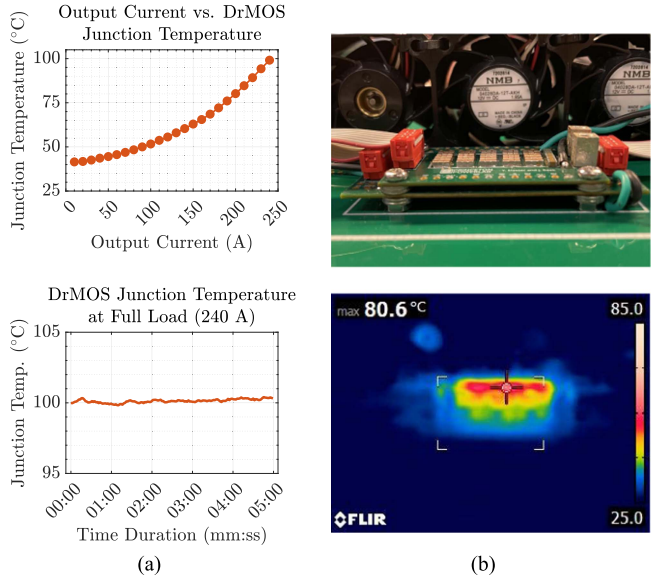

Fig. 28. (a) Plot of the output load current vs. DrMOS junction temperature for the Mini-LEGO converter during the 48 to 1 V operation test (top). The temperature reported is the temperature at the end of a five minute interval where the converter is left running at the specified load current. The bottom plot shows the junction temperature at the full load operating point during the duration of the five minute time interval. (b) Side view image and corresponding thermal image of the Mini-LEGO converter at the full load operating point of 240 A.

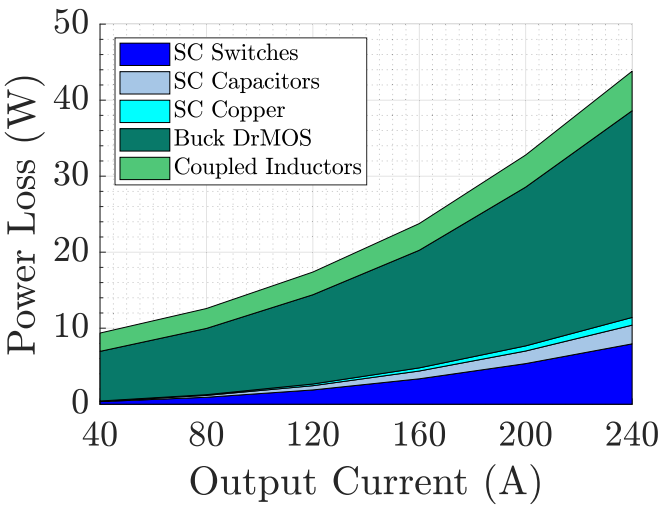

Fig. 29. Calculated loss breakdown of the Mini-LEGO converter during 48 to 1 V operation. The SC stage loss is split into switching and conduction losses due to the switches, energy and conduction losses due to the capacitors, and loss due to the PCB and vertical copper connectors. In the multiphase buck stage, the loss is divided into the device switching and conduction losses and the winding and core losses from the coupled inductors.

a small motherboard was conducted. With reduced cooling capability from the motherboard, the DrMOS junction temperature increases by 7.4 to 103 °C.

Junction temperature data from the multiphase buck stage DrMOS devices is plotted in Fig. 28(a) during a 48 to 1 V operation test. At each output current level, the converter was left operating for 5 min before the current is increased to the next higher level. The temperature is plotted at the end of each interval. The junction temperature is also plotted over the full 5-min interval for the full load operating point. At full load, the DrMOS junction temperature is approximately 100 °C, which matches well with the ANSYS Icepak 3-D simulation of Fig. 27. Fig. 28(b) shows the fan setup and a captured thermal image at 240 A. Three 36 cubic feet per minute (CFM) fans are placed 2 cm away from the converter. The thermal image taken from the side view shows the PCBs reaching roughly 81 °C during full load operation.

VII. Performance Benchmarking and Discussion

A theoretical loss breakdown is presented in Fig. 29. The calculations use experimentally measured duty ratios and junction temperatures to account for the temperature impact on switch resistance values. In the SC stage, the loss comes from the dual-channel MOSFETs and synchronous rectifier DrMOS devices, the PCB copper and vertical copper rods that connect the two stages together, and both the flying and filter capacitors. In the buck stage, the loss comes from the DrMOS devices and the coupled inductor. The coupled inductor loss is discussed in detail in Section V-C. At 120 A, the peak efficiency point, the converter has 17.8 W of loss, with 15 W coming from the multiphase buck stage. Most of the loss comes from the buck stage DrMOS devices, which are switching at a high frequency.

TABLE VI
PERFORMANCE COMPARISON OF THE MINI-LEGO VRM AGAINST OTHER 48-TO-1-V POINT-OF-LOAD VOLTAGE REGULATOR DESIGNS

Year	Note	At Peak Efficiency			At Full Load Efficiency				Switching Frequency‡
		Output Current	Efficiency	Power Density†	Output Current	Efficiency	Power Density†	Area Density	
This Work	Mini-LEGO	160 A	84.1%	929 W/in^3	240 A	82.3%	1390 W/in^3	0.71 A/mm^2	1515 kHz
2022	LEGO-PoL [13]	190 A	88.4%	124 W/in^3	450 A	84.8%	294 W/in^3	0.30 A/mm^2	1000 kHz
2020	Sigma [34]*	50 A	94.0%	256 W/in^3	80 A	92.5%	410 W/in^3	0.13 A/mm^2	600 kHz
2020	Vicor [35], [36]	120 A	90.1%	224 W/in^3	214 A	≈87%¶	400 W/in^3	0.20 A/mm^2	1025 kHz
2021	On-Chip [37]	1.5 A	90.2%	37 W/in^3	8 A	76.0%	198 W/in^3	0.03 A/mm^2	2500 kHz
2021	ADI [38]	30 A	90.8%	53 W/in^3	50 A	88.1%	89 W/in^3	0.06 A/mm^2	350 kHz
2021	24 V VIB [15]	144 A	93.3%	75 W/in^3	450 A	88.1%	232 W/in^3	0.16 A/mm^2	417 kHz
2022	SDIH [39]§	50 A	81.4%	285 W/in^3	116 A	73.2%	663 W/in^3	0.15 A/mm^2	750 kHz
2022	Dickson^2 [40]	100 A	91.6%	133 W/in^3	270 A	87.7%	360 W/in^3	0.14 A/mm^2	280 kHz
2023	MSC-PoL [20]	80 A	91.1%	221 W/in^3	220 A	85.8%	607 W/in^3	0.26 A/mm^2	500 kHz
2023	Sw. Bus [41]	380 A	92.4%	192 W/in^3	1200 A	87.5%	607 W/in^3	0.23 A/mm^2	200 kHz
2023	MHB-CDR [42]‖	40 A	93.1%	345 W/in^3	120 A	87.8%	1037 W/in^3	0.15 A/mm^2	600 kHz

† The power density is calculated with the box volume (maximum length × width × height) of the prototype, including the gate drive circuitry.
‡ The switching frequency of the voltage regulation stage, which strongly influence the transient dynamics of the voltage regulator.
* The gate drive loss is not included in the efficiency of the Sigma converter.
¶ The full load efficiency (Vicor) 48-V-to-1-V solution is not available and an estimate is presented here for comparison purposes.
§ The efficiency (SDIH) including the gate drive losses is calculated using the average gate drive energy per switching cycle provided in [39].
‖ The efficiency and density (MHB-CDR) is reported for 48 V to 1.8 V conversion.

At 240 A, there is 45 W of loss, with around 10 W from the SC stage and 35 W from the multiphase buck stage. The efficiency of the SC stage at this point is 95.5%, and the efficiency of the multiphase buck stage is 88.1%.

The Mini-LEGO converter was benchmarked against state-of-the-art 48-V-to-1-V voltage regulator modules from both academia and industry, as presented in Table VI and Fig. 30. The top section compares the Mini-LEGO against the LEGO-PoL prototype presented in [13]. The Mini-LEGO switches at 1.5 times the frequency, and improves on both the power density and the current area density, by trading off a 4.3% peak efficiency and a 2.5% full load efficiency. This implementation includes all of the gate drive circuitry within the power stage area.

The Mini-LEGO converter is able to achieve extremely high power density and current area density compared to existing state-of-the-art designs. In terms of regulation stage switching frequency, it switches at the highest frequency of the discrete implementations considered; its switching frequency is only exceeded by fully integrated solutions such as the one presented in [37]. The peak efficiency of the Mini-LEGO is lower than most other designs. However, due to the low maximum phase current, the full load efficiency is comparable to other designs despite the lower peak efficiency. Better magnetic materials more suitable to the 1–10 MHz range can help to reduce the fixed losses present in the multiphase buck stage to obtain higher peak efficiency. While the latest DrMOS devices are suitable for switching frequencies up to 2 MHz, their performance past 1 MHz still limits the overall system efficiency at higher switching frequencies.

The DrMOS devices used in the multiphase buck stage were optimized for 1 MHz, which placed limitations on how fast the devices could switch before performance significantly degraded.

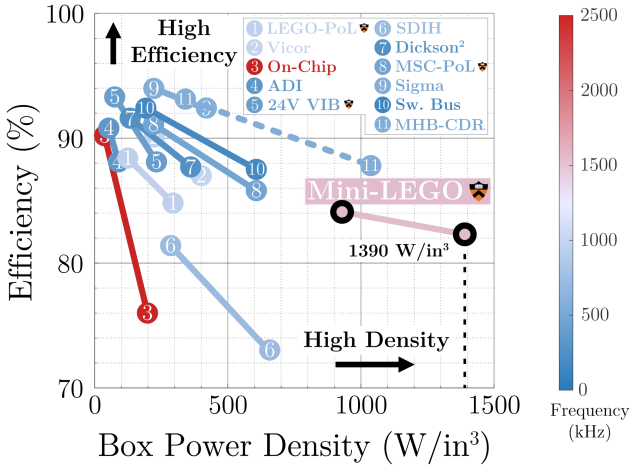

Fig. 30. Plot of the peak efficiency and box power density at the peak efficiency point, as well as the full load efficiency and box power density at the full load efficiency point, connected with a line, for all of the 48-V-to-1-V converters presented in Table VI. All designs plotted include the gate driving size and all include the gate driving losses, with the exception of "⑨ Sigma." The line for "⑪ MHB-CDR" is dashed as the density and efficiency are reported for 48-V-to-1.8-V conversion. The Mini-LEGO achieves unprecedented power density at both the peak and full load efficiency points, achieving a 1390 W/in^3 density at 240 A of output current with 84.1% efficiency. The Mini-LEGO converter was optimized to achieve the highest density with the highest switching frequency while sacrificing efficiency, given sufficient cooling capability near microprocessors.

In regards to the overall system height, further opportunities to reduce the passive component size will present themselves with devices that can maintain acceptable performance at 2 MHz and beyond. The coupled inductor still occupies roughly 30% of the height, similar to the original LEGO-PoL design.

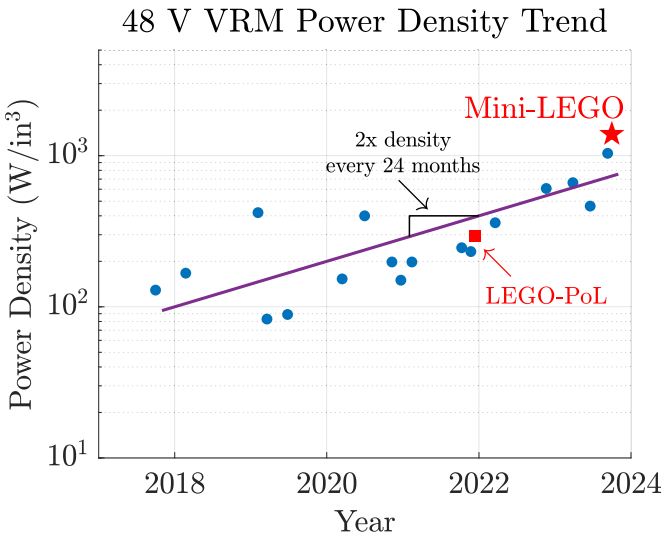

Fig. 31. Trend of the power density (in W/in^3) of various 48 to 1 V CPU VRMs. The date represents either the date of publication in a journal, the date presented in a conference, or the date of release of the initial datasheet revision [13], [15], [20], [23], [34], [35], [36], [37], [38], [39], [40], [41], [42], [43], [44], [45], [46], [47], [48]. The Mini-LEGO design significantly improves on the power density of the LEGO-PoL design after 24 months of circuit-magnetics co-optimization.

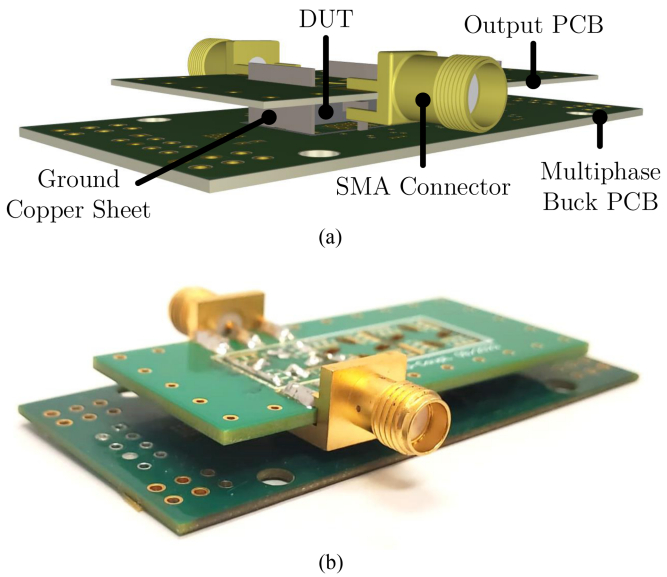

Fig. 32. (a) Altium 3-D Rendering of the test fixture assembly and (b) fully assembled test fixture with DUT in place. The DUT is connected to the multiphase buck board used in the Mini-LEGO converter. An output board is designed and connected to the DUT and ground copper sheets. Two SMA connectors are placed on the output board and used to interface with the VNA to conduct the measurements.

Fig. 31 shows a plot of the power densities of 48 V VRMs that have been designed over the last six years. Designs from both academia and industry are plotted based on the date in which the design was published in a journal or the date of release of the initial datasheet revision [13], [15], [20], [22], [23], [34], [35], [36], [37], [38], [39], [40], [43], [44], [45], [46], [47], [48], [49], [50]. Fitting a trend line to the data highlights

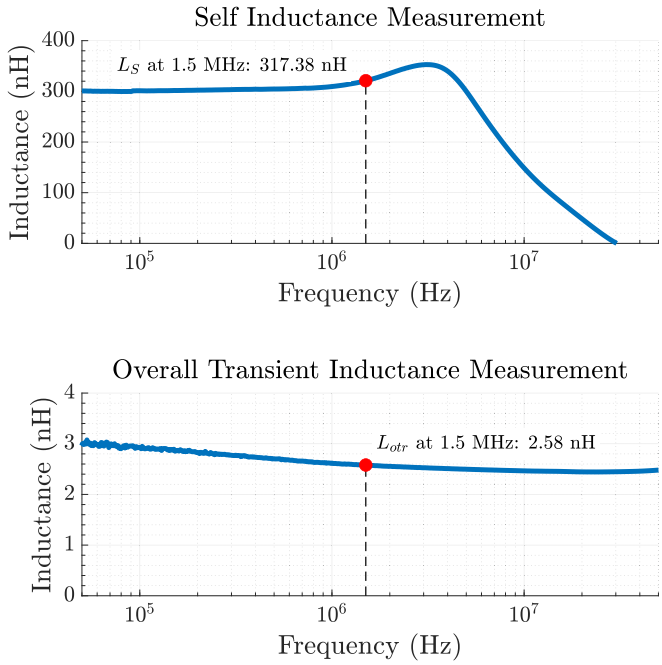

Fig. 33. Measured data of the self inductance (top) and overall transient inductance (bottom) of the vertical coupled inductor. The self inductance is 317.38 nH at 1.5 MHz, and the overall transient inductance is 2.58 nH at 1.5 MHz. The measurements include parasitic inductances of PCBs and GND copper sheets on paths.

that designers have been roughly doubling the power densities of 48 V VRMs every two years—analogous to the empirical observation of Moore's Law, which observed a doubling in the number of transistors in an integrated circuit every 18–24 months. The Mini-LEGO converter continues this trend, and achieves a two times reduction in height and two times reduction in area over the original LEGO-PoL design in approximately 24 months. As semiconductor device technology continues to improve and support higher frequency operation, particularly with the advent of Gallium Nitride (GaN) power devices, this, along with continued development of magnetic materials for higher frequency operation, enables designers to continue to further reduce passive component sizes and increase power densities [51]. Circuits-magnetics codesign to maximize the benefits of magnetic components in a topology while shrinking their size will be essential in further continuing this trend.

VIII. Conclusion

This article presents the design of the Mini-LEGO converter, a 1.5-MHz 240-A 48-V-to-1-V CPU voltage regulator module with a LEGO-PoL architecture. The area of the converter is 336 mm^2 and the height is 8.4 mm. The Mini-LEGO design improves on the previous iteration of the LEGO-PoL architecture with more compact device implementation, simplified gate drive circuitry, an optimized vertical coupled inductor structure, smaller height, and reduced overall system volume. The Mini-LEGO prototype achieves a power density of 1390 W/in^3, a current area density of 0.71 A/mm^2, a peak efficiency of 87.1% at 120 A, and a full load efficiency of 84.1% at 240 A for

48–1 V voltage conversion with vertical power delivery. The Mini-LEGO design reduces the area and height by a factor of two and triples the power density of the previous LEGO-PoL design (considering the power stage only) after approximately 24 months of circuit-magnetics co-optimization.

APPENDIX
VERTICAL COUPLED INDUCTOR CHARACTERIZATION

This appendix discusses how to characterize the parameters of vertical coupled inductor (device under test, or DUT), designed in Section V that determine its steady-state and transient performance when it is fully assembled in the Mini-LEGO converter. Two measurements were taken to fully characterize the coupled inductor's electrical performance: the self inductance (L_S), and the overall transient inductance (L_{otr}). These two measurements were then used to determine the full inductance matrix, and thus the circuit performance of the coupled inductor.

A test fixture was designed to characterize the inductor's performance. Inductances along the winding path, such as the inductance contributed by the PCBs, contribute to the steady-state and transient performance of the inductor. The test fixture is designed to include all of these in the measurement setup. Fig. 32(a) shows a rendering of the full assembly of the test fixtures for the DUT. The multiphase buck board (see Section III) is placed on the bottom. The DUT is connected to the multiphase buck board in the same manner as it would be during normal converter operation. A new fixture was designed for the output connection, which is placed on top of the DUT and houses two SMA connectors. These connectors interface with a vector network analyzer (VNA), which is used to conduct the inductance measurements. The fully assembled test fixture assembly is shown in Fig. 32(b).

The self inductance was measured by electrically connecting the switch node, which is connected to the inductor winding, to the ground pad of the DrMOS adjacent to the switch node to complete the signal path. The overall transient inductance is measured by connecting all four of the switch nodes to their adjacent DrMOS ground pad. This places all four of the phases in parallel, and characterizes the overall transient inductance, which is equivalent to the per-phase transient inductance divided by the number of phases ($L_{\text{otr}} = {}^{L_{\text{ptr}}}/_{M}$, where M is the number of phases). The inductance measurements are plotted in Fig. 33. The measured self-inductance at 1.5 MHz is 317 nH and the measured overall transient inductance is 2.58 nH. These values can be used to calculate the full inductance matrix of the coupled inductor using

$$L_M = \frac{1}{M-1}\left(M \times L_{\text{otr}} - L_S\right) \tag{6}$$

assuming that the inductor is fully symmetric [30]. Each phase is assumed to have the same self inductance, based on symmetry. The accuracy of this assumption is limited only by imperfections in construction. The mutual inductances are also approximated to be the same between any two given phases. The full inductance matrix based on measurements of the fabricated coupled inductor is

$$\mathbf{L} = \begin{bmatrix} 317.38 & -102.35 & -102.35 & -102.35 \\ -102.35 & 317.38 & -102.35 & -102.35 \\ -102.35 & -102.35 & 317.38 & -102.35 \\ -102.35 & -102.35 & -102.35 & 317.38 \end{bmatrix} \text{nH}. \tag{7}$$

This correlates to the fabricated vertical coupled inductor having a per-phase transient inductance of 10.3 nH and steady-state ripple amplitude in the circuit with a duty cycle of 0.125 equal to that of an uncoupled 63 nH inductor. The copper winding dc resistance was also measured using a milliohm meter at 0.185 mΩ.

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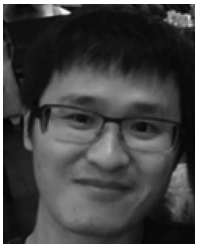

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