NPL.H: Neutral-Point-Less H-Type 3-Level Inverter

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***Abstract*—This article introduces a neutral-point-less H-type (NPL.H) 3-level dual inverter topology for motor drive applications. This multilevel topology craftily eliminates the neutral clamp and neutral point current altogether, resulting in a drastically lower minimum dc-link capacitance, compared with conventional 3-level inverter topologies, while retaining the multilevel benefits. NPL.H has additional merits, including lower output harmonics, lower current stress, and lower capacitor current ripple. The topology is optimal for balanced 6-phase, dual 3-phase, or 3-phase open-end winding motors. This article proposes a low-order frequency form (LoF) for fast and accurate calculations of the important circuit variables (e.g., rms currents of switching devices, inverter bridge input, and dc-link capacitor, and the voltage ripple of the dc-link capacitor), and demonstrates an example in detail with the sinusoidal pulsewidth modulation. Many practical design parameters (e.g., dead time) are reflected in our method to enhance the accuracy of the analytical model. The theoretical rms current expressions of NPL.H are successfully derived via LoF. Through simulation and experiment, we validate the precision and effectiveness of LoF as well as the strengths of the NPL.H topology. Our NPL.H can eliminate at least 75% of the dc-link capacitance of the conventional T-type 3-level topology while maintaining the same voltage ripple performance under otherwise same operating conditions, and up to 73% compared with the traditional 2-level inverter. Our new NPL.H topology unlocks a significantly higher power density for electric transportation and other high-power applications, where the size of a dc-link capacitor bank has traditionally been a major blockade for a high power density.**

***Index Terms*—DC-link, drive, dual, H-type, inverter, low-order frequency form (LoF), low-order, motor, multilevel, neutral-point-clamped (NPC), neutral-point-less, neutral-point-less H-type (NPL.H).**

I. Introduction

THE dual three-phase inverters have become one of the mainstream research topics due to the increasing demands in high-power medium-voltage motor drive applications, such as electric vehicles (EVs) [1], railway traction [2], elevator, aerospace [3], and electric naval propulsion [4]. Compared with traditional single three-phase inverters, the dual versions have the advantages of lower current stress, lower dc-link capacitor current/voltage ripples, higher power density, improved fault-tolerant capability, and lower torque harmonics for both dual three-phase motors or single three-phase open-end winding (OEW) motor applications [5], [6], [7], [8], [9], [10], [11], [12], [13], [14]. Meanwhile, the three-level (3 L) inverters are also drawing increasing attention for large-capacity medium-voltage applications, as they improve output voltage quality, reduce device voltage stresses, reduce conduction and switching losses, and enhance a fault tolerance [15], [16], [17], [18]. The combination of a 3 L inverter and a dual three-phase structure can further improve a motor drive's overall performance and reliability.

A dual three-phase motor drive based on two sets of independent T-type 3 L inverters is proposed in [19]. The dc-link capacitor voltages are well balanced in both steady-state and transient conditions. In addition, the current flow through the dc-link capacitors is reduced due to the interleaved modulation strategy. Nevertheless, the number of switches, the size, and the overall cost are greatly increased compared with two-level inverters. The authors in [20] and [21] introduced 3 L dual-output inverters based on the neutral-point-clamped (NPC) 3 L inverter to reduce the number of switches in comparison with the conventional two 3 L inverters. However, the switching modes are limited, and the neutral point voltage is difficult to be balanced [20]. In [21], a new topology was formed by adding eight switches and six clamp diodes for a lower neutral current and a better neutral point voltage balancing. However, not only has the number of switches increased, complicating the modulation but also the neutral point current and voltage fluctuations cannot be sufficiently suppressed, necessitating the presence of a large dc-link capacitance.

This article introduces a neutral-point-less H-type (NPL.H) 3 L dual inverter topology for motor drive applications. In addition to the aforementioned benefits (i.e., lower minimum dc-link capacitance, retained multilevel benefits, lower output harmonics, lower current stress, and lower capacitor current ripple), NPL.H also eliminates the necessity of the voltage balance among dc-link capacitors in a traditional multilevel inverter topology. This article has three main contributions.

First, this article presents a *neutral-point-less* multilevel inverter topology and includes analytical derivations of a dc-link capacitor's voltage and current ripples for the first time. A ripple performance analysis has traditionally played a vital role in evaluating the performance of an inverter, designing parameters, and selecting appropriate devices [22], [23], [24], [25], [26],

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TABLE I
COMPARISON OF THE PROPOSED LOF ANALYTICAL METHOD WITH EXISTING METHODS

Method	Simplicity	Applied range	Object	Calculation frequency	Accuracy
Indirect method [26], [27]	Simple	Limited phase structures	dc-link capacitor voltage ripple	Fundamental frequency	Low
Integral-based method [28]–[32]	Complex	Arbitrary phase structures	Device rms currents, dc-link capacitor rms current and voltage ripple	Switching frequency	Medium
Proposed LoF method	**Simple**	**Arbitrary phase structures**	Device rms currents, dc-link capacitor rms current and voltage ripple	**Fundamental frequency**	**High**

The bold entities emphasize the strong performance and advantages of the proposed topology when compared to other methods presented in this table.

[27], and are particularly emphasized in multiphase motor drive applications, such as EVs, where the volume, weight, cost, and reliability are of crucial importance. These statements are still true with the proposed inverter. However, the new topology no longer has a neutral point current, which, in existing topologies, has been the primary element that drives the capacitor-related calculations and decisions. The neutral point current often has an overpowering impact such that all the other current entities associated with the dc-link capacitor can be simply ignored during the derivation. In our new topology, the nonexistence of the neutral point fundamentally reshapes the mathematical landscape and necessitates a new derivation of ripple performances.

Second, an accurate low-order frequency form (LoF) for analyzing various circuit variables is created to serve as a numerical model. This LoF approach—essentially a switching period equivalent root-mean-square (rms)—transforms an unmanageably long chain of obscure switching frequency calculations into a drastically short and intuitive analysis at a much lower ac frequency. LoF is used for the calculations of the device rms current, inverter bridge input rms current, dc-link capacitor rms current, and dc-link capacitor voltage ripple. For conventional two-level three-phase inverters, the rms value of the dc-link capacitor current is calculated in the time domain at the switching frequency [28], [29], [30], and the inverter input current is obtained by the switching functions and output phase currents. In [31] and [32], the double Fourier integral-based method is adopted to demonstrate the dc-link current harmonics for unconventional pulsewidth modulation (PWM) strategies. Recent publications [33], [34], [35] explored rms current and voltage ripple calculations for multilevel and multiphase inverters using various methods. However, to the best of the authors' knowledge, there is no published work on accurate modeling and analysis from the perspective of low-order frequencies, and no intuitive and concise calculation formulae that show influential variables and their impacts on ripples have been obtained.

Finally, our ripple performance analysis and formulae are comprehensive, including many practical and influential factors in the modeling process (e.g., power factor angle, modulation index, switching frequency, output power/current rating, and dead time.), and highly accurate. This is especially beneficial for wide bandgap applications. For example, while the antiparallel diode's reverse recovery is well known and must be accounted for insulated-gate bipolar transistor (IGBT) devices [36], that for silicon-carbide (SiC) field-effect transistors (FETs) is almost negligible. In contrast, a dead time must be considered in ripple calculations for SiC applications, as opposed to for IGBT applications, due to a higher switching frequency. The comparison of the proposed LoF analytical method with existing methods in terms of simplicity, applied range, object, calculation frequency, and accuracy has been given in Table I.

TABLE II
COMPARISON OF THE PROPOSED NPL.H TOPOLOGY WITH NPC 3 L AND T-TYPE 3 L TOPOLOGIES

Topology	Device voltage stress	Device current stress	Device count	Capacitor size
Dual NPC 3-level [12]	$V_{dc}/2$	AC peak current	24 switches, 12 diodes	1 p.u. (4C)
Dual T-type 3-level [11]	$V_{dc}, V_{dc}/2$	AC peak current	24 switches	1 p.u. (4C)
Proposed NPL.H	V_{dc}	**AC peak current**	**18 switches**	**0.25 p.u. (C)**

The bold entities emphasize the strong performance and advantages of the proposed topology when compared to other methods presented in this table.

In addition, a comparison of the proposed NPL.H topology with dual NPC 3 L and dual T-type 3 L topologies is given in Table II. It is evident that our NPL.H can eliminate at least 75% of the dc-link capacitance of the conventional dual NPC 3 L and dual T-type 3 L topologies and reduce the total number of switches required while maintaining the same voltage ripple performance under otherwise same operating conditions, and upto 73% compared with the 2-level inverter. NPL.H unlocks a significantly higher power density for electric transportation and other high-power applications, where the size of a dc-link capacitor bank has traditionally been a major blockade for a high power density.

The rest of this article is organized as follows. First, the topology and operational principle of the proposed NPL.H are introduced in Section II. Section III presents the switching period equivalent rms current concept, referred to as the LoF. LoF of the inverter rms currents and voltage ripple, considering the dead-time effect, are also obtained. Section IV provides the simulation verification of the proposed LoF for various rms currents and voltage ripple calculations. Section V presents the discussion on ripple performance of NPL.H and its implication on dc-link capacitance. Section VI presents the experimental results under various inverter operating conditions and a comprehensive comparison against calculation and simulation. Finally, Section VII concludes this article.

II. TOPOLOGY AND OPERATIONAL PRINCIPLE OF NPL.H

The proposed NPL.H topology is shown in Fig. 1. It is composed of six half-bridge legs and three interphase commutation legs. The six half-bridge legs are constructed with two conventional three-phase 2-level inverters. The three interphase legs are added in to provide commutation paths and generate the 3 L output voltages. The dv/dt and output voltage harmonics of

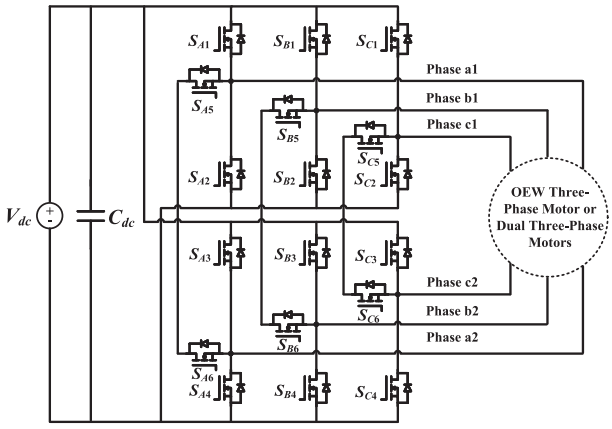

Fig. 1. Proposed neutral-point-less dual H-type 3 L inverter topology.

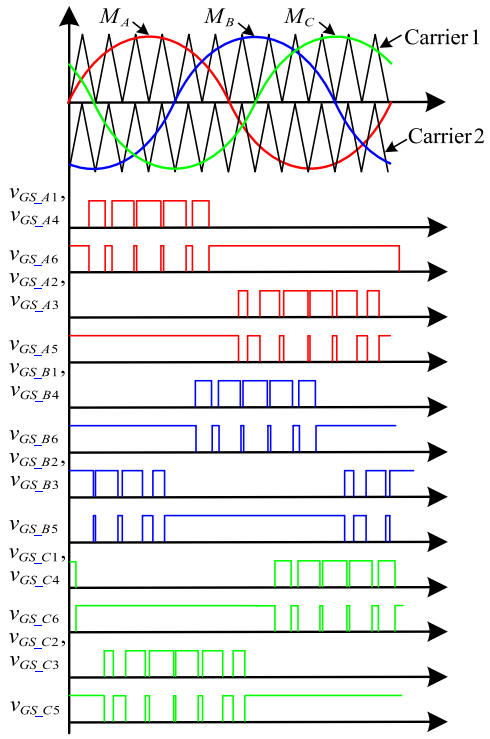

Fig. 2. NPL.H modulation waveforms and gate signals.

NPL.H are, therefore, naturally reduced. The voltage from the midpoint of each half-bridge leg to ground in NPL.H can be $V_{\rm dc}$, $\frac{V_{\rm dc}}{2}$, or 0. Hence, the line-to-line output voltage in NPL.H can be $+V_{\rm dc}$, $+\frac{V_{\rm dc}}{2}$, 0, $-\frac{V_{\rm dc}}{2}$, or $-V_{\rm dc}$.

Furthermore, no switch current is injected to or extracted from the midpoint of the dc-link capacitors, thereby significantly reducing the dc-link voltage ripple. NPL.H has a great merit for dual-motor applications as the required capacitance and overall volume of the dc-link capacitors can be greatly reduced, compared to existing inverters for dual-motor applications [5], [6], [7], [8], [9], [11].

The modulation waveforms and gate signals for NPL.H are presented in Fig. 2. The sinusoidal pulsewidth modulation (SPWM)-based phase disposition modulation technique is adopted here [37]. M_A, M_B, and M_C are the modulation

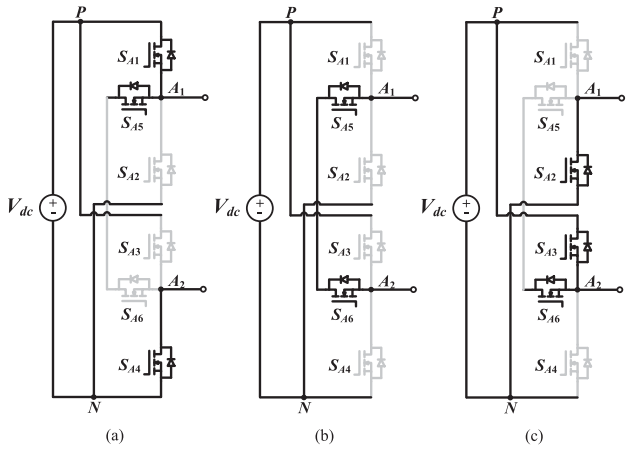

Fig. 3. Switching states for H-leg A in NPL.H inverter.

waveforms for the dual three-phase legs. As shown in Fig. 2, the switch pair S_{A1} and S_{A4} have the same PWM signal, and so do the pairs S_{A2} and S_{A3}, S_{B1} and S_{B4}, S_{B2} and S_{B3}, S_{C1} and S_{C4}, and S_{C2} and S_{C3}. The gate signals of switches S_{A6}, S_{A5}, S_{B6}, S_{B5}, S_{C6}, and S_{C5} are complementary to the gate signals of switches S_{A1}, S_{A2}, S_{B1}, S_{B2}, S_{C1}, and S_{C2}, respectively. According to the modulation waveforms above, there is a 180° phase difference between two sets of three-phase output voltages in NPL.H (e.g., 1, 4, and 6 versus 2, 3, and 5). When a balanced load is connected to an inverter phase, NPL.H will have two sets of three-phase currents with the same value in the opposite directions.

Three different switching states of one H-leg are shown in Fig. 3. "[P]" denotes a state where the top switch of the upper inverter, the bottom switch of the lower inverter, and one switch of the interphase are turned on while other switches are turned OFF. The terminals A_1 and A_2 are connected to the positive dc-bus (P) and negative dc-bus (N) with voltages of $+V_{\rm dc}$ and 0, respectively. "[O]" denotes a state where the two switches of the interphase are turned on while other switches are turned OFF. In this state, A_1 and A_2 are essentially shorted. Assuming the inverter operates with balanced three-phase loads, the voltage of A1 and A2 will be clamped to $+\frac{V_{\rm dc}}{2}$ by the load impedances, resulting in the generation of the same voltage potential of $+\frac{V_{\rm dc}}{2}$. "[N]" denotes a mirrored case of "[P]," where A_1 and A_2 are at 0 and $+V_{\rm dc}$, respectively. This clearly generates three voltage levels in one H-leg: $V_{\rm dc}$; $\frac{V_{\rm dc}}{2}$; and 0.

A total of 27 switching modes with 3-phase H-legs are characterized and summarized in Fig. 4. The switching modes are further divided into five groups based on a combination of their phase output voltages in Table III. The switching modes [P P P], [O O O], and [N N N] can serve as zero vectors, providing zero line-to-line voltages for both inverters. As expected, the line-to-line voltages generate five output voltage levels: $+V_{\rm dc}$; $+\frac{V_{\rm dc}}{2}$; 0; $-\frac{V_{\rm dc}}{2}$; and $-V_{\rm dc}$.

III. Analytical Modeling of Low-Order Form rms Currents and dc-Link Capacitor Voltage Ripple

In this section, analytical expressions for the inverter bridge input rms current, dc-link capacitor rms current, and dc-link

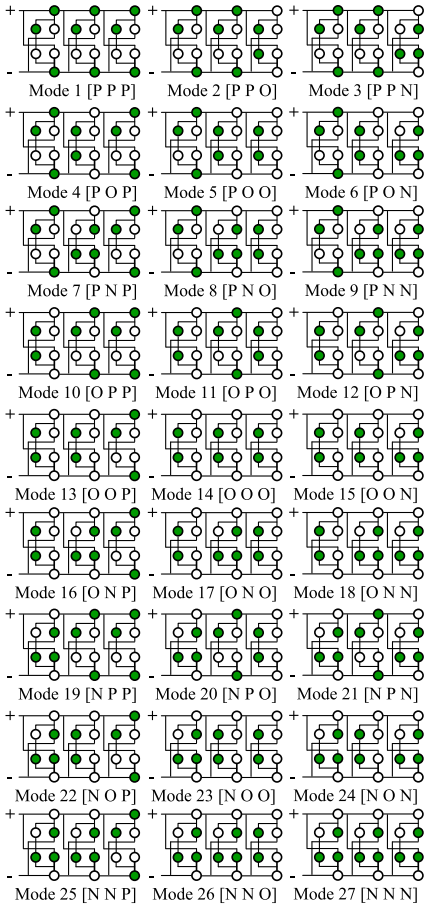

Fig. 4. 27 switching modes of NPL.H inverter.

TABLE III
SWITCHING MODES AND AC VOLTAGES OF NPL.H INVERTER

Line voltages / Switching modes	Inverter 1: v_{A1B1}, v_{B1C1}, v_{C1A1}	Inverter 2: v_{A2B2}, v_{B2C2}, v_{C2A2}
1,14,27	0, 0, 0	0, 0, 0
2,4,5,10,11,13,15,17,18,23,24,26	0, $-\frac{V_{dc}}{2}$, $\frac{V_{dc}}{2}$	0, $\frac{V_{dc}}{2}$, $-\frac{V_{dc}}{2}$
3,7,9,19,21,25	0, V_{dc}, $-V_{dc}$	0, $-V_{dc}$, V_{dc}
6,16,20	$\frac{V_{dc}}{2}$, $\frac{V_{dc}}{2}$, $-V_{dc}$	$-\frac{V_{dc}}{2}$, $-\frac{V_{dc}}{2}$, V_{dc}
8,12,22	$-\frac{V_{dc}}{2}$, $-\frac{V_{dc}}{2}$, V_{dc}	$\frac{V_{dc}}{2}$, $\frac{V_{dc}}{2}$, $-V_{dc}$

voltage ripple are derived assuming SPWM. The two output loads of NPL.H are assumed to be balanced here. The traditional switching frequency-based calculation method is simplified and the low-order form calculation formulae of the rms currents and ripple voltage are derived with considering the effects of different variables, such as dead time. The rms currents and voltage ripple expressions of the traditional dual three-phase 2-level inverter are also derived by the proposed low-order form method for verification.

A. Low-Order Form Analysis for Inverter Switch rms Current

An accurate calculation of the current of a power transistor is crucial in design and analysis of an inverter. The peak current of the transistor—or switch—is normally in a good agreement with

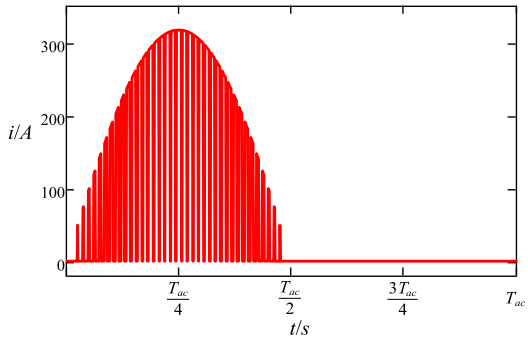

Fig. 5. Typical current waveform of NPL.H's upper switch.

the amplitude of the fundamental ac current. However, because of the facts that the switch current is operating at the switching frequency and that the dead time exists in switching patterns, the calculation of its rms current is not straightforward. Fig. 5 shows the current of NPL.H's upper switch as an example.

The switch current of phase A1's upper switch, S_{A1}, can be expressed by the product of the switching function and phase A1 output current, as shown in (1). The switch rms current can be, therefore, calculated according to the rms definition over one ac cycle. This calculation method is accurate, but complex and not intuitive given that the switching frequency is much higher than the fundamental ac frequency

$$i_{SA1}(t) = S_{A1} \cdot I_{\text{ac}} \sin(\omega t + \theta) \tag{1}$$

Here, S_{A1} is the switching function, I_{ac} is the amplitude of the ac current, ω is the grid angular frequency, and θ is the phase angle of the ac current with respect to the ac voltage.

The low-order form method for a switch rms current calculation creates a low-frequency waveform that offers an rms equivalent switch current at each high-frequency cycle, as shown in Fig. 6. Once obtained, it dramatically decreases the calculation and simplification overhead as the convoluted expressions from the rms calculation at the switching frequency disappear.

Fig. 6(a) shows an example of a switch current in one switching period, defined as

$$i_{\text{sw}} = \begin{cases} I_a & 0 \le t < D \cdot T_{\text{sw}} \\ 0 & D \cdot T_{\text{sw}} \le t < T_{\text{sw}} \end{cases} \tag{2}$$

where I_a is the current value when switch is turned ON, T_{sw} is the switching period, and D is the duty ratio of the switch.

The rms value $i_{\text{sw\_rms}}$ of the switch current in Fig. 6(a) can be derived as

$$i_{\text{sw\_rms}} = \sqrt{\frac{\int_0^{DT_{\text{sw}}} I_a^2 dt}{T_{\text{sw}}}} = |I_a| \cdot \sqrt{D}. \tag{3}$$

For NPL.H, the switch current value evaluated at a time point depends on the ac output current (i.e., $|I_a| = |I_{\text{ac}} \sin(\omega t + \theta)|$) and the duty ratio is determined by the modulation functions (i.e., $D = M \sin(\omega t) - D_{Td}$). With these relationships, (3) becomes the low-order form of the switch rms current i_{SA1_rms}

$$i_{SA1\_\text{rms}} = |I_{\text{ac}} \sin(\omega t + \theta)| \cdot \sqrt{M \sin(\omega t) - D_{Td}} \tag{4}$$

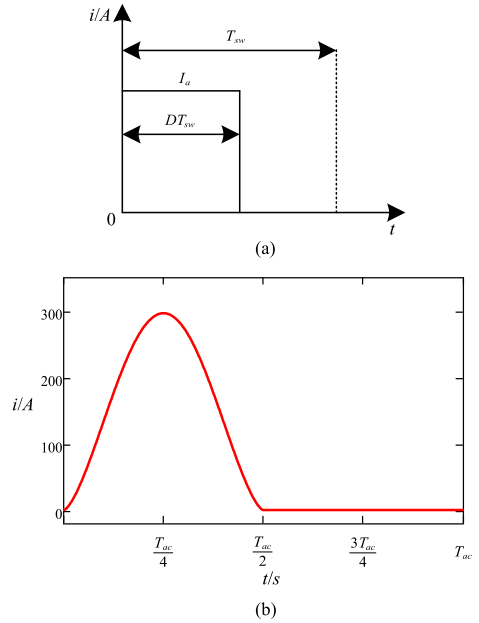

Fig. 6. Low-order equivalence of switch current. (a) Switching period current waveform. (b) Equivalent switching-cycle rms current waveform.

where M is the modulation index, D_{Td} is the duty ratio of the dead time in one switching period (i.e., $\frac{T_{\text{dead}}}{T_{\text{sw}}}$), and T_{dead} is the duration of the dead time.

As a result, the switch current in Fig. 5 can be equivalent to the low-order form rms current, as shown in Fig. 6(b). Accordingly, the low-order forms of the rms currents of six upper switches S_{A1}, S_{A3}, S_{B1}, S_{B3}, S_{C1}, and S_{C3} in NPL.H can be derived as

$$
\begin{aligned}
i_{SA1\_\text{rms}} &= \begin{cases} |i_{\text{ac\_}A1}| \cdot \sqrt{+M_A - D_{Td}} & 0 \le \omega t < \pi \\ 0 & \pi \le \omega t < 2\pi \end{cases} \\
i_{SB1\_\text{rms}} &= \begin{cases} |i_{\text{ac\_}B1}| \cdot \sqrt{+M_B - D_{Td}} & 0 \le \omega t - \frac{2\pi}{3} < \pi \\ 0 & \pi \le \omega t - \frac{2\pi}{3} < 2\pi \end{cases} \\
i_{SC1\_\text{rms}} &= \begin{cases} |i_{\text{ac\_}C1}| \cdot \sqrt{+M_C - D_{Td}} & 0 \le \omega t + \frac{2\pi}{3} < \pi \\ 0 & \pi \le \omega t + \frac{2\pi}{3} < 2\pi \end{cases}
\end{aligned} \tag{5}
$$

and

$$
\begin{aligned}
i_{SA3\_\text{rms}} &= \begin{cases} 0 & 0 \le \omega t < \pi \\ |i_{\text{ac\_}A2}| \cdot \sqrt{-M_A - D_{Td}} & \pi \le \omega t < 2\pi \end{cases} \\
i_{SB3\_\text{rms}} &= \begin{cases} 0 & 0 \le \omega t - \frac{2\pi}{3} < \pi \\ |i_{\text{ac\_}B2}| \cdot \sqrt{-M_B - D_{Td}} & \pi \le \omega t - \frac{2\pi}{3} < 2\pi \end{cases} \\
i_{SC3\_\text{rms}} &= \begin{cases} 0 & 0 \le \omega t + \frac{2\pi}{3} < \pi \\ |i_{\text{ac\_}C2}| \cdot \sqrt{-M_C - D_{Td}} & \pi \le \omega t + \frac{2\pi}{3} < 2\pi. \end{cases}
\end{aligned} \tag{6}
$$

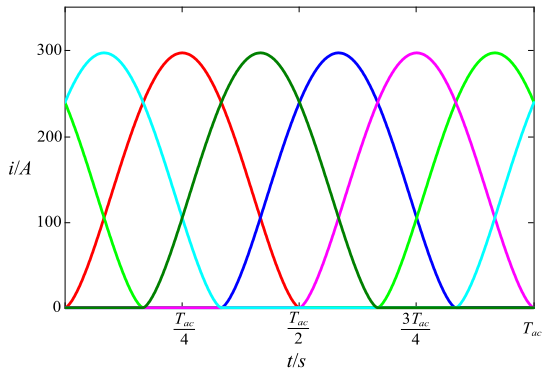

Fig. 7. Low-order instantaneous rms switch current waveforms of six upper switches S_{A1}, S_{A3}, S_{B1}, S_{B3}, S_{C1}, and S_{C3}.

Here, the definitions on the ac currents and modulation functions are

$$
\begin{cases} i_{\text{ac\_}A1} = +I_{\text{ac}} \sin(\omega t + \theta) \\ i_{\text{ac\_}B1} = +I_{\text{ac}} \sin\left(\omega t - \frac{2\pi}{3} + \theta\right) \\ i_{\text{ac\_}C1} = +I_{\text{ac}} \sin\left(\omega t + \frac{2\pi}{3} + \theta\right) \end{cases} \tag{7}
$$

$$
\begin{cases} i_{\text{ac\_}A2} = -I_{\text{ac}} \sin(\omega t + \theta) \\ i_{\text{ac\_}B2} = -I_{\text{ac}} \sin\left(\omega t - \frac{2\pi}{3} + \theta\right) \\ i_{\text{ac\_}C2} = -I_{\text{ac}} \sin\left(\omega t + \frac{2\pi}{3} + \theta\right) \end{cases} \tag{8}
$$

and

$$
\begin{cases} M_A = M \sin(\omega t) \\ M_B = M \sin\left(\omega t - \frac{2\pi}{3}\right) \\ M_C = M \sin\left(\omega t + \frac{2\pi}{3}\right) \end{cases} \tag{9}
$$

The low-order forms of the rms currents of six upper switches under the unity power factor condition are shown in Fig. 7.

Even though the ac currents are considered purely sinusoidal in (7) and (8), the harmonics can be included in this method for more accurate results without any limitation. Furthermore, the rms currents of lower switches and interphase switches of NPL.H can be calculated as

$$
\begin{aligned}
i_{SA2\_\text{rms}} &= \begin{cases} 0 & 0 \le \omega t < \pi \\ |i_{\text{ac\_}A1}| \cdot \sqrt{-M_A - D_{Td}} & \pi \le \omega t < 2\pi \end{cases} \\
i_{SB2\_\text{rms}} &= \begin{cases} 0 & 0 \le \omega t - \frac{2\pi}{3} < \pi \\ |i_{\text{ac\_}B1}| \cdot \sqrt{-M_B - D_{Td}} & \pi \le \omega t - \frac{2\pi}{3} < 2\pi \end{cases} \\
i_{SC2\_\text{rms}} &= \begin{cases} 0 & 0 \le \omega t + \frac{2\pi}{3} < \pi \\ |i_{\text{ac\_}C1}| \cdot \sqrt{-M_C - D_{Td}} & \pi \le \omega t + \frac{2\pi}{3} < 2\pi \end{cases}
\end{aligned} \tag{10}
$$

$$
\begin{aligned}
i_{SA4\_\text{rms}} &= \begin{cases} |i_{\text{ac\_}A2}| \cdot \sqrt{+M_A - D_{Td}} & 0 \le \omega t < \pi \\ 0 & \pi \le \omega t < 2\pi \end{cases} \\
i_{SB4\_\text{rms}} &= \begin{cases} |i_{\text{ac\_}B2}| \cdot \sqrt{+M_B - D_{Td}} & 0 \le \omega t - \frac{2\pi}{3} < \pi \\ 0 & \pi \le \omega t - \frac{2\pi}{3} < 2\pi \end{cases} \\
i_{SC4\_\text{rms}} &= \begin{cases} |i_{\text{ac\_}C2}| \cdot \sqrt{+M_C - D_{Td}} & 0 \le \omega t + \frac{2\pi}{3} < \pi \\ 0 & \pi \le \omega t + \frac{2\pi}{3} < 2\pi \end{cases}
\end{aligned} \tag{11}
$$

and

$$\begin{cases} i_{SA5\_\text{rms}} = i_{SA6\_\text{rms}} = |i_{\text{ac\_}A1}| \cdot \sqrt{1 - |M_A| + D_{Td}} \\ i_{SB5\_\text{rms}} = i_{SB6\_\text{rms}} = |i_{\text{ac\_}B1}| \cdot \sqrt{1 - |M_B| + D_{Td}} \\ i_{SC5\_\text{rms}} = i_{SC6\_\text{rms}} = |i_{\text{ac\_}C1}| \cdot \sqrt{1 - |M_C| + D_{Td}}. \end{cases} \tag{12}$$

Considering that the switch currents may have a positive or negative polarity with a nonunity power factor, the absolute function is applied to the ac currents in (5), (6), (10), (11), and (12). The switch rms currents in NPL.H can be obtained by simply integrating the square of above equations in one fundamental ac period and taking the square root. Similarly, the low-order expressions of the switch RMS currents for the dual three-phase 2-level inverter can be derived as

$$\begin{cases} i_{TA1\_\text{RMS}} = |i_{\text{ac\_}A1}| \cdot \sqrt{\frac{M_A+1}{2}} \\ i_{TB1\_\text{RMS}} = |i_{\text{ac\_}B1}| \cdot \sqrt{\frac{M_B+1}{2}} \\ i_{TC1\_\text{RMS}} = |i_{\text{ac\_}C1}| \cdot \sqrt{\frac{M_C+1}{2}} \end{cases} \tag{13}$$

$$\begin{cases} i_{TA2\_\text{RMS}} = |i_{\text{ac\_}A1}| \cdot \sqrt{\frac{1-M_A}{2}} \\ i_{TB2\_\text{RMS}} = |i_{\text{ac\_}B1}| \cdot \sqrt{\frac{1-M_B}{2}} \\ i_{TC2\_\text{RMS}} = |i_{\text{ac\_}C1}| \cdot \sqrt{\frac{1-M_C}{2}} \end{cases} \tag{14}$$

$$\begin{cases} i_{TA3\_\text{RMS}} = |i_{\text{ac\_}A2}| \cdot \sqrt{\frac{M_A+1}{2}} \\ i_{TB3\_\text{RMS}} = |i_{\text{ac\_}B2}| \cdot \sqrt{\frac{M_B+1}{2}} \\ i_{TC3\_\text{RMS}} = |i_{\text{ac\_}C2}| \cdot \sqrt{\frac{M_C+1}{2}} \end{cases} \tag{15}$$

and

$$\begin{cases} i_{TA4\_\text{RMS}} = |i_{\text{ac\_}A2}| \cdot \sqrt{\frac{1-M_A}{2}} \\ i_{TB4\_\text{RMS}} = |i_{\text{ac\_}B2}| \cdot \sqrt{\frac{1-M_B}{2}} \\ i_{TC4\_\text{RMS}} = |i_{\text{ac\_}C2}| \cdot \sqrt{\frac{1-M_C}{2}}. \end{cases} \tag{16}$$

Here, i_{TA1} through i_{TA4}, i_{TB1} through i_{TB4}, and i_{TC1} through i_{TC4} are the RMS currents of respective phase switches in dual three-phase 2-level inverter.

B. Low-Order Forms of Inverter Bridge Input RMS Current and DC-Link Capacitor RMS Current

The inverter bridge input RMS current and dc-link capacitor RMS current are crucial for the efficacy analysis and performance evaluation of an inverter and dc-link capacitor design. The instantaneous bridge input current is the sum of all switch currents connected to the top node

$$i_{\text{inv\_in}} = i_{SA1} + i_{SB1} + i_{SC1} + i_{SA3} + i_{SB3} + i_{SC3}. \tag{17}$$

The switching cycle rms current is then

$$i_{\text{inv\_in\_rms}} = \sqrt{\frac{\int i_{\text{inv\_in}}^2 dt}{T_{\text{sw}}}}. \tag{18}$$

The instantaneous dc-link capacitor current is

$$\begin{aligned} i_{C\text{dc}} &= I_{\text{dc}} - i_{\text{inv\_in}} \\ &= I_{\text{dc}} - (i_{SA1} + i_{SB1} + i_{SC1}) - (i_{SA3} + i_{SB3} + i_{SC3}) \end{aligned} \tag{19}$$

where I_{dc} is the dc input current. The switching cycle rms of it is

$$i_{C\text{dc\_rms}} = \sqrt{\frac{\int i_{C\text{dc}}^2 dt}{T_{\text{sw}}}}. \tag{20}$$

Due to the three-phase structure, the inverter bridge input current and dc-link capacitor current have the periodicity of $\frac{1}{6}$ fundamental period (T_{ac}). Therefore, the following analysis and calculation will be carried out in the unit of $\frac{T_{\text{ac}}}{6}$. In the time interval $t = [0, T_{\text{ac}}/6]$, NPL.H's inverter bridge input current is $i_{\text{inv\_in}} = i_{SA1} + i_{SC1} + i_{SB3}$. Then, (18) and (20) are, respectively, simplified to

$$\begin{aligned} i_{\text{inv\_in\_rms}} &= \sqrt{\frac{\int \left((i_{SA1} + i_{SC1}) + (i_{SB3})\right)^2 dt}{T_{\text{sw}}}} \\ &= \sqrt{A + B} \end{aligned} \tag{21}$$

and

$$\begin{aligned} &i_{C\text{dc\_rms}} \\ &= \sqrt{\frac{\int \left(I_{\text{dc}} - (i_{SA1} + i_{SC1} + i_{SB3})\right)^2 dt}{T_{\text{sw}}}} \\ &= \sqrt{i_{\text{inv\_in\_rms}}^2 + I_{\text{dc}}^2 - 2I_{\text{dc}} \cdot \frac{\int (i_{SA1} + i_{SC1} + i_{SB3})\, dt}{T_{\text{sw}}}} \\ &= \sqrt{A + B + i_{\text{dc}}^2 + C} \end{aligned} \tag{22}$$

where A, B, and C are defined as

$$\begin{cases} A = i_{SA1\_\text{rms}}^2 + i_{SC1\_\text{rms}}^2 + i_{SB3\_\text{rms}}^2 \\ B = \frac{\int 2i_{SA1} \cdot i_{SC1} + 2i_{SA1} \cdot i_{SB3} + 2i_{SC1} \cdot i_{SB3} dt}{T_{\text{sw}}} \\ C = -2I_{\text{dc}} \cdot \frac{\int (i_{SA1} + i_{SC1} + i_{SB3}) dt}{T_{\text{sw}}}. \end{cases} \tag{23}$$

The switch rms currents in (23)'s A are individually calculated in the previous section, and the low-order form rms current expressions of all switches are presented in (5) and (6). In addition, C in (23) can also be readily calculated by the corresponding ac currents and modulation functions—essentially equivalent duty ratios. The remaining challenge is to calculate B in (23). As it involves multiplications of two switch currents, the detailed analysis on NPL.H's upper switch currents and duty ratios are required, considering their piecewise characteristics during an ac cycle, to create the low-order form.

There are three different combinations for any two upper switch currents, as depicted in Fig. 8. Although the upper switch currents may have a positive or negative polarity under nonunity power factor conditions, it can be shown that the polarities of the switch currents do not affect the validity of the analysis and calculations here. For simplicity, the currents in Fig. 8 are all drawn with a positive polarity.

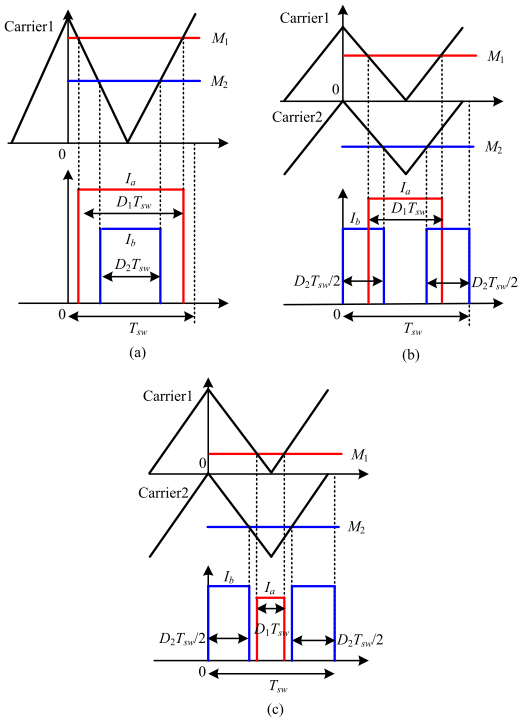

Fig. 8. Cases with upper switch currents. (a) Case 1. (b) Case 2. (C) Case 3.

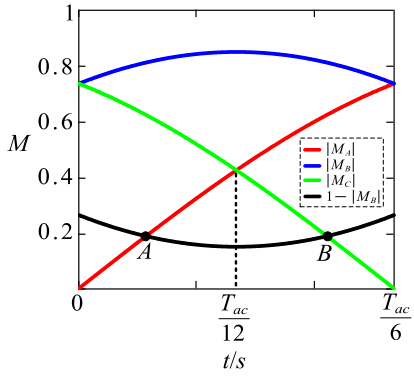

Fig. 9. Modulation waveforms during $t = [0,\ T_{\text{ac}}/6]$.

TABLE IV
RANGES AND CORRESPONDING CASES FOR $\frac{\int i_a i_b dt}{T_{\text{sw}}}$ IN $t = [0,\ \frac{T_{\text{ac}}}{6}]$

Cases: $i_a \cdot i_b$ / t	$i_{SA1} \cdot i_{SC1}$	$i_{SA1} \cdot i_{SB3}$	$i_{SC1} \cdot i_{SB3}$
$[0,\ t_A]$:	Case 1	Case 3	Case 2
$\left[t_A,\ \frac{T_{\text{ac}}}{12}\right]$:	Case 1	Case 2	Case 2
$\left[\frac{T_{\text{ac}}}{12},\ t_B\right]$:	Case 1	Case 2	Case 2
$\left[t_B,\ \frac{T_{\text{ac}}}{6}\right]$:	Case 1	Case 2	Case 3

First of all, a combination of two upper switch currents can be divided into three cases. Case 1 in Fig. 8(a) shows the waveforms where the two switch currents are from the same inverter. Cases 2 and 3 in Fig. 8(b) and (c), respectively, are the waveforms with currents from different inverters.

To calculate the integral of sum products of currents in "B" of (23), the current waveforms in each case of Fig. 8 will be subject to the integral $\frac{\int i_a i_b dt}{T_{\text{sw}}}$. For Case 1

$$\frac{\int_0^{T_{\text{sw}}} i_a \cdot i_b dt}{T_{\text{sw}}} = \frac{\int_0^{D_2 T_{\text{sw}}} I_a \cdot I_b dt}{T_{\text{sw}}} = D_2 \cdot (I_a \cdot I_b)\,. \tag{24}$$

The effective duty ratio of Case 1 is determined by the smaller duty ratio, D_2. For Case 2

$$\begin{aligned}\frac{\int_0^{T_{\text{sw}}} i_a \cdot i_b dt}{T_{\text{sw}}} &= \frac{\int_{\frac{(1-D_1)T_{\text{sw}}}{2}}^{\frac{D_2 T_{\text{sw}}}{2}} I_a \cdot I_b dt + \int_{T_{\text{sw}}-\frac{D_2 T_{\text{sw}}}{2}}^{\frac{(1+D_1)T_{\text{sw}}}{2}} I_a \cdot I_b dt}{T_{\text{sw}}} \\ &= (D_1 + D_2 - 1) \cdot (I_a \cdot I_b)\,.\end{aligned} \tag{25}$$

The effective duty ratio of Case 2 is $(D_1 + D_2 - 1)$ and depends on the duty ratios of both switches. On the other hand, the calculation result for Case 3 is always 0, as the two currents do not overlap in time. This occurs when the two currents are from different inverters and $D_1 < (1 - D_2)$.

The modulation waveforms of the switches S_{A1}, S_{C1}, and S_{B3} during $t = [0,\ T_{\text{ac}}/6]$ are shown in Fig. 9 as red, green, and blue curves, respectively. The black curve denotes $1 - |M_B|$ and can be used to calculate the range and boundary points of Case 3. The time points, t_A and t_B, corresponding to boundary points A and B in Fig. 9, can be calculated as

$$\begin{cases} t_A = \frac{1}{2\pi f}\left[\arcsin\left(\frac{\sqrt{3}}{3 \cdot M}\right) - \frac{\pi}{6}\right] \\ t_B = \frac{1}{2\pi f}\left[-\arcsin\left(\frac{\sqrt{3}}{3 \cdot M}\right) + \frac{\pi}{2}\right]. \end{cases} \tag{26}$$

Table IV gives different time ranges and corresponding case designations for the calculation of the integral of interest, $\frac{\int i_a i_b dt}{T_{\text{sw}}}$, in the $\frac{1}{6}$ fundamental period. Based on this table, the calculation of B in (23) can be completed.

Once A, B, and C of (23) are obtained, the simplified low-order form of the inverter bridge input rms current, (21), and dc-link capacitor rms current, (19), can be calculated as

$$\begin{aligned} i_{\text{inv\_in\_RMS}} = \\ I_{\text{ac}} \sqrt{\begin{array}{l} \left(\begin{array}{c} \left(2\sqrt{3}M + 6\sqrt{3} \cdot \sqrt{M^2 - \frac{1}{3}}\right) \\ -3\sqrt{3}\left(\frac{1}{2} + 2D_{Td}\right) \\ +\sqrt{3}M\left(\frac{5}{3M^2} - 2\right) \cdot \sqrt{1 - \frac{1}{3M^2}} \end{array}\right) \cdot \frac{\cos 2\theta}{2\pi} \\ -\left(\frac{2D_{Td}+1}{4\pi}\left(3 - \frac{2}{M^2}\right)\right)\sin(2\theta) - 1 - 3D_{Td} \\ +\frac{6 \cdot (2D_{Td}+1) \cdot t_A}{T_{\text{ac}}} + \frac{\left(3\sqrt{3}+9\right)M}{2\pi} - \frac{9M - 6\sqrt{3} \cdot \sqrt{M^2 - \frac{1}{3}}}{2\pi} \end{array}} \end{aligned} \tag{27}$$

and

$$i_{C\text{dc\_RMS}} = \sqrt{I_{\text{ac}}^2 \left(\begin{array}{c} \left(\begin{array}{c} \left(2\sqrt{3}M + 6\sqrt{3}\cdot\sqrt{M^2-\frac{1}{3}}\right) \\ -3\sqrt{3}\left(\frac{1}{2}+2D_{Td}\right) \\ +\sqrt{3}M\left(\frac{5}{3\,M^2}-2\right)\cdot\sqrt{1-\frac{1}{3\,M^2}} \end{array} \right)\cdot\frac{\cos 2\theta}{2\pi} \\ -\left(\frac{2D_{Td}+1}{4\pi}\left(3-\frac{2}{M^2}\right)\right)\sin(2\theta) - 1 - 3D_{Td} \\ +\frac{6\cdot(2D_{Td}+1)\cdot t_A}{T_{\text{ac}}} + \frac{\left(3\sqrt{3}+9\right)M}{2\pi} - \frac{9M-6\sqrt{3}\cdot\sqrt{M^2-\frac{1}{3}}}{2\pi} \end{array} \right) + I_{\text{dc}}^2 - I_{\text{dc}} I_{\text{ac}}\left(3M\cos(\theta) - \frac{4D_{Td}}{\pi}\cos(\theta)\right).} \tag{28}$$

The proposed low-order form method can also obtain the dual two-level inverter's bridge input and dc-link capacitor RMS currents. The end results are

$$i_{\text{inv\_in\_RMS\_2}\,L} = 2I_{\text{ac}}\sqrt{\frac{M}{\pi}\left(\begin{array}{c}\frac{3\sqrt{3}}{4}+\frac{\sqrt{3}}{2}\cos(2\theta) \\ +\left(\frac{3}{4}-\frac{\sqrt{3}}{2}\right)\sin(2\theta)\end{array}\right)} \tag{29}$$

and

$$i_{C\text{dc\_RMS\_2}\,L} = \sqrt{4I_{\text{ac}}^2\left[\frac{M}{\pi}\left(\begin{array}{c}\frac{3\sqrt{3}}{4}+\frac{\sqrt{3}}{2}\cos(2\theta) \\ +\left(\frac{3}{4}-\frac{\sqrt{3}}{2}\right)\sin(2\theta)\end{array}\right)\right] + I_{\text{dc}}^2 - 3MI_{\text{dc}}I_{\text{ac}}}. \tag{30}$$

Here, "2 L" at the end of the subscripts designates that these are the results for the dual three-phase 2-level inverter. Please note that as the steps are nearly identical to NPL.H's, the detailed derivation is omitted, and the end results are directly provided.

Equations (27) and (28) now clearly and intuitively express the impacts of the practical design variables, I_{ac}, M, θ, I_{dc}, and D_{Td}, on the inverter bridge input rms current and dc-link capacitor rms current. Different parameter values and/or operating conditions can be easily calculated with (27) and (28) for a new design. Analysis and evaluation of an existing design can be directly performed with our equations as well.

C. Low-Order Form of DC-Link Capacitor Voltage Ripple

The dc-link capacitor voltage ripple is closely related to the dc-link capacitor current and is an important basis for a determination of a dc-link capacitance. Like the dc-link capacitor current, the dc-link capacitor voltage repeats every $\frac{1}{6}$ fundamental period.

To analyze and calculate the dc-link capacitor voltage ripple, different types of dc-link capacitor currents and voltages are illustrated for the time interval of $t = [0,\ T_{\text{ac}}/6]$ in Fig. 10. Here, since the switching frequency normally is much larger than the ac frequency, the switch current is considered constant within one switching cycle. Note that with the modulation shown in Fig. 2, there are three upper switches conducting currents at any switching cycle in one ac period. There are eight combinations based on the polarities and duty ratios of the three switch currents.

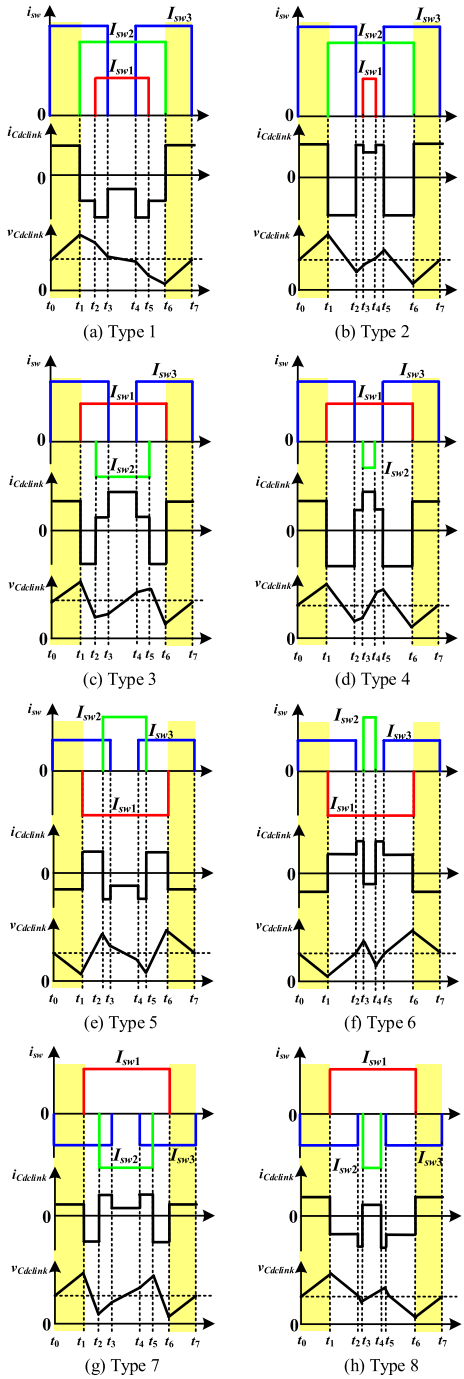

Fig. 10. Types of DC-link capacitor currents and voltages in one switching period. (a) Type 1. (b) Type 2. (c) Type 3. (d) Type 4. (e) Type 5. (f) Type 6. (g) Type 7. (h) Type 8.

The three switch currents are labeled as I_{sw1}, I_{sw2}, and I_{sw3} in Fig. 10. Among these three, two currents always come from the upper switches of the same inverter and the other from the upper switches of the other inverter. In addition, with the power factor angle from $-\frac{\pi}{2}$ to $+\frac{\pi}{2}$, at most two currents have negative polarities at the same time, and they must be from the upper switches of different inverters.

Types 1 and 2 appear when three switch currents are all positive (i.e., $I_{\text{sw1}} > 0$, $I_{\text{sw2}} > 0$, $I_{\text{sw3}} > 0$). The conditions are

$D_{sw1} > 1 - D_{sw3}$ in type 1 and $D_{sw1} \leq 1 - D_{sw3}$ in type 2. Types 3 and 4 exist when one of the two switch currents from the same inverter is negative (i.e., $I_{sw1} > 0$, $I_{sw2} < 0$, $I_{sw3} > 0$). The conditions are $D_{sw2} > 1 - D_{sw3}$ in type 3 and $D_{sw2} \leq 1 - D_{sw3}$ in type 4. Types 5 and 6 are similar to 3 and 4 except for the flipped polarities of I_{sw1} and I_{sw2} (i.e., $I_{sw1} < 0$, $I_{sw2} > 0$, $I_{sw3} > 0$). The conditions are $D_{sw2} > 1 - D_{sw3}$ in type 5 and $D_{sw2} \leq 1 - D_{sw3}$ in type 6. Types 7 and 8 are the cases of two negative currents and one positive current (i.e., $I_{sw1} > 0$, $I_{sw2} < 0$, $I_{sw3} < 0$). Here, $D_{sw2} > 1 - D_{sw3}$ in type 7 and $D_{sw2} \leq 1 - D_{sw3}$ in type 8.

An examination of these plots reveals that the amplitude of the dc-link capacitor voltage ripple in one switching cycle for all types can be determined by considering only two ascending/descending time periods, $t = [t_0,\ t_1]$ and $t = [t_6,\ t_7]$, which are highlighted in yellow. During these two time periods, only one switch current exists for all types, and the dc-link capacitor voltage increases monotonically. The dc-link capacitor voltage ripple in $\frac{1}{6}$ ac period is derived as

$$\begin{aligned}\Delta V_{C\mathrm{dc}\_pp} &= \frac{1}{C_{\mathrm{dc}}}\int_0^{2\Delta t} i_{C\mathrm{dc}}\ \mathrm{d}\tau = \frac{1}{C_{\mathrm{dc}}}\int_0^{2\Delta t} |I_{\mathrm{dc}} - I_{\mathrm{sw3}}|\ \mathrm{d}\tau \\ &= \frac{\int_0^{2\Delta t} \left|I_{\mathrm{dc}} + I_{\mathrm{ac}}\sin\left(\omega t - \frac{2\pi}{3} + \theta\right)\right|\ \mathrm{d}\tau}{C_{\mathrm{dc}}} \\ &= \frac{\left|I_{\mathrm{dc}} + I_{\mathrm{ac}}\sin\left(\omega t - \frac{2\pi}{3} + \theta\right)\right| \cdot 2\Delta t}{C_{\mathrm{dc}}}.\end{aligned} \tag{31}$$

According to the modulation waveforms during $t = [0,\ \frac{T_{\mathrm{ac}}}{6}]$ in Fig. 9, the duty ratio relationship of the three switches are

$$\begin{cases} t = \left[0,\ \frac{T_{\mathrm{ac}}}{12}\right]: & D_{SB2} > D_{SC1} > D_{SA1} \\ t = \left[\frac{T_{\mathrm{ac}}}{12},\ \frac{T_{\mathrm{ac}}}{6}\right]: & D_{SB2} > D_{SA1} > D_{SC1} \end{cases}. \tag{32}$$

Therefore, during $t = [0,\ \frac{T_{\mathrm{ac}}}{12}]$, the Δt is

$$\Delta t = \frac{T_{\mathrm{sw}}\left(1 - D_{SC1}\right)}{2} = \frac{T_{\mathrm{sw}}\left(1 - M\sin\left(\omega t + \frac{2\pi}{3}\right) + D_{Td}\right)}{2}. \tag{33}$$

During $t = [\frac{T_{\mathrm{ac}}}{12},\ \frac{T_{\mathrm{ac}}}{6}]$, the Δt is

$$\Delta t = \frac{T_{\mathrm{sw}}\left(1 - D_{SA1}\right)}{2} = \frac{T_{\mathrm{sw}}\left(1 - M\sin\left(\omega t\right) + D_{Td}\right)}{2}. \tag{34}$$

By substituting (33) and (34) into (31), the envelope of the dc-link capacitor voltage ripple is obtained as a function of inverter parameters. If the dc-link capacitance is designed based on a dc-link capacitor voltage ripple requirement, the design criterion of the capacitance is

$$C_{dc} \geq \frac{\max\left|\left[I_{\mathrm{dc}} + I_{\mathrm{ac}}\sin\left(\omega t - \frac{2\pi}{3} + \theta\right)\right] \cdot 2\Delta t\right|}{\Delta V_{C\mathrm{dc}\_pp}} \tag{35}$$

where $0 \leq t \leq \frac{T_{\mathrm{ac}}}{6}$.

TABLE V
NPL.H PARAMETERS FOR SIMULATION

V_{ll_rms}	450 $\mathrm{V_{rms}}$	θ	$\left[-\frac{\pi}{2},\ \frac{\pi}{2}\right]$
f_{ac}	125 Hz	M	[0.7, 1]
f_{sw}	10 kHz	S	[0 kVA, 350 kVA]
$V_{\mathrm{dc-link}}$	[735 V, 1050 V]	I_{ac}	[0 A, 318 A]
C_{dc}	100 µF	T_{dead}	300 ns

Meanwhile, the dc-link capacitor voltage ripple of the dual 2-level inverter can be derived as

$$\begin{aligned}\Delta V_{C\mathrm{dc}\_pp\_2\,L} &= \frac{1}{C_{\mathrm{dc}}}\int_0^{2\Delta t_{2\,L}} |i_{C\mathrm{dc}\_2\,L}|\ \mathrm{d}\tau \\ &= \frac{\max\left|\left(I_{\mathrm{dc}} \cdot 2\Delta t_{1\_2\,L}\right), \left(I_{\mathrm{dc}} \cdot 2\Delta t_{1\_2\,L} + \left(I_{\mathrm{dc}} - 2i_{\mathrm{ac}}\right) \cdot 2\Delta t_{2\_2\,L}\right)\right|}{C_{\mathrm{dc}}}\end{aligned} \tag{36}$$

where $\Delta V_{C\mathrm{dc}\_pp\_2\,L}$ refers to the dc-link capacitor voltage ripple of the dual three-phase 2-level inverter and $\Delta t_{1\_2\,L}$ and $\Delta t_{2\_2\,L}$ are the new ascending/descending time period defined as

$$\Delta t_{1\_2\,L} = \begin{cases} \frac{T_{\mathrm{sw}}\left(1 - \frac{M\sin\left(\omega t + \frac{2\pi}{3}\right) + 1}{2}\right)}{2} & 0 \leq t < \frac{T_{\mathrm{ac}}}{12} \\ \frac{T_{\mathrm{sw}}\left(1 - \frac{M\sin\left(\omega t\right) + 1}{2}\right)}{2} & \frac{T_{\mathrm{ac}}}{12} \leq t < \frac{T_{\mathrm{ac}}}{6} \end{cases} \tag{37}$$

$$\Delta t_{2\_2\,L} = \begin{cases} \frac{T_{\mathrm{sw}}\left(M\sin\left(\omega t + \frac{2\pi}{3}\right) - M\sin\left(\omega t\right)\right)}{4} & 0 \leq t < \frac{T_{\mathrm{ac}}}{12} \\ \frac{T_{\mathrm{sw}}\left(M\sin\left(\omega t\right) - M\sin\left(\omega t + \frac{2\pi}{3}\right)\right)}{4} & \frac{T_{\mathrm{ac}}}{12} \leq t < \frac{T_{\mathrm{ac}}}{6} \end{cases} \tag{38}$$

and i_{ac} are the related ac phase currents in the time interval of $t = [0,\ T_{\mathrm{ac}}/6]$

$$i_{\mathrm{ac}} = \begin{cases} I_{\mathrm{ac}}\sin\left(\omega t + \frac{2\pi}{3} + \theta\right) & 0 \leq t < \frac{T_{\mathrm{ac}}}{12} \\ I_{\mathrm{ac}}\sin\left(\omega t + \theta\right) & \frac{T_{\mathrm{ac}}}{12} \leq t < \frac{T_{\mathrm{ac}}}{6}. \end{cases} \tag{39}$$

IV. Simulation Verification

In this section, a simulation model for NPL.H is built in PSIM software to verify the effectiveness of the proposed low-order form method and validate the calculation of the rms currents and voltage ripple in the previous section. The main parameters of the inverter model are given in Table V. The line-to-line rms ac output voltage is fixed to $450\mathrm{V_{rms}}$, ac frequency is 125 Hz, switching frequency is 10 kHz, and dead time in one switching cycle is set to 300 ns. The parameter ranges of the power factor

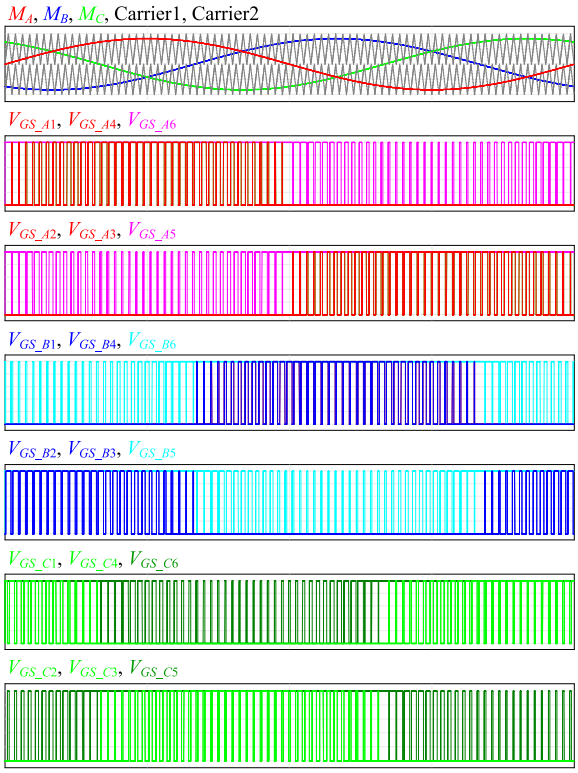

Fig. 11. Simulated modulation waveforms of NPL.H.

angle (θ), modulation index (M), and output apparent power (S) are given in Table V.

The dc-link capacitor voltage ($V_{\text{dc-link}}$), dc input current (I_{dc}), and ac phase current amplitude (I_{ac}) can be expressed as

$$\begin{cases} I_{\text{ac}} = \dfrac{\sqrt{6}S}{6 \cdot V_{ll\_\text{rms}}} \\ V_{\text{dc-link}} = \dfrac{2\sqrt{6}V_{ll\_\text{rms}}}{3\,M} \\ I_{\text{dc}} = \dfrac{3I_{\text{ac}} \cdot \cos(\theta) \cdot M}{2}. \end{cases} \tag{40}$$

The simulated waveforms of NPL.H with the SPWM modulation are presented in Fig. 11. The PWM signals for NPL.H are generated by three modulation waveforms, M_A, M_B, and M_C, and two carrier waveforms, "Carrier 1" and "Carrier 2," shown in Fig. 2. In addition, also shown in Fig. 12 are the simulated waveforms of the inverter output phase voltages, phase currents, input current, inverter bridge input currents, and dc-link capacitor current and voltage. Here, the dc input voltage of 900 V, power factor angle of $-\frac{\pi}{6}$, and output power of 350 kVA are used.

Different operating conditions of NPL.H are further tested in simulation and presented in Fig. 13. The calculation results using the proposed low-order form of the rms currents and voltage ripple are overlaid on top. The simulation results of the inverter bridge input rms current, $I_{\text{inv\_in\_rms}}$, and the corresponding theoretical calculation results are in excellent agreement under different inverter operating conditions. The base case is

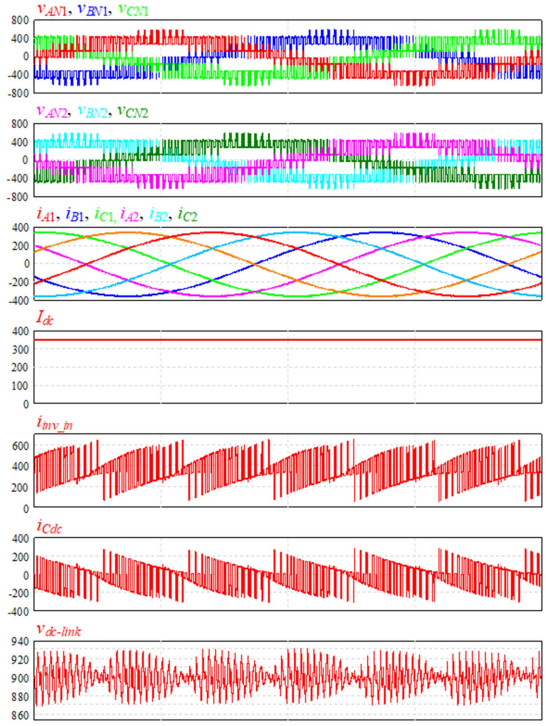

Fig. 12. Simulated voltage and current waveforms of NPL.H.

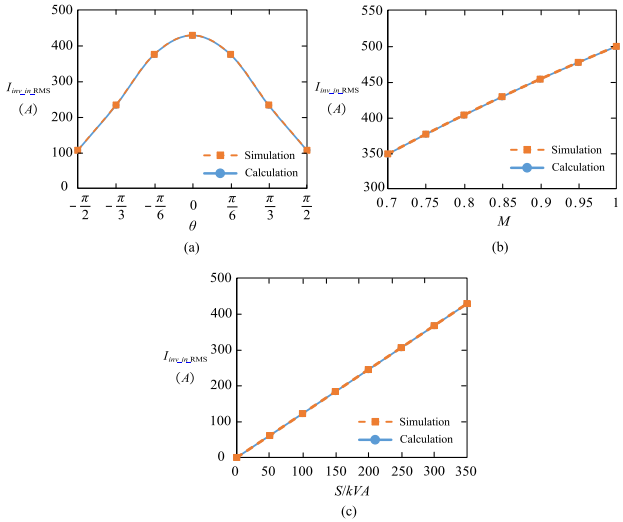

Fig. 13. NPL.H bridge input rms current varies with variables. (a) $I_{\text{inv\_in\_rms}}$ varies with different θ. (b) $I_{\text{inv\_in\_rms}}$ varies with different M. (c) $I_{\text{inv\_in\_rms}}$ varies with different S.

the power factor angle (θ) of 0, modulation index (M) of 0.85, and output apparent power (S) of 350 kVA. Each subplot shows a variation caused by a single parameter.

The simulation and calculation results of the dc-link capacitor rms current, $I_{C\text{dc\_rms}}$, are presented in Fig. 14. Again, they are in excellent agreement. A single parameter variation with the same base case is used for each subplot.

Fig. 15 presents the comparison of simulation and calculation results of the dc-link capacitor voltage ripple, $\Delta V_{C\text{dc}}$, with 100 μF dc-link capacitance. The simulation and theoretical

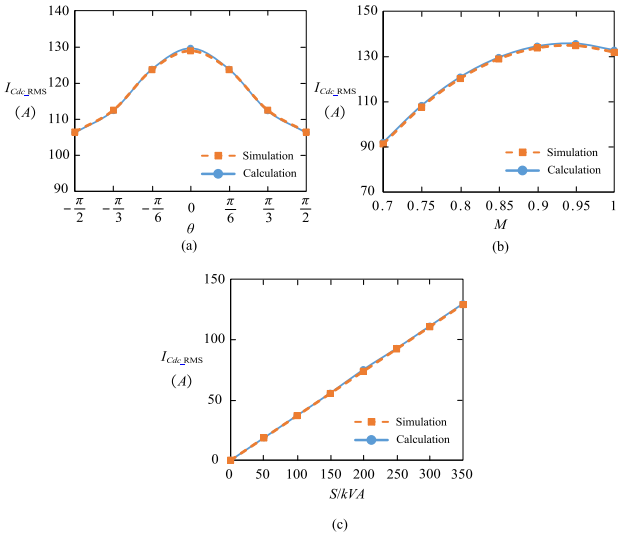

Fig. 14. NPL.H DC-link capacitor rms current varies with variables. (a) $I_{C\mathrm{dc\_rms}}$ varies with different θ. (b) $I_{C\mathrm{dc\_rms}}$ varies with different M. (c) $I_{C\mathrm{dc\_rms}}$ varies with different S.

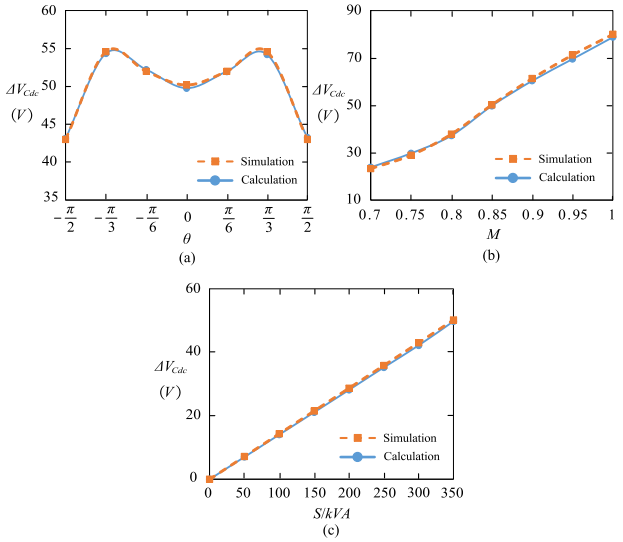

Fig. 15. NPL.H DC-link capacitor voltage ripple varies with variables. (a) $\Delta V_{C\mathrm{dc}}$ varies with different θ. (b) $\Delta V_{C\mathrm{dc}}$ varies with different M. (c) $\Delta V_{C\mathrm{dc}}$ varies with different S.

calculation results under different inverter operating conditions are still in excellent agreement. A single parameter variation with the same base case is also used for each subplot.

To better evaluate the accuracy of the proposed theoretical calculation model using the low-order forms of the rms currents and voltage ripple, the errors between simulation and calculation results are plotted in Fig. 16. Under different operating conditions, the errors are all less than 3%, thereby proving the effectiveness and excellent accuracy of the proposed analytical model.

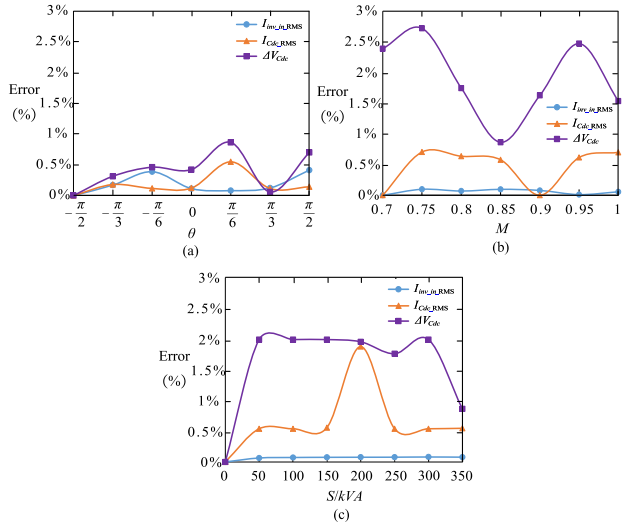

Fig. 16. Error between calculation and simulation results varies with variables. (a) Error varies with different θ. (b) Error varies with different M. (c) Error varies with different S.

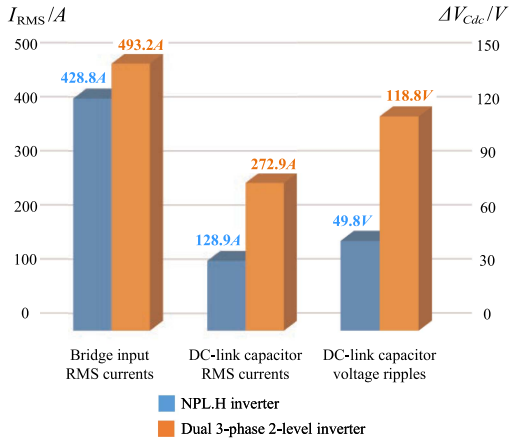

Fig. 17. RMS currents and ripple voltage comparison of NPL.H and dual 3-phase 2-level inverters at rated condition.

V. Discussion on Ripple Performance of NPL.H and Its Implication on DC-Link Capacitance

The ripple performance of NPL.H in the inverter bridge input rms current, dc-link capacitor rms current, and dc-link capacitor voltage is compared with that of the dual T-type 3 L inverter and dual 3-phase 2-level inverter under different operating conditions. Since there is little difference (<3%) between the theoretical calculation results from the derived low-order form expressions and the simulation results, the following comparisons are made based on the simulation. Fig. 17 shows the rms currents and voltage ripple performance of NPL.H and dual 3-phase 2-level inverters at the rated condition used in the previous section (i.e., power factor angle (θ) of 0, modulation index (M) of 0.85, and output apparent power (S) of 350 kVA). NPL.H shows significantly improved performance, compared with the 2-level inverter, in both dc-link current and voltage ripples. It also provides the same output power at a slightly lower input rms current, owing to its low ripple characteristics. For a

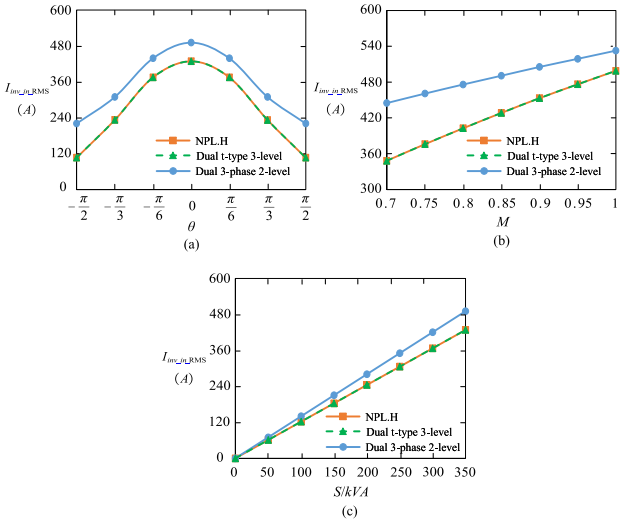

Fig. 18. Comparison results of input rms current varies with variables. (a) $I_{\text{inv\_in\_rms}}$ varies with different θ. (b) $I_{\text{inv\_in\_rms}}$ varies with different M. (c) $I_{\text{inv\_in\_rms}}$ varies with different S.

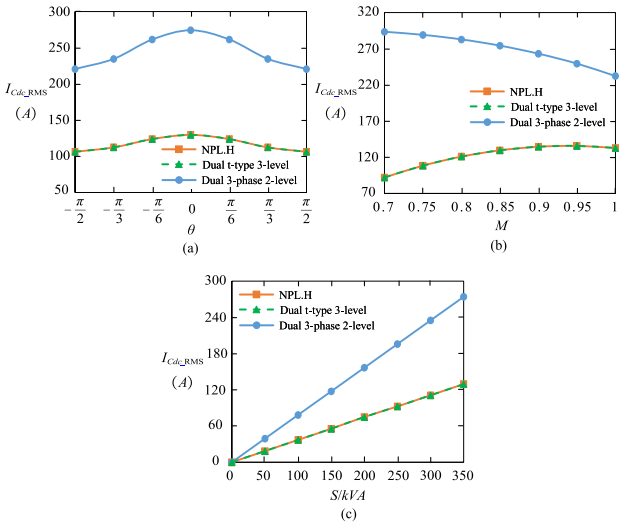

Fig. 19. Comparison results of DC-link capacitor rms current varies with variables. (a) $I_{C\text{dc\_rms}}$ varies with different θ. (b) $I_{C\text{dc\_rms}}$ varies with different M. (c) $I_{C\text{dc\_rms}}$ varies with different S.

more comprehensive comparison, different operating conditions are further tested in simulation, as presented in Figs. 18, 19, and 20. The inverter bridge input rms current, $I_{\text{inv\_in\_rms}}$, dc-link capacitor rms current, $I_{C\text{dc\_rms}}$, and dc-link capacitor voltage ripple, $\Delta V_{C\text{dc}}$, are illustrated as subplots with a single parameter sweep. It can be seen from the comparison results that the rms currents and voltage ripples of NPL.H are significantly smaller than that of traditional dual 3-phase 2-level inverter in every single case in a wide range of operating conditions. It validates the topological advantage of the proposed NPL.H, especially in rms current stress and lower dc-link voltage ripple, which translates into a massive reduction in dc-link capacitance.

It can be found from Figs. 18–20 that the proposed NPL.H has the same rms currents and voltage ripple performance as

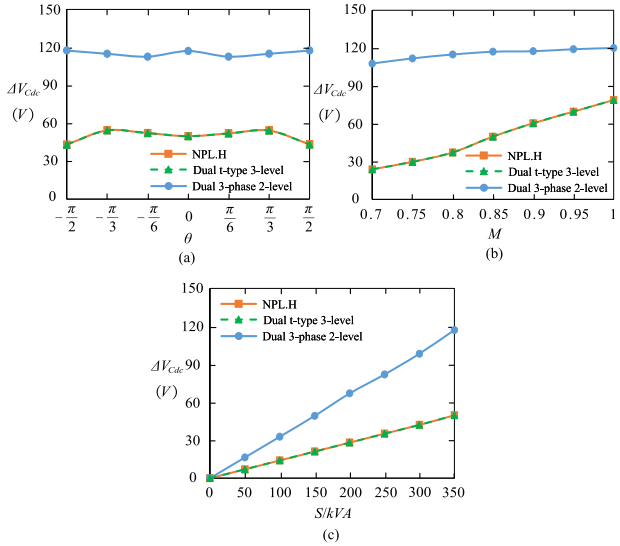

Fig. 20. Comparison results DC-link capacitor voltage ripple varies with variables. (a) $\Delta V_{C\text{dc}}$ varies with different θ. (b) $\Delta V_{C\text{dc}}$ varies with different M. (c) $\Delta V_{C\text{dc}}$ varies with different S.

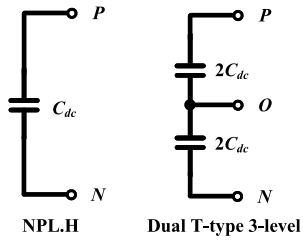

Fig. 21. Comparison of required physical capacitors between NPL.H inverter and dual T-type 3 L inverter.

the dual T-type inverter under the same inverter operation conditions. Nevertheless, the proposed NPL.H not only has a fewer number of switches but also can greatly reduce the required physical capacitance. Fig. 21 shows the dc-link capacitor bank configurations of NPL.H and dual T-type inverter. Although two inverters require the same overall dc-link capacitance under the same dc-link voltage ripple requirement, the dual T-Type 3 L inverter requires two sets of $2C_{\text{dc}}$ capacitors (i.e., $4\,C_{\text{dc}}$ in total) connected in series due to the existence of neutral points, while NPL.H only needs one set of C_{dc} capacitors (i.e., $1\,C_{\text{dc}}$ in total). Therefore, NPL.H reduces the required physical capacitance—hence physical volume as well—to 25% of the capacitance required by the dual T-type 3L inverter.

Table VI gives the dc-link capacitance required by the dual T-type 3 L inverter, NPL.H, and dual 2-level inverter under the same operation condition and dc-link voltage ripple requirement. The capacitance reduction percentages for each case are also presented for convenience. According to Table VI, NPL.H can reduce the required dc-link capacitance by at least 40.2% and as high as 73.4% compared with the dual 2-level inverter and by 75% compared with the T-type 3 L inverter. This substantial reduction of the required dc-link capacitance can lead to an unprecedentedly high level of power density.

TABLE VI
COMPARISON RESULTS OF REQUIRED DC-LINK CAPACITANCE FOR NPL.H, DUAL T-TYPE 3 L, AND DUAL 3-PHASE 2-LEVEL INVERTERS

Conditions \ Inverter		Dual T-type 3 L (i)	Dual 2-level (ii)	**NPL.H (iii)**	Capacitance Reduction w.r.t. (i, ii) by
$S = 350rm$ kVA	$\theta = 0$	264.4 μF	248.4 μF	66.1 μF	75%, 73.4%
$M = 0.75$	$\theta = \frac{\pi}{6}$	477.2 μF	236.7 μF	119.3 μF	75%, 49.6%
$\Delta V_{C\mathrm{dc}} = 5\%V_{\mathrm{dc}}$	$\theta = \frac{\pi}{3}$	560.4 μF	234.3 μF	140.1 μF	75%, 40.2%
$S = 350$ kVA	$\theta = 0$	442.4 μF	260.2 μF	110.6 μF	75%, 57.5%
$M = 0.85$	$\theta = \frac{\pi}{6}$	464.4 μF	250.2 μF	116.1 μF	75%, 53.6%
$\Delta V_{C\mathrm{dc}} = 5\%V_{\mathrm{dc}}$	$\theta = \frac{\pi}{3}$	482.8 μF	255.3 μF	120.7 μF	75%, 52.7%
$S = 350$ kVA	$\theta = 0$	618 μF	264.7 μF	154.5 μF	75%, 41.6%
$M = 0.95$	$\theta = \frac{\pi}{6}$	539.6 μF	266.9 μF	134.9 μF	75%, 49.5%
$\Delta V_{C\mathrm{dc}} = 5\%V_{\mathrm{dc}}$	$\theta = \frac{\pi}{3}$	422.4 μF	286.4 μF	105.6 μF	75%, 63.1%

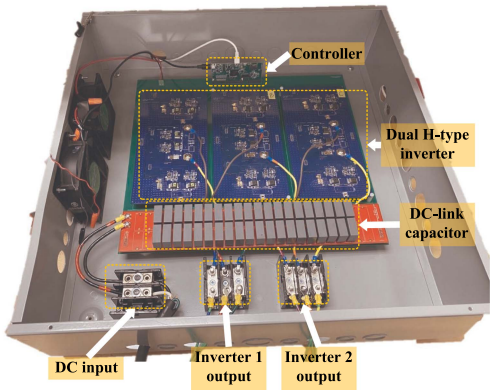

Fig. 22. Experiment prototype of downscaled NPL.H.

TABLE VII
DIFFERENT TEST CASES IN EXPERIMENT

Test cases	Load conditions
Case 1	$R_{\mathrm{load}} = 20\ \Omega,\ L_{\mathrm{load}} = 2$ mH
Case 2	$R_{\mathrm{load}} = 20\ \Omega,\ L_{\mathrm{load}} = 7$ mH
Case 3	$R_{\mathrm{load}} = 20\ \Omega,\ L_{\mathrm{load}} = 10$ mH
Case 4	$R_{\mathrm{load}} = 30\ \Omega,\ L_{\mathrm{load}} = 10$ mH
Case 5	$R_{\mathrm{load}} = 40\ \Omega,\ L_{\mathrm{load}} = 17$ mH

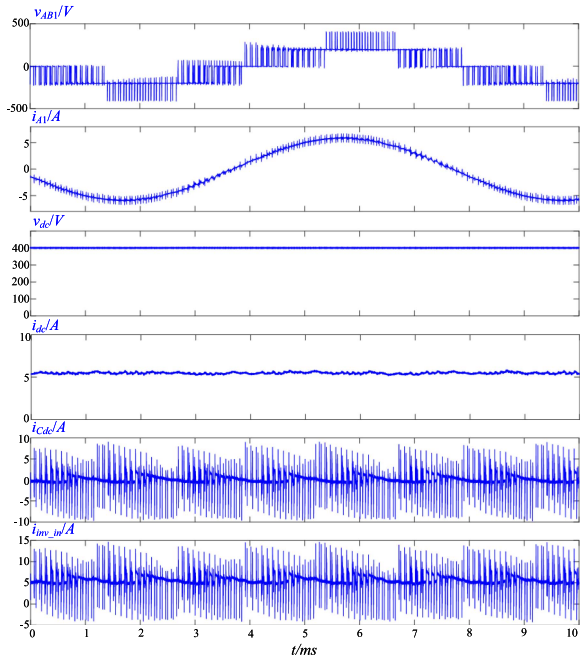

Fig. 23. Experiment waveforms of downscaled NPL.H.

VI. EXPERIMENTAL VERIFICATION

The proposed NPL.H topology and the low-order form analytical model of current and voltage ripple characteristics are evaluated on a scaled-down experimental prototype, as shown in Fig. 22. The prototype consists of two 3 L H-type inverters with same dc-link bus. The detailed experiment parameters are: $V_{\text{dc-link}} = 400$ V, $M = 0.65$, $f_{\text{ac}} = 125$ Hz, $f_{\text{sw}} = 10$ kHz, $C_{\text{dc}} = 200\ \mu$F, and $T_{\text{dead}} = 1.5\ \mu$s. The list of equipment used in the experiment is: 600 V dc power supply (TS600-24 from Magna-Power), oscilloscope (MDA 8208HD from Teledyne Lecroy, bandwidth: 2 GHz, sampling rate: 1.25 GS/s), voltage probes (HVD3106 A from Teledyne LeCroy, bandwidth: 120 MHz), current probes for measuring the dc input and output phase currents (TCP312 A from Tektronix, bandwidth: 100 MHz), and current shunt for measuring the dc-link capacitor current (SDN-414-10 from T&M Research, bandwidth: 2 GHz).

To assess the performance of the analytical method for rms currents and ripple voltage, the experiments are repeated in different inverter operating conditions. The proposed low-order analytical model is verified by five groups of experimental test cases under different RL load conditions, as given in Table VII. For each experiment, the voltage and current waveforms are recorded, and the analytical calculation method was applied to yield corresponding results of the inverter bridge input rms current, dc-link capacitor rms current, and voltage ripple. The experimental waveforms of NPL.H under Case 1 in Table VII with 2.5 kW power are presented in Fig. 23. The experiment waveforms are nearly identical to the aforementioned theoretical analysis and simulation results, validating the functionality and effectiveness of the proposed NPL.H. The iTHD calculated from the experiment results in Fig. 23 is 3.53%.

Then, the measured inverter bridge input rms currents, dc-link capacitor rms currents, and voltages under different test cases with different power factor angles (θ) and output apparent power (S) are processed, and the corresponding theoretical calculation results are obtained through the proposed low-order form analytical method. The comparison results of experimental results and calculation results are shown in Fig. 24. It can be found that under different inverter operating conditions, the experimental results are in good agreement with the theoretical calculation results.

In addition, the errors between the obtained experimental results and theoretical calculation results in Fig. 24 are further calculated and drawn in Fig. 25. There are three curves, which represent the calculation errors of the inverter bridge input rms currents $I_{\text{inv\_in\_rms}}$, dc-link capacitor rms currents $I_{C\text{dc\_rms}}$, and dc-link capacitor voltage ripples $\Delta V_{C\text{dc}}$, respectively. Fig. 25

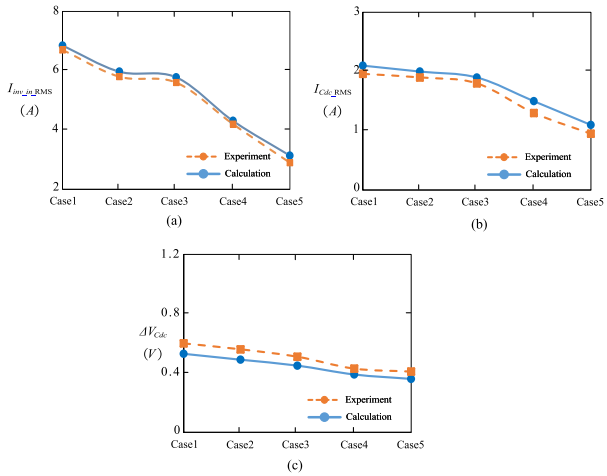

Fig. 24. Comparison of experimental results and calculation results under different test cases. (a) $I_{\text{inv\_in\_rms}}$ under different cases. (b) $I_{C\text{dc\_rms}}$ under different cases. (c) $\Delta V_{C\text{dc}}$ under different cases.

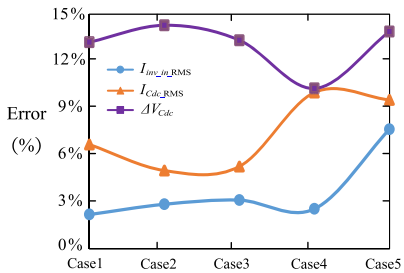

Fig. 25. Error between calculation results and experimental result varies with different test cases.

shows detailed error percentages under different test cases. The error between the calculation and experiment is slightly larger than the error between the calculation and simulation. Potential sources of this error are that the experiments are carried out at a smaller scale, resulting in an increased proportion of calculation errors; and the nonidealities that are difficult to quantify, such as magnetic losses, measurement-related errors, turn-ON and turn-OFF, and transient processes of switching devices, are not fully considered. However, the absolute level of the calculation error is still acceptable to show the validity of the proposed low-order form analytical model, as well as the topological superiority of NPL.H.

VII. Conclusion

A novel NPL.H 3 L dual inverter topology and an improved analytical model of inverter rms currents and voltage ripple are introduced for motor drive applications, especially those with balanced 6-phase, dual 3-phase, or 3-phase OEW motor configurations. The proposed NPL.H has the advantages of multilevel output, lower output harmonics, lower current stress, fewer power switches, and lower capacitor current and voltage ripples while eliminating the neutral clamp, the neutral point current, and the necessity of capacitor voltage balancing altogether. Moreover, the dc-link capacitance in NPL.H can be reduced by 75% compared with the conventional T-type 3 L inverter, and by upto 73% compared with the 2-level inverter, under the same dc-link voltage ripple requirements. These traits will be the essence of the low-cost and high power density future motor drive systems.

Our concise and highly accurate analytical model for calculating the inverter bridge input rms current, dc-link capacitor rms current, and voltage ripple, including the dead-time effect, is introduced. The low-order form approach is proposed to simplify the calculations at the full switching frequency and can be readily expanded to different inverter topologies and modulation methods. The proposed low-order form calculation method is demonstrated to be more effective and enhanced than the traditional methods, with comprehensive consideration of the influence of different variables. Furthermore, the calculation formulae are simple and straightforward, avoiding the need for switching frequency computation components. This low-order form analysis method has been verified through simulation and experiment under various circuit and design parameters and can be used as a general calculation tool for rms currents and voltage ripple in different inverter topologies.

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