Three-Phase ARCP Inverter Using Soft-Switching With a Single Shared Inductor

Thomas Lehmeier, Adrian Amler, Yan Zhou, and Martin März

***Abstract*—Soft-switching in power inverters for drive and grid applications can both enhance the efficiency by reducing switching losses and improve electromagnetic interference (EMI) due to lower switching speeds with their associated $\mathrm{d}v/\mathrm{d}t$. An advantageous topology is the well-known auxiliary resonant commutated pole (ARCP) inverter. The development of such power electronic inverters often focuses on reducing weight, volume, and cost. Considering a three-phase ARCP system, this article presents a novel single shared inductor ($\mathbf{S^2I}$)-ARCP approach to reduce the passive component count in the auxiliary circuit from three to one. The simultaneous use of the shared inductor by more than one phase must be detected and avoided by the control algorithm. A frequency analysis of such occurrences is performed, and a method for avoiding them by shifting the switching edges is presented. The proposed $\mathbf{S^2I}$-ARCP topology together with an appropriate control algorithm is implemented and validated at 10 kW with an 800 V dc-link. Efficiency measurement results indicated a significant loss reduction under soft-switching operation by more than 38% compared with hard-switching, with a peak efficiency value of 99.58%. It is demonstrated that a mere adjustment in the control signal generation can save two resonant inductors without significant disadvantages.**

***Index Terms*—Auxiliary resonant commutated pole (ARCP), collision avoidance, electromagnetic interference (EMI), reduced passive component count, single shared inductor, soft-switching technique, three-phase inverter, two-level topology, zero-current switching (ZCS), zero-voltage switching (ZVS).**

NOMENCLATURE

General Parameters and Components

f [Hz]	Frequency.
i, I [A]	Instantaneous current, constant current.
m_a [–]	Modulation index, $(m_\mathrm{a} = 2\hat{v}_0/V_\mathrm{dc})$.
P [W]	Active power.
s [–]	Switching signal.
t [s]	Time.
t_X [s]	Time instant for event X.
T [s]	Time duration.
v, V [V]	Instantaneous voltage, constant voltage.
η [%]	Efficiency.
φ [°]	Phase angle between voltage and current.
ω [1/s]	Angular frequency.
C [F]	Capacitor or capacitance.
L [H]	Inductor or inductance.
R [Ω]	Resistor or resistance.
S [–]	Switch.
T [–]	Transistor.
D [–]	Diode.

Abbreviations and Indices

aux	Auxiliary circuit characteristics.
DC+, DC−	Positive and negative dc-rail.
el	Fundamental harmonic output characteristics.
HS, LS	High-side, low-side.
load	ac-side load characteristics.
loss	Losses.
min, max	Minimum and maximum value.
p, n	Auxiliary inductor current direction.
R, S, T	ac-side output phase.
r	Characteristic values at resonant frequency.
ripple	Ripple related characteristics.
sn	Snubber (capacitor).
sw	Switching cycle related characteristics.
0	dc-link midpoint.

ARCP Related Parameters

I_boost [A]	Commutation current at the start of the transition.
I_ramp [A]	Auxiliary inductor current at the start of the transition, $(I_\mathrm{ramp} = I_\mathrm{load} + I_\mathrm{boost})$.
I_th [A]	Threshold for auxiliary circuit activation.
T_act [s]	Auxiliary circuit activation time.
$T_\mathrm{com,acsc}$ [s]	Auxiliary circuit supported commutation duration.
$T_\mathrm{com,csc}$ [s]	Capacitive self-commutation duration.
T_dead [s]	Main switch dead-time.
T_lock [s]	Auxiliary circuit reactivation lockout-time.
T_p [s]	Pulse cycle, $(T_\mathrm{p} = T_\mathrm{sw}/2)$.
T_ramp [s]	Auxiliary current ramp-up/ramp-down time.
T_zvs [s]	ZVS precision tolerance.
$\mathcal{P}_\mathrm{rel}$ [%]	Relative collision rate in relation to fundamental period.
Q_tot [As]	Total charge stored in snubber capacitors.

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I. Introduction

HIGHER efficiency, less heat to be removed, lower electromagnetic interference (EMI), less noise emission, better controllability, simplified power module design, and smaller passive components are among the main goals when designing power electronic systems. On one hand, for drive or grid inverters in the medium to high kilowatt power range, a high switching frequency is beneficial for waveform quality, controllability, and the design of passive components. On the other hand, EMI requirements, the semiconductors, and the power module design limit the switching speed [1], [2].

In the 1990s, the constraints of the available power semiconductors, such as early insulated gate bipolar transistors (IGBTs) or gate turn-OFF-thyristors (GTO) were especially prevalent. To improve the efficiency and raise the switching frequency, topologies realizing soft-switching were developed [3], [4], [5], [6]. Soft-switching reduces the dependency of the losses on the switching speed. This gives an additional degree of freedom to the system design. Realizing higher switching frequencies may increase the efficiency of electric motors [7], whereas active and passive circuit components can be utilized to their full potential [8]. A limited voltage slew-rate reduces the stress on bearings and the isolation system of electric machines, as well as overvoltages at the machine terminals [8], [9]. Moreover, EMI properties can be improved [10], [11]. Although there are better power semiconductors available today, the issue is still prevalent as new, more demanding application areas emerge, such as solar-to-grid inverters or drive inverters for electric vehicles (EVs). These systems require high efficiency and an increased power density without exceeding the limits for EMI and $\mathrm{d}v/\mathrm{d}t$. Therefore, the full potential of available wide band-gap power semiconductors and even IGBTs cannot be utilized using the standard hard-switching two-level voltage source inverter (VSI) topology [12]. So, it is appropriate to consider soft-switching concepts for the mentioned applications.

Methods for realizing soft-switching in two-level VSIs can be classified into three categories. First, there are the "load resonant" systems, as mentioned in [13]. They employ only inherent components of the circuit, namely the load inductance and the parasitic switch capacitance, for realizing a soft transition. Only certain combinations of the switching direction and the load current can be loss-relieved. Thus, a high current ripple is necessary for continuous soft-switching, which is impractical for high-power and drive applications [6]. Second, in systems with a "resonant link" or "quasiresonant link" an auxiliary circuit is added to the dc-link to reduce the link voltage at the bridge inverter temporarily, thus achieving zero-voltage switching (ZVS). Examples of this category are the resonant dc-link inverter [5] or the active clamped resonant dc-link inverter [4], [14]. However, high switching overvoltages and oscillations are among the problems of topologies in this category [15]. It is also necessary for the auxiliary circuit to conduct the load current continuously, thus causing significant additional losses [6]. Systems with a "resonant transition" or "resonant snubber" belong to the third category. Suitable examples are the auxiliary resonant commutated pole (ARCP) [3], the zero-current transition inverter [7], or the zero-voltage transition inverter with its derivatives (e.g., coupled inductor, single switch, or single inductor) [8], [16], [17]. These topologies are advantageous as the auxiliary circuit only conducts current while supporting a commutation process, and traditional modulation schemes, such as space vector modulation are generally applicable [6], [9].

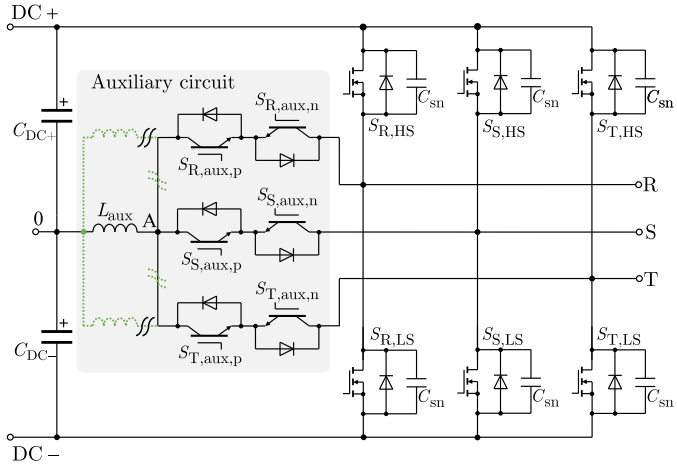


Fig. 1. Circuit diagram of the proposed three-phase two-level ARCP topology with a single shared inductor (solid black line) and the conventional ARCP circuit configuration (dotted green line).

For the mentioned reasons, the "resonant transition" concepts are preferable for modern drive or grid applications. In particular, the ARCP principle offers comparatively higher efficiency [17] and also avoids an excessive number of components or complex components, such as coupled magnetics [8]. Research interest on ARCP has increased recently and different applications for dc/dc converters [18] and EV drives [9] and implementations considering semiconductor properties [19], EMI [20], topological modifications [5], [21], [22], [23], and control schemes [24] have been discussed.

However, the ARCP topology has the potential to further reduce the number of passive components, particularly the potentially bulky and heavy resonant inductors. This has not been adequately addressed in literature. As the current flows in the inductors only for a fraction of a switching cycle, the same inductor could be used for the different phases of a multiphase system. Gong et al. [23] proposed the use of two inductors for the two commutation directions in a three-phase system, thus sparing one inductor. The number of inductors can be further reduced if only a single shared inductor is used for a three-phase system, as proposed in this article. The topological reduction and its implementation, as suggested in the pending patent [25], is analyzed in detail in this article. The suggested topology versus the conventional topology is shown in Fig. 1.

The inverter consists of a VSI bridge-type inverter with its six main switches (three high-side switches S_{HS} and three low-side switches S_{LS} with their snubber capacitors C_{sn}) and three bidirectional auxiliary switches ($S_{\mathrm{aux,p}}$ for the positive auxiliary current direction and $S_{\mathrm{aux,n}}$ for the negative auxiliary current direction), all connected to the only auxiliary inductor L_{aux}. As

mentioned, it is advantageous for an inverter topology, especially in grid and drive system applications, to enable all common modulation schemes without limiting the modulation degree, the direction of the power flow or the phase angle. Therefore, without using an adapted modulation scheme, such as in [18] and [23], situations can arise in which more than one phase requires the simultaneous use of the shared auxiliary inductor. This article analyzes the probability of such "collisions." Possible collision avoidance methods are discussed, as a dc-link short due to an inadequate control of the main and auxiliary switches must be avoided. The functioning of the presented concepts is verified by the implemented single shared inductor (S^2I)-ARCP inverter, realizing a power transfer of 10 kW from an 800 V dc-link.

The rest of this article is organized as follows. An introduction into drive inverters and into the considered topology is given in Section I. Section II contains a detailed analysis of the voltage and current waveforms during the auxiliary circuit supported switching. This is the base for analyzing the constraints and possible control methods of the S^2I-ARCP topology in Section III. Section IV presents an experimental realization of the proposed circuit. The discussion in Section V looks into the measured results and insights into the implementation. Finally, Section VI concludes this article.

II. General Considerations for ARCP

The ARCP principle of operation, timing, and analytical description has for the most part already been dealt with in detail in the past literature, for example [3], [26], and [27]. Therefore, only the basic and most important relationships are recalled while introducing the used operational strategy to allow a more in-depth understanding of the S^2I-ARCP behavior and its collision rate results in Section III.

A. Operation Principle and Timing

This section describes the operation principle of the ARCP circuit and thus applies to both the conventional ARCP and the S^2I-ARCP. For this purpose, a single-phase two-level ARCP circuit diagram is shown in Fig. 2. The depicted clamping diodes (illustrated in dashed lines) are optional and do not take part in the normal commutation process. They can be introduced as a precautionary measure, limiting the voltage in case of a mistimed S_{aux}-switch-OFF with a current-carrying L_{aux} [20] or in case of excessive parasitic oscillations between L_{aux} and the output capacitance of the auxiliary switches [28].

For a better system performance, a load dependent "variable timing" control for the auxiliary circuit is used, similar to [24], [22], [29], and [30]. Depending on the load current level and direction, the operation of the ARCP can generally be divided into two different operational modes with three different cases. Fig. 3 shows the different cases for both commutation directions. The upper half plane corresponds to rising edge transitions with commutations from LS-switch to HS-switch, whereas the lower half plane corresponds to falling edge transitions with commutations from HS-switch to LS-switch.

Assuming a commutation direction from LS to HS, case (Ia) is applied at positive load currents with the support of the auxiliary

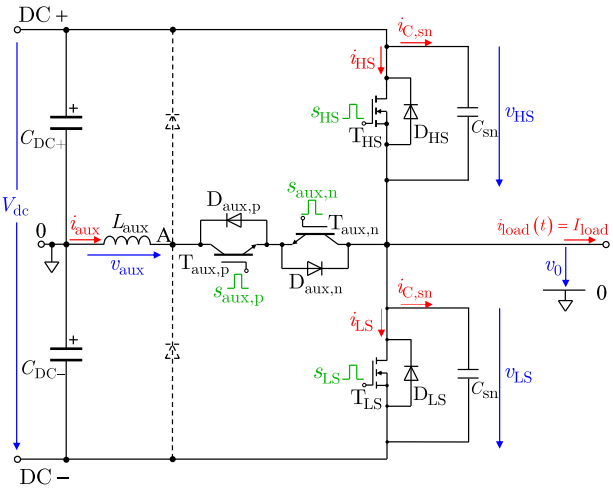


Fig. 2. Single-phase two-level ARCP circuit with current and voltage notation definition.

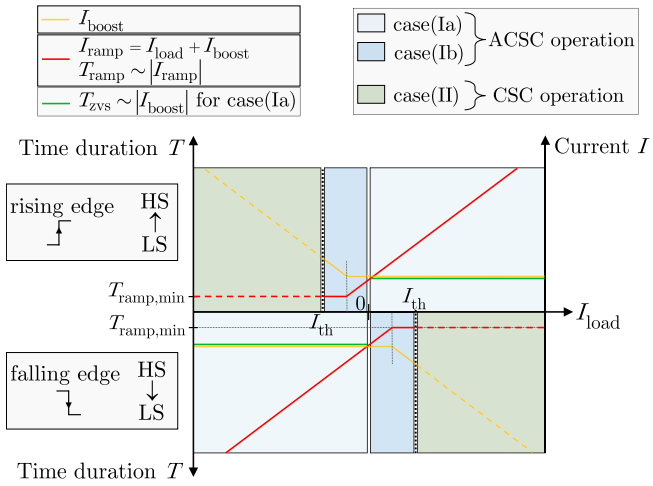


Fig. 3. Operational strategy in different operating points under ACSC and CSC. The dashed lines (- -) represent an operation with exclusively ACSC in use.

circuit, in the following referred to auxiliary circuit supported commutation (ACSC). Negative currents at light load conditions also demand ACSC for an accelerated commutation and are described by case (Ib). Commutation case (II) is used for high negative load currents when switching from LS to HS. In this case, the auxiliary circuit is not needed and the snubber capacitors self-commutate automatically with the given load current, referred to capacitive self-commutation (CSC). The boundary between ACSC and CSC is reached at the threshold current level I_{th}. The threshold current represents an additional control parameter and leads to an increase in the control complexity compared with pure ACSC operation [30]. But the losses in the disabled auxiliary circuit are reduced significantly with the combination of ACSC and CSC operation, which is therefore also applied in this work. Case (Ia) must be swapped with case (Ib)+(II) for the inverse commutation direction. ACSC is now necessary for a high negative I_{load}, while CSC is applicable for a high positive I_{load}. The implementation of the control

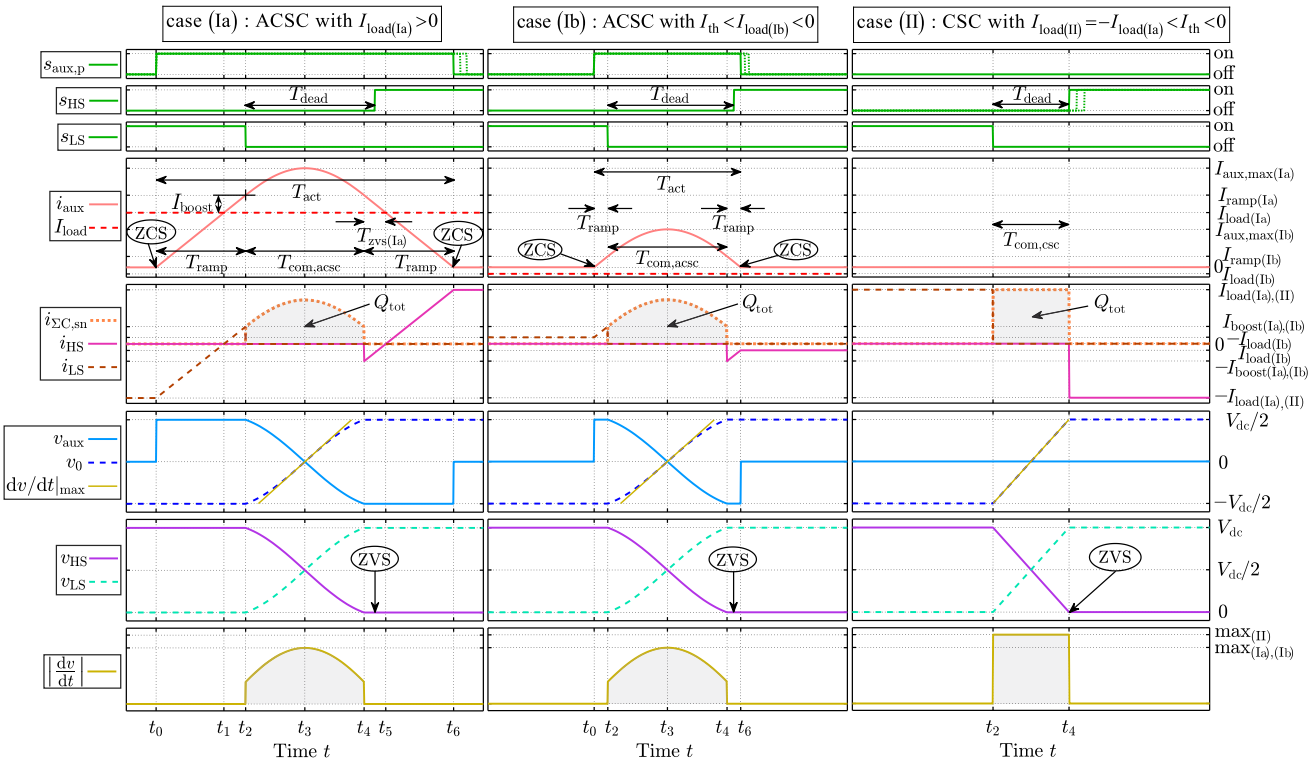


Fig. 4. Timing diagram with switching signals, current and voltage waveforms, and voltage slew-rate for the three different cases during rising edge transitions (corresponds to a commutation from LS-switch to HS-switch). Note that the scaling of the x-axis and the y-axis is valid for all cases. $I_{load(II)}$ is not displayed. The current and voltage waveforms for a HS $\rightarrow$ LS commutation would each be mirrored vertically.

strategy used and the choice of control parameters will be discussed in more detail in a later section.

To simplify the following analysis of the commutation process, several common assumptions and simplifications are made.

1) The split dc-link capacitor is perfectly balanced and its midpoint 0 is used as reference potential.
2) The power semiconductors are assumed ideal (in particular voltage independence of C_{sn}, no forward voltage drop, infinitely short switching times) as well as the passive components.
3) The load current is constant in time $i_{load} = I_{load}$ during the short commutation process, thus neglecting the current ripple under the consideration of a high load inductance.

Fig. 4 shows the three discussed commutation cases in a timing diagram with all relevant switching signals as well as voltage and current waveforms, including the voltage slew-rate $\mathrm{d}v/\mathrm{d}t$. The stages of ACSC operation for case (Ia) and case (Ib) can be described as follows.

1) *Initial state* $\{t < t_0\}$*:* $\mathrm{T_{LS}}$ is turned-ON and I_{load} is flowing through $\mathrm{T_{LS}}$ in the reverse direction.
2) *At* t_0*:* $\mathrm{T_{aux,p}}$ is turned-ON under zero-current switching (ZCS) condition.
3) *Pre-charging stage* $\{t_0 < t < t_1\}$*:* As v_{aux} is equal to $V_{dc}/2$, i_{aux} ramps up linearly to the level of I_{load}, while the current through $\mathrm{T_{LS}}$ simultaneously decreases to zero.
4) *Boosting stage* $\{t_1 < t < t_2\}$*:* i_{aux} continues to ramp up linearly to accumulate more energy for boosting the following commutation process; the current direction through $\mathrm{T_{LS}}$ reverses and increases in the forward direction.
5) *At* t_2*:* $\mathrm{T_{LS}}$ is turned-OFF at $i_{aux} = I_{ramp}$ and $i_{LS} = i_{\Sigma C,sn} = I_{boost}$, causing the controlled triggering of the resonant transition.
6) *Resonant commutation stage* $\{t_2 < t < t_4\}$*:* L_{aux} resonates with C_{sn} of both switches; the voltage across the HS-switch swings down to zero in a slow, smooth, and sinusoidal manner until the conduction condition of the antiparallel diode is reached while the voltage across the LS-switch swings up to V_{dc}; the $\mathrm{d}v/\mathrm{d}t$ curve clarifies the "*S*-shape" of the voltage transition; the maximum $\mathrm{d}v/\mathrm{d}t$ occurs at t_3; the vertical jumps at t_2 and t_4 are smoothed in practice due to the nonlinear output capacitance of the switches and the finite switching speed.
7) *Clamping stage* $\{t_4 < t < t_5\}$*:* $\mathrm{D_{HS}}$ starts to conduct at t_4 and clamps the voltage across the HS-switch; as v_{aux} is now equal to $-V_{dc}/2$, i_{aux} ramps down linearly to the level of I_{load} while the current through $\mathrm{D_{HS}}$ simultaneously decreases; during this stage $\mathrm{T_{HS}}$ is turned-ON under ZVS condition and takes over the current from $\mathrm{D_{HS}}$ in the reverse direction.
8) *Discharging stage* $\{t_5 < t < t_6\}$*:* The current direction through $\mathrm{T_{HS}}$ reverses at t_5 and increases in the forward direction while i_{aux} continues to ramp down to zero.
9) *Final state* $\{t > t_6\}$*:* $\mathrm{T_{HS}}$ takes over the full load current at t_6 while i_{aux} drops to zero and $S_{aux,p}$ can be turned-OFF

TABLE I
OVERVIEW OF THE IMPORTANT ARCP VALUES FOR EACH CASE

Commutation direction	$I_{\text{load}} > 0$	$I_{\text{load}} < 0$
HS ↑ LS	case (Ia)	case (Ib) | (II)
		$I_{\text{load}} \geq I_{\text{th}} \mid < I_{\text{th}}$
	$S_{\text{aux,p}}$ ON	$S_{\text{aux,p}}$ ON | OFF
	$I_{\text{ramp}} > 0$	$I_{\text{ramp}} > 0 \mid = 0$
	$I_{\text{boost}} > 0$	$I_{\text{boost}} > 0 \mid = 0$
	$v_{\text{aux}}(t_2) = V_{\text{dc}}/2$	$v_{\text{aux}}(t_2) = V_{\text{dc}}/2 \mid = 0$
	$v_{\text{LS}}(t_2) = 0$	$v_{\text{LS}}(t_2) = 0$
HS ↓ LS	case (Ib) | (II)	case (Ia)
	$I_{\text{load}} \leq I_{\text{th}} \mid > I_{\text{th}}$	
	$S_{\text{aux,n}}$ ON | OFF	$S_{\text{aux,n}}$ ON
	$I_{\text{ramp}} < 0 \mid = 0$	$I_{\text{ramp}} < 0$
	$I_{\text{boost}} < 0 \mid = 0$	$I_{\text{boost}} < 0$
	$v_{\text{aux}}(t_2) = -V_{\text{dc}}/2 \mid = 0$	$v_{\text{aux}}(t_2) = -V_{\text{dc}}/2$
	$v_{\text{LS}}(t_2) = V_{\text{dc}}$	$v_{\text{LS}}(t_2) = V_{\text{dc}}$

under ZCS condition (whereby the exact turn-OFF time after time instant t_6 is not that relevant).

Note that the precharging and discharging stages are not present in case (Ib). The effective subcircuits for each stage presented in [3] may be of interest to readers seeking further explanation. Regarding the operational strategy, if the load current falls below zero, described by case (Ib) in Fig. 3, I_{ramp} continues to decrease linearly until a minimum ramp duration $T_{\text{ramp,min}}$ is reached. $T_{\text{ramp,min}}$ is introduced to ensure a clean switching transition and a clear distinction between ACSC and CSC operation. Thus, the turn-ON of the auxiliary switch at t_0 should always precede the turn-OFF of the main switch at t_2. From this point on, I_{boost} linearly increases automatically to compensate for the rise of I_{load} in the negative direction, since T_{ramp} cannot be further reduced.

Case (II) under CSC is shown on the right-hand side of Fig. 4. During a capacitive commutation, the voltages transition linearly since only the C_{sn} of both main switches are involved in the commutation process and these are charged and discharged by a constant I_{load}. Therefore, the $\mathrm{d}v/\mathrm{d}t$ is constant and generally unequal to cases (Ia) and (Ib).

The area below the $i_{\Sigma\text{C,sn}}$ curve between t_2 and t_4 corresponds to the total charge Q_{tot} stored in the snubber capacitors C_{sn}, which must be charged and discharged at each commutation. C_{sn} comprises the parallel connection of the switch output capacitance, parasitic structure-related capacitances, and, if needed, another discretely connected capacitor. It can be estimated as follows:

$$C_{\text{sn}} = \frac{Q_{\text{tot}}}{2V_{\text{dc}}}. \tag{1}$$

The area below the $\mathrm{d}v/\mathrm{d}t$ curve is proportional to Q_{tot} and is equal to the value of the voltage transition $\Delta V = V_{\text{dc}}$, which is identical in all three cases. Therefore, short commutation times results inherently in a high $\mathrm{d}v/\mathrm{d}t$.

For further analysis, the characteristic ARCP values for each case are given in Table I.

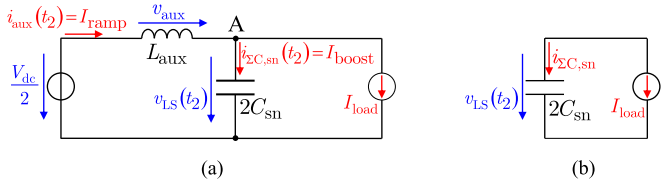


Fig. 5. Equivalent circuit during commutation stage under (a) ACSC and (b) CSC with the initial values at time instant t_2.

B. Analytical Description

The following analytical expressions are valid for both polarities of I_{load} and for both commutation directions. The equivalent circuits during the resonant stage under ACSC and during CSC with the given initial conditions, according to Table I, are shown in Fig. 5.

1) ACSC Operation: The *LC* resonant circuit under ACSC operation is driven by $V_{\text{dc}}/2$ and influenced by I_{load}, wherein both C_{sn} act in parallel. The circuit can be represented in a second order differential equation without attenuation. The solution for the inductor current during the resonant stage $t_2 \leq t < t_4$ as well as the ramp stages $t_0 \leq t < t_2$ and $t_4 \leq t \leq t_6$ can be expressed as follows:

$$i_{\text{aux}}(t) = \begin{cases} \frac{V_{\text{dc}}}{2L_{\text{aux}}}(t - t_0), & \text{if } t_0 \leq t < t_2 \\ I_{\text{load}} + i_{\Sigma\text{C,sn}}(t), & \text{if } t_2 \leq t < t_4 \\ I_{\text{ramp}} - \frac{V_{\text{dc}}}{2L_{\text{aux}}}(t - t_4), & \text{if } t_4 \leq t \leq t_6 \end{cases} \tag{2}$$

with

$$i_{\Sigma\text{C,sn}}(t) = I_{\text{boost}} \cos\left[\omega_{\text{r}}(t - t_2)\right] + \frac{V_{\text{dc}}}{2Z_{\text{r}}} \sin\left[\omega_{\text{r}}(t - t_2)\right]$$

whereby $i_{\Sigma\text{C,sn}}$ is the total current charging and discharging the snubber capacitors. During the linear ramp-up interval $t_0 \leq t < t_2$ and ramp-down interval $t_4 \leq t < t_6$, i_{aux} rises with a slope of $\mathrm{d}i_{\text{aux}}/\mathrm{d}t = V_{\text{dc}}/2L_{\text{aux}}$ and falls with $\mathrm{d}i_{\text{aux}}/\mathrm{d}t = -V_{\text{dc}}/2L_{\text{aux}}$. Z_{r} and ω_{r} are the characteristic impedance and the angular frequency of the resonant circuit, respectively. They solely depend on the components L_{aux} and C_{sn} involved in the resonance

$$Z_{\text{r}} = \sqrt{\frac{L_{\text{aux}}}{2C_{\text{sn}}}} \qquad \omega_{\text{r}} = \frac{1}{\sqrt{2L_{\text{aux}}C_{\text{sn}}}}. \tag{3}$$

In the precharging and boosting stage i_{aux} ramps up to I_{ramp} during the auxiliary current ramp interval

$$T_{\text{ramp}} = \frac{2L_{\text{aux}}\,|I_{\text{ramp}}|}{V_{\text{dc}}} = \frac{2L_{\text{aux}}\,|I_{\text{load}} + I_{\text{boost}}|}{V_{\text{dc}}}. \tag{4}$$

The current through the auxiliary inductor at t_4 in Fig. 4 and thus at the end of commutation is equal to the start value of the resonance at t_2. Solving (2) for $i_{\Sigma\text{C,sn}}(t = t_2) = i_{\Sigma\text{C,sn}}(t = t_4)$ yields the resonant commutation duration $T_{\text{com,acsc}}$. With help of $\tan(x/2) = (1 - \cos x)/\sin x$ follows:

$$T_{\text{com,acsc}} = \frac{2}{\omega_{\text{r}}} \arctan\left(\frac{V_{\text{dc}}}{2Z_{\text{r}}\,|I_{\text{boost}}|}\right) \leq T_{\text{dead}}. \tag{5}$$

The resulting total activation time of the auxiliary switch and hence the auxiliary circuit can be given by

$$T_{\text{act}} = \underbrace{\frac{4L_{\text{aux}}\,|I_{\text{ramp}}|}{V_{\text{dc}}}}_{2T_{\text{ramp}}} + \underbrace{\frac{2}{\omega_{\text{r}}}\arctan\left(\frac{V_{\text{dc}}}{2Z_{\text{r}}\,|I_{\text{boost}}|}\right)}_{T_{\text{com,acsc}}} \tag{6}$$

with its maximum value $T_{\text{act,max}}$ at $I_{\text{load,max}}$.

The clamping phase is the time range in which the main switch can turn-ON under ZVS condition. This time range corresponds to the switching precision tolerance duration for ZVS operation, which is denoted as T_{zvs} and is given for both ACSC cases in the following:

$$T_{\text{zvs(Ia)}} = \frac{2L_{\text{aux}}\,|I_{\text{boost}}|}{V_{\text{dc}}} \tag{7}$$

$$T_{\text{zvs(Ib)}} \geq T_{\text{zvs(Ia)}}. \tag{8}$$

For a practical selection of T_{zvs}, it is essential to consider the switching times of the power semiconductor switches, the clock cycle of the microcontroller, and the expected current ripple to enable complete ZVS at every switching instant. Further considerations regarding the parameter selection are discussed in the later Section IV-B.

Case (Ia) results in the tallest and widest i_{aux} pulses during the fundamental period. Its amplitude $I_{\text{aux,max}}$ occurs in Fig. 4 at t_3 and can be calculated with (2) by

$$|I_{\text{aux,max}}| = |I_{\text{load}}| + \sqrt{(I_{\text{boost}})^2 + \left(\frac{V_{\text{dc}}}{2Z_{\text{r}}}\right)^2}. \tag{9}$$

$I_{\text{aux,max}}$ is relevant for short-term maximum component current stress and, if necessary, for designing an appropriate magnetic circuit. The shape of the voltage during the resonant commutation stage ($t_2 \leq t < t_4$) can be derived through differentiating i_{aux} by time. This again leads to a sinusoidal expression for the voltage across L_{aux} and hence for all voltages, e.g. $v_{\text{LS}}(t)$, involved in the commutation cell

$$\begin{aligned} v_{\text{LS}}(t) &= \frac{V_{\text{dc}}}{2} - \overbrace{L_{\text{aux}}\frac{\mathrm{d}i_{\text{aux}}(t)}{\mathrm{d}t}}^{v_{\text{aux}}(t)} \\ v_{\text{LS}}(t) &= I_{\text{boost}}Z_{\text{r}}\sin\left[\omega_{\text{r}}\left(t-t_2\right)\right] + \ldots \\ &\quad + \frac{V_{\text{dc}}}{2}\left\{1-\cos\left[\omega_{\text{r}}\left(t-t_2\right)\right]\right\}. \end{aligned} \tag{10}$$

The resulting slew-rate of all voltages can be obtained by differentiating once again

$$\left|\frac{\mathrm{d}v}{\mathrm{d}t}\right| = \left|\frac{V_{\text{dc}}}{2}\omega_{\text{r}}\sin\left[\omega_{\text{r}}\left(t-t_2\right)\right] + \frac{I_{\text{boost}}}{2C_{\text{sn}}}\cos\left[\omega_{\text{r}}\left(t-t_2\right)\right]\right|. \tag{11}$$

The maximum $\mathrm{d}v/\mathrm{d}t$ occurs at $t = t_3 = t_2 + T_{\text{com,acsc}}/2$, which marks $I_{\text{aux,max}}$ and the intersection of the voltages

$$\begin{aligned} \left|\frac{\mathrm{d}v}{\mathrm{d}t}\right|_{\text{max}} &= \left|\frac{V_{\text{dc}}}{2}\omega_{\text{r}}\sin\left(\frac{\omega_{\text{r}}T_{\text{com,acsc}}}{2}\right) + \ldots\right. \\ &\quad \left. + \frac{I_{\text{boost}}}{2C_{\text{sn}}}\cos\left(\frac{\omega_{\text{r}}T_{\text{com,acsc}}}{2}\right)\right|. \end{aligned} \tag{12}$$

2) CSC Operation: As already discussed in the previous section, the auxiliary circuit can be disabled for transitions with certain load conditions. CSC operation should only be used when $|I_{\text{load}}| > |I_{\text{th}}|$ to keep the commutation duration within acceptable limits. Using Fig. 5(b), the commutation duration can be derived as follows:

$$T_{\text{com,csc}} = \frac{2V_{\text{dc}}C_{\text{sn}}}{|I_{\text{load}}|} \leq T_{\text{dead}}. \tag{13}$$

However, the $\mathrm{d}v/\mathrm{d}t$ is no longer controllable under CSC and differs from ACSC, since $T_{\text{com,csc}}$ depends on the load current level during commutation. Therefore, the $\mathrm{d}v/\mathrm{d}t$ is greatest at the load current peak.

III. Distinction Between S²I-ARCP and Conventional ARCP

While the considerations of the previous chapter are generally applicable for all single and multiphase ARCP systems, the implications of sharing the same resonant inductor in a multiphase S²I-ARCP topology must be discussed further. In principle, an S²I-ARCP inverter behaves similarly to the conventional ARCP with multiple inductors. The voltage and current waveforms are identical during the resonant transition. However, special attention must be paid to the component stress, power losses, and the control algorithm.

The voltage across the auxiliary switches can be V_{dc} at maximum during commutation of another phase in the case of S²I-ARCP, whereas the maximum component stress is ideally only $V_{\text{dc}}/2$ for conventional ARCP. For this reason, the blocking voltage of the auxiliary switches can be chosen lower in conventional ARCP compared with S²I-ARCP. However, a new issue then arises because oscillations between L_{aux} and the parasitic capacitances of the auxiliary switches can reach amplitudes of V_{dc}, which are higher than the blocking voltage of the switches. To avoid damage, measures such as saturable cores to damp the oscillations [31] or clamping diodes [28] are required. Therefore, not being able to reduce the blocking voltage of the auxiliary switches is no major disadvantage for S²I-ARCP.

Regarding the losses in the auxiliary switches for the S²I-ARCP topology, the conduction losses are the same compared with the conventional ARCP, assuming the same switching devices are used. However, higher switching losses are to be expected during ZCS turn-ON since the effective parasitic output capacitance of the auxiliary switches connected in parallel is considerably higher. On the other hand, the rms current in the single inductor of the proposed topology is only $\sqrt{3}$ higher than the rms current of one resonant inductor in conventional ARCP. Therefore, when using the same inductor, the total losses for the three phases are identical, but two inductors are saved. When using the same amount of material for the auxiliary inductor(s) in conventional ARCP and S²I-ARCP, for the latter, the total inductor losses are lower.

To control the S²I-ARCP soft-switching inverter, the switching signals for the main switches can be generated utilizing common pulsewidth modulation (PWM) methods, such

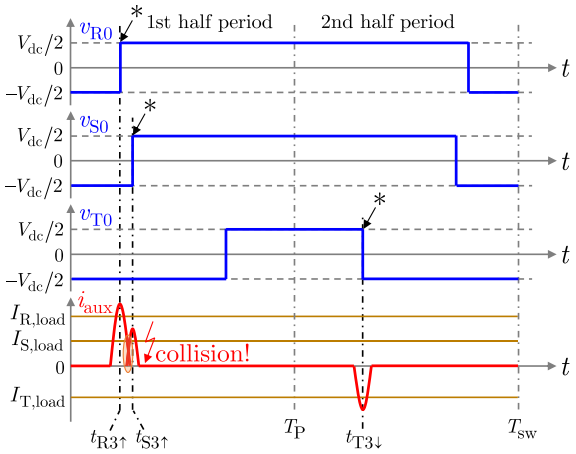


Fig. 6. Single collision between phase R and S. Note that t_{R3}, t_{S3}, and t_{T3} correspond to time instant t_3 in Fig. 4.

as sinusoidal modulation (SPWM) [32], space vector modulation (SVPWM) [33], etc.

To avoid additional conduction losses in the auxiliary circuit and to reduce the current stress of the semiconductor devices, a variable timing control scheme for the auxiliary circuit, as already assumed in Fig. 3, can be implemented [24], [27]. For this case, I_{ramp} as well as T_{ramp} and hence, $I_{aux,max}$ as well as T_{act} are variable in time and are determined by the instantaneous value of $i_{load}(t)$ in each output phase. I_{boost} and thus also $T_{com,acsc}$ is kept fixed to generate identical voltage transitions throughout the whole fundamental cycle T_{el}. The control of I_{boost}, together with the predetermined values of C_{sn} and L_{aux}, determines the voltage waveform calculated by (10) and its corresponding frequency spectrum during the commutation process [20]. In addition, the maximum $\mathrm{d}v/\mathrm{d}t$ is actively controlled with (12) under the usage of ACSC and can be set to a predefined value throughout T_{el}. Since variable timing control depends on I_{load}, additional calculations are required in the microcontroller compared with fixed timing control. Still, variable timing control is preferred for the aforementioned reasons.

The control of the S^{2}I-ARCP topology is more complicated compared with the well-known conventional ARCP topology. This is because the three phases can interfere in a collision with each other when activating the auxiliary circuit. It must always be ensured that only one phase occupies the auxiliary circuit at a certain time stamp, otherwise a short circuit between at least two phases can occur. Fig. 6 shows a sample case for a single collision between the close adjacent edges of phases R and S.

The asterisks mark the edges where the use of ACSC is desired. Both rising edges of v_{R0} and v_{S0} are so close together in time, that the activation intervals of both phases overlap in time and cause a collision. The rare case of an activation interval overlap of all three phases is henceforth called a double collision.

A. Collision Rate Analysis

The issue of collisions is very crucial in S^{2}I-ARCP. Its consequences for the control and practical implementation must be further analyzed in depth. To gain a more profound understanding of the collision mechanism and dependencies, a series of different calculations are performed at different operating points. For this purpose, the relative collision rate $\mathcal{P}_{rel}$ is defined, which indicates the fraction of switching cycles requiring collision avoidance within a fundamental period. The analysis is based on sinusoidal modulation with a ratio of switching frequency to fundamental frequency $f_{sw}/f_{el} = 600$. The dependencies are shown in Fig. 7.

The ARCP design parameters L_{aux} and C_{sn} are varied in Fig. 7(a). As can be seen, $\mathcal{P}_{rel}$ rises with ascending values for L_{aux} and C_{sn}. This can be explained with (4)–(6). Larger parameter values lead to longer time durations and thus increase the probability that the activation intervals of different phases overlap. Note, that the arctan characteristic of the $T_{com,acsc}$ calculation is recognizable in the plotted curves.

Fig. 7(b) describes the dependency of $\mathcal{P}_{rel}$ when varying phase angle φ_{load} and modulation index m_a. Most collisions occur in the case of resistive loads and least for inductive or capacitive loads. The most significant change in behavior occurs at around $\varphi_{load} = \pm 45°$. As will be shown later in Fig. 8, collisions do not occur randomly, but at certain times during the fundamental period. The reason for the mentioned transition is that the current of one phase involved in the collision changes its polarity and no longer requires ACSC operation. It can also be observed that $\mathcal{P}_{rel}$ increases hyperbolically with descending values of m_a. A low modulation index results in small duty cycles with edges very close to each other and hence in high collision rates. The dependence of I_{load} and I_{boost} on the collision rate is examined in Fig. 7(c). The results can be explained with (4)–(6) as well. The higher I_{load}, the longer the ramp phases last and the more collisions will occur. Increasing boost currents lead to a longer T_{ramp} but decreases the commutation duration. The arctan characteristic of the $T_{com,acsc}$ calculation is again recognizable in the plotted curves. In the case of $I_{load} = I_{boost} = 0$, the ramp duration becomes zero and T_{act} is given by

$$T_{act}\Big|_{I_{load}=0,\, I_{boost}=0} = \pi\sqrt{2L_{aux}C_{sn}} \tag{14}$$

which is unequal to zero. Therefore, collisions can still occur at a low rate. Last to note, the steps in the $\mathcal{P}_{rel}$ curves result from the finite ratio between f_{sw} and f_{el} combined with a synchronous pulse pattern.

The location of collisions in the space vector diagram is examined in the next step, which is shown in Fig. 8 for two different load conditions.

Fig. 8(a)–(c) represent low load conditions with ascending phase angles. Once again, the strong dependence of the collision rate on φ_{load} can be observed. Collisions (displayed in red) occur primarily in a rotationally symmetric arrangement at the sector transitions of the space vector diagram (multiples of 60°). This can be explained in the time domain, where the output voltages of two phases intersect at the sector transitions. The duty cycles of both phases are identical at this point and lead to a similar situation, as shown in Fig. 6. The collision region around the sector transitions becomes smaller as the phase angle

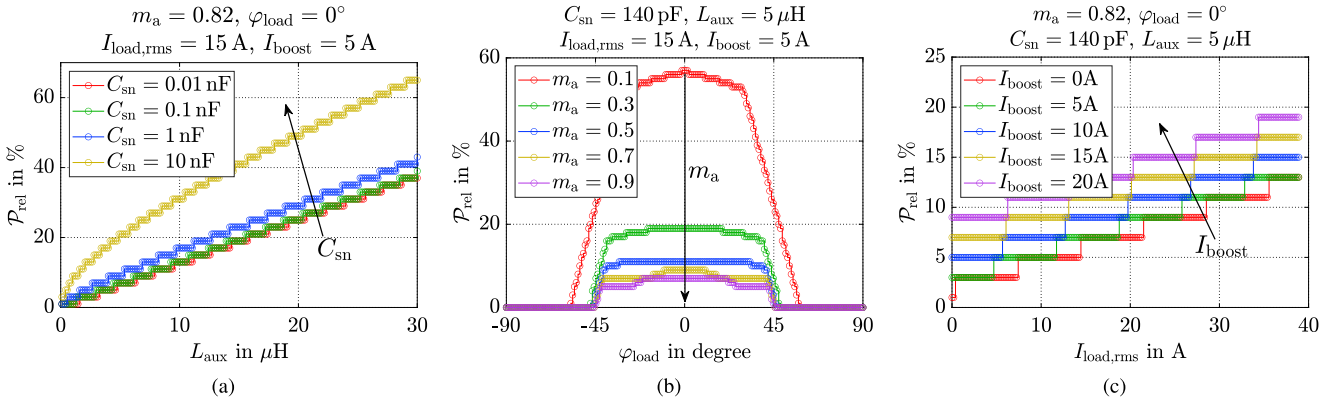


Fig. 7. Single collision rate analysis for different operating points. (a) $\mathcal{P}_{rel}$ versus L_{aux} and C_{sn}. (b) $\mathcal{P}_{rel}$ versus φ_{load} and m_a. (c) $\mathcal{P}_{rel}$ versus $I_{load,rms}$ and I_{boost}. $V_{dc} = 800$ V, $f_{sw} = 30$ kHz, $f_{el} = 50$ Hz, and $f_{sw}/f_{el} = 600$ apply to all operating points.

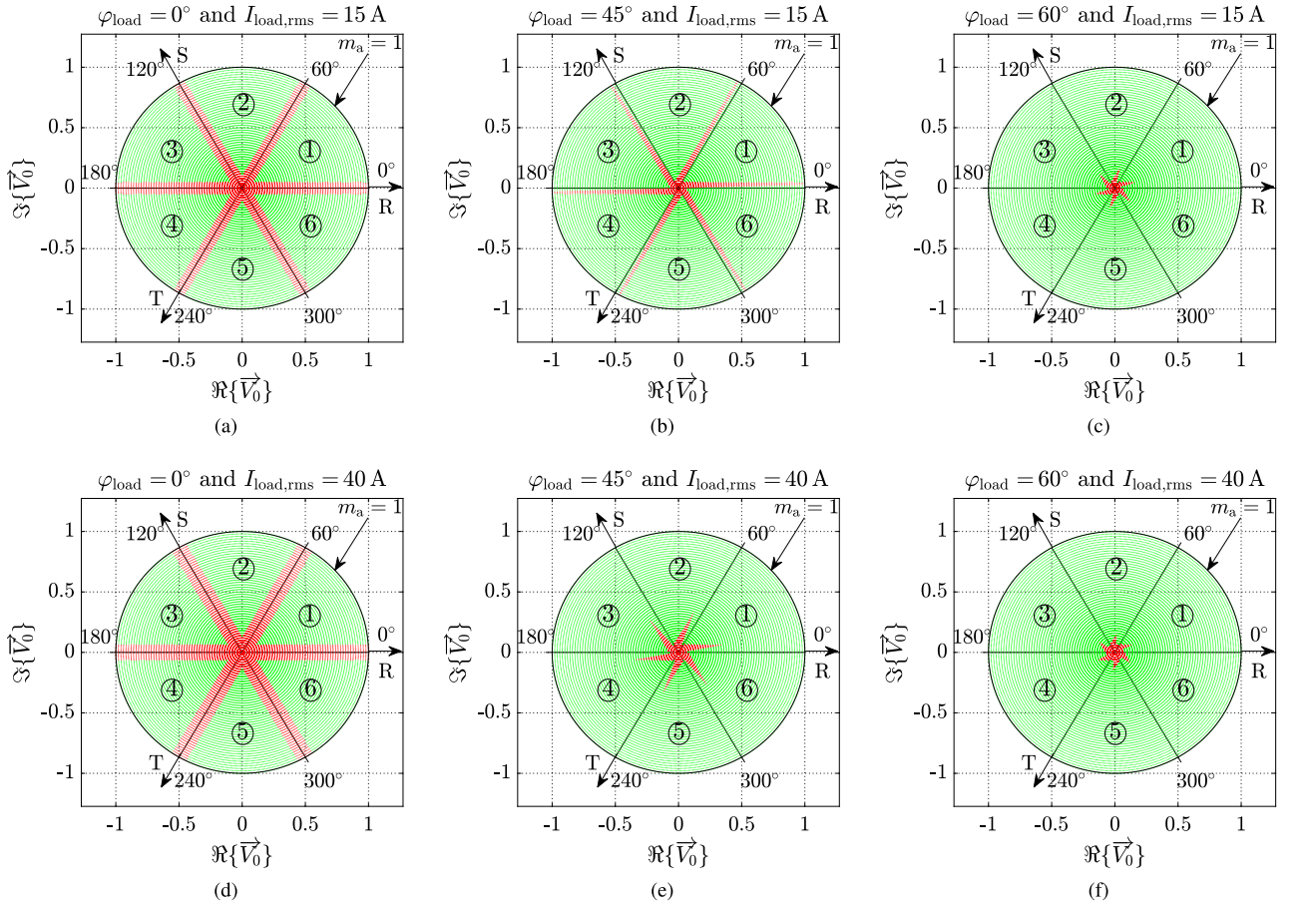


Fig. 8. Location of collisions in the space vector diagram for different operating points. No collisions are marked with the green area, whereas one or more collisions are marked with the red area. (a)–(c) With ascending phase angle in low load condition. (d)–(f) With ascending phase angle in high load condition. $V_{dc} = 800$ V, $f_{sw} = 30$ kHz, $I_{boost} = 5$ A, $C_{sn} = 140$ pF, and $L_{aux} = 5\,\mu$H apply to all operating points.

increases, with collisions now occurring predominantly at a small modulation index [compare also with Fig. 7(b)].

Fig. 8(d)–(f) show the results for high load currents. The collision area around the sector transitions expands noticeably with resistive loads. However, for $\varphi_{load} = 45°$, fewer or no collisions can be observed at higher modulation degrees. It is further observed that very small m_a with very close edges always lead to collisions regardless of the load.

B. Collision Avoidance Method

To prevent a short circuit between two phases or even three phases, a method for handling the aforementioned collisions

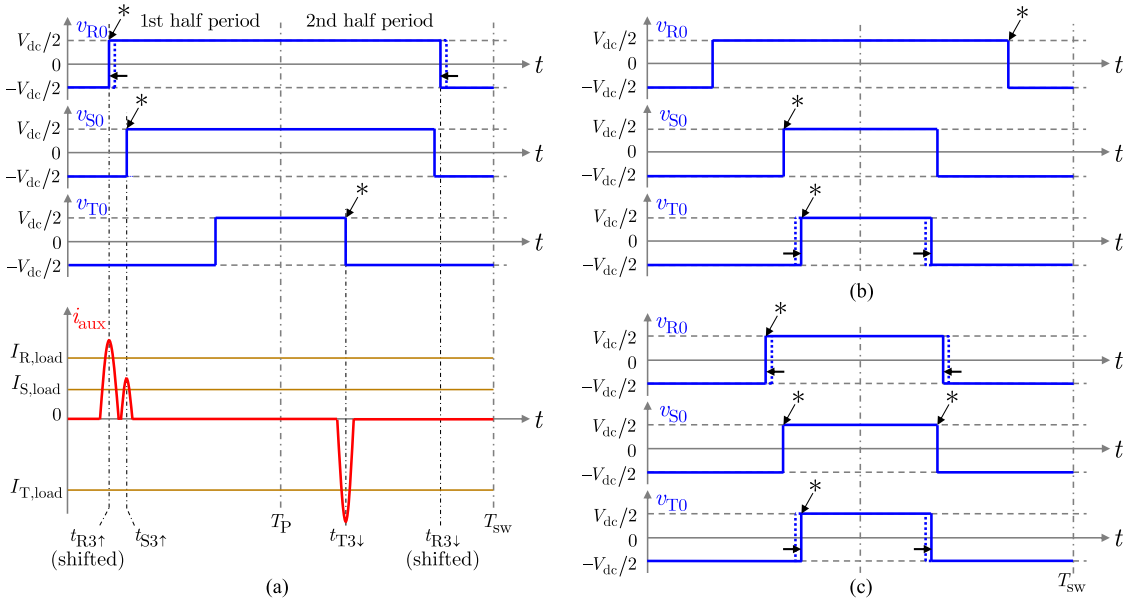


Fig. 9. (a) Single collision avoidance by shifting the rising and falling edge of phase R relative to phase S. Note that t_{R3}, t_{S3}, and t_{T3} correspond to time instant t_3 in Fig. 4. (b) Single collision avoidance by shifting the edges of phase T. (c) Double collision avoidance by shifting the edges of phase R and T.

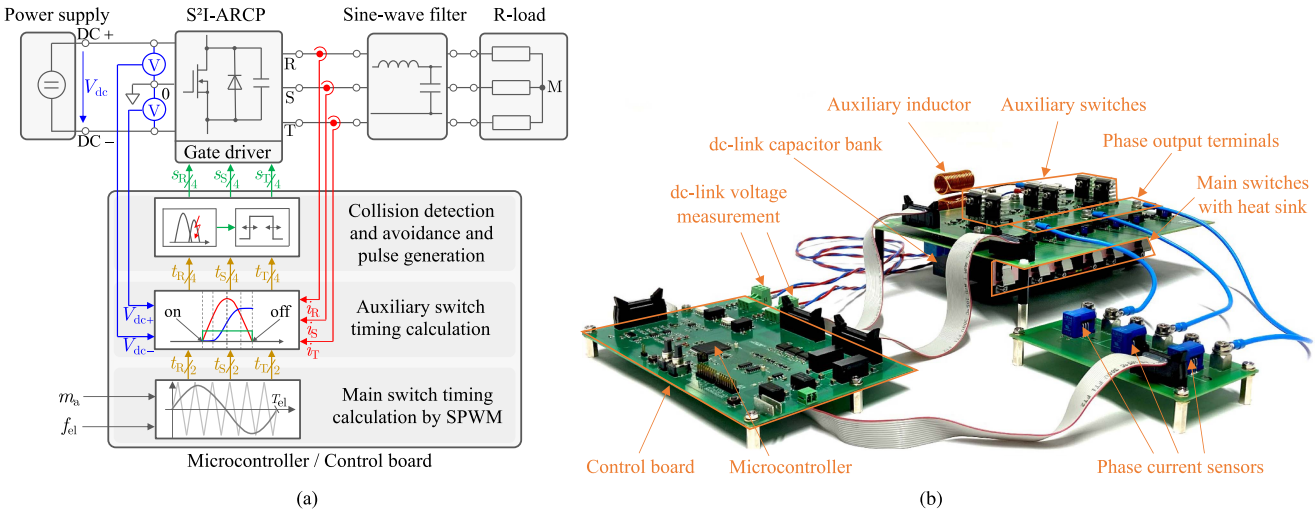


Fig. 10. (a) Experimental setup structure and the stages of pulse generation for the proposed three-phase ARCP inverter with a single shared inductor. (b) Experimental prototype of the S^2I-ARCP.

needs to be implemented. Conceivable methods are described in [25]. This includes shifting the switching edges of the phases involved in the collision to ensure sequential access to the auxiliary circuit. Fig. 9 shows the procedure. In Fig. 9(a), the rising edge of phase R is shifted to the left by at least the overlap time of both auxiliary circuit activations. To keep the required duty cycle constant, the falling edge is also corrected by the same shift to the left. The distortion caused by the small, uniform displacement of both edges can be neglected in practical operation. Other exemplary cases of a single and double collision are shown in Fig. 9(b) and (c). In rare cases, e.g., due to compliance with the minimum pulse duration, the shifting of a switching edge is not possible or would cause a deviation of the duty cycle. Then, the minor deviation of the duty cycle could be disregarded, hard-switching could be performed on this edge, or colliding space vectors, as shown in Fig. 8, could be avoided.

IV. Practical Realization of the Proposed Topology

A three-phase 10 kW S^2I-ARCP inverter prototype was built to verify the proposed topological reduction to a single shared auxiliary inductor. The prototype and the experimental setup with the stages of pulse generation are shown in Fig. 10.

It consists of a control board with a microcontroller and a dc-link voltage measurement, of three-phase current sensors, and of the main circuit board with the auxiliary circuit and a resonant

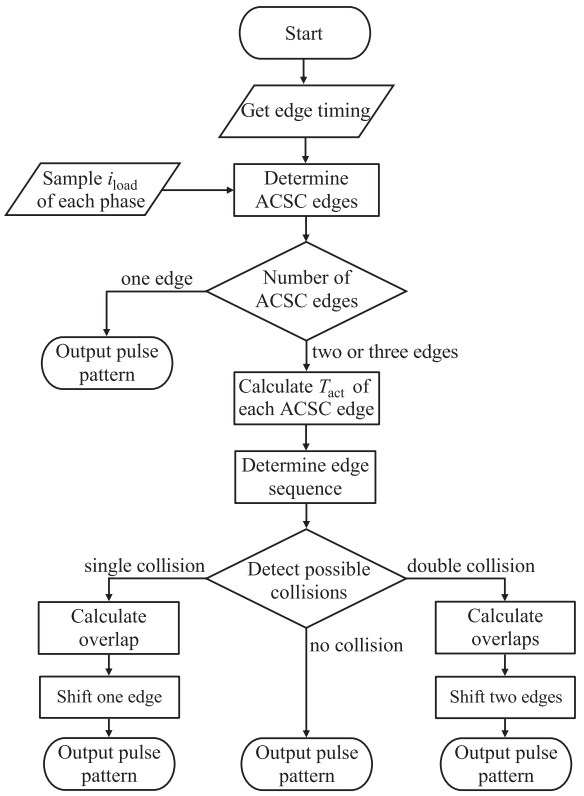


Fig. 11. Flowchart of the implemented control algorithm by shifting the switching edges.

inductor designed as an air coil on the top and the B6-topology with its main switches on the bottom. The auxiliary circuit can be disconnected for a fair comparison with hard-switching tests. A sinusoidal modulation is used to generate the PWM gate signals for the main switches. Besides the dead-time generation and collision avoidance, the signals are not further modified and are directly forwarded to the gate drivers. A variable timing control scheme, as previously described, and a collision avoidance algorithm are implemented for the auxiliary switches. Both control algorithms run sequentially on the microcontroller. Variable timing control relies on the online calculation of T_{ramp} with the phase current sampling and the dc-link voltage measurement at the start of each pulse cycle T_{P}. The polarity of I_{load} determines whether $S_{\text{aux,p}}$ or $S_{\text{aux,n}}$ must be turned ON.

A. Implementation of the Collision Avoidance Algorithm

The flow chart of the implementation of the proposed collision avoidance algorithm, as presented in Section III-B, is shown in Fig. 11.

The algorithm starts with the edge timing t_{R3}, t_{S3}, and t_{T3} calculated by the modulation scheme (here SPWM) and the current sampling of each phase. Next, the number of voltage edges within a pulse cycle T_{P} using ACSC needs to be determined. If ACSC is required for only one edge, the control algorithm is continued by placing the edges as originally requested. If two or three edges require ACSC operation, it is also necessary to determine the edge sequence of the three phases when calculating the activation times of each ACSC edge. Next, collision detection takes place for both cases. If no collision is detected, the control algorithm is continued by placing the edges as originally requested. In the case of a single collision between two phases, one involved edge is shifted so that ACSC can always be activated for both edges. If the first and second edge causes the collision, the first edge is shifted to the left by at least the overlap time [see Fig. 9]. If the single collision is caused by the second and third edges, the third edge is shifted to the right by at least the overlap time. In the case of a double collision between three phases, the first edge is at least shifted by the overlap time to the left and the third edge is at least shifted by the overlap time to the right. Thus, ACSC can be activated for all edges. When the shift is complete, the control algorithm continues with the new edges and outputs the collision-free pulse pattern.

The algorithm is executed once within T_{sw}, whereby the collision-free pulse pattern is output in the following switching cycle. The algorithm here is optimized for a short execution time of the avoidance algorithm within the limited resources of the microcontroller. Therefore, a minor deviation of the edge placement is possible, especially in the rare case of double collisions, which can lead to an altered duty cycle and modulation index. For the considered operating points, no significant impact can be observed in Fig. 13, and no double collisions occurred. But if a more precise realization of the originally calculated pulse pattern is required, other collision avoidance methods as previously mentioned can be applied.

B. Component and Parameter Selection

The selection of the correct components and design parameters is very essential for the correct operation of the S^{2}I-ARCP inverter and is discussed in the following. An overview of the results is given in Table II.

The design of the parameters I_{boost}, L_{aux}, C_{sn}, and I_{th} for S^{2}I-ARCP is similar to that for conventional ARCP, described in detail in [27], [30], and [32]. However, when selecting a proper value for the parameters in S^{2}I-ARCP, the collision rate should also be considered. This leads to the following parameter design.

To ensure complete ZVS in every switching instant over the whole fundamental cycle, two conditions must always be met

$$T_{\text{com,acsc}} \leq T_{\text{dead}}$$
$$T_{\text{com,acsc}} + T_{\text{zvs}} \geq T_{\text{dead}}. \tag{15}$$

The dead-time of the main switches is set to $T_{\text{dead}} = 150\,\text{ns}$, which leads to a maximum permitted commutation time $T_{\text{com,acsc,max}} = 150$ ns according to Fig. 4 and (15). The choice of a relatively low dead-time is possible due to the design with very low gate resistor values, which is particularly advantageous for the S^{2}I-ARCP topology to keep the collision rate low.

The phase currents are sampled at the start of each pulse cycle to obtain the current value of the fundamental. Complete ZVS should also be provided in case of a deviation of the actual current from the regular sampled value due to current ripple and in case of imprecise timing because of finite clock frequencies of the microcontroller. Since mainly the load current ripple I_{ripple} limits the precision of the timing, it is essential to consider it in the

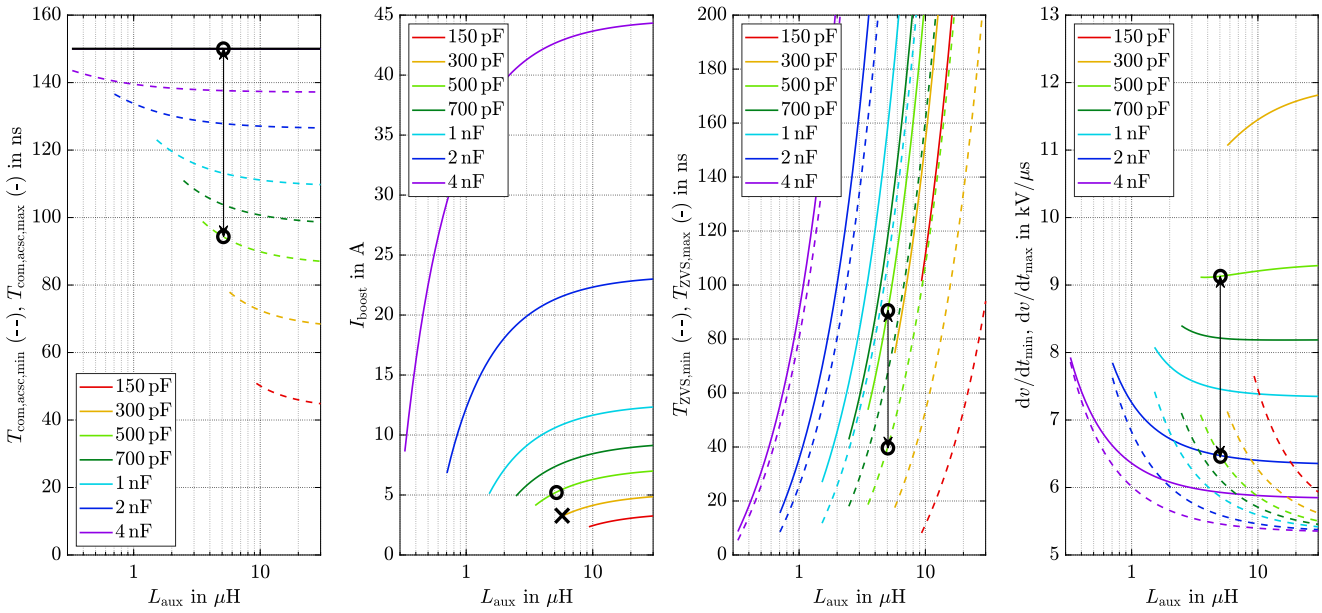


Fig. 12. Design of L_{aux}, C_{sn}, and I_{boost} under the constraint of complete ZVS in all switching instants over the whole fundamental cycle. V_{dc} is assumed to be 800 V, $T_{\mathrm{dead}} = 150\,\mathrm{ns}$, $T_{\mathrm{com,acsc,max}} = T_{\mathrm{dead}}$, and $I_{\mathrm{ripple}} = |\pm 2\,\mathrm{A}|$.

TABLE II
MAIN DESIGN PARAMETERS AND COMPONENTS OF THE PROTOTYPE

	Parameter / Component	Value
ARCP	dc-link voltage V_{dc}	800 V
	dc-link capacitors $C_{\mathrm{dc}+}$ / $C_{\mathrm{dc}-}$	132 μF
	Switching frequency f_{sw}	30 kHz
	Gate driver resistor (turn-ON)	4.7 Ω
	Gate driver resistor (turn-OFF)	0
	Main switches S_{LS}, S_{HS}	G3R30MT12K
	Auxiliary switches $S_{\mathrm{aux,p}}$, $S_{\mathrm{aux,n}}$	IGW25N120H3 IDK10G120C5
	Auxiliary inductor L_{aux}	5.2 μH
	Snubber capacitance C_{sn}	500 pF
	Boost current I_{boost}	5 A
	Current threshold I_{th}	5 A
	Main switch dead-time T_{dead}	150 ns
	Minimum com. duration $T_{\mathrm{com,acsc,min}}$	95 ns
	Maximum com. duration $T_{\mathrm{com,acsc,max}}$	150 ns
	Minimum ZVS tolerance $T_{\mathrm{zvs,min(Ia)}}$	40 ns
	Maximum ZVS tolerance $T_{\mathrm{zvs,max(Ia)}}$	90 ns
	Reactivation lockout-time T_{lock}	100 ns
	Minimum voltage slew-rate in ACSC	6.5 kV/μs
	Maximum voltage slew-rate in ACSC	9.2 kV/μs
μC	Type	XMC 4700
	Clock frequency	144 MHz

design. According to the measurement, I_{ripple} is at most about $|\pm 2\,\mathrm{A}|$. Furthermore, two cases must be distinguished in this context. If the instantaneous load current is lower by I_{ripple}, I_{ripple} adds to the desired I_{boost}, resulting in a minimum commutation duration $T_{\mathrm{com,acsc,min}}$ and maximum tolerance duration $T_{\mathrm{zvs,max}}$. If the instantaneous load current is higher by I_{ripple}, I_{ripple} subtracts from the desired I_{boost}, resulting in a maximum commutation duration $T_{\mathrm{com,acsc,max}}$ and a minimum tolerance duration $T_{\mathrm{zvs,min}}$. The two cases must always satisfy the ZVS conditions specified in (15).

Fig. 12 shows the solution space as a function of L_{aux} and C_{sn}, which fulfills the constraint for complete ZVS.

The procedure is as follows. At first, I_{boost} is calculated so that $T_{\mathrm{com,acsc,max}}$ equals T_{dead} resulting in the key figures $T_{\mathrm{com,acsc,min}}$, $T_{\mathrm{com,acsc,max}}$, I_{boost}, $T_{\mathrm{zvs,min}}$, $T_{\mathrm{zvs,max}}$, $\mathrm{d}v/\mathrm{d}t_{\mathrm{min}}$, and $\mathrm{d}v/\mathrm{d}t_{\mathrm{max}}$. Solutions that do not meet the conditions are hidden in the next step. Finally, a valid design point is selected.

I_{boost} should not be selected too high to limit the conduction losses [30], the maximum short-term component current stress [see (9)], the maximum $\mathrm{d}v/\mathrm{d}t$, and specifically in S^{2}I-ARCP the collision rate [see Fig. 7(c)]. The design of L_{aux} is again a tradeoff. The upper bound is restricted by the collision rate [see Fig. 7(a)] and conduction losses in the auxiliary circuit. The lower bound is limited by the maximum $\mathrm{d}i/\mathrm{d}t$ and its EMI behavior and by the capability of the microcontroller. The `Infineon XMC 4700` is based on the ARM Cortex-M4 processor core, with a clock frequency of 144 MHz ($\approx$7 ns clock cycle). The clock cycle limits the precision of I_{boost}. If the current rises too fast, the timing of the switch turn-OFF at t_2, as shown in Fig. 4, can no longer be maintained accurately enough.

$T_{\mathrm{com,acsc}}$ is significantly influenced by C_{sn}, which in turn is the most important parameter for shaping the voltage edges and influencing the resulting $\mathrm{d}v/\mathrm{d}t$ [34] to attenuate the high-frequency content. But C_{sn} should not be selected too high to keep the collision rate, the peak current and the conduction losses in the auxiliary circuit low. Therefore, C_{sn} is selected as low as possible by using only the output capacitance of the semiconductors and the parasitic structure-related capacitances and avoiding additional discretely connected capacitors. It can be estimated to $C_{\mathrm{sn}} = 300\,\mathrm{pF}$.

Considering the mentioned tradeoffs and constraints, the design marked with an **X** in Fig. 12 was originally selected. The design parameters then were $I_{\text{boost}} = 3.2\,\text{A}$ and $L_{\text{aux}} = 5.7\,\mu\text{H}$. As will be discussed later, the effective C_{sn} in ACSC operation is actually somewhat higher than in the first rough estimate and amounts about 500 pF. L_{aux} was originally realized with $5.2\,\mu\text{H}$ leading to the design marked with the circles **O** in Fig. 12. The resulting key figures are given in Table II.

This leads to a characteristic impedance $Z_{\text{r}} = 72\,\Omega$ and a resonant frequency $f_{\text{r}} = 2.2\,\text{MHz}$ of the resonant circuit. Based on the choice of the design parameters V_{dc}, L_{aux}, C_{sn}, I_{boost}, the maximum load current $I_{\text{load,max}} = \sqrt{2} \cdot 14.4\,\text{A}$, and (4)–(6), the maximum ramp time is $T_{\text{ramp,max}} = 330$ ns, the resonant commutation duration is $T_{\text{com,acsc,max}} = 150$ ns, and the maximum activation time is $T_{\text{act,max}} = 810$ ns. The activation time should be a small fraction of the switching cycle T_{sw}. By selecting the switching frequency to be 30 kHz, the maximum activation time of the auxiliary circuit amounts to 2.4% of T_{sw}. In addition, an auxiliary circuit reactivation lockout-time of 100 ns is introduced for safety precaution to avoid the joint activation of the auxiliary circuit by different phases.

Finally, the maximum permissible commutation time of 100 ns under CSC operation results with (13) in a selected threshold current level $I_{\text{th}} = 5\,\text{A}$. C_{sn} is again assumed to be 300 pF for simplicity. However, it is important to note that the effective C_{sn} under CSC operation differs from ACSC operation.

Six $1200\,\text{V}/50\,\text{A}/30\,\text{m}\Omega$ SiC MOSFETs `GeneSiC G3R30MT12K` constitute the B6-topology with its six main switches. The SiC MOSFETs were selected for their low conduction losses at low load compared with IGBTs. Six $1200\,\text{V}/25\,\text{A}$ IGBTs (without freewheeling diodes) `Infineon IGW25N120H3` with separate antiparallel $1200\,\text{V}/10\,\text{A}$ SiC Schottky diodes `Infineon IDK10G120C5` form the auxiliary switches. The auxiliary switches only have to carry the current for a short period of time and can therefore be rated for a much lower continuous current load than the main switches. However, the selection should consider that the peak current load in the auxiliary switch is higher than in the main switch. The selected SiC Schottky diodes and IGBTs are highly overloadable for a short time. The choice of power semiconductor components used is based on availability and already considers future experiments with power transfers above 10 kW. The IGBTs were chosen because of their low cost and simpler control, since a bidirectional switch based on IGBTs naturally turns OFF at time instant t_6 when i_{aux} changes its polarity. Hence, the exact turn-OFF time of S_{aux} is not relevant. Conventional fast recovery Si diodes resulted in significant forward recovery losses in practical tests and were therefore replaced by SiC Schottky diodes.

V. Experimental Results and Discussion

The previously discussed inverter design is experimentally verified at the operating point given in Table III unless otherwise specified.

The modulation index is chosen to 0.82, which corresponds to a phase rms voltage of 230 V. The three-phase resistive load is connected to the output terminals of the inverter in wye (Y) configuration via a sine-wave filter. According to Fig. 7(b), the choice of a resistive load leads to the highest collision rate and should therefore be examined. The potential of the load-side neutral point is floating. To simultaneously acquire the time signals, a `Keysight MXR058A` oscilloscope with eight channels is used. A series of three-phase experiments are presented and compared in the following.

TABLE III
Experimental Operating Point Parameters

Parameter / Component	Value
Modulation index m_{a}	0.82 ($\hat{=} V_{0,\text{rms}} = 230\,\text{V}$)
Fundamental frequency f_{el}	50 Hz
Load resistance R_{load}	$16\,\Omega$
Phase angle φ_{load}	$\approx 0°$
Load current $I_{\text{load,rms}}$	14.4 A
Output power P_{load}	10 kW

A. Results Over Two Fundamental Cycles

Fig. 13 shows the filtered phase voltages, the collision detection signal, the phase currents, and the auxiliary inductor current over two fundamental cycles using soft-switching.

Series of collisions occur in 60° intervals at the intersection points of two phase voltage curves, which corresponds to the sector transitions of the space vector diagram [see also Fig. 8(a) and the explanations in the previous chapter]. The collisions are correctly detected and eliminated. The avoidance algorithm causes hardly any distortions, which proves its working principle. The phase currents are in phase with the phase voltages and reach a peak value $I_{\text{load,max}} = 20\,\text{A}$. Corresponding to (9), i_{aux} reaches its peak at $I_{\text{load,max}}$ with $I_{\text{aux,max}} = 25.8\,\text{A}$. Similar to the collision detection signal, the envelope of i_{aux} is 60° periodical due to the sharing of the single inductor by the three phases. Therefore, the usual absence of i_{aux} pulses for CSC operation, as shown in [27], can no longer be observed. I_{load} and thus T_{act} of the two phases are maximum in sum at the intersections of the phase currents, which for $\varphi_{\text{load}} = 0°$ coincides with the collision region and therefore confirming the highest collision rate $\mathcal{P}_{\text{rel}}$ observed in Fig. 7(b). Looking into the switching edges for the presented operating point, 2097 out of 3600 edges required ACSC operation. In 600 switching cycles within a fundamental period, about 60 collisions occurred, which all had been fully resolved by the edge shifting algorithm. Therefore, the resulting collision rate is 10%, which coincides well with the theoretical calculation from Section III-A and Fig. 7(a) predicting a collision rate of about 9%.

B. Switching Transition Waveforms

The proposed S^2I-ARCP with its collision avoidance algorithm through edge shifting is verified in the following. For this purpose, the switching transition waveforms and the timing for an ACSC transition [case (Ia)], a CSC transition [case (II)] and,

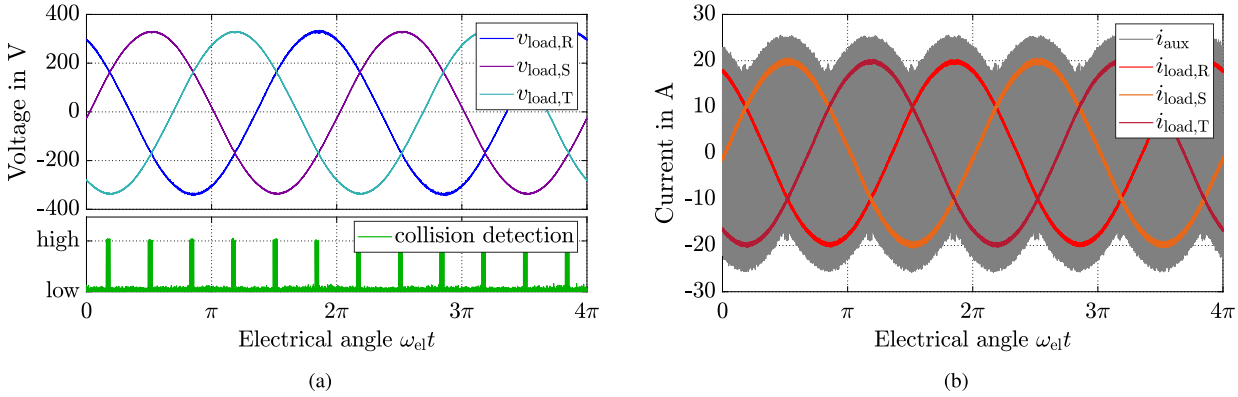


Fig. 13. Load-side experimental results (after the sine-wave filter) over two fundamental cycles using soft-switching. (a) Phase voltages and collision detection signal. (b) Phase currents and auxiliary inductor current.

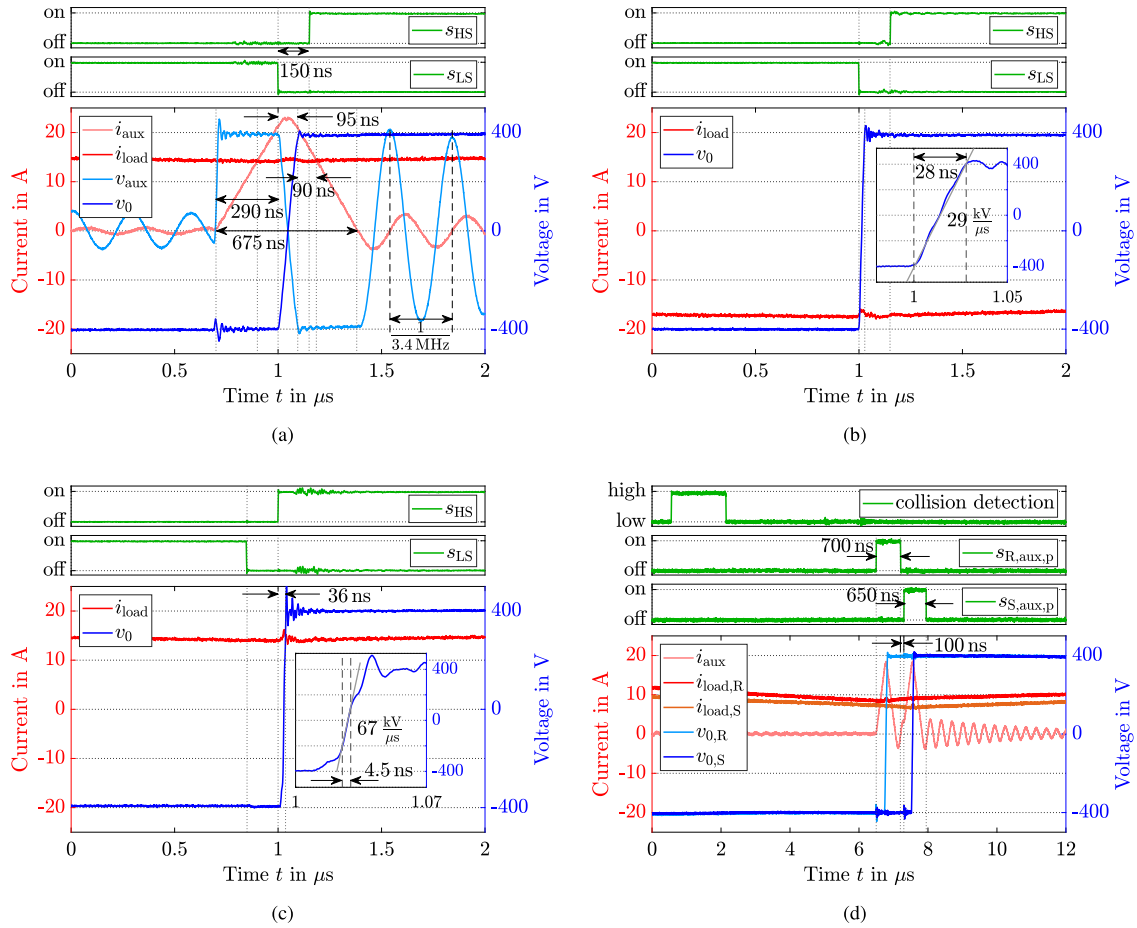


Fig. 14. Switching signals, current and voltage waveforms during rising edge transitions. (a) Rising edge transition under ACSC operation [case (Ia)]. (b) Rising edge transition under CSC operation [case (II)]. (c) Rising edge transition under hard-switching. (d) Collision avoidance under ACSC operation by shifting switching edges. Note that the propagation delay of the logic signals has been removed for clear displaying purposes.

for comparison, a hard-switching transition as well as an ACSC collision case are shown in Fig. 14 .

The operation point under ACSC operation in Fig. 14(a) is $I_{\mathrm{load}} = 15\,\mathrm{A}$, $T_{\mathrm{ramp}} = 290\,\mathrm{ns}$, $T_{\mathrm{com,acsc}} = 95\,\mathrm{ns}$, and $T_{\mathrm{act}} = 675\,\mathrm{ns}$. According to (5), this indicates an effective snubber capacitance of 500 pF under ACSC operation. Furthermore, the resulting maximum $\mathrm{d}v/\mathrm{d}t_{\mathrm{max}}$ is about $9\,\mathrm{kV}/\mu\mathrm{s}$. The occurring parasitic oscillation in the auxiliary circuit is caused by L_{aux} and the output capacitance of the six auxiliary switches with their antiparallel diodes. The frequency is about 3.4 MHz, indicating an effective capacitance of 420 pF in the auxiliary circuit. The excitation of this oscillation after the auxiliary switch turn-OFF

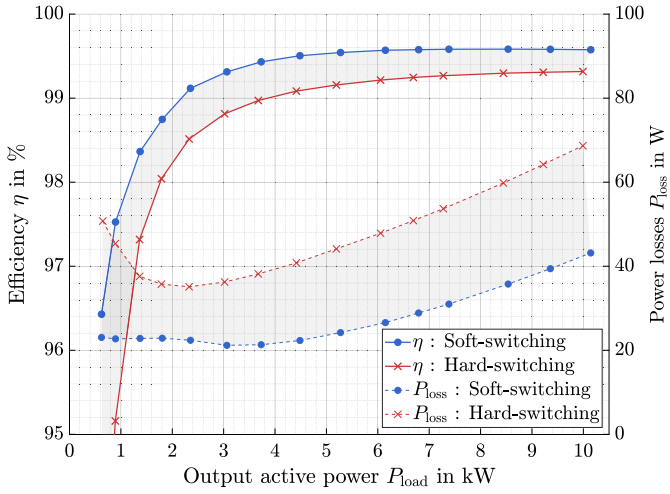


Fig. 15. Measured efficiency results and total power losses under soft-switching and hard-switching as a function of output active power.

is an inherent characteristic of the ARCP principle and occurs to the same extent in S^{2}I-ARCP. If avoiding these oscillations for EMI reasons is desired, damping or saturated inductors [31] could be employed. However, the use of clamping diodes as proposed in [28] is not possible in the S^{2}I-ARCP inverter due to the placement of the resonant inductor. The transition waveforms of CSC operation with $I_{\text{load}} = -16\,\text{A}$ are shown in Fig. 14(b). The voltage ramps up linearly within $T_{\text{com,csc}} = 28\,\text{ns}$, resulting in a constant $\mathrm{d}v/\mathrm{d}t = 29\,\text{kV}/\mu\text{s}$ with a voltage overshoot of about 25 V. According to (13), this indicates an effective snubber capacitance of 280 pF under CSC operation, which is lower than under ACSC operation due to the disabled auxiliary circuit. Hard-switching with $I_{\text{load}} = 15\,\text{A}$ is shown in Fig. 14(c). Here, the auxiliary circuit is disconnected and the HS-switch is turned-ON within 36 ns under full voltage (V_{dc}) causing high switching losses. The $\mathrm{d}v/\mathrm{d}t$ peaks 67 kV/μs, resulting in high EMI emission with the largest voltage overshot of about 100 V.

The concept of shifting the switching edges to avoid collisions under ACSC operation is validated in Fig. 14(d). A collision between phase R and S, as assumed in Fig. 6, is detected by the algorithm. It then calculates the collision-free pulse pattern with the shifted switching edges under the compliance of $T_{\text{lock}} = 100\,\text{ns}$ and outputs the pulse pattern in the immediately following switching cycle. According to Fig. 13, collisions can be observed when two phase currents are approximately $\pm 10\,\text{A}$, which corresponds to the intersections of phase voltages for pure resistive loads. Note that the slightly higher current level of $i_{\text{load,R}}$ results in a slightly longer turn-ON duration of $S_{\text{R,aux}}$.

C. Efficiency and Power Loss Analysis

An efficiency measurement was performed using the precise power meter `Yokogawa WT5000`. The auxiliary circuit was disconnected for the hard-switching test. Power losses occurring in the sine-wave filter are not included in the measurement results. Short-time operation ($<5\,\text{s}$) was used to keep the temperature of the heat sink at room temperature at each measurement point to ensure comparable measurement conditions. Fig. 15 shows the efficiency curves and the power losses for pure resistive loads ($\varphi_{\text{load}} \approx 0°$) against the ac output power under soft-switching and hard-switching.

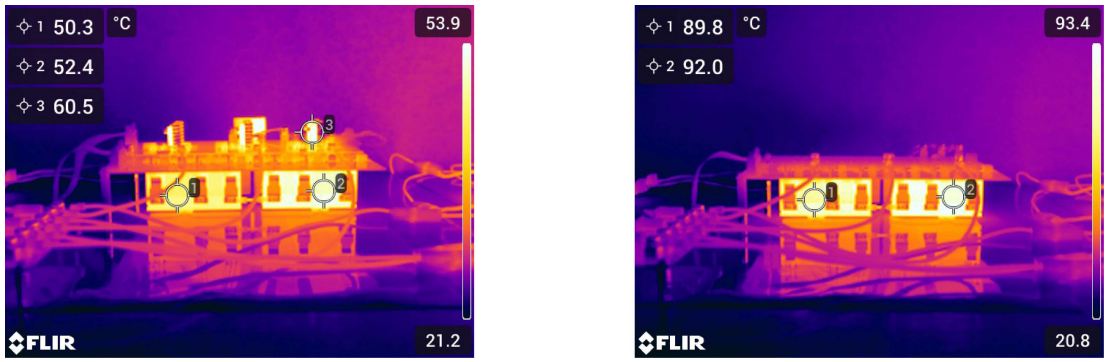
Soft-switching in S^{2}I-ARCP improves the efficiency by about 0.45% at 4 kW and by about 0.25% at 10 kW, which corresponds to a loss reduction of 44% at 4 kW and 38% at 10 kW compared with hard-switching. The efficiency of the inverter peaks at 99.58% in soft-switching operation and decreases very slightly at high loads. At these load conditions, conduction losses begin to dominate over other losses. It can be seen that the improvement in efficiency and the reduction of power losses are even greater at low loads. In addition, an increase in losses can be observed for the hard-switching but not for the soft-switching operation. Depending on the current direction under hard-switching, only one switch of the half-bridge causes losses, while the other turns ON and OFF virtually lossless. At low currents, the turn-ON of the complementary switch is prone to losing the loss-less turn-ON because the capacitively driven voltage transition is too slow. As the switching energy for turn-ON is higher in our setup due to our gate resistor selection, a significant rise in losses could thus be explained at low load. Likewise, this loss increase proves the need for ACSC in case (Ib) in our soft-switching inverter.

Furthermore, a thermographic comparison between soft-switching and hard-switching is performed by using a thermal imaging camera `FLIR T530`. For this purpose, a thermal image was taken under steady-state conditions for both cases. The cooling is provided by natural convection. The results are shown in Fig. 16.

The temperature is measured with two different measurement points at the heat sink of the main switch (1, 2) and at the heat sink of the auxiliary switch (3). With soft-switching, the temperature of the main switch heat sink is about 30 K above room temperature, while for hard-switching it reaches 70 K above room temperature. Thus, minimizing switching losses through soft-switching results in a temperature rise that is less than half that of hard-switching. The temperature at the heat sink of S_{aux} reaches about 40 K above room temperature. However, it should be noted that the heat sink of the auxiliary switches is much smaller than the heat sink of the main switches. Obviously, a part of the saved switching losses is transferred to the losses of the auxiliary circuit. But the power losses are distributed to more electrical components. With the reduction in power losses and with this kind of thermal spreading, soft-switching can enable higher power transfers with the given prototype or allows the choice of a considerably smaller heat sink compared with hard-switching.

D. Discussion

In summary, the presented challenges of implementing an S^{2}I-ARCP and its results can be evaluated as follows. The proposed concept can save two of the three resonant inductors compared with the conventional three-phase ARCP. Hence, the single resonant inductor is better utilized through the joint



(a) (b)

Fig. 16. Thermographic comparison in steady-state operation. (a) Soft-switching. (b) Hard-switching.

use of the three phases, but brings the problem of collisions. When selecting the design parameters, the number of collisions that occur must also be considered. With consideration of the permissible $\mathrm{d}v/\mathrm{d}t_{\mathrm{max}}$, C_{sn} should be kept as low as possible to obtain low collision rates, resulting in rather short commutation durations. The parallel connection of additional large discrete capacitors, such as in [21], [24], [26], and [35], to increase the value of C_{sn}, is therefore undesirable in S^{2}I-ARCP compared with conventional ARCP.

Determination of the appropriate design parameters should be based on the actual value of the snubber capacitors. Since C_{sn} mainly consists of the output capacitances of the semiconductors and different switching configurations are active during ACSC and CSC operation, the effective value of C_{sn} differs. In addition, the total value is not known sufficiently accurate due to additional parasitic structure-related capacitances. Those originate mainly from the printed circuit board layers (for this prototype 130 pF between node A and DC$-$ and 77 pF between an output terminal R, S, T, and DC$-$). However, the value of an effective C_{sn} for both operational modes can be easily determined by measurement and recalculation. They are $C_{\mathrm{sn}} = 500\,\mathrm{pF}$ for ACSC and $C_{\mathrm{sn}} = 280\,\mathrm{pF}$ for CSC, respectively. This allows the control parameters, such as T_{dead}, I_{th}, or I_{boost}, to be tuned to an optimized fixed value. To obtain an initial selection of the design parameters, a rough estimate was made using $C_{\mathrm{sn}} = 300\,\mathrm{pF}$. However, the measurements indicate an actual effective C_{sn} under ACSC operation that is 200 pF higher than originally assumed.

The phase currents are sampled once at the start of each pulse cycle to obtain the fundamental value. The determination of a collision-free pulse pattern, based on sinusoidal modulation, is then performed. The variable ACSC parameters I_{ramp} and hence T_{ramp} are calculated based on the sampled I_{load}. The pulse pattern is forwarded to the output stage in the following pulse cycle. Therefore, the pulse position regarding the output current ripple and the time offset of the current sampling are neglected when calculating the ACSC timing. This leads to a considerable deviation of the sampled current from the actual instantaneous value when the auxiliary circuit is activated. The result is a deviation of the actual I_{boost} from the desired value. The deviation is at most about $\pm 2\,\mathrm{A}$, resulting in different $T_{\mathrm{com,acsc}}$ covering a time range of 95–150 ns and thus leading to different voltage slew-rates of about 6.5–$9.2\,\mathrm{kV}/\mu\mathrm{s}$. Since $T_{\mathrm{com,acsc}}$ does not remain constant over time, the time instant t_4 and t_5 cannot be calculated accurately. However, to ensure complete ZVS over the whole fundamental cycle, a suitable ZVS precision tolerance T_{zvs} and thus I_{boost} were chosen according to the maximum boost current deviation.

Moreover, T_{act} and thus, the time instant t_6 cannot be calculated accurately. For this reason, the S_{aux} turn-OFF is delayed by 80 ns, as shown in Fig. 14(d), to ensure L_{aux} is never turned-OFF at harmful current levels.

VI. Conclusion

In this article, a novel three-phase ARCP inverter with a single shared resonant inductor is presented. The topological reduction can lead to a forbidden simultaneous use of the shared auxiliary inductor by the three phases, and thus to collisions when accessing the auxiliary circuit. A collision avoidance algorithm with shifting the switching edges is presented to avoid simultaneous use of the auxiliary circuit by different phases. The dependence of the collision rate on different operating parameters has been analyzed in detail. To verify the functionality of the proposed approach, a three-phase 800 V 10 kW S^{2}I-ARCP inverter with the suggested collision avoidance algorithm has been implemented and put into operation. The results of the measurements have confirmed the proposed concept and the analytical theory. Efficiency measurement results indicated a significant loss reduction in soft-switching operation by more than 38% compared with hard-switching, with a peak efficiency value of 99.58%. Overall, the S^{2}I-ARCP inverter offers a better alternative to the conventional ARCP soft-switching topology due to its reduced passive component count and the better utilization of the shared resonant inductor without compromising the output voltage quality. The savings in volume (in the case of air coils), weight, and cost (in the case of magnetic cores) outweigh the more complex control. Due to its advantageous characteristics and controllable $\mathrm{d}v/\mathrm{d}t$, the S^{2}I-ARCP is well suited for applications, such as grid inverters for renewable energy or inverters in traction drives for electric vehicles.

Future work may include other collision avoidance methods, such as a modified edge-shifting algorithm using simultaneous commutation of suitable phases or occasional hard-switching. In addition, studies will be conducted on the system's EMI behavior and its efficiency regarding different semiconductor combinations.

REFERENCES

[1] M. D. Bellar, T. S. Wu, A. Tchamdjou, J. Mahdavi, and M. Ehsani, "A review of soft-switched DC-AC converters," *IEEE Trans. Ind. Appl.*, vol. 34, no. 4, pp. 847–860, Jul./Aug. 1998.

[2] S. A. Q. Mohammed and J.-W. Jung, "A State-of-the-Art review on soft-switching techniques for DC–DC, DC–AC, AC–DC, and AC–AC power converters," *IEEE Trans. Ind. Informat.*, vol. 17, no. 10, pp. 6569–6582, Oct. 2021.

[3] R. W. de Doncker and J. P. Lyons, "The auxiliary resonant commutated pole converter," in *Proc. IEEE Int. Conf. Ind. Appl. Soc.*, 1990, pp. 1228–1235.

[4] R. W. de Doncker and J. P. Lyons, "The auxiliary quasi-resonant DC link inverter," in *Proc. IEEE Power Electron. Spec. Conf.*, 1991, pp. 248–253.

[5] Y. Jung, H. L. Liu, G. C. Cho, and G. H. Cho, "Soft switching space vector PWM inverter using a new quasi-parallel resonant DC link," *IEEE Trans. Power Electron.*, vol. 11, no. 3, pp. 503–511, May 1996.

[6] D. M. Divan and G. Skibinski, "Zero-switching-loss inverters for high-power applications," *IEEE Trans. Ind. Appl.*, vol. 25, no. 4, pp. 634–643, Jul./Aug. 1989.

[7] J.-Y. Choi, M. A. Herwald, D. Boroyevich, and F. C. Lee, "Effect of switching frequency of soft switched inverter on electric vehicle system," in *Proc. IEEE Power Electron. Transp.*, 1998, pp. 63–69.

[8] J.-S. Lai, "Fundamentals of a new family of auxiliary resonant snubber inverters," in *Proc. IEEE Int. Conf. Ind. Electron. Control Instrum.*, 1997, pp. 645–650.

[9] P. Korta, L. V. Iyer, and N. C. Kar, "Soft–switching EV traction inverter exploiting full potential of wide bandgap devices," in *Proc. IEEE Ind. Electron. Soc. Conf.*, 2020, pp. 4703–4708.

[10] H.-J. Pfisterer and H. Spath, "Switching behaviour of an auxiliary resonant commutated pole (ARCP) converter," in *Proc. IEEE Int. Power Electron. Congr. Tech.*, 2000, pp. 359–364.

[11] W. Dong et al., "Comparative experimental evaluation of soft-switching inverter techniques for electric vehicle drive applications," in *Proc. IEEE Ind. Appl. Soc.*, 2001, pp. 1469–1476.

[12] N. Iwamuro and T. Laska, "IGBT history, state-of-the-art, and future prospects," *IEEE Trans. Electron Devices*, vol. 64, no. 3, pp. 741–752, Mar. 2017.

[13] S. Bagawade, M. Pahlevani, and P. Jain, "Novel soft-switched three-phase inverter with output current ripple cancellation," *IEEE Trans. Ind. Electron.*, vol. 38, no. 1, pp. 1232–1248, Jan. 2023.

[14] Y. P. Li, F. C. Lee, and D. Boroyevich, "A simplified three-phase zero-current-transition inverter with three auxiliary switches," *IEEE Trans. Power Electron.*, vol. 18, no. 3, pp. 802–813, May 2003.

[15] K. Sayed, A. Almutairi, N. Albagami, O. Alrumayh, A. G. Abo-Khalil, and H. Saleeb, "A review of DC-AC converters for electric vehicle applications," *Energies*, vol. 15, no. 3, Feb. 2022, Art. no. 1241.

[16] M. Yoshida, M. Yamamoto, E. Hiraki, S. Chandhaket, and M. Nakaoka, "Active resonant leg-link snubber-assisted three phase soft commutation PFC converter and its practical evaluations," in *Proc. IEEE Int. Conf. Ind. Electron. Control Instrum.*, 2000, pp. 2660–2665.

[17] W. Dong et al., "Efficiency considerations of load side soft-switching inverters for electric vehicle applications," in *Proc. IEEE Appl. Power Electron. Conf.*, 2000, pp. 1049–1055.

[18] J. Voss, J. Warmuz, D. Mathai, and R. W. de Doncker, "Adapted auxiliary-resonant commutated pole in the dual-active bridge," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 7, no. 4, pp. 2553–2560, Dec. 2019.

[19] W. Zhou, X. Yuan, and I. Laird, "Performance comparison of the auxiliary resonant commutated pole inverter (ARCPI) using SiC MOSFETs or Si IGBTs," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2019, pp. 1981–1987.

[20] A. Charalambous, X. Yuan, N. McNeill, Q. Yan, N. Oswald, and P. Mellor, "EMI reduction with a soft-switched auxiliary commutated pole inverter," in *Proc. Energy Convers. Congr. Expo.*, 2015, pp. 2650–2657.

[21] X. Yuan, G. Orglmeister, and I. Barbi, "ARCPI resonant snubber for the neutral-point-clamped inverter," *IEEE Trans. Ind. Appl.*, vol. 36, no. 2, pp. 586–595, Mar./Apr. 2000.

[22] A. Charalambous and X. Yuan, "A soft-switched three-level T-type inverter with auxiliary commutated poles," in *Proc. Int. Power Electron. Conf.*, 2018, pp. 1634–1641.

[23] W. Gong, S. Pan, W. Lin, J. Gong, and Y. Shang, "A novel auxiliary resonant commutated pole soft-switching inverter," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2021, pp. 2166–2170.

[24] K. Ma, D. Xu, T. Zhang, and S. Igarashi, "The evaluation of control strategies for auxiliary resonant commutated pole inverter," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2009, pp. 810–816.

[25] A. Amler and Y. Zhou, "Verfahren zum Ansteuern und Schaltanordnung für einen mehrphasigen Zweipunkt-Wechselrichter," *Germany Pat. DE102022207036 (pending pat. appl.)*, 2022.

[26] W. Zhou and X. Yuan, "Experimental evaluation of SiC MOSFETs in comparison to Si IGBTs in a soft-switching converter," *IEEE Trans. Ind. Appl.*, vol. 56, no. 5, pp. 5108–5118, Sep./Oct. 2020.

[27] A. Charalambous, X. Yuan, and N. McNeill, "High-frequency EMI attenuation at source with the auxiliary commutated pole inverter," *IEEE Trans. Power Electron.*, vol. 33, no. 7, pp. 5660–5676, Jul. 2018.

[28] W. Zhou, X. Yuan, and I. Laird, "Elimination of overshoot and oscillation in the auxiliary branch of a SiC auxiliary resonant commutated pole inverter (ARCPI)," in *Proc. Int. Conf. Power Electron.*, 2019, pp. 383–389.

[29] W. Zhou, M. Diab, X. Yuan, and C. Wei, "Mitigation of motor overvoltage in SiC-based drives using soft-switching voltage slew-rate (dv/dt) profiling," *IEEE Trans. Ind. Electron.*, vol. 37, no. 8, pp. 9612–9628, Aug. 2022.

[30] R. Teichmann, "Control parameter selection in auxiliary resonant commutated pole converters," in *Proc. IEEE Ind. Electron. Soc. Conf.*, 2001, pp. 862–869.

[31] M. Zocher, N. Grass, and R. Kennel, "Minimizing voltage stress in auxiliary resonant commutated pole inverters using saturable inductors," in *Proc. Eur. Conf. Power Electron. Appl.*, 2022, pp. 1–9.

[32] E. Chu, X. Zhang, and L. Huang, "Research on a novel modulation strategy for double auxiliary resonant commutated pole soft-switching inverter with the shunt dead time," *IEEE Trans. Power Electron.*, vol. 31, no. 10, pp. 6855–6869, Oct. 2016.

[33] D. Ma, P. Wang, R. Wang, S. Li, and Q. Sun, "Hybrid SVPWM modulation strategy for auxiliary resonant commutated pole inverter," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 9, no. 4, pp. 4750–4761, Aug. 2021.

[34] T. Bruckner and S. Bernet, "Investigation of a high-power three-level quasi-resonant DC-link voltage-source inverter," *IEEE Trans. Ind. Appl.*, vol. 37, no. 2, pp. 619–627, Mar./Apr. 2001.

[35] M. Luh and T. Blank, "Auxiliary resonant commutated pole inverter (ARCPI) with SiC MOSFETs for efficient vehicle-to-grid (V2G) charging," in *Proc. Eur. Conf. Power Electron. Appl.*, 2021, pp. 1–10.

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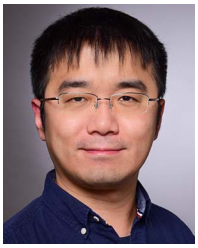

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