Fast-Processing Capacitor Voltage Balancing Algorithm for Single-End Five-Level NPC Converters Based on Redundant Level Modulation

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***Abstract*—Five-level neutral point clamped (5L-NPC) topologies have been proposed for the medium-voltage grid and drive applications since the 1990s. However, their practical implementation has been hindered due to the inherent capacitor voltage drift issue, especially in a single-end configuration. This work proposes a fast-processing, carrier-based voltage balancing algorithm to address this issue, which is based on the latest redundant level modulation (RLM) concept. The proposed approach is fully based on closed-form expressions and basic logic operations, which can be straightforwardly programmed in microcontrollers, as enabled by a fully transparent mathematical model. In contrast, the existing methods treat it as a black box problem, which requires mandatory PI/PID controllers that complicate the implementation. This method shows effective and superior voltage balancing performance against existing methods without affecting the converter output capacity throughout all operating conditions. The fundamental principles and analysis of the capacitor operation are presented to enable a better understanding of the problem and its solution. This work also evaluates the increased switching actions as a side effect of the RLM operation, which is the mandatory cost for all known modulation-based voltage balancing approaches for 5L-NPC converters. For comparison across different systems, a new normalization term is proposed to quantify the capacitor voltage ripples for evaluation with the switching frequency factored in.**

***Index Terms*—Five-level, grid modernization, multilevel converter, neutral point clamped (NPC), voltage balancing.**

I. Introduction

MULTILEVEL converters have been actively researched in past decades as the solution for medium/high-voltage conversion systems for grid applications. Given the limited rating of power semiconductors, voltage source converters need to be constructed in multilevel topologies to enable the handling of a medium/high voltage. The family of multilevel topologies traces back to 1979 when the three-level neutral point clamped (NPC) topology was first brought up in [1]. To cope with a higher voltage at upstream sections of the power grid, a higher number of voltage levels is required. As possible solutions, modular multilevel converters and cascaded H-bridges [2], [3] can be stacked to achieve a higher voltage handling capability, while their power density tends to be low due to the single-phase, bulky capacitors and a higher count of devices. Alternatively, NPC topologies with higher voltage levels have been explored as derivations of three-level NPCs, such as the four-level π-type [4], [5] and four-level active NPC (ANPC) converters [6], because they benefit from the common dc-link capacitor configuration and lower count of both active and passive devices offering better power densities.

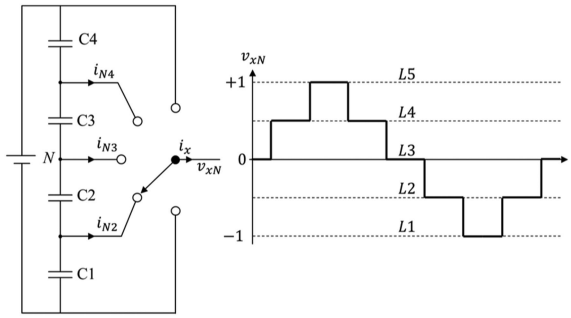

Fig. 1. Five-level NPC converter.

Five-level NPC (5L-NPC) converters can be utilized in medium-voltage applications (e.g., 4, 6.6, or 10 kV), such as motor drive [7], [8], [9] or grid-connected converters for MVDC [10] and STATCOM [11], [12] systems. Various 5L-NPC topologies have been proposed, such as the diode-clamped [7], [8], [13] and E-type [14] configurations. Fig. 1 illustrates a generic 5L-NPC structure that outputs five voltage levels from one phase leg. However, as reported in [10], [15], and [16], the voltage drifting is an inherent issue for 5L-NPC topologies, especially in a single-end configuration with a passive front end, which has been hindering their applications. To function as intended, the four capacitor voltages need to maintain at a quarter of the dc link, while they completely drift away under regular sinusoidal pulsewidth modulation (SPWM). There are several approaches to address this issue. The first category is to install auxiliary

Manuscript received 8 April 2023; revised 30 June 2023 and 10 September 2023; accepted 16 October 2023. Date of publication 31 October 2023; date of current version 6 December 2023. This work was supported in part by the U.K. EPSRC National Center for Power Electronics under Grant EP/R004137/1, and in part by the U.K. Royal Academy of Engineering and the University of Bristol under the Engineering Faculty Postdoctoral Research Prize. *(Corresponding author: Xibo Yuan.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2023.3328980.

Digital Object Identifier 10.1109/TPEL.2023.3328980

voltage balancers [7], [8], [13], [14] to regulate the capacitor voltages. However, this approach suffers from the additional hardware and power devices, which contradicts the reliability, efficiency, and power density targets.

The second category is modulation-based voltage balancing approaches without introducing additional circuits. There are a few common degrees of freedom to realize modulation-based voltage balancing. The first option is the redundant switching state, which is commonly effective in ANPC topologies, such as [17]. However, there is no such redundancy in a 5L-NPC converter. The second option is the zero-sequence signal injection (ZSI) [18], [19], which is equivalent to the nearest three vector [20], [21], [22] approach in space-vector modulation (SVM), utilizing the redundancy in between phase voltages that cancels out in the line voltages. The ZSI approach is widely used in three-level converters [18], [19], while it is reported to significantly lose its effectiveness in a single-end 5L-NPC converter under a high power factor $cos\ \varphi$ and a high modulation index M, as demonstrated in [12] and [23]. As a solution to ease the problem, the active-front-end (back-to-back) configuration is applied to extend the operating range of a 5L-NPC converter [9], [10], [15], [24], [25], [26]. However, this approach still cannot reach the full operating range (e.g., $M > 0.94$ and $cos\ \varphi = 1$) [26] and it limits the application of 5L-NPC converters in the systems with a passive front end.

As an additional degree of freedom in modulation emerged over the past decade, utilization of redundant voltage levels has been applied in the literature for three-level NPC [27], [28], [29], four-level NPC [30], [31], [32], [33], [34], 5L-NPC [35], [36], five-level flying capacitor topologies [37], [38], and general frameworks for n-level converters [39], [40], [41], [42]. Although under different names, such as virtual space vector [34] or carrier-overlapped [41] or redundant level modulation (RLM) [33], these methods all equivalently introduce additional voltage level(s) in one switching window to aid the voltage balancing. Specifically, for 5L-NPC converters, the approaches in [35] and [36] can solve the voltage balancing problem in a 5L-NPC, but they are challenging to reproduce since they are subject to complicated implementation (i.e., special carriers or space vectors). More importantly, these approaches [35], [36], [39] all require mandatory PI/PID controllers/compensators that are not transparent to replicate, which is due to their lack of complete analytical models to determine the voltage regulation efforts.

As a contribution, this article proposes a fast-processing algorithm to solve the fundamental voltage balancing issue in 5L-NPC topologies to enable their practical implementation. This work utilizes and extends a timely concept, RLM proposed in the authors' previous work [32], [33], [43] for four-level NPC converters. In the context of a 5L-NPC, this work presents a complete analysis explaining the necessity of applying RLM and a transparent mathematical model of the solution leading to an optimized utilization of the redundant level thanks to the fully identified boundary conditions of duty ratios, which does not exist in the literature. As a result, the proposed approach is easy to implement with regular level-shifted carriers and outperforms other alternatives, which offer the following features.

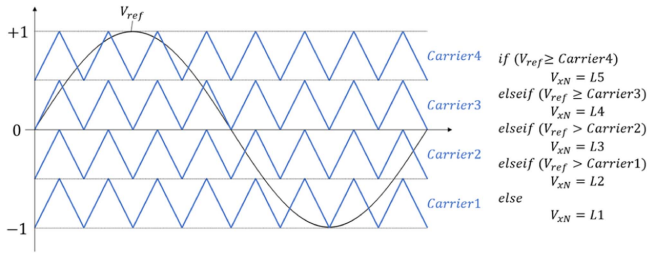

Fig. 2. Operation principle of a 5L-NPC converter.

- Fast-processing and reduced computation load. This approach only involves closed-form expressions and logical operations. No mandatory PI/PID controllers or storage of historical signals are required.
- Simplified prototyping process of the controller with reduced parameter tuning
- Closed-loop, precise, and seamless capacitor voltage control on a switching cycle basis. The compensation strength is translated from real-time measured voltage unbalance and load current cycle-by-cycle, which avoids over/under-compensation.
- Mathematically expressed boundary conditions to maximize the dynamic performance without violating the modulation rules.
- Addressed level-skipping problem by appropriately limiting the boundary conditions of duty ratios
- Effective over the full operation range of modulation index ($M = 0$–1.15), power factor ($\cos\varphi = 0$–1), low fundamental frequency, and low switching frequency

II. Operation and Unbalance of Capacitors in a 5L-NPC

A. Operation Principle of a 5L-NPC

The operation principle of a 5L-NPC is illustrated in Fig. 2 with PWM through level-shifted carriers. As the dc-link voltage is split to four quarters by the four capacitors in series (*C1–C4*), the converter phase leg outputs five voltage levels (*L1–L5*) to synthesize the fundamental-frequency component commanded by the sinusoidal reference voltage V_{ref}.

B. Neutral Point Currents and Capacitor Voltage Variation

As the 5L-NPC converter outputs currents, it draws neutral point (NP) currents (i_{N4}, i_{N3}, i_{N2}) from the dc-link NPs. For example, when one phase leg output v_{xN} is tapped onto *L4*, the load current of this phase i_{x} is drawn from the corresponding NP contributing to i_{N4}. The NP currents lead to the charge or discharge of the dc-link capacitors, causing their voltages to vary during the converter operation. The deviations (ΔV_{Cn}, $n = 1, 2, 3, 4$) of the capacitor voltages are defined as follows:

$$\Delta V_{C4} = V_{C4-ref} - V_{C4}$$
$$\Delta V_{C3} = V_{C3-ref} - V_{C3}$$

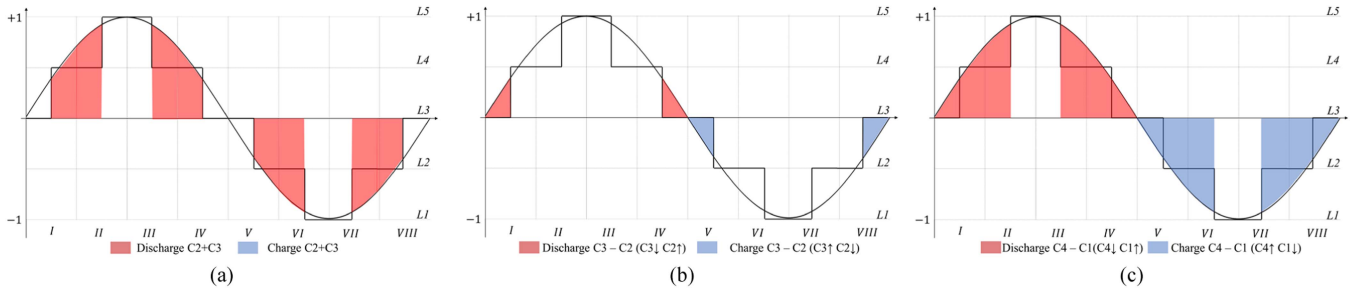

Fig. 3. Capacitor operation diagrams (CODs) of 5L-NPC under unity power factor corresponding to control objectives. (a) C2+C3. (b) C2-C3. (c) C4-C1.

$$\Delta V_{C2} = V_{C2-ref} - V_{C2}$$
$$\Delta V_{C1} = V_{C1-ref} - V_{C1} \quad (1)$$

where $\Delta V_{\mathrm{Cn\text{-}ref}}$ is the reference capacitor voltage, which normally equals a quarter of the dc-link voltage V_{dc}. In one switching cycle T_{sw}, the effect of NP currents on the capacitor voltages can be derived into three sets as follows.

- $\Delta V_{\mathrm{C3+C2}}$, sum of inner capacitors C2 and C3.
- $\Delta V_{\mathrm{C2-C3}}$, difference between inner capacitors C2 and C3.
- $\Delta V_{\mathrm{C1-C4}}$, difference between outer capacitors C1 and C4.

$$\Delta V_{C2+C3} = \Delta V_{C2} + \Delta V_{C3} = (I_{N4} - I_{N2}) \cdot T_{sw}/\mathrm{C} \quad (2a)$$
$$\Delta V_{C2-C3} = \Delta V_{C2} - \Delta V_{C3} = I_{N3} \cdot T_{sw}/\mathrm{C} \quad (2b)$$
$$\Delta V_{C1-C4} = \Delta V_{C1} - \Delta V_{C4} = (I_{N4} + I_{N3} + I_{N2}) \cdot T_{sw}/\mathrm{C}. \quad (2c)$$

The NP currents are the sum of all phase legs, with their average value within one switching cycle expressed as follows:

$$I_{N4} = \sum i_x (D_{4x}); I_{N3} = \sum i_x (D_{3x}); I_{N2} = \sum i_x (D_{2x}) \quad (3)$$

where D_{nx} is the original duty ratio of *level n* (n = 1, 2, 3, 4, 5) of phase x ($x = a, b, c$ in a three-phase system). The above-mentioned expressions represent the capacitor voltage variation as a function of the load current.

C. Capacitor Operation and Voltage Balancing Problem

To understand the operation of capacitors in a 5L-NPC, this work proposes to analyze it through capacitor operation diagrams (CODs) as illustrated in Fig. 3. When the power factor is unity, the most problematic issue is $\Delta V_{\mathrm{C3+C2}}$, because it witnesses the discharge (red) area throughout a fundamental cycle without any charge (blue) area. Without any control scheme or auxiliary circuits, $V_{\mathrm{C3+C2}}$ will collapse to zero. In contrast, the CODs show that the dc-link capacitors are self-balanced regarding $V_{\mathrm{C3-C2}}$ and $V_{\mathrm{C4-C1}}$ over fundamental cycles. The charge and discharge of $V_{\mathrm{C3\text{-}C2}}$ only occur when the third level (*L3*) is utilized. These observations can inform the priority of control objectives to balance these capacitors. When an unbalance is present, there are three control objectives (*OA*, *OB*, and *OC*) to regulate the capacitor voltages by pulling back their deviation

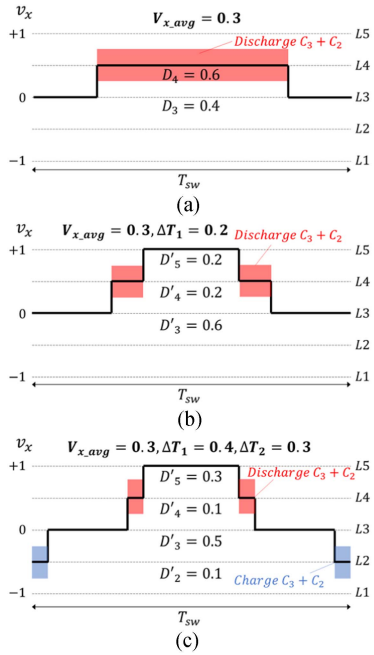

Fig. 4. Examples of output voltage patterns with an equal average voltage $V_{\mathrm{x\_avg}} = 0.3$ ($I_{\mathrm{x}} > 0$) within one switching cycle. (a) Regular modulation. (b) RLM-3. (c) RLM-4.

within one switching cycle as follows:

$$OA = -\Delta V_{C2+C3} \cdot C \cdot f_{sw} = \sum i_x (D_{4x} - D_{2x}) \quad (4)$$
$$OB = -\Delta V_{C2-C3} \cdot C \cdot f_{sw} = \sum i_x (D_{3x}) \quad (5)$$
$$OC = -\Delta V_{C1-C4} \cdot C \cdot f_{sw} = \sum i_x (D_{4x} + \mathrm{D}_{3x} + D_{2x}) \quad (6)$$

where the minus sign indicates the compensation of unbalance. *OA* is the top priority according to the analysis in this section.

III. RLM IN 5L-NPC

To solve the challenging voltage balance problem in 5L-NPC topologies, an extra degree of freedom needs to be utilized, which is referred to as the RLM. Without violating the average output voltage in one carrier cycle, RLM introduces additional voltage levels to enable extra control on capacitor voltages. Fig. 4 illustrates examples of converter output voltage patterns in one switching cycle with the equal average voltage (volt-second

TABLE I
COMPUTATION OF DUTY RATIOS AND CONSTRAINTS

	$0.5 \le V_{ref} \le 1$	$0 \le V_{ref} < 0.5$	$-0.5 \le V_{ref} < 0$	$-1 \le V_{ref} < -0.5$
Original duty ratios	$D_5 = \lvert V_{ref}\rvert \cdot 2 - 1$ $D_4 = (1 - \lvert V_{ref}\rvert) \cdot 2$	$D_4 = \lvert V_{ref}\rvert \cdot 2$ $D_3 = (1 - \lvert V_{ref}\rvert) \cdot 2$	$D_3 = (1 - \lvert V_{ref}\rvert) \cdot 2$ $D_2 = \lvert V_{ref}\rvert \cdot 2$	$D_2 = (1 - \lvert V_{ref}\rvert) \cdot 2$ $D_1 = \lvert V_{ref}\rvert \cdot 2 - 1$
Modified duty ratios	$D'_5 = D_5 + \Delta T_1$ $D'_4 = D_4 - 2\Delta T_1 + \Delta T_2$ $D'_3 = \Delta T_1 - 2\Delta T_2$ $D'_2 = \Delta T_2$	$D'_5 = \Delta T_1$ $D'_4 = D_4 - 2\Delta T_1 + \Delta T_2$ $D'_3 = D_3 + \Delta T_1 - 2\Delta T_2$ $D'_2 = \Delta T_2$	$D'_4 = \Delta T_2$ $D'_3 = D_3 + \Delta T_1 - 2\Delta T_2$ $D'_2 = D_2 - 2\Delta T_1 + \Delta T_2$ $D'_1 = \Delta T_1$	$D'_4 = \Delta T_2$ $D'_3 = D_3 + \Delta T_1 - 2\Delta T_2$ $D'_2 = D_4 - 2\Delta T_1 + \Delta T_2$ $D'_1 = \Delta T_1$
Constraints	$\Delta T_1 > 0$ $\Delta T_2 > 0$ $D_4 - 2\Delta T_1 + \Delta T_2 > 0$ $\Delta T_1 - 2\Delta T_2 > 0$	$\Delta T_1 > 0$ $\Delta T_2 > 0$ $D_4 - 2\Delta T_1 + \Delta T_2 > 0$ $D_3 + \Delta T_1 - 2\Delta T_2 > 0$	$\Delta T_1 > 0$ $\Delta T_2 > 0$ $D_2 - 2\Delta T_1 + \Delta T_2 > 0$ $D_3 + \Delta T_1 - 2\Delta T_2 > 0$	$\Delta T_1 > 0$ $\Delta T_2 > 0$ $D_2 - 2\Delta T_1 + \Delta T_2 > 0$ $\Delta T_1 - 2\Delta T_2 > 0$

product) $V_{\mathrm{x\_avg}}$ established. The additional voltage levels are not required for synthesizing the fundamental-frequency component, hence they are "redundant," while they can offer extra controllability over capacitor voltages for balancing purposes. RLM is introduced in a three-level NPC inverter [29] or a four-level NPC inverter [33] to introduce one extra voltage level when needed to achieve voltage balancing control in these topologies. This operation results in three voltage levels appearing in one switching cycle, as illustrated in Fig. 4(b), instead of two voltage levels in regular modulation [Fig. 4(a)], which is named *RLM-3* in this work. However, in the case of a 5L-NPC converter, *RLM-3* can only reduce the discharge period (i.e., the red area in Fig. 4), while it cannot introduce any charging period. As analyzed in Fig. 3(a), under a unity power factor, this still leads to the complete discharge/voltage drift of C3+C2.

Therefore, in the 5L-NPC case, it is necessary to introduce another additional level, i.e., the fourth level, to enable a bidirectional control by gaining a charge period (i.e., the blue area) in one switching cycle. Therefore, this operation is named *RLM-4*. This special modulation only alters the output voltage pattern on a switching cycle basis and subsequently alters the high-frequency output behavior of the converter without affecting the fundamental-frequency output. The downside of it is the additional switching actions, which lead to increased switching loss and high-frequency harmonics, as reported in [29] and [33]. This is a mandatory running cost for balancing the capacitor voltages in the 5L-NPC, given the above-mentioned theoretical analysis.

Note in this case the average voltage in one carrier cycle is still maintained the same, e.g., 0.3 p.u., throughout the three cases illustrated in Fig. 4. This rule is guaranteed by introducing two offset values ΔT_1 and ΔT_2 to the duty ratios in the manner of (7)–(10), considering V_{ref} is between 0 and 0.5 as an example.

$$D'_5 = \Delta T_1 \tag{7}$$

$$D'_4 = D_4 - 2\Delta T_1 + \Delta T_2 \tag{8}$$

$$D'_3 = D_3 + \Delta T_1 - 2\Delta T_2 \tag{9}$$

$$D'_2 = \Delta T_2 \tag{10}$$

where D_{n} is the original duty ratio of *level n* (n = 1, 2, 3, 4, 5); and D'_{n} is the altered duty ratio. This alteration also ensures that all duty ratios add up to unity. As the fundamental constraint, all the altered duty ratios should be greater or equal to zero to avoid modulation errors. For example, when V_{ref} is between 0 and 0.5, these constraints are

$$\begin{aligned} \Delta T_1 &> 0 \\ \Delta T_2 &> 0 \\ D_4 - 2\Delta T_1 + \Delta T_2 &> 0 \\ D_3 + \Delta T_1 - 2\Delta T_2 &> 0. \end{aligned} \tag{11}$$

The computation of duty ratios under different V_{ref} is summarized in Table I along with the constraints. The optimal offset values ΔT_1 and ΔT_2 are found in the control algorithms below as it becomes a 2-D problem.

A. Regulate C3 and C2 (Middle Capacitors) Through RLM

As analyzed in Section II, the top control priority is Objective A to regulate the voltage sum of C_3 and C_2. For an individual phase leg in a three-phase converter, this control objective can be considered as one-third of the total target for simplicity. Since the *RLM-4* operation also alters the duty ratio of the middle-level $D_{3\mathrm{x}}$, the desired value of $D_{3\mathrm{x}}$ can be found in Objective B, which concerns the neutral current I_{N3}. Note this manipulation of duty ratio is for each phase independently, which means the process is individually repeated in each phase.

$$OA/(3 \cdot i_x) = (D'_{4x} - D'_{2x}) = D_4 - 2\Delta T_1 \tag{12}$$

$$OB/(3 \cdot i_x) = D'_{3x} = D_3 + \Delta T_1 - 2\Delta T_2. \tag{13}$$

With two unknowns, the above-mentioned two equations can be solved to yield the closed-form solutions for ΔT_1 and ΔT_2 as follows:

$$\Delta T_{1-ref} = 0.5D_{4x} - OA/(6 \cdot i_x) \tag{14}$$

$$\Delta T_{2-ref} = -0.5D_{4x} + 0.5D_{3x} + OA/(12 \cdot i_x) - OB/(6 \cdot i_x). \tag{15}$$

Note this method factors in both the polarity and amplitude of the load current i_{x} and the measured voltage unbalance, so it simplifies the algorithm by avoiding looking up a table that is indexed by the polarity of the load current and the capacitor voltage deviation as applied in [36]. Moreover, the compensation level is quantitatively worked out from the load current level and the control objectives through the models, in contrast to a

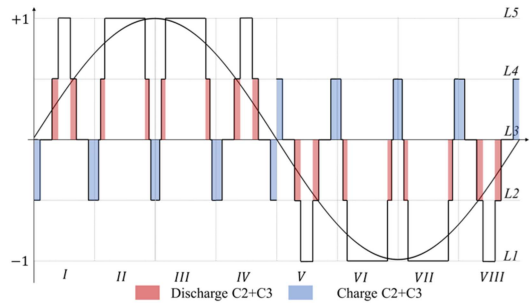

Fig. 5. COD with RLM concerning *OA*.

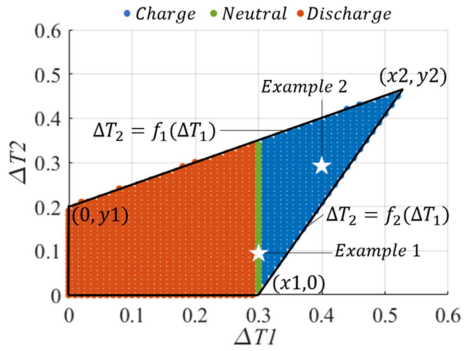

Fig. 6. Pool of possible (ΔT_1, ΔT_2) concerning V_{C3+C2} ($V_{\text{ref}} = 0.3$, $I_{\text{x}} > 0$).

fixed compensation strength (e.g., a fixed dwell time in [36]). This means the proposed method achieves precise control of the control objectives that do not over/under-compensate the imbalance of capacitor voltages. As an illustration, the COD becomes Fig. 5 when equal charge and discharge of C2+C3 is achieved by RLM in each switching cycle.

B. Boundary Conditions of ΔT_1 and ΔT_2 in RLM

The retrieved reference values $\Delta T_{1\text{-ref}}$ and $\Delta T_{2\text{-ref}}$ can be unrealistic because they attempt to pull back the voltage unbalance within one carrier cycle, which may cause modulation errors. Therefore, $\Delta T_{1\text{-ref}}$ and $\Delta T_{2\text{-ref}}$ need to be limited to comply with the constraints listed in Table I. Without violating the constraints in (11), the achievable combinations of ΔT_1 and ΔT_2 values are a 2-D pool, which can be illustrated as an area in Fig. 6.

As can be solved from (11), the coordinates can be expressed as follows:

$$\begin{aligned} y_1 &= \frac{D_3}{2} \\ x_1 &= \frac{D_4}{2} \\ x_2 &= \frac{2D_4 + D_3}{3} \\ y_2 &= \frac{D_4 + 2D_3}{3} . \end{aligned} \tag{16}$$

Hence, the boundary conditions of ΔT_1 and ΔT_2 can be mathematically expressed in each switching cycle, e.g., by f_1 and f_2 in Fig. 6. Note that Objective A only concerns ΔT_1 as expressed in (12), which needs to be prioritized. Therefore, ΔT_1 should be selected before proceeding to find ΔT_2. For example, if $\Delta V_{\text{C3+C2}}$ needs to be charged, a ΔT_1 is selected first in the blue area (e.g., $\Delta T_1 = 0.4$) in Fig. 6 following (14). Then, between the upper bound and the lower bound at $\Delta T_1 = 0.4$, a ΔT_2 is then selected following (15). Example 1 in Fig. 6 shows a ΔT_1 of 0.3 leading to a charging area equal to the discharge area for $\Delta V_{\text{C3+C2}}$, which reflects the output voltage pattern in Fig. 4(c).

C. Regulate C4 and C1 Through ZSI

Once C2 and C3 are regulated, the voltage balance between C4 and C1 can be solved by utilizing another degree of freedom, ZSI. The principle of ZSI is injecting a zero-sequence signal V_{ZSI} into the reference voltages

$$V'_{x-ref} = V_{x-ref} + V_{ZSI} \quad (x = a, b, c) . \tag{17}$$

The added zero-sequence component is canceled out in the line-to-line voltages hence. By injecting a V_{ZSI}, the charge/discharge status of the capacitors can be manipulated to serve the purpose of voltage balancing. The V_{ZSI} is selected out from the constrained range as follows to avoid over-modulation:

$$-1 - \min(V_{x-ref}) \le V_{ZSI} \le 1 - \max(V_{x-ref}) . \tag{18}$$

As expressed in (6), *Objective C* concerns the sum of all the NP currents. When there is a zero-sequence signal, the altered duty ratios lead to the NP currents as follows:

$$\bar{i}_{N2-ZSI} = I_a D_{a2-ZSI} + I_b D_{b2-ZSI} + I_c D_{c2-ZSI} \tag{19}$$

$$\bar{i}_{N3-ZSI} = I_a D_{a3-ZSI} + I_b D_{b3-ZSI} + I_c D_{c3-ZSI} \tag{20}$$

$$\bar{i}_{N4-ZSI} = I_a D_{a4-ZSI} + I_b D_{b4-ZSI} + I_c D_{c4-ZSI}. \tag{21}$$

By iteratively traversing all possible V_{ZSI} values within one carrier cycle, an optimal V_{ZSI} can be found that yields the smallest objective function to track the control target, which is the difference between the altered sum of NP currents and the reference as follows:

$$S = |(\bar{i}_{N3-ZSI} + \bar{i}_{N2-ZSI} + \bar{i}_{N3-ZSI} + \bar{i}_{N1-ZSI}) - OB| . \tag{22}$$

This "optimal searching" approach for selecting V_{ZSI} is similar to the common approach in a three-level converter [29], [44], which can be implemented in real-time microcontrollers with a fixed step size or a fixed number of trial attempts.

IV. Carrier-Based Implementation

A. Carrier-Based RLM

The proposed RLM can be implemented through regular level-shifted carriers. The alteration of duty ratios can be achieved by two steps: (1) split the original modulating wave into four waves corresponding to the four carriers; and (2) introduce two offsets V_{RLM1} and V_{RLM2} for each phase's reference voltages individually corresponding to the two variations ΔT_1 and ΔT_2, respectively. The reason for introducing two offsets is to add two extra redundant levels, instead of one offset to

TABLE II
SPLIT FUNCTION AND RLM ALTERATION THROUGH OFFSETS

	$0.5 \le V_{x-ref} \le 1$	$0 \le V_{x-ref} < 0.5$	$-0.5 \le V_{x-ref} < 0$	$-1 \le V_{x-ref} < -0.5$
Split function	$V_{x4} = V_{x-ref}$ $V_{x3} = 0.5$ $V_{x2} = 0$ $V_{x1} = -0.5$	$V_{x4} = 0.5$ $V_{x3} = V_{x-ref}$ $V_{x2} = 0$ $V_{x1} = -0.5$	$V_{x4} = 0.5$ $V_{x3} = 0$ $V_{x2} = V_{x-ref}$ $V_{x1} = -0.5$	$V_{x4} = 0.5$ $V_{x3} = 0$ $V_{x2} = -0.5$ $V_{x1} = V_{x-ref}$
Altered modulating waves	$V'_{x4} = V_{x4} + V_{RLM1}$ $V'_{x3} = V_{x3} - V_{RLM1} + V_{RLM2}$ $V'_{x2} = V_{x2} - V_{RLM2}$ $V'_{x1} = V_{x1}$		$V'_{x4} = V_{x4}$ $V'_{x3} = V_{x3} + V_{RLM2}$ $V'_{x2} = V_{x2} + V_{RLM1} - V_{RLM2}$ $V'_{x1} = V_{x1} + V_{RLM2}$	

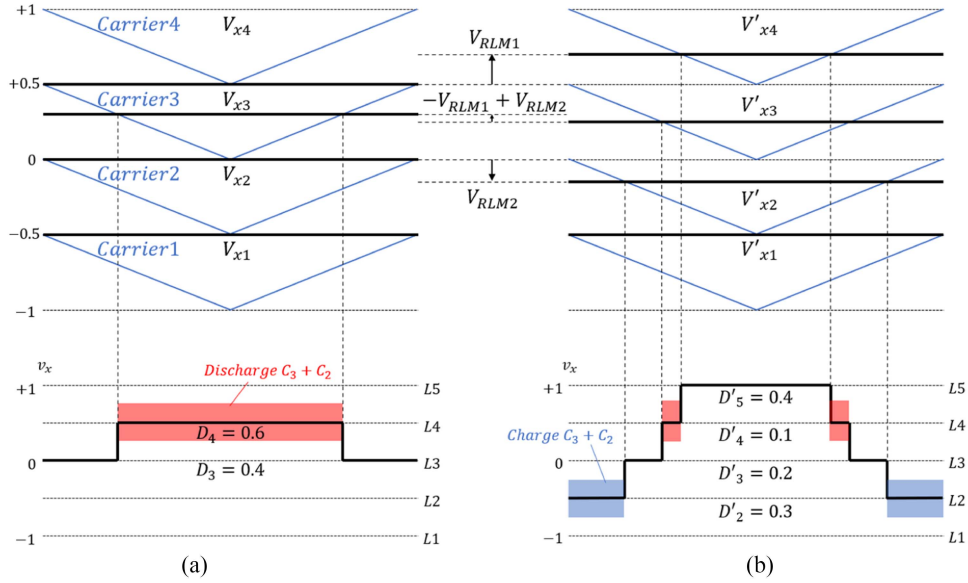

Fig. 7. RLM and output voltage pattern with level-shifted carriers ($V_{x-ref} = 0.3, I_x > 0, V_{RLM1} = 0.2, V_{RLM2} = 0.15$). (a) Regular modulation. (b) RLM-4.

achieve one extra level (*RLM-3*) in [33]. Note the "split" function in the first place does not affect the original duty ratios. The relationship between the duty ratio variation and the offset values can be found as follows:

$$\begin{cases} V_{RLM1} = \Delta T_1/2 \\ V_{RLM2} = \Delta T_2/2 \end{cases}. \tag{23}$$

The split functions and introduction of offsets are achieved by the expressions summarized in Table II. The effect of this operation is visualized in Fig. 7. As the figure shows, in one carrier cycle, the offset values V_{RLM1} and V_{RLM2} lead to an alteration of duty ratios to realize the desired ΔT_1 and ΔT_2, while the synthesized average output voltage of this cycle remains equal. Fig. 7(b) corresponds to *Example 2* in Fig. 6, in which an overall charge of $V_{\mathrm{C3+C2}}$ is achieved.

This carrier-based approach has been implemented in three-level [28], [29] and four-level NPC converters [33] achieving an *RLM-3* operation, while this work extends it to achieve an *RLM-4* operation as required by a 5L-NPC topology. Note it is possible to translate the proposed carrier-based implementation into an SVM, since the equivalence between them has been well established in [45]. Although, the vector space in a three-phase 5L-NPC converter is 125 vectors, which can be complex to apply in SVM. Additionally, while it is more complex to expand SVM for a multiphase system due to the number of vectors growing exponentially, the proposed carrier-based approach can be extended straightforwardly, because the closed-loop *RLM-4* operation is independent between phases.

B. Closed-Loop Control and Modulation Scheme

For the RLM stage, Fig. 8 illustrates the closed control loop to regulate C3 and C2 that tracks the control Objectives A and B. After computing the desired $\Delta T_{1\text{-ref}}$, a saturation stage (Sat.1 in Fig. 8) is applied as below to retrieve the feasible $\Delta T'_1$ as follows:

$$0 \le \Delta T_1 < \frac{2D_4 + D_3}{3}. \tag{24}$$

After a $\Delta T'_1$ is selected, it informs the computation of the boundaries for ΔT_2 following the pool in Fig. 6 expressed by the mathematical functions defined in (16). Note that the correct boundary conditions are important to achieve the full voltage balancing capability. As the contribution of this work, these boundary conditions are expressed mathematically through closed-form expressions. If the boundaries are limited, the converter

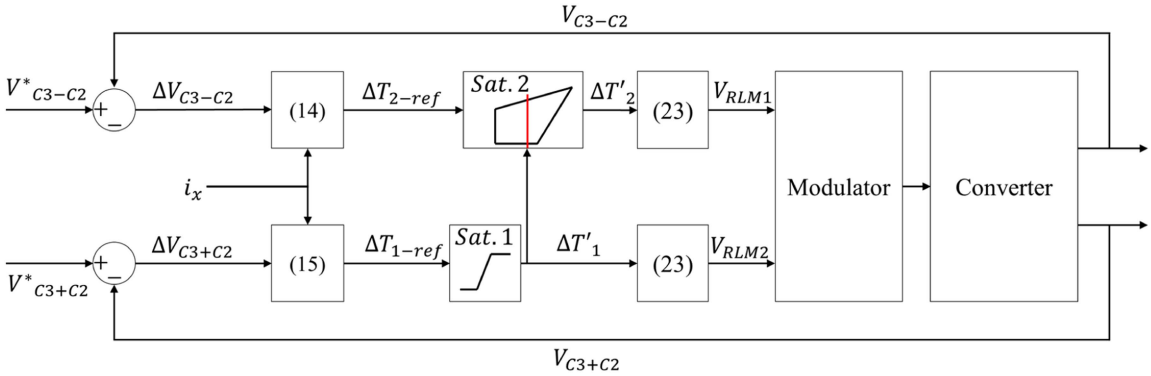

Fig. 8. Closed-loop control of capacitor voltages C3 and C2.

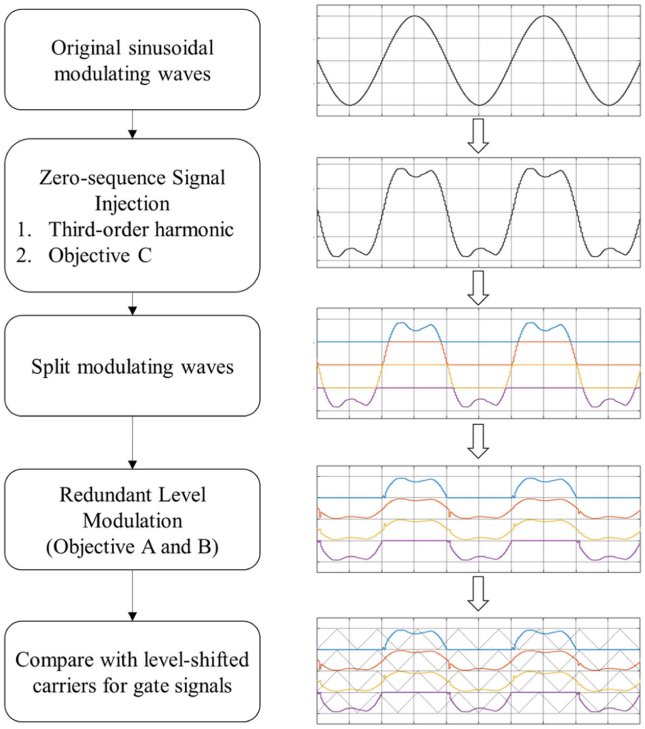

Fig. 9. Flowchart of the control and modulation scheme with visualized modulating waves.

may lose bidirectional controllability. For example, if the selection of ΔT_1 is limited to the red area in Fig. 6, the control loop is not able to charge C3+C2. In other words, a full utilization of the whole range in Fig. 6 results in the optimal duty ratio toward the voltage balancing commands.

The flow of the control scheme and the alteration of modulating waves is illustrated in Fig. 9. Starting from the original sinusoidal modulating waves, the algorithm first alters the waves by injecting a zero-sequence signal to track the control objective C. The next step is to split the waves as a preparation for the carrier-based implementation of RLM. With the control loop shown in Fig. 8, the variations of duty ratios and the offsets are found and applied in the waves. Eventually, the altered waves are fed to the block with level-shifted carriers to generate the gate signals and control the converter behavior.

C. Over-Modulation Strategy

The ZSI block contains two stages – the first stage optionally injects the below ZSI component $V_{\text{ZSI-3rd}}$ into the original sinusoidal waves, which is a common third-order harmonic term, e.g., implemented in [28], to extend the maximum modulation index M to 1.15.

$$V_{VSI-3rd} = -\left[\max\left(V_a, V_b, V_c\right) + \min\left(V_a, V_b, V_c\right)\right]/2. \quad (25)$$

On top of the waves containing the third-order harmonics, the second stage of this block performs the "searching" algorithm in Section III-C to find an "additive" zero-sequence component V_{ZSI} to achieve the control toward *Objective C* to balance the C4/C1 voltages. After these two stages, the modulating waves are modified as follows:

$$V'_{x-ref} = V_{x-ref} + V_{ZSI-3rd} + V_{ZSI} \ (x = a, b, c) \ . \quad (26)$$

By design, the voltage balancing stage does not undermine the third-order harmonic injection stage, which is achieved by working out the range of V_{ZSI} after the third-order harmonic is injected, as shown in the following equation:

$$\begin{aligned} -1 - \min\left(V_{x-ref} + V_{ZSI-3rd}\right) &\le V_{ZSI} \\ &\le 1 - \max\left(V_{x-ref} + V_{ZSI-3rd}\right) \ . \end{aligned} \quad (27)$$

Hence, this overmodulation strategy enables the converter to achieve the maximum output voltage range ($M = 1.15$).

D. Level-Skipping Problem and Implementation of Dwell Levels

Fig. 10(a) illustrates the case where the selection of ΔT_2 falls on the boundary, which leads to the altered duty ratio of the *L3* reaching zero. In this case, the converter output voltage skips level 3, which is undesirable considering the switching loss, device voltage stress, and harmonic performance, similar to the "minimum-energy" operation in [15].

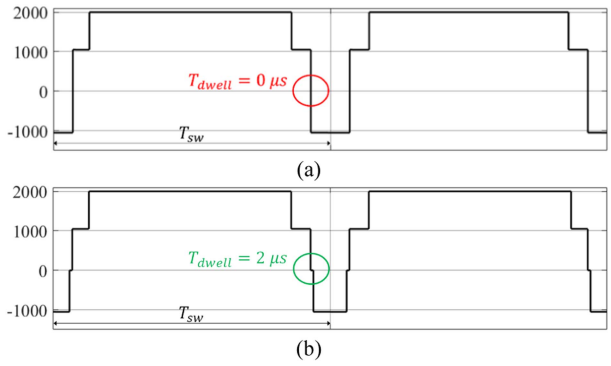

Fig. 10. Before/after minimum dwell time implementation.

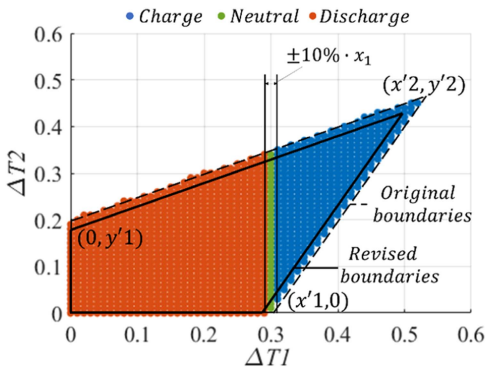

Fig. 11. Revised boundaries of $(\Delta T_1, \Delta T_2)$ concerning V_{C3+C2} ($V_{\text{ref}} = 0.3$, $I_x > 0$).

A dwell time T_{dwell} can be implemented by slightly revising the boundary conditions for ΔT_2 after a ΔT_1 is selected, as shown in Fig. 11.

The coordinates for the altered boundaries are

$$\begin{aligned} y'_1 &= \frac{D_3}{2} - \frac{T_{dwell}}{T_{sw}} \\ x'_1 &= \frac{D_4}{2} - \frac{T_{dwell}}{T_{sw}} \\ x'_2 &= \frac{2D_4 + D_3}{3} - \frac{T_{dwell}}{T_{sw}} \\ y'_2 &= \frac{D_4 + 2D_3}{3} - \frac{T_{dwell}}{T_{sw}} \end{aligned} \tag{28}$$

where T_{sw} is the period of one carrier cycle. Shrinking the boundary conditions for ΔT_2 ensures that the altered duty ratios (7)–(10) are always greater than zero, which avoids the level-skipping problem. As shown in Fig. 10(b), this approach can effectively result in a dwell level in the output voltage.

V. Performance Evaluation

A. Voltage Balancing Under Various Operating Conditions

To evaluate the effectiveness of the proposed voltage balancing algorithm, a simulation model is developed in MATLAB/Simulink with the parameters listed in Table III given a medium-voltage (4 kV) single-end inverter for grid applications.

TABLE III
Simulation Parameters

DC-link voltage	4 kV
Carrier frequency f_{sw}	5 kHz
Capacitance	$C = C4 = C3 = C2 = C1 = 1$ mF
Minimum dwell time T_{dwell}	2 μs
Control loop delay	One carrier cycle + 500 ns turn-ON delay
Passive load	$R = 22\ \Omega\ 6$, $L = 6$ mH per phase

The performance of the control scheme is shown in Fig. 12. Fig. 12(a) shows the case where the converter operates under a range of modulation index M and fundamental frequency f_0. This figure demonstrates that the proposed control method performs well – it not only maintains the capacitor voltages around the reference values, but also suppresses the ripples to high-frequency components on a switching cycle basis. Fig. 12(b) shows the performance under various modulation index and power factor angle φ. In the worst case where a high modulation index M and a high-power factor $cos\ \varphi$ are in place, the control scheme offers satisfactory voltage balancing capability. Meanwhile, it is visible that the C4/C1 voltages show larger ripple under a low power factor, which is caused by the limitations of the ZSI method that is applied to balance the C4/C1 voltage – a similar observation is made in the existing method [35]. When there is a step change of the operating point, e.g., modulation index, the control loop offers a seamless transition with no observable distortion. Fig. 12(c) demonstrates the validity of the proposed approach under the maximum modulation index $M = 1.15$ achieved with third-order harmonic injection in the ZSI stage. In short, the proposed scheme is effective and versatile under all operating conditions. However, low-frequency oscillations can still appear in the outer capacitor C4/C1 voltages when the power factor is low due to the limitations of the ZSI approach under such an operating point, which is similar to the case in a three-level NPC converter.

Additionally, the proposed approach is evaluated in the case of nonlinear loads, e.g., a three-phase diode rectifier with an RC load. The performance of the converter is shown in Fig. 13 in this case. The nonlinear load introduces significant odd-order, low-frequency harmonics in the converter output phase current, while the proposed algorithm still performs very well, because it can successfully suppress the capacitor voltage ripples down to high-frequency ripples as a result of the cycle-by-cycle voltage balancing, which is not influenced by the low-order components in the load current. The proposed scheme is also effective in the case of nonlinear loads containing rich even-order harmonics as evaluated in simulation.

A zoomed-in view of the steady-state capacitor voltages is shown in Fig. 14, which shows the capacitor voltage ripples are all suppressed to high-frequency ripples.

B. Power Loss and THD in a Five-Level E-Type NPC

The power loss and THD performance of the proposed method are evaluated in a five-level E-type NPC (5L-ENPC) converter, shown in Fig. 15(a), in this section. As references, the results are compared against (1) a two-level counterpart as a baseline; (2)

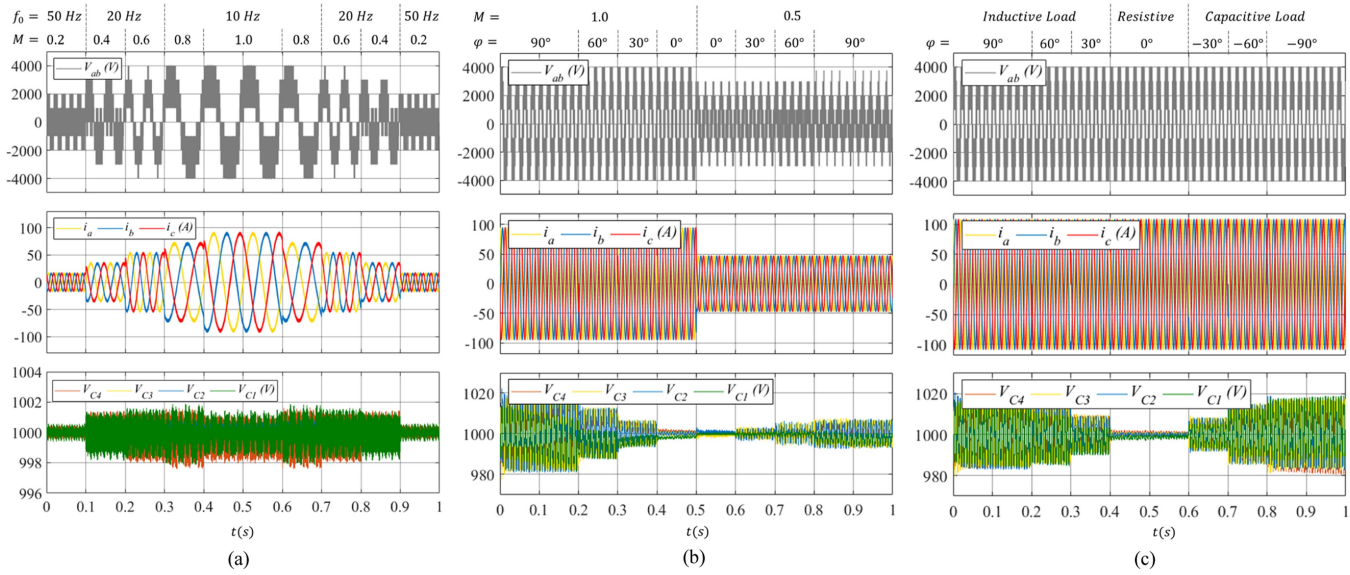

Fig. 12. Inverter performance under various operating conditions. (a) f_0 and M (passive load). (b) M and φ ($f_0 = 50$ Hz). (c) $M = 1.15$ ($f_0 = 50$ Hz).

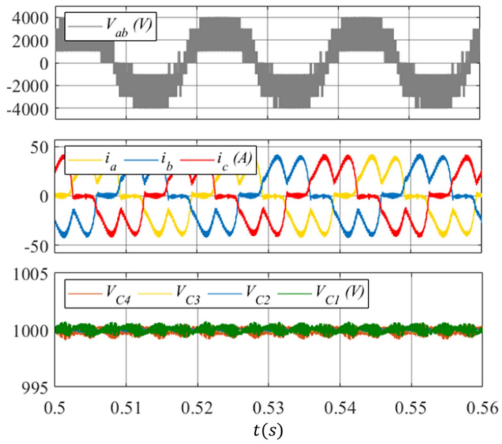

Fig. 13. Waveforms with a diode rectifier and RC load ($R = 100\ \Omega$, $C = 10$ mF).

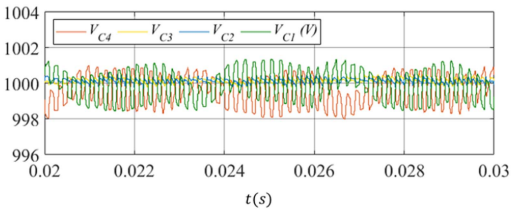

Fig. 14. Zoomed-in capacitor voltage waveforms under the proposed algorithm ($f_0 = 50$ Hz, $f_{sw} = 5$ kHz, $M = 1.0$, $\cos\varphi = 0.996$).

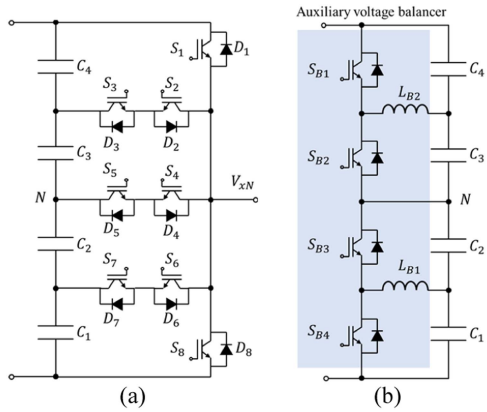

Fig. 15. (a) 5L-ENPC structure. (b) Auxiliary voltage balancer (not required for the proposed scheme).

TABLE IV
POWER DEVICE SELECTION FOR THE 4 KV 5L-ENPC CONVERTER

Switch	Switching voltage	Static blocking voltage	Part
S1/S8	$V_{DC}/4 = 1kV$	$V_{DC} = 4\ kV$	FZ800R45KL3, 4500V
S3/S6	$V_{DC}/4 = 1kV$	$3V_{DC}/4 = 3kV$	FZ825R33HE4D, 3300V
S4/S5	$V_{DC}/4 = 1kV$	$V_{DC}/2 = 2kV$	FF1800R23IE7, 2300V
S2/S7	$V_{DC}/4 = 1kV$	$V_{DC}/4 = 1kV$	FZ400R17KE3, 1700V

an ideal 5L-ENPC converter with four ideal dc sources in series to form the dc-link, for which the ordinary SPWM is applied; and (3) a 5L-ENPC converter equipped with an auxiliary voltage balancing circuit (voltage balancer) shown in Fig. 15(b), which is an alternative to balance the capacitor voltages [13] and commonly implemented as buck-boost circuits. Note if the proposed modulation-based scheme is implemented, there is no need to install the auxiliary circuits. In the case of employing the voltage balancer, standard SPWM modulation can be applied with a simple ZSI stage to balance the middle NP N as implemented in [13]. The selected power devices are listed in Table IV.

Silicon-based IGBT devices from Infineon are selected in this case for the evaluated 4 kV application. As the baseline, both the switching voltage and static blocking voltage are the full dc-link voltage in a two-level topology. Hence, a 6500 V rated

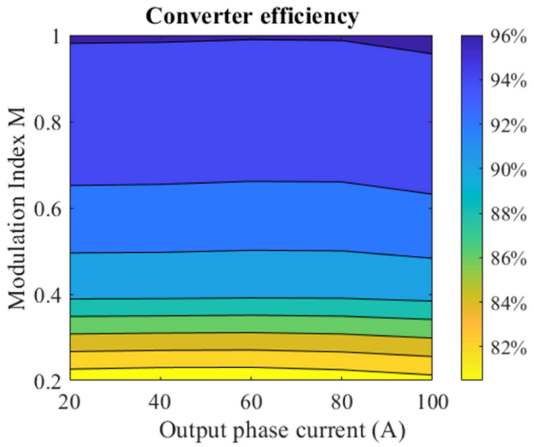

Fig. 16. Converter efficiency map of a three-phase 5L-ENPC with proposed voltage balancing scheme (cos $\varphi = 1, f_{\rm sw} = 5$ kHz).

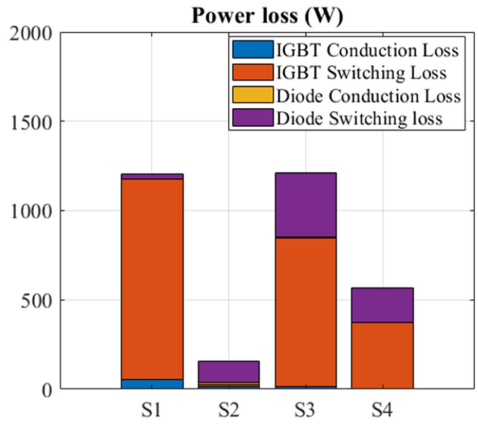

Fig. 17. Device loss breakdown (cos $\varphi = 0.9, f_{\rm sw} = 5$ kHz, $P_{\rm out} = 400$ kW).

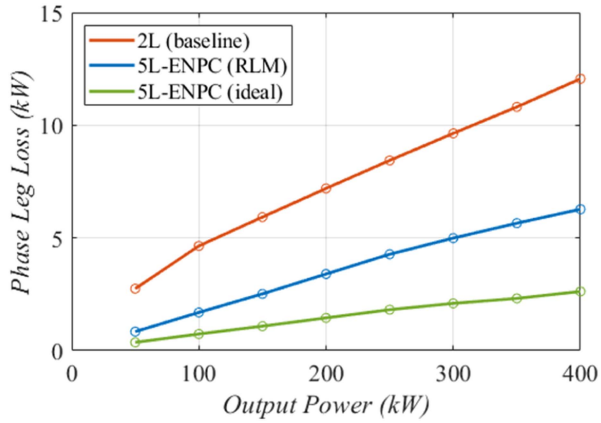

Fig. 18. Phase leg loss versus output power (cos $\varphi = 0.9$, $M = 0.9, f_{\rm sw} =$ 5 kHz).

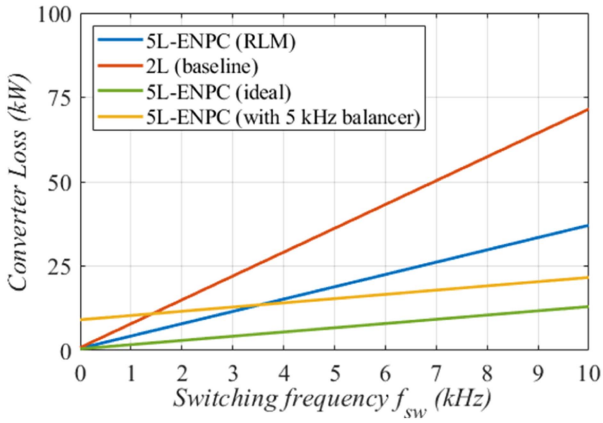

Fig. 19. Converter loss versus converter switching frequency (cos $\varphi = 0.9$, M = 0.9, *output power* = 400 kW).

device (FZ250R65KE3) is selected to leave a >50% margin for the switching voltage. For the reference case with the voltage balancer, the power devices are implemented with 3.3 kV rated power devices FZ825R33HE4D.

The power loss of the converter is estimated in Simulink/PLECS with the proposed *RLM-4* algorithm applied and the specifications listed in Table III. The two-level converter case applies regular SPWM. Fig. 16 shows that the 5L-ENPC converter can offer an efficiency of above 96% when the modulation index is close to unity across various currents.

Fig. 17 shows a breakdown of the loss distribution among devices. It can be seen that the switching loss is the dominant loss mechanism in this case, which is typical in a medium-voltage converter.

Fig. 18 shows a comparison of phase leg power loss of the 5L-ENPC (RLM) case against the alternative options. The 5L-ENPC (RLM) case shows a nearly halved loss compared with the two-level case. Although the switching voltage in the five-level converter is only 25% of a two-level counterpart, the loss reduction is only 50% due to the side effect of the RLM operation to balance the dc-link capacitor voltages. Compared with the ideal case, the switching loss is tripled by the *RLM-4* operation, because it introduces four additional switching transitions in each switching cycle compared with SPWM as illustrated in Fig. 4. This side effect applies to all the other existing modulation-based methods (e.g., [36] and [35]) due to the same principles of applying the *RLM-4* pattern that is mandatory in a 5L-NPC converter. Note the ideal case is for theoretical comparison only and not feasible in real applications. Additionally, this drawback on increased switching transitions can be moderated by applying low-switching-loss wide-bandgap power devices, e.g., Silicon Carbide MOSFETS, as pointed out in [46].

Fig. 19 shows the comparison of loss on a converter level. Another reference case with the auxiliary voltage balancer is provided. The charging inductors $L_{\rm B2}$ and $L_{\rm B1}$ are sized as 5 mH, similar to [8], to limit the charging current to <100 A under a switching frequency $f_{\rm bsw}$ of 5 kHz. Acting as an independent part, the dc-link voltage balancer leads to power losses adding on top of the overall converter loss of an ideal case, as plotted in the yellow curve. When the phase leg $f_{\rm sw}$ is lower than 3.5 kHz (depending on the balancer's design), the RLM case still shows better efficiency overall,

TABLE V
COMPARISON WITH EXISTING VOLTAGE BALANCING

	Auxiliary circuits	Modulation implementation	Mandatory PI controller	Closed-loop control	Complexity	Voltage balancing performance
[7], [8], [14]	YES	Regular carriers	YES	YES	−	+++
[36]	NO	Space vector	NO	Partial	− − − −	++
[41]	NO	Overlapped carriers	NO	NO	− −	+
[35]	NO	Overlapped carriers	YES	YES	− − −	+++
This work	**NO**	**Regular carriers**	**NO**	**YES**	**− −**	**++++**

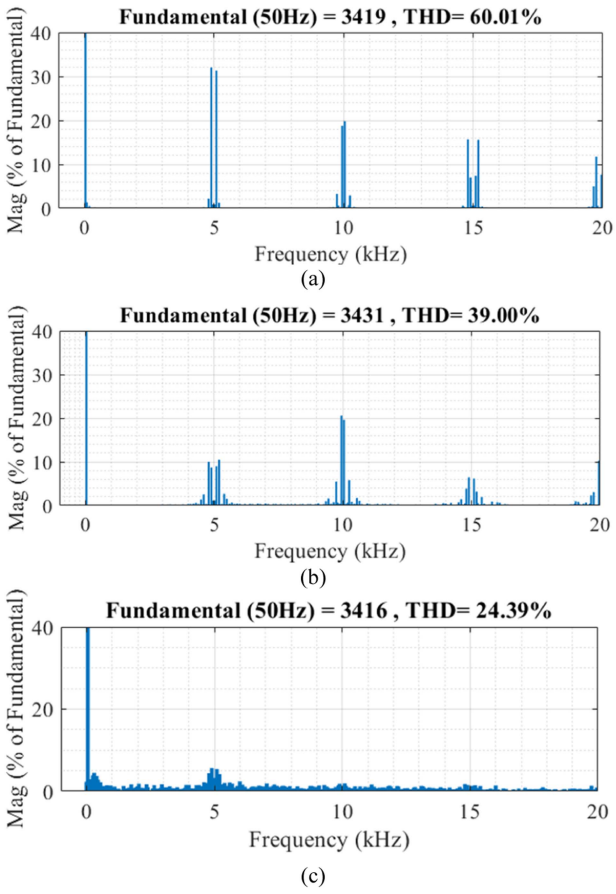

Fig. 20. THD performance of line voltage ($M = 1$). (a) Equivalent two-level counterpart. (b) 5L-ENPC with the proposed *RLM-4* operation applied. (c) 5L-ENPC with an auxiliary voltage balancer operating at 5 kHz.

since the auxiliary circuit introduces comparable conduction and switching losses. Note this evaluation only considers the power device losses with the inductor (L_{B2} and L_{B1}) losses neglected.

Fig. 20 shows a comparison of the harmonics performance of the converter output line voltages in the evaluated cases. Despite the usage of redundant voltage levels, the 5L-ENPC case still shows an improved THD of 39% compared to 60% in the two-level case, with the significant harmonics at the switching frequency (5 kHz) moderated. In comparison, Fig. 20(c) shows that the configuration with an auxiliary balancer can yield the lowest THD and lower harmonics at multiples of $f_{sw,}$ since the converter is able to output the regular five-level waveforms through SPWM without introducing additional redundant levels. Overall, the proposed modulation-based voltage balancing scheme can achieve a comparable performance as auxiliary voltage balancer circuits while it avoids the additional hardware circuits, which increase the cost, complexity, and size of the converter.

TABLE VI
COMPARISON OF ΔV_{NORM} UNDER A NEAR-UNITY POWER FACTOR

	This work	[35]	[36]
	($M = 1.0$)	($M = 1.0$)	($M = 0.95$)
C4/C1	**9.7**	48.3	92.3
C3/C2	**2.0**	27.6	76.9

C. Comparison With Existing Methods

To provide a comparison, Table V summarizes the fundamental differences between this work and the existing methods in literature with the key points explained as follows. The methods in [7], [8], and [14] are based on auxiliary balancing circuits or back-to-back structures that introduce additional hardware. For modulation-based approaches [35], [36], [41], although the implementation appears different, these approaches fundamentally utilize redundant voltage levels to achieve voltage balancing, which is similar to the *RLM-4* concept introduced in this work. Thanks to the fully resolved model, the proposed algorithm in this work uniquely involves only closed-form equations and logical operators and does not require mandatory PI/PID controllers, which achieves fast processing of real-time signals for closed-loop control. In contrast, Wang et al. [35] adapt PI controllers to process the measured voltage balance into the variation of duty ratios, treating it as a black box problem that does not consider the load current amplitude due to the lack of a complete analytical model. While [36] does not require a linear controller, its compensation values (e.g., ΔT_1 and ΔT_2) are found through a stepped lookup table leading to voltage vectors with a fixed dwell time. In contrast, the proposed approach dynamically calculates the duration of voltage levels following the measured level of unbalance and load current to offer a precise control without an under/over-compensation.

Regarding the steady-state performance of voltage balancing, as a metric, a normalized value describing the peak-to-peak capacitor voltage ripples ΔV_{C_norm} is proposed in this work as a function of the actual voltage ripple ΔV_C, the load current I_{rms}, capacitances C, the switching frequency f_{sw} and the fundamental frequency f_0 to quantify the evaluation across various systems for a fair comparison. Compared with the common normalization

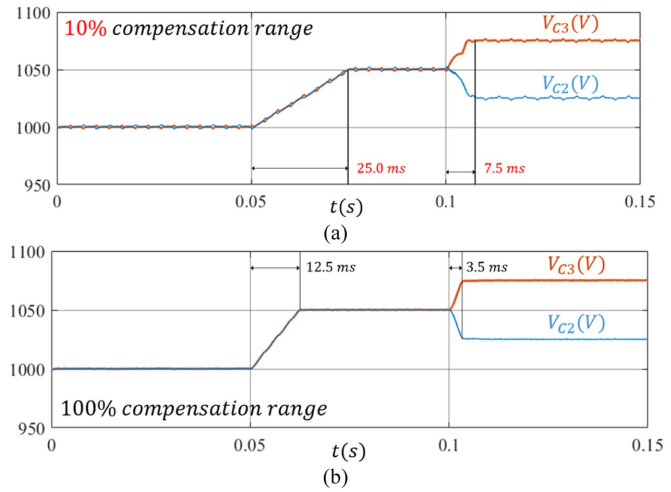

Fig. 21. Comparison of dynamic voltage balancing performance ($M = 1$). (a) Limited compensation range (10% as in [35]). (b) Utilizing the full range within the boundaries of Fig. 6 (proposed method).

term in [47], the proposed approach factors in both $f_{\rm sw}$ and f_0, while the classic term fails to capture the impact of $f_{\rm sw}$. For both $f_{\rm sw}$ and f_0, the higher they are, the easier the voltage balancing task is. As demonstrated in [29], in the case where the low-frequency oscillation is eliminated by the balancing scheme, a higher $f_{\rm sw}$ can still lead to lower amplitude of the high-frequency NP voltage ripples due to the balancing action achieved on a cycle-by-cycle basis.

$$\Delta V_{C\_norm} = \frac{\Delta V_C}{\Delta V_{C\_base}} = \Delta V_C \div \frac{I_{rms}}{f_{sw} \cdot f_0 \cdot C}. \quad (29)$$

For example, in this work, a peak-to-peak voltage ripple of 2.46 V is observed for C4/C1 in the waveforms shown in Fig. 14. With other specifications listed in Table III, the $\Delta V_{\rm C\_norm}$ is worked out as 9.7 in this case. Based on the disclosed waveforms in [36] and [35], a quantified comparison is conducted and shown in Table VI. Comparing the normalized capacitor voltage ripples, it can be seen that the proposed method in this work yields the best performance, e.g., with a ΔV_{C_norm} of 9.7 compared to 54.7 [35] and 92.3 [36].

Regarding the dynamic performance of voltage balancing, in [35], the variation range of duty ratios is limited to <10% of the original duty ratio (i.e., ±10% of x_1 as visualized in Fig. 11), which effectively limits its dynamic performance. As a comparison, when the reference voltages see a step change, Fig. 21 shows that it takes 25.0 ms for the limited control scheme to track the control command of *Objective A*, while the full-range scheme proposed in this work only needs 12.5 ms. For *Objective B*, Fig. 21(a) takes 7.5 ms to reach the steady state, while Fig. 21(b) only takes 3.5 ms, which demonstrates the superiority of the proposed scheme. It can also be observed that there are larger voltage ripples in Fig. 21(a) due to the limited controllability.

Regarding the complexity of implementation, the work in [35] and [41] is based on irregular "overlapped" carriers, which are not straightforward to reproduce. The work in [36] is based on SVM, which is complex for the five-level converter case, and requires predefined lookup tables for voltage balancing purposes. In contrast, the proposed scheme can be adapted with regular level-shifted carriers with the balancing scheme realized in modular blocks as shown in Fig. 9 to alter the modulating waves step-by-step. Overall, the proposed algorithm features a simple and fast-processing implementation with regular carriers while it offers the most effective and versatile control capability.

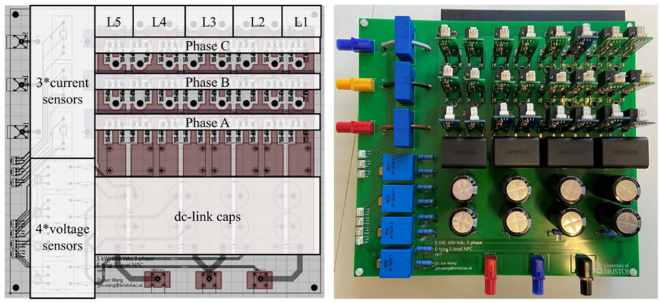

Fig. 22. 5L-ENPC inverter prototype. (a) PCB design. (b) Photograph of hardware.

TABLE VII
TEST RIG SPECIFICATIONS AND COMPONENTS

DC-link voltage and supply	200 V, EA-PS 81000-30 3U
Carrier frequency $f_{\rm sw}$	5 kHz
Fundamental frequency f_0	50 Hz
DC-link capacitors	$C = C4 = C3 = C2 = C1$ = 1 mF
Load	R = 33 Ω , L = 6.3 mH per phase

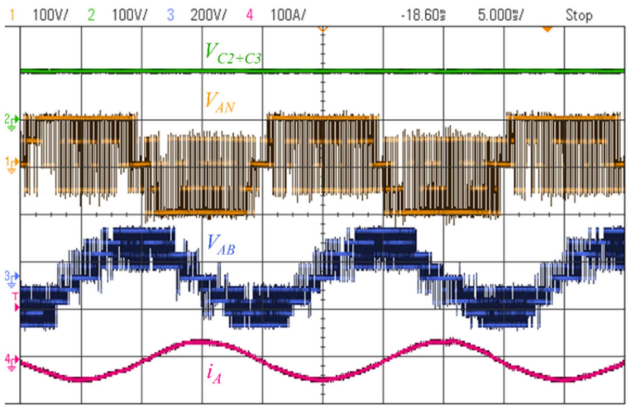

Fig. 23. Measured output waveforms ($M = 0.95$).

VI. EXPERIMENTAL VALIDATION

To validate the proposed approach, a 5L-ENPC prototype is built as shown in Fig. 22, and tested in a downscaled test rig. The specifications of the prototype and test rig are listed in Table VII.

The four capacitor voltages are sensed through sensors LV-25P and the three-phase load currents are sensed by LA-25. The control algorithm is developed in a digital signal processor F28335 from Texas Instrument. As Fig. 23 shows, the single-end

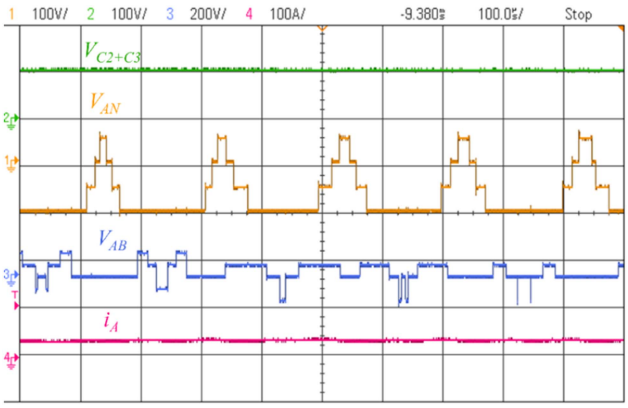

Fig. 24. Measured output waveforms (zoomed-in).

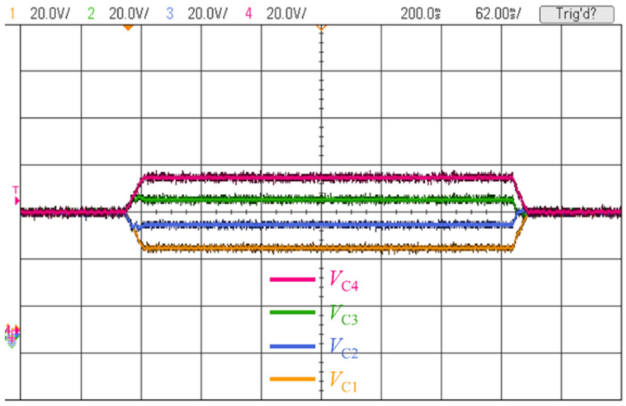

Fig. 25. Dynamic voltage balancing performance.

inverter can successfully achieve voltage balancing under a near-unity power factor ($\cos\varphi = 0.998$) and a high modulation index, which can steadily output five voltage levels. In a zoomed-in view in Fig. 24, the phase output voltage shows four voltage levels as intended by the *RLM-4* operation without skipping any levels.

When a step change is applied on the reference voltages for the four capacitors, the control loop can well track the command and demonstrates a decoupled, bidirectional control capability on individual capacitors as shown in Fig. 25. In summary, the effectiveness of the proposed approach is validated in the experiment.

VII. Conclusion

This article proposes a fast-processing algorithm to address the voltage balancing issue in a single-end, 5L-NPC converter. As the key concept, the RLM is utilized to gain extra control of the capacitor voltages, for which the principle is explained with the aid of the capacitor operation diagrams (CODs). A closed-loop control scheme is developed and implemented with regular level-shifted carriers. As a result of fully transparent mathematical models and boundary conditions of duty ratios, the proposed approach can achieve maximum controllability without involving opaque PI/PID controllers treating the system as a black box, which makes it straightforward to reproduce in prototyping. Both qualitative and quantitative comparisons are conducted to validate the superiority of the proposed method against existing approaches. An improved normalization term with the switching frequency included is proposed to quantify the voltage ripples for the evaluation of voltage balancing performance across different systems. The authors hope that this easy-to-implement, modulation-based voltage balancing algorithm can enable the 5L-NPC topology to be better adopted in the medium-voltage grid and drive applications.

As a side effect, the *RLM-4* operation is found to result in increased harmonics and switching loss due to the tripled switching actions in one carrier cycle, which is considered the mandatory cost for balancing the capacitor voltages in a 5L-NPC converter without introducing additional hardware. In future work, this side effect could be improved through constraining the usage of *RLM-4* in the control/modulation flow.

References

[1] A. Nabae, I. Takahashi, and H. Akagi, "A new neutral-point-clamped PWM inverter," *IEEE Trans. Ind. Appl.*, vol. 1A-17, no. 5, pp. 518–523, Sep. 1981.
[2] X. Yuan, "Derivation of multilevel voltage source converter topologies," *IEEE Trans. Ind. Electron.*, vol. 64, no. 2, pp. 966–976, Feb. 2017.
[3] X. Yuan, "Ultimate generalized multilevel converter topology," *IEEE Trans. Power Electron.*, vol. 36, no. 8, pp. 8634–8639, Aug. 2021.
[4] X. Yuan, "A four-level π-type converter for low-voltage applications," in *Proc. IEEE Eur. Conf. Power Electron. Appl.*, 2015, pp. 1–10.
[5] B. Jin and X. Yuan, "Topology, efficiency analysis and control of a four-level π-type converter," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 7, no. 2, pp. 1044–1059, Jun. 2019.
[6] B. Wang, "Four-level neutral point clamped converter with reduced switch count," in *Proc. IEEE Annu. Power Electron. Specialists Conf.*, 2008, pp. 2626–2632.
[7] N. Hatti, K. Hasegawa, and H. Akagi, "A 6.6-kV transformerless motor drive using a five-level diode-clamped PWM inverter for energy savings of pumps and blowers," *IEEE Trans. Power Electron.*, vol. 24, no. 3, pp. 796–803, Mar. 2009.
[8] N. Hatti, Y. Kondo, and H. Akagi, "Five-level diode-clamped PWM converters connected back-to-back for motor drives," *IEEE Trans. Ind. Appl.*, vol. 44, no. 4, pp. 1268–1276, Jul./Aug. 2008.
[9] M. Mazuela, I. Baraia, A. Sanchez-Ruiz, I. Echeverria, I. Torre, and I. Atutxa, "DC-link voltage balancing strategy based on SVM and reactive power exchange for a 5L-MPC back-to-back converter for medium-voltage drives," *IEEE Trans. Ind. Electron.*, vol. 63, no. 12, pp. 7864–7875, Dec. 2016.
[10] M. Saeedifard, R. Iravani, and J. Pou, "A space vector modulation strategy for a back-to-back five-level HVDC converter system," *IEEE Trans. Ind. Electron.*, vol. 56, no. 2, pp. 452–466, Feb. 2009.
[11] Z. Shu, N. Ding, J. Chen, H. Zhu, and X. He, "Multilevel SVPWM with DC-link capacitor voltage balancing control for diode-clamped multilevel converter based STATCOM," *IEEE Trans. Ind. Electron.*, vol. 60, no. 5, pp. 1884–1896, May 2013.
[12] M. Saeedifard, R. Iravani, and J. Pou, "Control and DC-capacitor voltage balancing of a space vector-modulated five-level STATCOM," *IET Power Electron.*, vol. 2, no. 3, pp. 203–215, 2009.
[13] H. Akagi, H. Fujita, S. Yonetani, and Y. Kondo, "A 6.6-kV transformerless STATCOM based on a five-level diode-clamped PWM converter: System design and experimentation of a 200-V 10-kVA laboratory model," *IEEE Trans. Ind. Appl.*, vol. 44, no. 2, pp. 672–680, Mar./Apr. 2008.
[14] M. di Benedetto, A. Lidozzi, L. Solero, F. Crescimbini, and P. J. Grbovi, "Five-level E-type inverter for grid-connected applications," *IEEE Trans. Ind. Appl.*, vol. 54, no. 5, pp. 5536–5548, Sep./Oct. 2018.
[15] M. Marchesoni and P. Tenca, "Diode-clamped multilevel converters: A practicable way to balance DC-link voltages," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 752–765, Aug. 2002.
[16] M. Saeedifard, R. Iravani, and J. Pou, "Analysis and control of DC-capacitor-voltage-drift phenomenon of a passive front-end five-level converter," *IEEE Trans. Ind. Electron.*, vol. 54, no. 6, pp. 3255–3266, Dec. 2007.

[17] K. Wang, L. Xu, Z. Zheng, and Y. Li, "Capacitor voltage balancing of a five-level ANPC converter using phase-shifted PWM," *IEEE Trans. Power Electron.*, vol. 30, no. 3, pp. 1147–1156, Mar. 2015.
[18] J. Wang, X. Yuan, K. J. Dagan, P. Mellor, D. Drury, and A. Bloor, "Universal neutral point balancing algorithm for three-phase three-level converters with hybrid of zero-sequence signal injection and virtual zero-level modulation," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2018, pp. 2200–2206.
[19] C. Wang and Y. Li, "Analysis and calculation of zero-sequence voltage considering neutral-point potential balancing in three-level NPC converters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, pp. 2262–2271, Jul. 2010.
[20] Y. Jiao, F. C. Lee, and S. Lu, "Space vector modulation for 3-level NPC converter with neutral point voltage balancing and switching loss reduction," *IEEE Trans. Power Electron.*, vol. 29, no. 10, pp. 5579–5591, Oct. 2014.
[21] J. Pou, R. Pindado, and D. Boroyevich, "Voltage-balance limits in four-level diode-clamped converters with passive front ends," *IEEE Trans. Ind. Electron.*, vol. 52, no. 1, pp. 190–196, Feb. 2005.
[22] S. Busquets-Monge, J. Bordonau, D. Boroyevich, and S. Somavilla, "The nearest three virtual space vector PWM—A modulation for the comprehensive neutral-point balancing in the three-level NPC inverter," *IEEE Power Electron. Lett.*, vol. 2, no. 1, pp. 11–15, Mar. 2004.
[23] D. Cui, Q. Ge, Z. Zhou, and B. Yang, "A closed-loop voltage balance method for five-level diode-clamped inverters," in *Proc. IEEE Annu. Conf. IEEE Ind. Electron. Soc.*, 2017, pp. 503–508.
[24] Z. Pan and F. Z. Peng, "A sinusoidal PWM method with voltage balancing capability for diode-clamped five-level converters," *IEEE Trans. Ind. Appl.*, vol. 45, no. 3, pp. 1028–1034, May/Jun. 2009.
[25] M. Marchesoni and L. Vaccaro, "Extending the operating range in diode-clamped multilevel inverters with active front ends," in *Proc. IEEE Int. Energy Conf. Exhib.*, 2012, pp. 63–68.
[26] P. Fazio, G. Maragliano, M. Marchesoni, and L. Vaccaro, "A new capacitor balancing technique in diode-clamped multilevel converters with active front end for extended operation range," in *Proc. IEEE Eur. Conf. Power Electron. Appl.*, 2011, pp. 1–10.
[27] I. Lopez et al., "Modulation strategy for multiphase neutral-point-clamped converters," *IEEE Trans. Power Electron.*, vol. 31, no. 2, pp. 928–941, Feb. 2016.
[28] J. Pou et al., "Fast-processing modulation strategy for the neutral-point-clamped converter with total elimination of low-frequency voltage oscillations in the neutral point," *IEEE Trans. Ind. Electron.*, vol. 54, no. 4, pp. 2288–2294, Aug. 2007.
[29] J. Wang, X. Yuan, K. J. Dagan, and A. Bloor, "Optimal neutral point voltage balancing algorithm for three-phase three-level converters with hybrid zero-sequence signal injection and virtual zero-level modulation," *IEEE Trans. Ind. Appl.*, vol. 56, no. 4, pp. 3865–3878, Jul./Aug. 2020.
[30] K. Wang, Z. Zheng, and Y. Li, "Topology and control of a four-level ANPC inverter," *IEEE Trans. Power Electron.*, vol. 35, no. 3, pp. 2342–2352, Mar. 2020.
[31] K. Wang, Z. Zheng, L. Xu, and Y. Li, "A composite voltage balancing method for four-level NPC inverters," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 3, pp. 3394–3406, Jun. 2021.
[32] J. Wang, X. Yuan, B. Jin, and I. Laird, "Closed-loop DC-link voltage balancing algorithm for a four-level π-type converter," in *Proc. Annu. Conf. IEEE Ind. Electron. Soc.*, 2019, pp. 3529–3534.
[33] J. Wang, X. Yuan, and B. Jin, "Carrier-based closed-loop DC-link voltage balancing algorithm for four level NPC converters based on redundant level modulation," *IEEE Trans. Ind. Electron.*, vol. 68, no. 12, pp. 11707–11718, Dec. 2021.
[34] S. Busquets-Monge, J. Bordonau, and J. Rocabert, "A virtual-vector pulsewidth modulation for the four-level diode-clamped DC–AC converter," *IEEE Trans. Power Electron.*, vol. 23, no. 4, pp. 1964–1972, Jul. 2008.
[35] K. Wang, Z. Zheng, L. Xu, and Y. Li, "Neutral-point voltage balancing method for five-level NPC inverters based on carrier-overlapped PWM," *IEEE Trans. Power Electron.*, vol. 36, no. 2, pp. 1428–1440, Feb. 2021.
[36] Z. Zhao, J. Zhao, and C. Huang, "An improved capacitor voltage-balancing method for five-level diode-clamped converters with high modulation index and high power factor," *IEEE Trans. Power Electron.*, vol. 31, no. 4, pp. 3189–3202, Apr. 2016.
[37] H. Tian and Y. W. Li, "Carrier-based stair edge PWM (SEPWM) for capacitor balancing in multilevel converters with floating capacitors," *IEEE Trans. Ind. Appl.*, vol. 54, no. 4, pp. 3440–3452, Jul./Aug. 2018.
[38] J. Wang, C. Wei, W. Zhou, and X. Yuan, "Capacitor voltage balancing algorithm with redundant level modulation for a five level converter with reduced device count," in *Proc. IEEE Int. Power Electron. Motion Control*, 2020, pp. 1758–1764.
[39] S. Busquets-Monge, A. Filba-Martinez, S. Alepuz, and A. Calle-Prado, "A modulation strategy to operate multilevel multiphase diode-clamped and active-clamped DC–AC converters at low frequency modulation indices with DC-link capacitor voltage balance," *IEEE Trans. Power Electron.*, vol. 32, no. 10, pp. 7521–7533, Oct. 2017.
[40] S. Busquets-Monge, R. Maheshwari, J. Nicolas-Apruzzese, E. Lupon, S. Munk-Nielsen, and J. Bordonau, "Enhanced DC-link capacitor voltage balancing control of DC–AC multilevel multileg converters," *IEEE Trans. Ind. Electron.*, vol. 62, no. 5, pp. 2663–2672, May 2015.
[41] K. Wang, Z. Zheng, L. Xu, and Y. Li, "A generalized carrier-overlapped PWM method for neutral-point clamped multilevel converters," *IEEE Trans. Power Electron.*, vol. 35, no. 9, pp. 9095–9106, Sep. 2020.
[42] S. Busquets-Monge, S. Alepuz, J. Bordonau, and J. Peracaula, "Voltage balancing control of diode-clamped multilevel converters with passive front-ends," *IEEE Trans. Power Electron.*, vol. 23, no. 4, pp. 1751–1758, Jul. 2008.
[43] J. Wang, W. Xu, X. Yuan, and L. Xie, "Investigation and mitigation of common-mode voltage in four-level NPC converters modulated by redundant level modulation," in *IEEE Proc. Eur. Conf. Power Electron. Appl.*, 2022, pp. 1–9.
[44] X. Yuan, Y. Li, and C. Wang, "Objective optimisation for multilevel neutral-point-clamped converters with zero-sequence signal control," *IET Power Electron.*, vol. 3, no. 5, pp. 755–763, 2010.
[45] K. Zhou and D. Wang, "Relationship between space-vector modulation and three-phase carrier-based PWM: A comprehensive analysis," *IEEE Trans. Ind. Electron.*, vol. 49, no. 1, pp. 186–196, Feb. 2002.
[46] X. Yuan, J. Wang, I. Laird, and W. Zhou, "Wide-bandgap device enabled multilevel converters with simplified structures and capacitor voltage balancing capability," *IEEE Open J. Power Electron.*, vol. 2, pp. 414–423, 2021.
[47] J. Pou, R. Pindado, D. Boroyevich, and P. Rodríguez, "Evaluation of the low-frequency neutral-point voltage oscillations in the three-level inverter," *IEEE Trans. Ind. Electron.*, vol. 52, no. 6, pp. 1582–1588, Dec. 2005.

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