Lossless Clamp Circuit With Turn-OFF Voltage and Current Reduction in High Step-Up DC–DC Converter With Coupled Inductor

Michał Harasimczuk, *Member, IEEE*, Rafał Kopacz, *Graduate Student Member, IEEE*, and Adam Tomaszuk

***Abstract*—A high power density, high voltage gain soft-switching pulsewidth modulation dc–dc converter with a tapped inductor is proposed in this article as a front-end for low-voltage sources in energy generation systems. The leakage inductance is incorporated into the resonant tank, decreasing the component count. The use of the boost capacitor connected in series with the secondary windings of the tapped inductor causes high voltage gain at the low turn ratio of the coupled inductor. By incorporating a resonant passive clamp circuit, not only the voltage spikes on the transistor are restrained, but zero-voltage switching of the transistor and zero-current turning-OFF of the diodes are obtained. The resonant operation results in low power losses in the switches, providing high efficiency in a wide output power range. Owing to soft-switching operation, the transistor can be driven with a high switching frequency, providing a consolidated design of the high power density converter. The principles of operation of the converter were also analyzed theoretically. Finally, the converter is validated through a laboratory model with a power rating of 300 W and a switching frequency of 200 kHz.**

***Index Terms*—Coupled inductor, dc–dc converters, high efficiency, high gain, resonant converter, soft switching.**

I. Introduction

VOLTAGE step up is required in many renewable energy systems, electric vehicles, aerospace, and military energy processing systems [1], where the energy generators operate at low voltage levels. Step-up converters, as the system submodules, adapt the energy produced by generators to the required dc-bus voltage of the energy system. The key requirements of step-up converters are high efficiency across a wide power range and high voltage gain. For instance, in the European system working with a fuel cell, a single photovoltaic PV module, or several modules connected in parallel, a low output voltage of these power generators needs to be stepped up to at least 380 V dc for single-phase grid systems to assure grid-inverter operation [1].

In the conventional boost converter, which maintains high efficiency, it is not possible to obtain high voltage gain and high output power simultaneously for several reasons. In the conventional boost converter, high voltage gain requires an extremely high duty cycle; thus, conduction losses increase significantly. Besides, transistor voltage stress is almost equal to the output voltage. Therefore, a transistor with a higher voltage rating and higher $R_{\mathrm{DS(ON)}}$ needs to be used. Moreover, in a conventional boost converter, a significant reverse recovery current of the output diode can be observed, which additionally increases the overall converter's switching losses.

There are a lot of methods to achieve high voltage gain in nonisolated converters: SEPIC converter under resonant operation voltage multiplier cell, switched inductor, coupled inductor, and others [2], [3], [4], [5], [6], [7], [8]. Thanks to the coupled inductor and switched capacitor techniques converging, there is a possibility to achieve both high voltage gain and high efficiency while using a low number of components [1], [9], [10], [11]. In a basic tapped-inductor step-up converter, the reverse recovery problem of the output diode is alleviated by the leakage inductance, which limits the slope of the output diode current during the turning-ON of the transistor. On the other hand, the leakage inductance causes voltage overshoots across the switch during turn-OFF. To prevent it in step-up converters with tapped inductors, a snubber circuit is applied. There are several clamp techniques [12], [13], [14] that recover the leakage energy and allow the use of switches with a low voltage rating.

In [5], [6], [8], [10], [15], [16], [17], [18], and [19], the nonisolated step-up converter with a tapped inductor and passive clamp circuit are presented. In these topologies, the passive clamp circuit consists of the diode and the capacitor. In this circuit, the voltage overshoot on the transistor is reduced, and the leakage energy is recovered. Thus, for the transistors driven with the pulsewidth modulation (PWM) technique, their switching conditions are improved. However, the transistor remains switching with nonzero voltage, which results in increased switching losses. In the active clamp technique, an additional switch allows leakage energy recovery and also reduces voltage overshoots on the main transistor [20], [21], [22]. Moreover, in that circuit, the zero voltage switching (ZVS) technique may be

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Michał Harasimczuk and Adam Tomaszuk are with the Faculty of Electrical Engineering, Bialystok University of Technology, 15-351 Bialystok, Poland (e-mail: m.harasimczuk@pb.edu.pl; adam.tomaszuk@pb.edu.pl).

Rafał Kopacz is with the Institute of Control and Industrial Electronics, Warsaw University of Technology, 00-661 Warsaw, Poland (e-mail: rafal.kopacz@pw.edu.pl).

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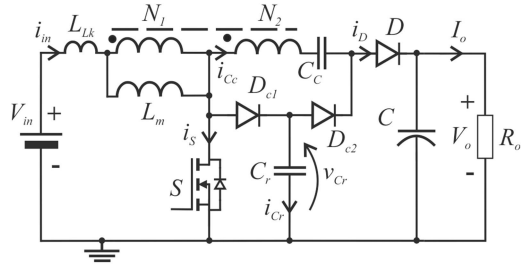

Fig. 1. High step-up DC–DC converter—a schematic of the topology.

applied. In this scenario, the effective duty cycle is decreased, and a coupled inductor with a higher turn ratio is required to compensate for this effect. One of the main problems in boost converters with a coupled inductor is the high input current ripple, which requires the use of additional input filters. This problem is solved in interleaved converters [11], [14], [21], [22]; however, such systems require the employment of many more components, and it can be unprofitable in applications with power in the range of hundreds of watts.

In [23], [24], and [25], converters with a coupled inductor and resonant capacitor connected in series with the secondary winding are presented. In such circuits, reverse recovery problems are eliminated. These converters operate in critical conduction mode (CRM) or discontinuous conduction mode (DCM), where conduction losses are high, restraining the efficiency and rated output power. Soft switching may be obtained in the converters with zero-voltage transition, zero-current transition, or active edge-resonant [26], [27], [28] cells. However, in these techniques, an additional active switch is required to achieve soft switching of the main transistor.

High voltage gain can also be achieved in three-winding coupled inductors [7], [29], [30]. However, in such circuits, there is a greater problem with recovering energy from the leakage inductance. This means that a larger number of semiconductor and reactance elements must be used in the system to achieve proper operation.

This article presents a high step-up soft-switching PWM dc–dc converter with a tapped inductor (see Fig. 1). In the proposed converter, the passive resonant circuit is used to achieve zero voltage turn-OFF of the transistor, whereas, in a similar topology presented in [10], the transistor is turned-OFF in hard switching conditions. A similar soft-switching technique was used in the SEPIC converter presented in [3] and in the buck-boost presented in [2]. However, in these circuits, the voltage gain is low because of the absence of a coupled inductor. The novel resonant passive clamp circuit allows for soft-switching operation, enables zero-voltage turn-OFF of a transistor, and improves the efficiency of the converter, maintaining high voltage gain. Similarly, like in [16], the transistor current slope during turning-ON and diode D current slope during turning-OFF are limited by the leakage inductance. This provides ZC turning-ON of the transistor and ZC turning-OFF of the diode. Moreover, clamp diodes D_{c1} and D_{c2} do not conduct during the transistor turn-OFF process, and the reverse recovery currents of all diodes are reduced.

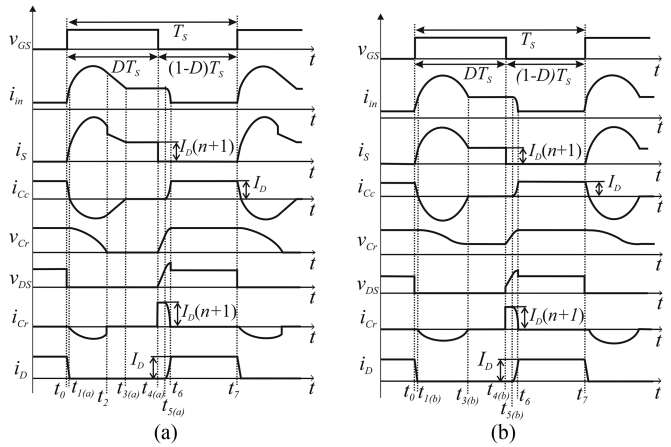

Fig. 2. Theoretical waveforms for $v_{cr}(t_3) = 0$ (left) and $v_{cr}(t_3) > 0$ (right).

This article is structured as follows. After a brief introduction, the operation of the converter is described based on the theoretical waveforms and mathematical equations. Furthermore, the design procedure, allowing proper selection of the components, is presented. Eventually, experimental results of the laboratory model are presented to confirm the performance of the proposed converter, and this article is summarized in the last section.

II. Principle of Operation

In Fig. 1, the topology of the analyzed converter is depicted. The input circuit is composed of the magnetizing inductor L_m with a leakage inductor L_{Lk} and the transistor S. Primary and secondary windings of the coupled inductors, whose turns ratio is N_2/N_1, are wound on the same magnetic core. The passive regenerative snubber consists of the resonant capacitor C_r, and diodes D_{c1} and D_{c2}. Capacitor C_c is the switched capacitor. The output filter circuit is formed by the rectifier diode D and the filter capacitor C. The converter can work in two different modes, depending on the capacitor C_r charge state during transistor S turn-ON time. The theoretical waveforms shown in Fig. 2 present both the cases when capacitor C_r is fully discharged and when a certain amount of charge remains in capacitor C_r.

A different theoretical approach was applied depending on the charge remaining in the resonant capacitor C_r during transistor turn-ON. The condition that should be met to discharge the resonant capacitor is described in Section IV-B of this article. Fig. 3. Illustrates the converter topology with highlighted current flow paths through the components in different modes of operation during a single switching cycle T_S.

The following assumptions were made to simplify the theoretical analysis of the proposed converter: magnetic components are considered ideal apart from the leakage inductance of the tapped inductor; the current in the magnetizing inductance L_m in a single switching period is constant; the voltage drops on forward-biased diode D and resistance $R_{DS(ON)}$ of the transistors are neglected; parasitic parameters of all components are omitted; the voltages of capacitors C and C_c are constant during the single switching period.

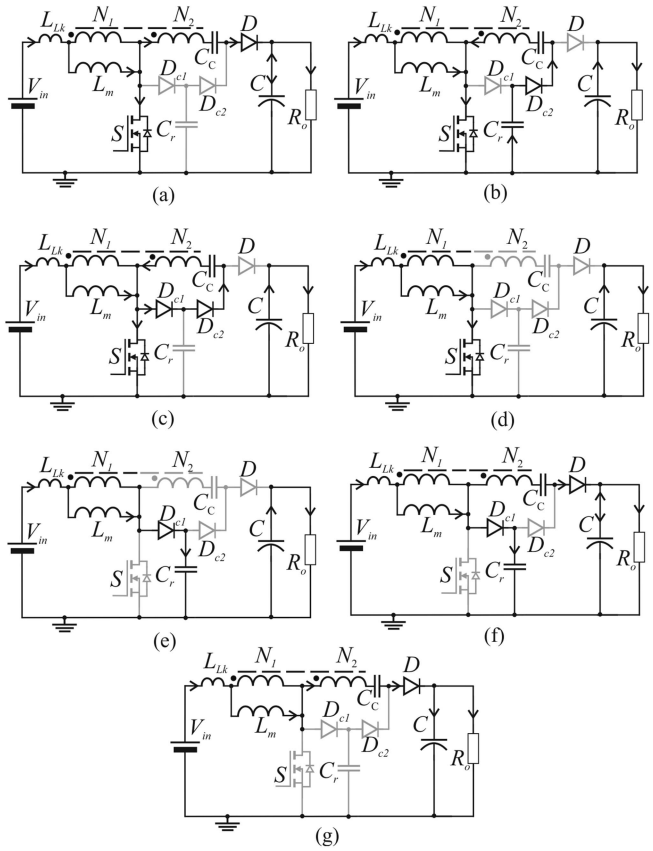

Fig. 3 Operation modes of the converter. (a) Mode 1. (b) Mode 2. (c) Mode 3. (d) Mode 4. (e) Mode 5. (f) Mode 6. (g) Mode 7.

Mode 1 [t_0–t_1, Fig. 3(a)]: For $t < t_0$, the current flows through the input voltage source V_{in}, the coupled inductor, capacitor C_{c}, diode D, and the load. At t_0 the transistor S turns ON and the diode D current decreases to 0, the transistor S current rises with a slope determined by the leakage inductance L_{Lk}. The energy is transferred from the input voltage source V_{in} to the inductor. In Mode 1, a voltage drop on the leakage inductance is equal

$$v_{\text{Lk}}(t-t_0) = \left(V_o - V_{Cc} + nV_{\text{in}}\right)/n. \tag{1}$$

The time span of Mode 1 covers the period when diode D current decreases from I_D to 0 and can be defined as

$$t_1 - t_0 = \left(nL_{\text{Lk}}I_D\right) / \left(v_{\text{Lk}}(t-t_0)\right). \tag{2}$$

Mode 2 [t_1–t_2, Fig. 3(b)]: Diode D is reverse-biased at t_1. The leakage inductance determines the slope of the diode's D current rise; it suppresses the reverse recovery current. The diode D_{C2} is forward-biased, and capacitor C_r discharges resonantly. The energy from the input voltage source V_{in} continues to be transferred to the coupled inductors. The capacitor C_c is charged while the transistor S remains ON. The input current and capacitor C_c current in Mode 1 are equal to

$$i_{\text{in}}(t) = I_{\text{in}} + \left(n^2 v_{\text{Lk}}(t_1)/Z_1\right)\sin\left(\omega_{r1}(t-t_1)\right) \tag{3}$$

$$i_{Cc}(t) = -\left(nv_{\text{Lk}}(t_1)/Z_1\right)\sin\left(\omega_{r1}(t-t_1)\right) \tag{4}$$

where $\omega_{r1} = 1/(n(L_{\text{Lk}}C_r)^{1/2})$ is the resonant pulsation and $Z_1 = n(L_{\text{Lk}}/C_r)^{1/2}$ is the resonant impedance. The voltages on the capacitor C_r and the leakage inductance L_{Lk} in Mode 2 are

$$v_{Cr}(t) = nv_{\text{Lk}}(t_1)\cos\left([\omega_{r1}(t-t_1)]\right) + V_{Cc} - nV_{\text{in}} \tag{5}$$

$$v_{\text{Lk}}(t_1) = \left(v_{Cr}(t_1) - V_{Cc} + nV_{\text{in}}\right)/n. \tag{6}$$

The voltage on the capacitor drops to 0 V at the end of the considered interval, leading to obtaining the ZVS condition. Based on (1) and (6), 0 V condition on capacitor C_r at time t_2 can be written as

$$\left(v_{Cr}(t_1) - V_{Cc} + nV_{\text{in}}\right)\cos\left(\omega_r(t_2-t_1)\right) + V_{Cc} - nV_{\text{in}} = 0. \tag{7}$$

Therefore, the considered interval is given by

$$t_2 - t_{1(a)} = a\cos\left(\frac{nV_{\text{in}} - V_{Cc}}{v_{Cr}(t_1) - V_{Cc} + nV_{\text{in}}}\right)\frac{1}{\omega_{r1}}. \tag{8}$$

If an otherwise certain amount of charge remains in the capacitor C_r during Mode 2, it determines the half-period discharge of capacitor C_r and is equal to $t_{3(\text{b})} - t_{1(\text{b})} = \pi/\omega_{r1}$.

Mode 3 [t_2–t_3, Fig. 3(c)]: Mode 3 occurs only if the capacitor C_r was completely discharged during Mode 2. At t_2, the diode D_{c1} is forward-biased, and the input current i_{in} decreases linearly down to the level of $I_D(n+1)$, whereas capacitor C_c is charged. In Mode 3, the current of coupled inductors' secondary windings i_{Cc} rises linearly

$$I_{\text{in}}(t_2) = I_D(n+1) + \left(n^2 v_{\text{Lk}}(t_1)/Z_1\right)\sin\left(\omega_{r1}(t_2 - t_{1(a)})\right) \tag{9}$$

$$i_{Cc}(t_2) = -\left(v_{\text{Lk}}(t_1)/Z_1\right)\sin\left(\omega_{r1}\left(t_2 - t_{1(a)}\right)\right). \tag{10}$$

Solving (10) leads to determining the span of Mode 3 (t_2–t_1)

$$t_{3(a)} - t_2 = L_{\text{Lk}}\left(i_{\text{in}}(t_2) - I_D(n+1)\right) / \left(-v_{\text{Lk}}(t-t_2)\right). \tag{11}$$

The voltage on the leakage inductance is accordingly equal

$$v_{\text{Lk}}(t-t_2) = \left(nV_{\text{in}} - V_{Cc}\right)/n. \tag{12}$$

Mode 4 [t_3–t_4, Fig. 3(d)]: In this mode, the energy is stored in a magnetic field of the coupled inductors. The current stops flowing through the secondary windings. In t_3, the diodes D_{C1} and D_{C2} are reverse-biased. Similarly, like in Mode 2, the leakage inductance suppresses their recovery currents.

Mode 5 [t_4–t_5, Fig. 3(e)]: The transistor S is turned-OFF at t_4. Forward-biased diode D_{c1} starts to conduct, and capacitor C_r is charged with constant current $i_{\text{in}}(t_1) = I_D(n+1)$, reaching the voltage level when diode D starts to conduct. If the capacitor C_r was completely discharged during Mode 3, the transistor S would turn-OFF at ZVS condition. The instantaneous voltage at t_5 can be defined as

$$v_{Cr}(t_5) = \left(V_o - V_{Cc} + nV_{\text{in}}\right) / \left(n+1\right). \tag{13}$$

If the capacitor C_r was completely discharged in Mode 3, the span of Mode 5 is given by

$$t_{5a} - t_{4a} = v_{Cr}(t_5)C_r / i_{\text{in}}(t_1) \tag{14}$$

and otherwise

$$t_{5b} - t_{4b} = C_r\left(v_{Cr}(t_5) - v_{Cr}(t_{4b})\right)/i_{\text{in}}(t_1). \tag{15}$$

Mode 6 *[t_5–t_6, Fig. 3(f)]:* In t_5, the diode D is forward-biased. The current of the diode D rises while both secondary windings current and capacitor C_r current decrease. Capacitor C_r is resonantly charged during a quarter of the resonance period. Thus, the time span of Mode 6 is equal

$$t_6 - t_5 = \pi n\sqrt{C_r L_{\mathrm{Lk}}}/\left(2n+2\right). \tag{16}$$

The instantaneous voltage of the capacitor C_r in t_6 transient is equal to its voltage at t_0 and t_1 transients

$$v_{Cr}(t_6) = v_{Cr}(t_0) = v_{Cr}(t_1) = v_{Cr}(t_5) + Z_2 I_D(n+1) \tag{17}$$

where $Z_2 = n(L_{\mathrm{Lk}}/C_r)^{1/2}/(n+1)$.

Mode 7 *[t_6–t_7, Fig. 3(g)]:* The energy stored in a magnetic field of the coupled inductors in Mode 7 is transferred to the output consisting of the capacitor C and the load resistance R_{o}.

III. Voltage Gain

A. Voltage Gain Formula When Capacitor C_{r} is Completely Discharged in Mode 2

In the converter, load current I_o is equal to the average current of diode D. Simultaneously, the average current of the capacitor C_c in a single switching period is constant at steady-state conditions and equal to 0. Consequently, in period $(t_{1(\mathrm{a})} < t < t_{3(\mathrm{a})})$, the average current of the capacitor C_c flows in the opposite direction than the current in period $(t_{5(\mathrm{a})} < t < t_7)$ and is equal to I_o.

The input current at transistor turn-ON is the sum of current $I_D(n+1)$ and a current that flows through capacitor C_c in a period of $(t_0 < t < t_{3\mathrm{a}})$ multiplied by the turns ratio of the tapped inductor given as:

$$\int_0^{DTs} i_{\mathrm{in}}(t)dt = I_D(n+1)DT_s - n\int_0^{t3(a)} i_{C_c}(t)dt \tag{18}$$

where T_S is a period of transistor driving signal and D is the duty cycle. Assuming that the input current within the period of $(t_{5(\mathrm{a})} < t < t_7)$ is equal to current I_D and is equal to the capacitor C_c current, the input current at transistor turn-OFF transient can be expressed as

$$\int_{DTs}^{Ts} i_{\mathrm{in}}(t)dt = I_D\left(n+1\right)\left(t_7 - t_6\right) - \int_0^{DTs}\left(i_{\mathrm{in}}(t)dt - I_D\left(n+1\right)\right). \tag{19}$$

Therefore based on (1)–(19), the voltage gain can be expressed as

$$G_{v(a)} = V_o/V_{\mathrm{in}} = I_{\mathrm{in}}/I_o = \left(f_s/f_{r1}\right)/\left(2\pi(1-D)^2\right) + \left(\sqrt{(n+1)^2 + \left(\frac{1}{2\pi\left(1-D\right)}\frac{f_s}{f_{r1}}\right)^2} + \frac{1}{\pi}\frac{R_o}{Z_1}\frac{f_s}{f_{r1}}\right)\Big/\left(1-D\right) \tag{20}$$

and V_{Cc} to V_o ratio can be thus resolved as

$$G_{Cc(a)} = V_{Cc}/V_o = \left(Z_1\left(n+1\right)/R_o + n\right)/G_{v1} + 1$$

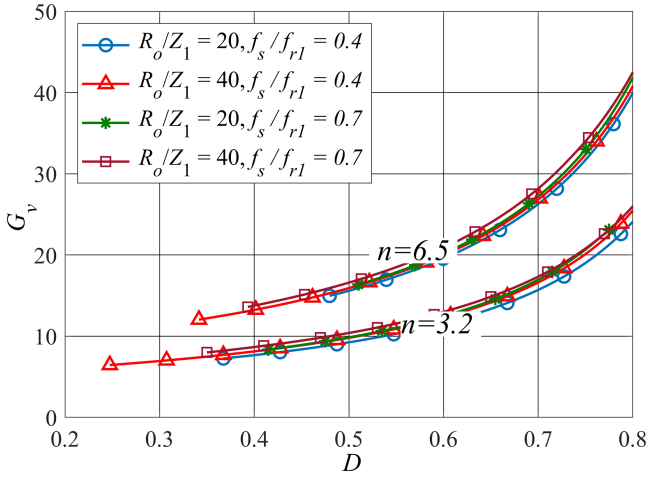

Fig. 4. Voltage gain of the proposed converter.

$$-2\pi(n+1)^2\frac{Z_1}{R_o}\frac{f_{r1}}{f_s}\left(\sqrt{\frac{(n+1)/G_{v1} + R_o/Z_1}{\pi(n+1)^2}\frac{f_s}{f_{r1}} + 1} - 1\right). \tag{21}$$

B. Voltage Gain Formula When Capacitor C_{r} is Not Completely Discharged in Mode 2

Assuming the average current of the capacitor C_r is equal to zero across a single switching period, the input current in the period of $(t_4 < t < t_6)$ is equal to I_o. The voltage gain formula can be determined by applying the output power to the input power proportion as

$$V_{\mathrm{in}}\int_0^{T_S} i_{\mathrm{in}}(t)dt = V_o\int_0^{T_S} i_D(t)dt \Rightarrow G_{v(b)} = \frac{n+2}{1-D}. \tag{22}$$

In the considered case, V_{Cc} to V_o ratio can be expressed as

$$G_{Cc(b)} = \frac{V_{Cc}}{V_o} = \frac{\frac{Z_1}{R_o}\left(G_{v(b)} - \pi\left(n+1\right)f_{r1}/f_s\right) + 1}{n+2} + \frac{n}{G_{v(b)}}. \tag{23}$$

Fig. 4 depicts the voltage gain in the function of duty cycle D at four different conditions, which are defined by two different values of f_s/f_r and R_o/Z_1 ratios accordingly. Analysis of Fig. 4 reveals that the voltage gain function is merely dependent on the parameters of the resonant circuit itself. Moreover, the load resistance change has a slight impact on the voltage gain providing steady operation of the proposed converter in a wide range of the output power.

IV. Soft Switching Condition

A. Diodes D_{c1}, D_{c2} Reverse Recovery Current Reduction

To minimize the power losses in the converter by lowering the maximum voltage across the switch S, transistor turn-ON time should be kept equal or higher than $(t_0 < t < t_3)$ period. In case of complete discharging of the capacitor C_r at Mode 2, neglecting a short period of $(t_0 < t < t_1)$, the minimal value of the duty

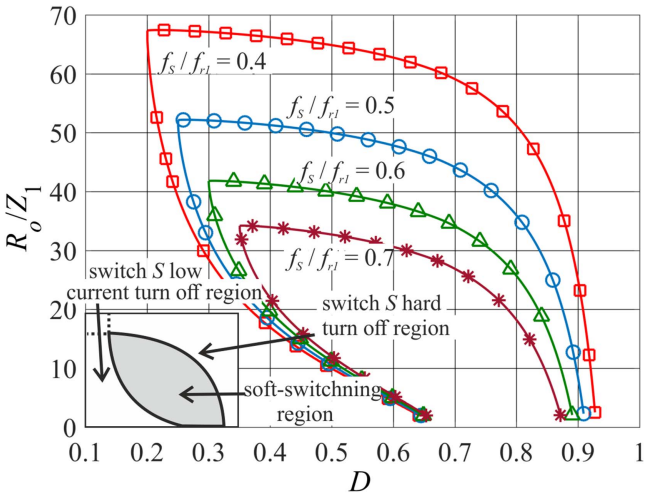

Fig. 5. Soft switching regions of the transistor ($n = 3.2$).

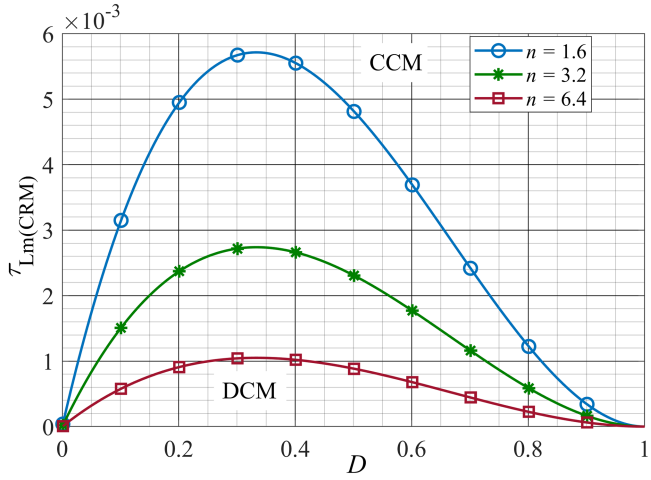

Fig. 6. Curves of the conduction mode of the proposed converter in function of the duty cycle.

cycle can be resolved as

$$D \geq \left(\frac{a\cos(\psi)}{2\pi}\right)\frac{f_s}{f_{r1}} + \frac{Z_1\left(I_{\text{in}}(t_2)/I_o - G_{v(a)}\right)}{2\pi R_o n\left(n/G_{v(a)} - G_{Cc(a)}\right)}\frac{f_s}{f_{r1}} \tag{24}$$

where

$$I_{\text{in}}(t_2) = \frac{I_o n R_o\,(n+2)\left(n - G_{Cc(a)}G_{v(a)}\right)\sqrt{1-\psi^2}}{G_{v(a)}Z_1\psi} + I_o G_{v(a)} \tag{25}$$

$$\psi = (n+1)\Big/\left(\frac{Z_1\left(G_{v(a)}+1\right)}{R_o\left(n/G_{v(a)} - G_{Cc(a)}\right)} + n + 2\right). \tag{26}$$

B. Zero Voltage Transistor Turn-off Region

The transistor can be turned-OFF at zero voltage only if the voltage of capacitor C_r is zero at the transistor turn-OFF transient. In this case, the capacitor C_{r} should be discharged in less than a half-wave of the resonant period. This condition is met when

$$2nv_{\text{Lk}}(t_1) > v_{Cr}(t_0). \tag{27}$$

Therefore, the condition can be expressed as

$$R_o/Z_1 \geq \pi f_{r1}\,(2n+3)\,/f_s - G_{v(b)}. \tag{28}$$

The condition (28) allows for determining soft-switching regions of the power devices, which are depicted in Fig. 5 for different operating points determined by four f_s/f_{r1} ratios. Analyzing Fig. 5, it is evident that to reduce the power losses in the converter, transistor S should be driven in a way to maintain the soft switching region. Fig. 5 shows that soft-switching operation is possible in a wide range of output power. Even if the converter works in the transistor's hard turn-OFF region at light loads (high values of R_{o}/Z_1 ratios, i.e., low output power), the switch turning-OFF voltage and switching losses remain low. The turn-OFF voltage of the transistor in the hard turn-OFF region (see Fig. 5) is equal to the capacitor C_r voltage at t_3 (see Figs. 2 and 3). Transistor turn-OFF voltage to the output voltage V_o ratio can be described by:

$$\frac{V_{DS(\text{turn\_OFF})}}{V_o} = \left((2n+3)\left(G_{Cc} - \frac{n}{G_v}\right) - G_v\frac{Z_1}{R_o} - 1\right)/(n+1)\,. \tag{29}$$

V. Conduction Mode

Operating under continuous conduction mode (CCM) is preferable for lowering input current ripple and reducing conduction losses in converter components. Simultaneously, operation under DCM allows achieving turning ON the transistor at zero voltage. However, thanks to leakage inductance, in CCM, the transistor is turning ON at zero currents. That is why, in the presented converter, DCM operation, for high-efficiency and high-frequency applications is not a necessity. In CRM, the maximum input current is two times higher than the average current in magnetizing inductance. In that case, to calculate the CRM region, which determines the region between DCM and CCM, input and output power should be compared

$$V_{\text{in}}\left(\frac{I_{Lm(\max)}D}{2} + I_o(n+2)\right) = V_{\text{out}}I_o \tag{30}$$

where $I_{\text{Lm(max)}} = (V_{\text{in}}/L_{\text{m}}) \times DT_{\text{S}}$.

Based on (30), CRM mode can be described as follows:

$$\tau_{Lm(\text{CRM})} = \frac{D(1-D)^2}{2(n+2)^2} \tag{31}$$

where $\tau_{Lm(\text{CRM})} = L_{\text{m}}/(R_{\text{o}}T_{\text{S}})$.

The curves presented in Fig. 6 can be useful to select a value of inductance for a specific switching period and output resistance.

VI. Power Devices

A. Voltage Stress

At t_6 the maximum voltage stress across the transistor S, which is equal to the maximum voltage on diode D_{c1}, is given by

$$V_{DS(\max)}/V_o = (G_v Z_1/R_o + n/G_v - G_{Cc} + 1)/(n+1)\,. \tag{32}$$

The maximum value of the diode D reverse voltage is equal to V_{out}, whereas the maximal reverse voltage of the diode D_{c1} is in the $(t_0 < t < t_1)$ period. Normalized voltage stress of the diode can be defined as

$$V_{Dc2(\max)}/V_o = (n + G_{Cc} - n/G_v)/(n+1)\,. \tag{33}$$

B. Current Stress

The RMS values of the transistor S current, the input current I_{in}, secondary windings' current I_{Cc}, and diode D_{c1} average current are given in (2)–(40), and they were determined presuming $2nv_{\text{Lk}}(t_1) = v_{Cr}(t_0)$, with the assumption of the transistor S working in the boundary region of soft-switching.

$$I_{D(\text{RMS})} = \frac{I_o G_{v(b)}}{n+1}\sqrt{\frac{(2-\pi)}{4\pi\,(n+1)}\frac{f_s}{f_{r1}} + \frac{n+1}{G_{v(b)}}} \tag{34}$$

$$I_{\text{in(RMS)}} = I_o\sqrt{\begin{array}{l}\frac{G_{v(b)}^2}{8\pi(n+1)}\left(\frac{2(2-\pi)}{(n+1)^2}+\pi-4\right)\frac{f_s}{f_{r1}} \\ +\left(\frac{\pi n}{2}\right)^2\frac{f_{r1}}{f_s}+G_{v(b)}\left(G_{v(b)}+n-1+\frac{1}{n+1}\right)\end{array}} \tag{35}$$

$$I_{Cc(\text{RMS})} = I_o\sqrt{\frac{\pi^2}{4}\frac{f_{r1}}{f_s} + \left(\frac{G_{v(b)}^2\,(2-\pi)}{4\pi(n+1)^3}\frac{f_s}{f_{r1}}\right) + \frac{G_{v(b)}}{n+1}} \tag{36}$$

$$I_{S(\text{RMS})} = I_o\sqrt{(\pi\,(n+1)\,/2)^2 f_{r1}/f_s + G_{v(b)}\left(G_{v(b)}+n\right)} \tag{37}$$

$$I_{\text{Dc1(RMS)}} = I_o G_{v(b)}\sqrt{\frac{(\pi-4)}{8\pi\,(n+1)}\frac{f_s}{f_{r1}} + \frac{1}{G_{v(b)}}} \tag{38}$$

$$I_{\text{Dc2(RMS)}} = I_o\pi\sqrt{f_{r1}/f_s}/2 \tag{39}$$

$$I_{\text{Dc1(AV)}} = I_{\text{Dc2(AV)}} = I_{\text{D(AV)}} = I_o. \tag{40}$$

VII. Experimental Verification

A. Laboratory Model of the Converter

To verify the theoretical considerations, the laboratory model of the proposed converter was developed and tested (see Fig. 7). Table I collates the main parameters of the converter as well as its component list.

The dimensions of the converter laboratory model are 54 mm × 75 mm × 53 mm. The high power density of 14 kW/dm^3 was achieved thanks to the high switching frequency (f_s = 200 kHz). The converter operates in an open-loop system.

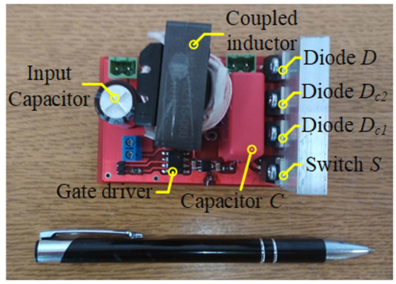

Fig. 7. Photography of the laboratory model.

TABLE I
Parameters and Component Selection of the Laboratory Model

Parameter	Value
Input voltage V_{in}	(30–50) V
Output voltage V_{out}	380 V
Switching frequency f_s	200 kHz
Rated output power P_{out}	300 W
Coupled inductor L_m	24 μH, EMS-432115 - 60 core, turns ratio n = 3.2 (42:13)
Resonance tank capacitor C_r	19.8 nF (9 COG 2,2 nF capacitors)
Resonant frequency f_{rl}	287 kHz
Leakage inductance L_{LK}	1.48 μH
Resonance impedance Z_1	27.7 Ω
Output capacitance C	1 μF
Input capacitance	10 μF
Capacitance C_{C}	2.2 μF
Transistor S	AOT2500L
Diodes D, D_{c2}	C3D06060A
Diode D_{c1}	MBR20200
Gate driver	TC4451 (0–12) V

The converter transistor is controlled via TC4451 gate driver, with the power supply voltage at 0–12 V.

B. Coupled Inductor

The design of the tapped inductor was based on an E-shape Sendust magnetic core, which was developed to work with the switching frequency range of hundreds of kHz. To determine the power losses of the magnetic core, current ripples of the magnetizing inductance L_m, and the peak input current were calculated as $\Delta I_{\text{Lm}} = 5.3$ A and $I_{\text{in\_peak}} = 10.5$ A assuming: $V_{\text{in}} = 50$ V, $G_{v1} = 7.6$, $\eta = 0.9$, $f_s = 200$ kHz, and $R_{o(\min)} = 480\,\Omega$. For a given input current ripple, L_m is designed for 24 μH. Primary and secondary windings were wound on the core with Litz wire. Their effective cross-sections were 2.12 mm^2 and 071 mm^2, respectively. For high-gain converters, one of the major concerns related to high efficiency is to minimize primary winding's RMS conduction losses. To meet this requirement, primary windings of coupled inductors were designed to have a low resistance of 12 mΩ. The turns ratio of 3.2 was dictated by two constraints. The first one is the required voltage gain (see Fig. 4), which ensures the output voltage of 380 V and the range of duty ratio of 0.3 to 0.6 to cover the whole input voltage range. The second constraint is to ensure proper work in the soft switching region (see Fig. 5).

C. Resonant Circuit

To minimize the RMS currents in the converter components, the resonant frequency should be as low as possible but higher than $1/(t_7–t_4)$, which is reciprocal of the transistor turn-OFF time. Based on Fig. 5 and considering the converter's parameters, frequency $f_s/f_{r1} = 0.7$ was selected. Resonant impedance affects the maximum voltage stress of the transistor but, on the other hand, decreases the range of the output power where the transistor is soft-switched while turning OFF. The assumption was made to achieve full soft switching of the transistor for 50% of the output power and beyond, which corresponds to the resonant impedance Z_1 equal to 27.7 Ω. The parameters of the resonant circuit were calculated based on the selected resonant frequency and resonant impedance. The leakage inductance was 1.48 μH, and the capacitance of the resonant tank was 19.8 nF. In the proposed circuit, a relatively high coupling coefficient allowed for the utilization of the leakage inductance, whereas in the conventional circuits, another magnetic component would need to be used, increasing the overall component count of the converter.

D. Capacitors

The capacitance of the capacitors C_c and C should be as low as possible; on the other hand, low capacitance has an impact on the voltage ripples, especially regarding the output capacitor C. Assuming constant output current I_o during one switching cycle, and based on the analysis of the capacitor C_C current when the transistor is turned-OFF, voltage ripples on capacitor C_C can be described as follows:

$$\Delta V_{Cc} = \frac{I_D}{C_C} T_S\,(1-D) = \frac{I_o}{C_C} T_S. \tag{41}$$

To calculate the voltage ripples on capacitor C, considering interval t_0–t_6, and assuming the square shape of the input current in interval t_4–t_6

$$\Delta V_C = \frac{I_o(T_S D - (t_6 - t_4))}{C} = \frac{I_o T_S (G_v - n - 1)}{G_V C}. \tag{42}$$

where t_6–$t_4 = T_S/G_V$.

According to (41) and (42), the maximum voltage ripple on capacitor C_C for data presented in Table I is around 1.8 V, whereas the maximum voltage ripple on capacitor C is around 2.6 V.

E. Experimental Results

The experimental waveforms of the proposed converter were captured to confirm the theoretical considerations. The experimental tests were carried out from 75 W to 300 W of the output power for three different input voltages of 30 V, 40 V, and 50 V at constant $V_{out} = 380$ V. The converter operates outside the soft-switching region ($f_s/f_{r1} = 0.7$ curves in Fig. 5) for the output power of around 160 W and below. For higher power (i.e., 200 W and 300 W), the transistor is turned-OFF at zero voltage; thus, the operating point of the converter is located within the soft-switching region. According to the theoretical assumptions, transistor S is turned on at zero current and turned-OFF at zero voltage. At the rated power (300 W), the peak transistor steady-state voltage was around 120 V. Fig. 8 shows the waveforms of the converter working under $V_{in} = 40$ V and three different output power $P_{out} = 100$ W, 200 W, and 300 W. The waveforms for $P_{out} = 200$ W and $P_{out} = 300$ W show transistor soft-switching operation when the transistor S is soft-switched at zero-voltage. Waveforms shown in Fig. 8(a)–(c) in show diode D transient waveforms in its soft-switching mode of operation. In the steady state, while the diode is reverse-biased, the maximum reverse voltage approaches the output voltage. Fig. 9 presents the calculated power loss distribution at full load conditions. In the proposed converter, conduction losses caused by RMS currents are dominant power losses. The power loss breakdown outlines that at the rated output power, around 43% of power is dissipated within the coupled inductors. It can be noted that the remaining 57% of losses are more equally distributed between all switching components (11% to 16%). With this approach, total power losses reach 6.33 W at full load. Power losses in converter components presented in Fig. 9 were calculated based on the (34)–(40), and using $I_{x(RMS)}{}^2 R_x$ relation for the transistors and the inductors; and $I_{x(RMS)}{}^2 R_x + I_{x(AV)} V_{x(F)}$ for the diodes. The parameters of the components are as follows: transistor on-resistance $R_{DS(ON)} = 9.1$ mΩ, coupled inductor primary winding resistance $R_{PW} = 12$ mΩ, secondary winding resistance $R_{SW} = 100$ mΩ, diode D_{c1} series resistance $R_{Dc1} = 40$ mΩ forward voltage $V_{F(Dc1)} = 0.6$ V and diode D_{c2} and D series resistance $R_{Dc2,D} = 128$ mΩ and forward voltage $V_{F(Dc2,\,D)} = 0.9$ V. For the power semiconductors, the data have been collected on the basis on the datasheets for the temperature of 75 °C. Losses in the core of the coupled inductor were calculated using Oliver's formula, the calculated ripples in the magnetizing inductance are $\Delta I_{Lm} = 3.8$ A, and the core data from the datasheet.

VIII. Performance Comparison

Table II contains the comparison of the proposed converter with six other topologies with coupled inductors. Converters described in [15] and [16] have the same topology as the converter presented in this article, however, in [15] and [16] the capacitance of the clamps capacitors is much higher than in the proposed converter. Thus, it causes a low voltage ripple on capacitor C_r; the transistor turn-OFF voltage is higher than $V_{in}/(1 - D)$, and a transistor is hard turned-OFF. On the other hand, in the proposed converter, the resonant capacitor is completely discharged at the soft-switching region (see Fig. 5), which allows the transistor to be turned-OFF at zero voltage. Resonant operation increases the maximum voltage on capacitor C_r which also increases the maximum voltage on the transistor. However, the voltage increase is slight, and the proposed converter is free of transistor voltage spikes during turning OFF. In other converters described in the literature [5], [8], [15], the voltage ripples across the clamp capacitor are low, and the transistor is hard turning OFF and thus exhibits substantial voltage overshoots. In the proposed converter, switching losses are decreased due to the reduction of transistor turn-OFF voltage. The overall percentage of transistor power loss (16%) is significantly smaller

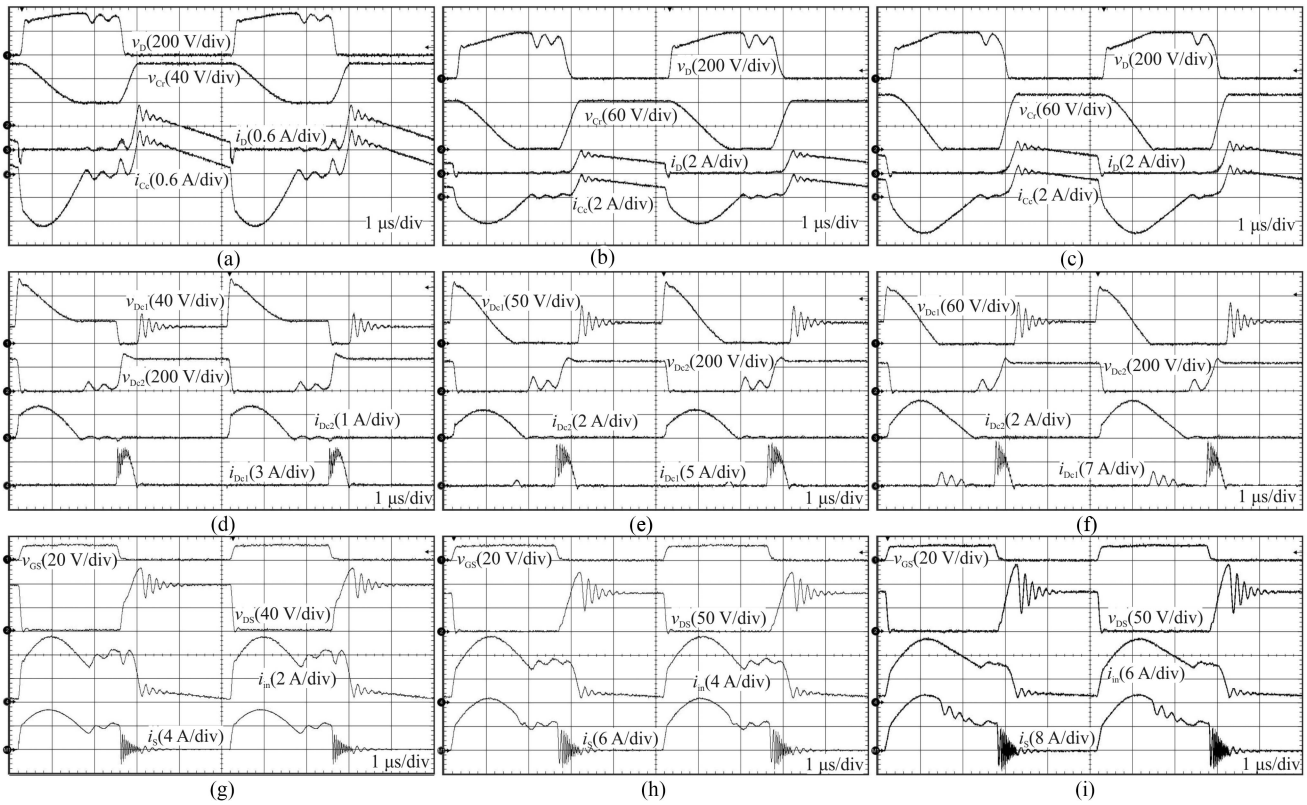

Fig. 8. Typical waveforms at $V_{\text{in}} = 40\,\text{V}$ and P_{out} of (a), (d), and (g) –100 W, (b), (e), and (h) –200 W, (c), (f), and (i) –300 W.

TABLE II
PERFORMANCE COMPARISON

Converter	Converter in [15]	Converter in [5]	Converter in [8]	Converter in [21]	Converter in [22]	Converter in [29]	Proposed converter
T / D / C / SI / 2WCI / 3WCI	1/3/3/0/1/0	1/3/3/0/1/0	1/5/5/0/1/0	4/6//8/0/2/0	2/3/5/1/1/0	1/4/5/1/0/1	1/3/3/0/1/0
Voltage gain	$\frac{n+2}{1-D}$	$\frac{n+1}{1-D}$	$\frac{n+3}{1-D}$	$\frac{7-D}{1-D}$	$\frac{n+2+D(n-1)}{1-D}$	$\frac{n_1+1+D}{(1-n_1)(1-D)}$	$\frac{n+2}{1-D}$
Voltage stress of the main active switch	$\frac{V_o}{n+2}$	$\frac{V_o}{n+1}$	$\frac{V_o}{n+3}$	$\frac{V_o}{1-D}$	$\frac{V_o}{n+2+D(n-1)}$	$\frac{V_o(1-n_2)}{n_1+1+D}$	$> \frac{V_o}{n+2}$
Voltage stress of the output diode	V_o	$\frac{nV_o}{n+1}$	V_o	$\frac{2V_o}{1-D}$	$\frac{V_o(n+1)}{n+2+D(n-1)}$	$\frac{V_o(n_1+1)}{n_1+1+D}$	V_o
Turn-ON condition of the active switch	ZCS	ZCS	ZCS	ZVS	ZVS	ZVS	**ZCS**
Turn-OFF condition of the active switch	hard	hard	hard	hard	hard	hard	**ZVS**
Reported switching frequency [kHz]	100	90	100	50	70	50	**200**
Maximum output power [W]	400	400	200	768	250	200	**300**
Reported peak efficiency [%]	97.4	97.5	97.1	98.5	96.8	98.34	**96.9**
Efficiency [%] and voltage gain [V/V] at nominal output power	96,4 16	96.5 8.3	96.4 8.3	94.8 10	93.8 14.3	95.93 10.6	**96.4** **7.6**
Used techniques	VM, PC	VM, PC	3×VM, PC	4×VM, 2×AC	2×VM, AC, *RC*	3×VM, PC	VM, **RPC**

T: power transistors, D: power diodes, C: capacitors, SI: single inductor, CI: coupled inductor, 2WCI: two-windings coupled inductor, 3WCI: three windings coupled, VM: voltage multiplier cell, *RC* – resonant cell, PC - passive clamp, AC – active clamp, RPC – resonant passive clamp.

in the presented converter (see Fig. 9) than in the hard-switched converter in [16], where it is 28%. The converter described in [15], unlike [16], includes an efficiency-oriented design, which is why that reference is listed in Table II. Besides, the converter in [15] achieved high efficiency at wide input voltage and output power, even compared to its newer counterparts. This is due to using a coupled inductor with high volume on the EE-55 core, which allows for reduced losses in the core and inductor wire. Furthermore, the high volume of the inductor made it possible to obtain a high turns ratio and, as a consequence, to reduce the duty ratio and maximum voltage of the transistor, as well as improve the efficiency. Additionally, the capacitance values were much higher.

Fig. 10 presents the results of efficiency measurement at the output voltage of 380 V and three different values of the input voltage: 30 V, 40 V, and 50 V. Efficiency was measured for the

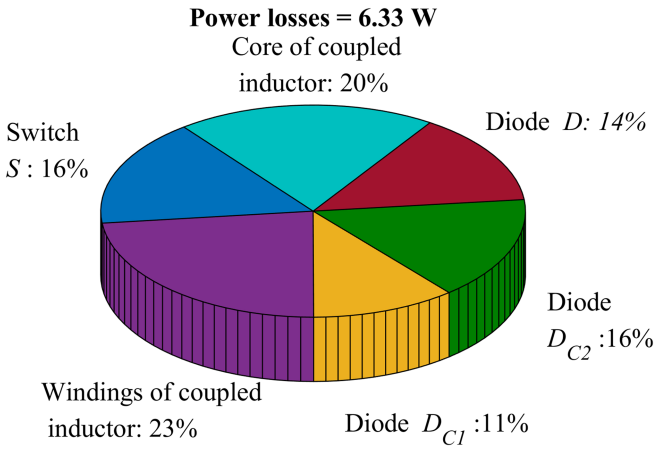

Fig. 9. Power losses in the converter's components at $P_o = 300\,\text{W}$ and $V_{\text{in}} = 40\,\text{V}$.

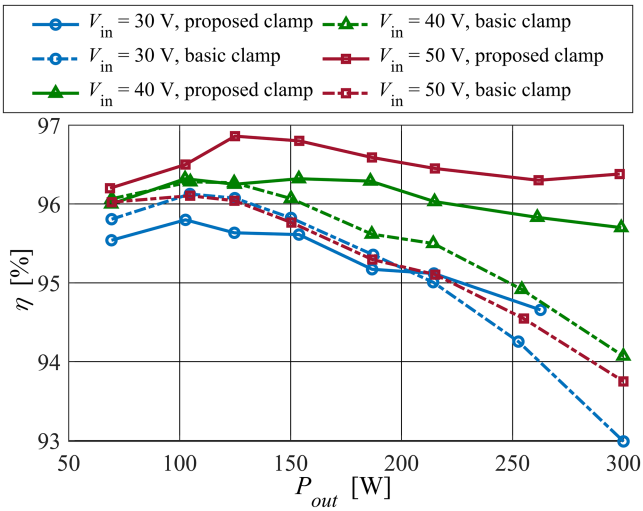

Fig. 10. Efficiency of the converter with basic clamp and proposed resonant clamp circuits.

proposed clamp circuit and a basic clamp [15] using the same converter and adding 4.7 μF film capacitor in parallel to C_{r}. The comparison was made to verify the efficiency improvement by using the proposed resonant clamp technique. The switching frequency is the same for both cases ($f_{\text{s}} = 200\,\text{kHz}$). For the proposed resonant clamp circuit, the peak efficiency $\eta = 96.9\%$ was reported at the output power of around 125 W and the input voltage $V_{\text{in}} = 50$ V. The lowest efficiency was 94.7% at the output power of 265 W and input voltage $V_{\text{in}} = 30$ V. When the efficiency between the proposed and conventional clamp circuits is compared; it can be seen that the efficiency of the proposed clamp circuit is much higher. E.g. for 40 V and maximum output power, the measured efficiency of the converter with resonant clamp is 96.4%, whereas for the basic clamp, it is just 94.1%. This is mostly caused by better turn-OFF transistor conditions, thanks to using the resonant operation of clamp capacitor C_{r}. Only for input voltage $V_{\text{in}} = 30\,\text{V}$ and power lower than 200 W the efficiency of the converter with a basic clamp is slightly higher than the case with the proposed resonant clamp circuit. The difference does not exceed 0.5 p.p.

The converter described in [5] consists of a similar structure with a passive clamp circuit to the one presented in the paper and exhibits the same component count. However, the components of the converter are connected differently, which reduces its voltage gain to (n + 1)/(1−D) instead of (n + 2)/(1−D) as in the case of the proposed converter. In the converter from [5], capacitor C_{r} forms the resonant circuit with the leakage inductance. That allows for a quasi-sinusoidal shape of the transistor current and windings of the coupled inductor, which reduces transistor and inductor current stresses and transistor turning-OFF current. However, in [5], unlike in the proposed solution, the resonant operation has little effect on the clamp capacitor voltage ripple. Therefore, the transistor is hard to turn-OFF, which significantly increases converter switching losses compared to the proposed resonant passive clamp circuit. The converter in [5] achieved higher efficiency compared to the presented solution primarily because of two reasons. First, in [5], the converter is controlled with a much lower frequency of 90 kHz compared to 200 kHz in the presented prototype, which reduces switching losses, especially transistor turning-OFF losses, and also minimizes the losses in the inductor core. Second, in [5], a more expensive transistor (IRFP4668PBF with $V_{\text{DSS}} = 200$) was used than in the presented solution (AOT2500L with $V_{\text{DSS}} = 150$), which enables the use of a transistor with higher V_{DSS} voltage at similar $R_{\text{DS(ON)}}$. Therefore, a coupled inductor with a much lower turn ratio of 1.72 could have been used in [5], despite the fact that output and input voltages are very similar for both cases. A lower turn ratio of the coupled inductor results in lower resistance of the inductor wire, lower root-mean-square current in the converter components, and the possibility of using a smaller core. Yet, as was mentioned, it comes at the cost of higher transistor voltage.

Overall, despite switching the transistor with a much higher frequency and using a worse transistor in the proposed solution, the difference in efficiency is minor. This is due to employing the proposed novel resonant clamp technique with a completely discharged clamp capacitor, eliminating the turning-OFF losses. The maximum output power of the converter in [5] is 400 W and is higher by 100 W compared to the prototype presented in this article. For 300 W operation, the efficiency of the converter in [5] is higher by 0.5% for the established maximum input voltages. Additionally, using a higher switching frequency enables the use of smaller passive components and improves the power density of the converter. The dimension base of the proposed converter is 54 mm × 75 mm, whereas for the converter in [5], it is 110 mm × 107 mm, which is a substantial improvement.

The converter described in [8] achieved a high efficiency of 96.4% at nominal output power. However, the circuit consists of two additional multiplier cells with two additional capacitors and two additional diodes; this is why the circuit is characterized by a higher voltage gain. However, voltage gain is only slightly higher, despite the fact that two additional voltage multiplier cells are used, which makes the converter less competitive to the proposed circuit. Furthermore, the efficiency of the converter is high. However, it is caused by using a transistor with a very high current rating of 300 A (very low $R_{\text{DS(ON)}}$) with a low output

power of 200 W, as well as two times lower switching frequency than in the presented converter (equal to 100 kHz).

In [21], an interleaved converter with an active clamp along with a voltage multiplier cell is presented. Thanks to using an interleaved structure, high output power 768 W was achieved, despite using an active clamp with an additional clamping transistor. The obtained efficiency at nominal output power is not higher than in the converter with the passive clamp. This is due to the fact that in all converters with coupled inductors, thanks to the leakage inductance, the transistor is turning ON at zero current. Thus, using a zero-voltage technique reduces the switching losses slightly. A main advantage of such a structure is the low input current ripple, which is an advantage of all interleaved converters.

The converter presented in [22] consists of an additional inductor at the input to reduce the input current ripples. Besides, a two-winding coupled inductor, two voltage multiplier cells, and an active clamp are used in the circuit. Moreover, a resonant technique to reduce switching losses is employed. Such a circuit is highly complicated and consists of many components; however, the voltage gain is high. The converter achieved a maximum efficiency of 93.8% at nominal output power $P_o = 250$ W despite low switching frequency.

In [29], a converter with a three-winding coupled inductor, voltage multiplier cells, and an additional input inductor, is presented. Using a three-winding coupled inductor increases the voltage gain; however, the circuit requires an additional voltage multiplier cell for proper operation, which increases the component count. The converter at the nominal output power of 200 W and voltage gain of around 10.5 achieved a lower converter efficiency of 95.5% than the proposed converter, despite that the switching frequency was four times lower and equal to 50 kHz.

The converter presented in this article and those in [5], [8], and [15] are characterized by high input current ripple. Input current ripple can be lowered by using an interleaving structure [21] or an additional input inductor [22], [29]. In both methods, the component count is increased, and the converter becomes more complex and with reduced efficiency. In the presented converter and in [5], [8], and [15], the input current ripple can be reduced by using an additional *LC* filter at the input. The volume of such an input filter depends on the power, input current ripple, and switching frequency. In such a type of structure, the input current ripple can be lowered by using a coupled inductor with a lower turn ratio. To achieve high voltage gain with a low turn ratio, more voltage multiplier cell structures must be used, like in [8], which again increases the component count.

The presented converter and the converters described in [5] and [15] are characterized by the same component count. Furthermore, the clamp circuit in [5] is also resonant, akin to the proposed solution. That is why a more accurate, general comparison of the presented converter with the proposed resonant passive clamp against a clamp in converter [5] and [15] is carried out.

Fig. 11 shows a comparison of the input current and clamp capacitor voltage transient shape in the proposed converter with the converters described in [5] and [15]. Comparison is made assuming that the transistor duty ratio, output, and magnetizing

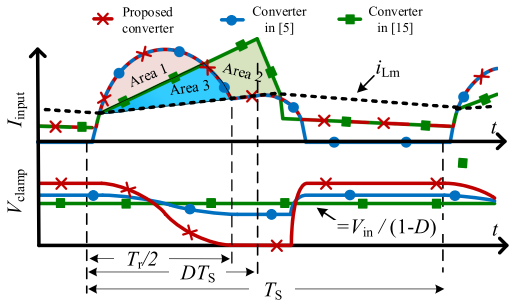

Fig. 11. Comparison of the input current and voltage across the clamp capacitor for the proposed converter and converters in [5] and [15].

currents are the same and converters operate in CCM. Following the waveforms in Fig. 11, input current ripples were determined in the three compared converters, assuming equal input and output conditions and equal resonant frequency for the proposed converter and the converter shown in [5]. To determine the input current ripple, it can be assumed that Area 1 and Area 2 in Fig. 11 are equal, and (Area 1 + Area 2)/T_S = (Area 1 + Area 3)/T_S = nI_o. The input current ripple in each considered converter is substantial due to the use of a coupled inductor. The input current ripple in the converter with the proposed resonant clamp circuit can be described as

$$\Delta i_{\text{in\_prc}} = I_o \left[\left(G_v + \frac{V_o^2 (n - G_v + 2)}{2P_{\text{out}} G_v^2 f_s L_m} \right) \frac{n-1}{n} + \frac{V_o^2}{4P_{\text{out}} G_v^2 f_s L_m} \frac{f_s}{f_{r1}} + \pi n \frac{f_{r1}}{f_s} \right]. \quad (43)$$

The input current ripple in [15] can be described as

$$\Delta i_{\text{in\_bc}} = I_o \left(\frac{2nG_v}{G_v - n - 2} + \frac{G_v (n-1)}{n} + \frac{V_o^2 (n+1)(G_v - n - 2)}{2G_v^2 P_{\text{out}} f_s L_m n} \right). \quad (44)$$

The input current ripple of the converter in [5] can be described as

$$\Delta i_{\text{in\_brc}} = I_o \left(\frac{V_o^2 \left(2(n+1) + G_v (f_s/f_r - 2)\right)}{4P_{\text{out}} G_v^2 f_s L_m} + \pi n \frac{f_r}{f_s} + G_v \right). \quad (45)$$

An input filter is a necessity to apply the proposed converter for renewable energy applications since the current ripples are notable. Still, as can be seen in Fig. 12, the input current ripple of the converter with the basic clamp circuit [15] is higher than in the proposed converter and the converter described in [5]. It is due to a quasi-resonant shape of input current during turning ON the transistor in both solutions. Ripples of the proposed converter and the converter described in [5] are similar, but still somewhat lower in the proposed solution for the nominal conditions. Overall, using the resonant passive clamp circuit reduces the input current ripples, which makes it possible to use an input current filter of lower volume, and renders this solution

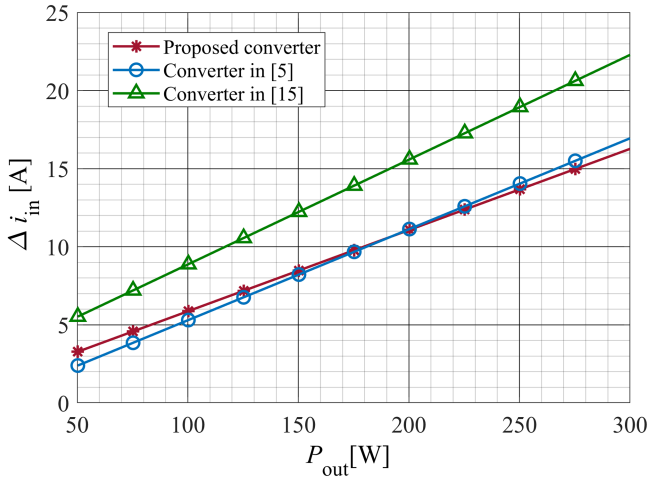

Fig. 12. Comparison of input current ripples (n = 3.2, $V_{\rm in}$ = 40 V, $V_{\rm o}$ = 380 V, $f_{\rm S}$ = 200 kHz, $L_{\rm m}$ = 24 μH, $f_{\rm S}/f_{\rm r1}$ = 0.69) for the proposed converter, and converters in [5] and [15].

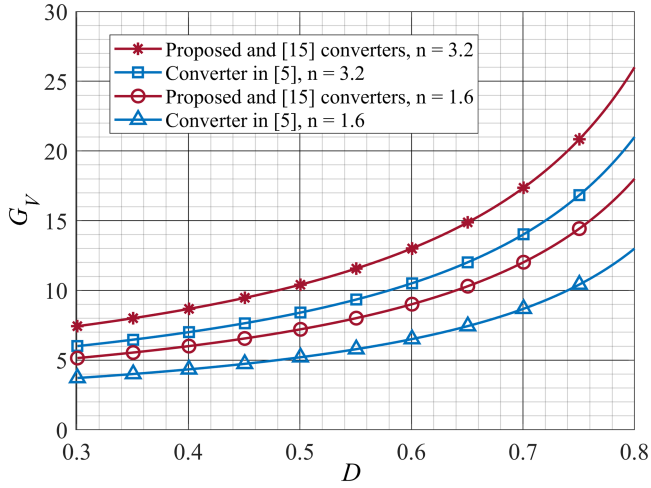

Fig. 13. Comparison of voltage gain of the proposed converter and the converters in [5] and [15].

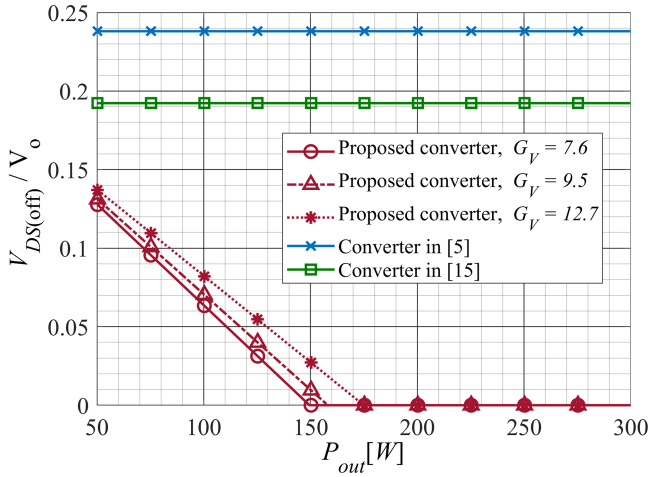

Fig. 14. Comparison of transistor turn-OFF voltage for the proposed converter (n = 3.2, Z_1 = 27.5, f_S/f_{r1} = 0.69, $V_{\rm o}$ = 380 V) and the converters in [5] and [15].

superior to its counterparts. Furthermore, when the capacitors and their voltage ripples are considered, the proposed converter also shows advantages. In all the converters from the references, as well as in the proposed converter, the capacitors are charged and discharged alternately at the time when the transistor is either ON or OFF. Moreover, the mean currents of the capacitors during the turning-ON and/or turning-OFF of the transistor are proportional to the output current. Therefore, the voltage ripples on the capacitors are mainly bound to the switching frequency and the capacitance values. Since in the proposed converter, the operating frequency is higher; it is possible to achieve lower voltage ripples than in the converter with another clamp circuit [5], [15] operating with a lower frequency. Thus, it can be assumed that the capacitor voltage ripples are generally lower in the proposed converter.

As can be seen in Fig. 11, a significant part of the time when the transistor of the converter described in [5] is on, in opposite to the presented solution and the converter described in [15], the input current is equal to 0. Thus, the voltage gain of the converter in [5] is lower. A comparison of the voltage gain of the three analyzed converters is shown in Fig. 13. The impact of the resonant impedance and output resistance on the voltage gain formula in the proposed converter is minimal (see Fig. 4), and thus it has been omitted. To achieve the same voltage gain of the converter in [5] as in the presented converter, the transistor must be controlled with a higher duty ratio. Simultaneously, the maximum voltage across the transistor in [5] during turning OFF, omitting the overshoots, is equal to $V_{\rm in}/(1 - D)$; higher voltage gain increases the maximum voltage on the transistor. On the other hand, in the presented converter, the maximum voltage across the transistor is increased due to the resonance after turning OFF the transistor (see Fig. 2, t_5–t_6). However, that voltage increase is not significant, and since the transistor is turned OFF at zero voltage, there is no additional voltage via overshoots. In contrast, in [5] and [15], transistors are hard to turn-OFF, which in reality leads to increases in maximum voltage through voltage spikes and might require using additional *RC* snubbers to suppress those overshoots.

Fig. 14 collates the comparison based on the theoretical calculations of the transistor turn-OFF voltage for three different values of voltage gain G_v as the function of output power $P_{\rm o}$. The comparison was made for the three considered converters. For the proposed converter, the turn-OFF voltage remains 0 V at the range below around 50% of the rated output power. For higher output power, it is more than two times lower compared to the other compared converters. Therefore, a passive clamp helps to alleviate the turn-OFF voltage stress of the transistor, which also affects the turn-OFF switching power losses. Please note, that in the case of the converter in [5], it was assumed that the transistor turning-OFF voltage of the converter with the resonant clamp circuit presented in [5] is equal to $V_{\rm in}/(1- D)$, as even though $V_{\rm DS(OFF)}$ is equal to the clamp capacitor voltage during the turning OFF of the transistor, and the clamp

capacitor resonates with the leakage inductance, which increases V_{DS}(OFF) voltage. However, the resonant impedance of that resonant circuit, due to high capacitance, is very low compared to the presented converter. Thus, the voltage ripple across the clamp is low, and its impact on $V_{\mathrm{DS(OFF)}}$ may be omitted.

According to Figs. 11 and 14, the turn-OFF current and voltage in [15], and turn-OFF voltage in [5], are much higher than in the proposed solution, which affects the power losses in a great manner, especially for high-frequency operation. Thus, in that regard, the proposed converter seems to be the superior solution.

In summary, utilizing the resonant operation while turning ON the transistor has no negative impact on its conduction losses. Moreover, RMS currents in the components remain low. All diodes are turned-OFF at zero current. Transistor turn- OFF voltage is zero in the soft switching region and much lower than in [15] and [16] in the hard switching region (see Fig. 5). The proposed converter achieved similar efficiency and voltage gain to the converter described in [5], however, in the presented converter with resonant passive clamp, the resonant frequency is 200 kHz versus 90 kHz [5]. As a consequence, the dimensions of the proposed converter are much lower. Similar parameters were also achieved for the converter presented in [8]. However, its maximum output power is lower (200 W), and an additional voltage multiplier cell and a transistor with very high current ratings are used.

Compared to all its counterparts, the proposed converter is distinguished by the following.

1) Reduced transistor switching losses, possibility to operate with the higher switching frequency thanks to transistor turning OFF at zero voltage and turning ON at zero current.
2) Leakage inductance is incorporated into the resonant tank.
3) Merely equal power loss distribution across the active components predestines the proposed converter to apply in high power density designs.
4) Improved efficiency compared to conventional clamping circuit.
5) Full soft switching of all converter switches.

IX. Conclusion

This article presents and discusses a novel approach to utilize the resonant features of the passive clamp circuit in a PWM boost converter with a coupled inductor and switched capacitor. The new resonant clamp circuit enables zero-voltage turn-OFF of the transistor and improves efficiency compared to known clamp circuits described in the literature. Detailed mathematical analysis and the characterization of operation principles of the proposed converter with an appropriate selection of the converter components are presented in the article.

Mathematic analysis was verified on the 300-W laboratory model of the converter, achieving a high efficiency of 96.9% with 200 kHz of switching frequency and even power loss distribution across the active components.

In conclusion, the proposed high-power density and high-efficiency soft-switching topology of the dc–dc converter allows efficient utilization of the power components, is robust to the output power variation, and is a worthy competitor to other state-of-the-art converters.

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Michał Harasimczuk (Member, IEEE) was born in Białystok, Poland. He received the M.Sc. and Ph.D. degrees in electrical engineering from the Bialystok University of Technology, Bialystok, Poland, in 2013 and 2019, respectively.

From 2020 to 2023, he was with the Warsaw University of Technology, Warsaw, Poland. He is currently with the Faculty of Electrical Engineering, Bialystok University of Technology. His research interests include power electronics, namely dc–dc soft-switching converters, multilevel converters, SiC-based converters, and ac–dc converters.

Rafał Kopacz (Graduate Student Member, IEEE) received the B.Sc. and M.Sc. degrees in electrical engineering, in 2018 and 2019, respectively, from the Warsaw University of Technology, Warsaw, Poland, where he is currently working toward the Ph.D. degree in power electronics.

He was a visiting Researcher with SINTEF Energy and Norwegian University of Science and Technology, Trondheim, Norway, in 2019, and Power Electronics System Laboratory, ETH Zurich, Zurich, Switzerland, in 2023. He is currently a Research Assistant with the Institute of Control and Industrial Electronics, Warsaw University of Technology. His main research interests include SiC-based power converters, energy conversion in MV range with series connection and multilevel topologies, and dc–dc converters for EV fast charging stations and renewable energy sources.

Adam Tomaszuk was born in Bialystok, Poland. He received the M.Sc. and Ph.D. degrees in electrical engineering from the Bialystok University of Technology, Bialystok, Poland, in 1998 and 2018, respectively.

After graduation, he gained worldwide experience in industry, telecom, and semiconductor sectors. Before his scientific activity, he held the position of senior staff Engineer with Analog Devices BV, Limerick, Ireland. His research interests include the field of high-efficiency power converters, dynamics of dc–dc converters, and renewable energy systems.