A High Power Density Zero-Voltage-Switching Totem-Pole Power Factor Correction Converter

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***Abstract*—The power factor correction (PFC) circuit is an essential component in high-power supplies with nonlinear loads, occupying nearly half the size of a typical power supply. To minimize the size of passive components in PFC converters, the switching frequency must be increased to several hundred kHz, a challenge even when employing gallium nitride (GaN) devices under hard-switching conditions. This article proposes a new GaN-based totem-pole (TP) PFC converter integrated with a bidirectional soft-switching cell. Unlike critical-conduction-mode TP PFC circuit, the proposed converter operates in continuous-conduction-mode with simple control. Design considerations and optimization of soft-switching cell are discussed and verified with simulations. As a proof of concept, a two-phase interleaved version of the proposed converter rated at 3700 W has been designed. The designed prototype achieves a peak efficiency of 99.14% and surpasses the hard-switched GaN-based TP PFC converters in both power density and cost.**

***Index Terms*—AC–DC converter, electric vehicle, on-board charger, power factor correction (PFC), totem-pole (TP), zero-voltage-switching (ZVS).**

I. Introduction

THE applications of power electronics have steadily grown over the past decade in industries, such as the automotive sector, communication/server infrastructure, and energy management systems. Due to higher electrification in these industries and advances in semiconductor technology, the power density and efficiency expectations of power converters have increased tremendously. As front-end power factor correction (PFC) circuits are common across high-power converters, it has always been of interest to shrink the size and improve the efficiency of this stage [1], [2], [3], [4], [5]. When efficiency for high-power applications is a concern, bridge-less PFC topologies are preferred over diode-bridge PFC converters. The basic and highly efficient PFC converter is the bridge-less boost PFC converter presented in [6]. To reduce electromagnetic interference (EMI) and current stress on the inductors, clamping diodes are added between the negative rail and the ac line [7], [8]. Even though the efficiency is higher, the number of components compromises its power density.

The introduction of wide-bandgap devices, such as gallium nitride (GaN)-based power devices, has paved the way for simplified power architectures. The system-level cost and power density advantages brought by GaN devices have been observed and proven in hard-switching half-bridge power stages [9], [10], [11], [12], [13]. This has led designers to move from classical diode-bridge based or semibridgeless topologies to totem-pole (TP) PFC circuits [14], [15]. With the absence of a P-N junction from source to drain in GaN power devices, both the switching losses and conduction losses can be reduced with synchronous switching, allowing for high efficiency and a compact converter size. The continuous-conduction-mode (CCM) control in TP PFCs is very similar to that in conventional PFCs, with the exception of the necessary soft-start scheme at near zero-crossings due to the large parasitic capacitance of line frequency FETs or diodes. To further reduce the size of passive components, it is necessary to increase the switching frequency. While the PFC boost inductance size decreases with higher switching frequency, the input current ripple frequency must exceed 400 kHz to achieve a smaller differential-mode (DM) filter volume than that obtained at 135 kHz, considering that EMI standards begin at 150 kHz for conducted emission. However, operating a hard-switched half-bridge leg with 600 V FETs at such frequencies is infeasible even with GaN devices due to thermal constraints. To increase the input current ripple frequency, a multiphase critical-conduction-mode (CrM) TP PFC converter has been proposed and extensively studied in [16] and [17]. The zero-voltage-switching (ZVS) feature allows for increasing the switching frequency, and the input current ripple frequency can be multiplied with the number of interleaving legs. Nonetheless, this topology poses significant challenges. For high output power, many interleaving legs are needed since the peak currents in inductors reach twice the average input current. Interleaving numerous legs, such as four, may address the issue but incurs higher system costs and challenges commonly associated with synchronizing interleaved legs at high frequencies [18], [19], [20], [21]. Another concern is the control of the CrM TP PFC. As a frequency-controlled converter with negative current on inductors at every switching cycle, ensuring adequate negative current and attaining unity power factor operation necessitates

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a complex controller. The interaction between these two loops can result in stability issues [17], [22].

Several other soft-switching PFC converters operating in CCM have been proposed in the literature [23], [24], [25], [26]. The soft-switching cells (SSCs) presented in these papers are designed for conventional PFCs consisting of a front-end diode-bridge followed by a boost converter, making the operation of these cells limited to only converters with unidirectional power flow. In [27], a soft-switched TP PFC has been proposed by employing an auxiliary resonant commuted pole concept. However, the turn-ON time of the auxiliary switch must be adaptive, as it varies with the input ac current. This requirement complicates the controller due to the need for online calculation.

In [28], an SSC incorporating a single resonant inductor is proposed and implemented in series with the upper switch. This converter suffers from large auxiliary inductor, as well as high circulating current. In addition, the SSC's large circulating current necessitates a larger auxiliary FET to handle the dissipated power, resulting in the need for an expensive, low on-resistance device.

Another interleaved soft switching TP converter with phase shifting control and an additional auxiliary inductor is presented in [29]. While this converter achieves soft switching over a moderate operating range, it should be noted that increasing the ZVS range leads to high circulating current in the auxiliary inductor. This converter requires considerably high inductance for auxiliary inductor, resulting in the increased inductor size, which in turn increases the overall size and cost of the converter. In addition, the involvement of phase-shifting in the control scheme adds a slight complexity to the controller design as well.

A highly promising soft switching interleaved TP PFC converter has also been proposed in [30]. Through the inclusion of two auxiliary inductors and a capacitor, this converter achieves a wide ZVS range. The converter employs an integrated triangular current mode (iTCM) approach, wherein the two added inductors operate under variable frequency TCM having a substantial current ripple. Simultaneously, the input inductor maintains a negligible ripple, resembling CCM, albeit with a variable frequency. Nonetheless, it is imperative to acknowledge the associated limitations of this converter. First, the intricate controller design presents a noteworthy challenge, such as accurate zero-crossing-detection and phase synchronization, between interleaved legs. Moreover, the converter's variable frequency nature introduces additional challenges in terms of EMI noise, thereby rendering the filter design process more complex and demanding in order to effectively counteract the EMI noise.

The aim of this research work is to develop a new PFC converter topology that takes advantage of the TP PFC structure to achieve low cost and high efficiency due to synchronous switching, while also achieving ZVS with CCM control. To achieve this, a bidirectional SSC is proposed and integrated into the TP PFC converter as shown in Fig. 1. The major benefits of the proposed converter, compared with the other competitive TP PFC topologies, can be summarized as follows.

1) The main FETs operating at high frequencies can achieve full soft-switching across a wide range of the ac line cycle and partial soft-switching during the remaining period. The auxiliary FET is turned ON with zero-current.

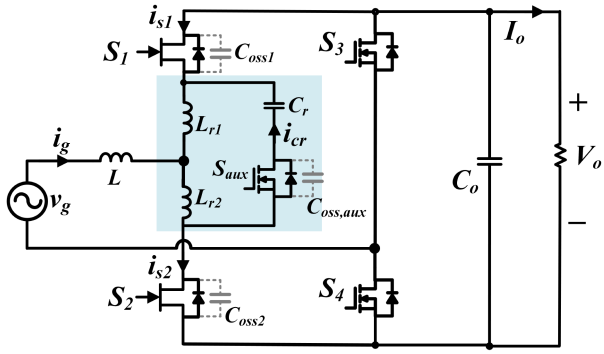

Fig. 1. Proposed new soft-switching TP PFC topology.

2) Unlike the variable frequency control in TCM/CrM TP PFC, the circuit operates in CCM, similar to the conventional TP PFC topology. This eliminates the need to control negative current distortion as the inductor current becomes negative at every cycle. In addition, there is no requirement for current zero-crossing detection circuits or ZVS control loops.
3) The SSC does not disrupt the regular operation of the circuit, and its control can be easily implemented using a digital controller.
4) The current passing through the auxiliary FET is quite low due to its conduction for a brief duration unlike other cases, which allows for the use of comparatively smaller and low cost GaN FET.
5) This converter requires very small resonant inductors compared to its other counterparts, which significantly reduces the overall size and cost of the converter.

II. New Soft-Switching TP PFC Topology

A. Modes of Operation

The proposed topology is essentially based on a TP structure, which is integrated with a bidirectional SSC consisting of two inductors, a capacitor and an auxiliary FET as highlighted in Fig. 1. The operation waveforms and modes of the converter shown in Figs. 2 and 3 are discussed below for the positive alternance of the ac input voltage, in which S_1 and S_2 are the synchronous and active FETs, respectively. Note that since the proposed topology is applicable for Si, SiC, and GaN FETs, the terms "body diode" and "third quadrant" operations are used interchangeably.

1) Mode I ($t_8 - t_0$): In this mode, S_2 is on while S_{aux} and S_1 are OFF. $i_L = i_{\text{Lr2}}, L$ and L_{r2} are charging with the slope $d(i_{\text{L}})/dt = v_g(t)/(L + L_{\text{r2}})$. The energy stored by L_{r2} is equal to $L_{\text{r2}} i^2_{\text{Lr2,pk}}/2$.

2) Mode II ($t_0 - t_1$): In this mode, S_2 is turned OFF while S_1 and S_{aux} remain OFF. A resonant circuit is formed between $L_{r1}, L_{\text{r2}}, C_{\text{oss1}}, C_{\text{oss2}}$, and C_o. Here, C_{oss} of both the FETs are same and C_o is assumed as a voltage source since $C_o >> C_{\text{oss}}$. In this interval, C_{oss} of the lower FET begins to charge to V_o, while C_{oss} of the upper FET discharges to zero.

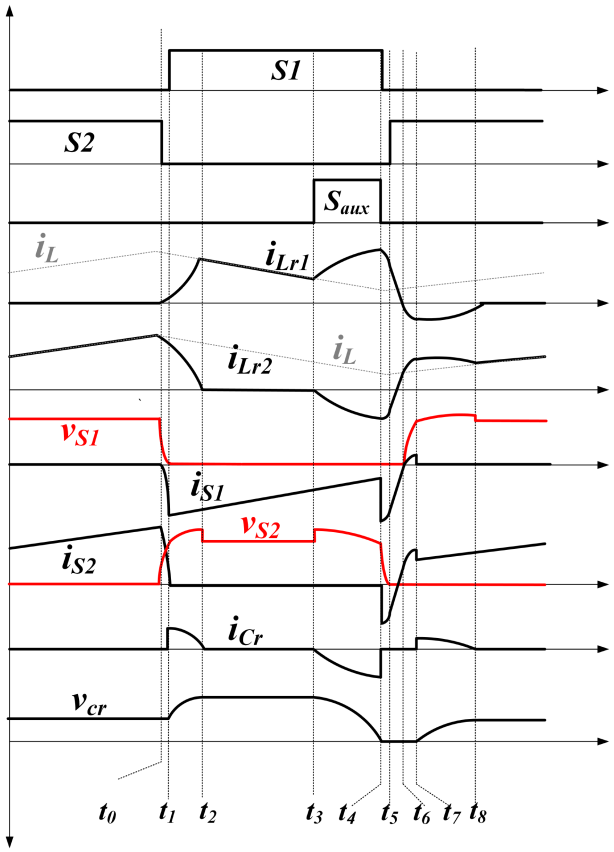

Fig. 2. Operation waveforms in positive ac mains cycle.

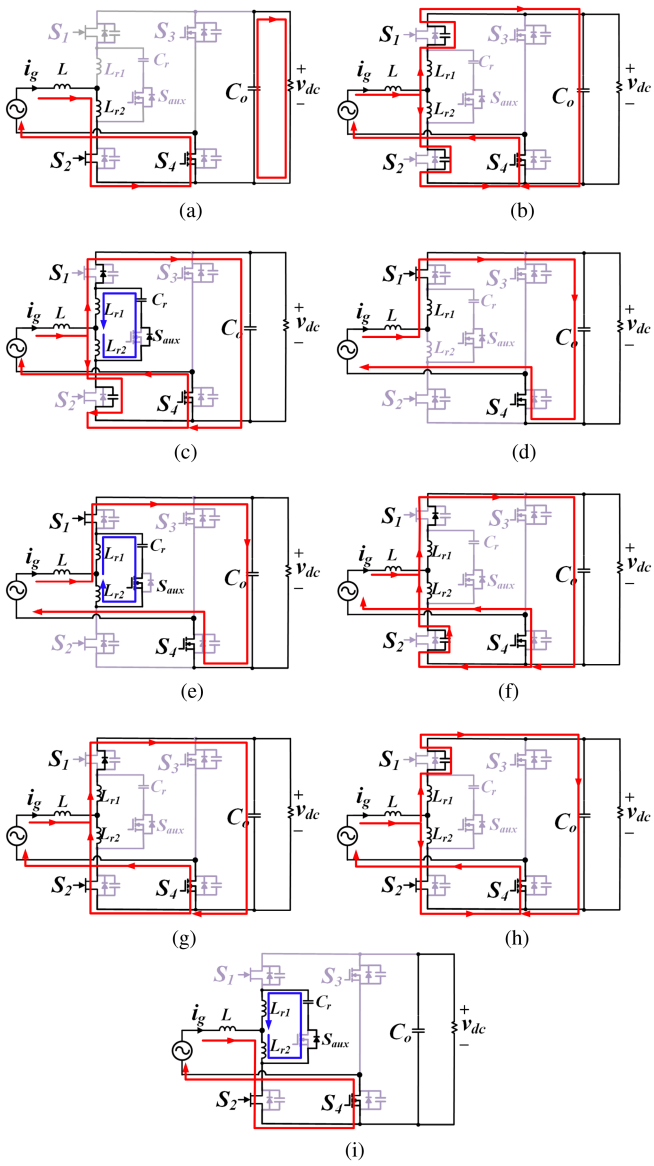

Fig. 3. Modes of operation. (a) Mode I. (b) Mode II. (c) Mode III. (d) Mode IV. (e) Mode V. (f) Mode VI. (g) Mode VII. (h) Mode VIII. (i) Mode IX.

When v_{DS1} reaches to zero, body diode of S_1 begins to conduct the current and S_1 is ready to turn-ON with ZVS. Before this mode, a very short resonance occurs between the C_r, C_{oss} of the auxiliary FET and resonant inductors L_{r1} and L_{r2}. Since the C_{oss} of the auxiliary FET is five times smaller than that of the main FETs, the effect of this resonance is negligible on the overall operation, allowing it to be safely ignored.

3) Mode III ($t_1 - t_2$): During this mode S_1, acting as a synchronous switch, is turned ON with ZVS, while all other switches remain OFF. i_{Lr2} begins to flow through body diode of S_{aux} forming a resonant circuit between L_{r2}, L_{r1}, and C_r. i_{Lr2} is discharged from nearly $i_{L,pk}$ to zero in this mode transferring all of its energy to C_r, which is previously charged to voltage of $\sqrt{C_{oss}/C_r}V_o$

$$L_r i_{L,pk}^2 = \frac{1}{2}C_r {V_{cr,pk}}^2 - \frac{1}{2}C_{oss}V_o^2. \tag{1}$$

Rearranging (1) for $V_{cr,pk}$ yields

$$V_{cr,pk} = \sqrt{\frac{2L_r i_{L,pk}^2 + C_{oss}V_o^2}{C_r}}. \tag{2}$$

Also, solving the resonance circuit of Mode III results in

$$v_{cr}(t) = \sqrt{\frac{2L_r i_{L,pk}^2 + C_{oss}V_o^2}{C_r}}\cos(\omega_r t - \alpha) \tag{3}$$

where

$$\alpha = \cos^{-1}\left(\sqrt{\frac{C_{oss}V_o^2}{(2L_r i_{L,pk}^2 + C_{oss}V_o^2)}}\right) \tag{4}$$

$$\omega_r = \frac{1}{\sqrt{2L_r C_r}}. \tag{5}$$

Note that initial voltage of C_r can easily be determined by using the resonance circuit formed during Mode IX.

4) Mode IV ($t_2 - t_3$): This mode starts when i_{Lr2} reaches to zero and i_{Lr1} becomes equal to i_L, while all the switches remain in previous states. This interval is the typical off-time interval of a TP PFC. The current through L and L_{r1} is decreased with a slope of $d(i_L)/dt = (v_g(t) - V_o)/(L + L_r)$.

5) Mode V ($t_3 - t_4$): In this mode, S_{aux} is turned ON, while S_2 and S_1 preserve their previous states. C_r discharges through

L_{r2} and L_{r1} by forming a resonant circuit

$$v_{cr}(t) = \sqrt{\frac{2L_r i_{L,pk}^2 + C_{oss}V_o^2}{C_r}}\cos(\omega_r t). \quad (6)$$

As $i_{Lr2} = i_{cr}$

$$i_{Lr2}(t) = -\omega_r C_r V_{cr,pk}\sin(\omega_r t) \quad (7)$$

$$i_{Lr2}(t) = -\sqrt{\frac{2L_r i_{L,pk}^2 + C_{oss}V_o^2}{2L_r}}\sin(\omega_r t). \quad (8)$$

When C_r is completely discharged i.e., $v_{cr} = 0$, S_{aux} is turned OFF, at this point L_{r2} has maximum negative current equal to

$$I_{Lr2,pk} = -\sqrt{\frac{2L_r i_{L,pk}^2 + C_{oss}V_o^2}{2L_r}}. \quad (9)$$

6) Mode VI ($t_4 - t_5$): This mode starts when S_{aux} and S_1 are turned OFF at the same time. i_{Lr2} discharges the C_{oss} of the main FET allowing ZVS turn-ON condition. In order to turn-ON S_2 with ZVS, the energy of the inductor must be greater than energy stored in its C_{oss}, so that it discharges C_{oss} completely Therefore, the voltage across S_2 during this interval can be expressed as

$$v_{DS2}(t) = V_o - \sqrt{\frac{2L_r i_{L,pk}^2 + C_{oss}V_o^2}{C_{oss}}}\sin(\omega_1 t). \quad (10)$$

Since, during this mode resonance occurs between L_{r1}, L_{r2}, and C_{oss}, hence

$$\omega_1 = \frac{1}{\sqrt{(2L_r C_{oss})}} \quad (11)$$

At the end of this mode, S_2 can be turned ON with ZVS as v_{DS2} reaches to zero. The current of L_{r2} is not equal to zero at the end of this mode, since C_r stores some extra energy as explained in Mode IX, which is then dumped into L_r.

Please note that, the effect of resonance between C_{oss} of auxiliary FET, C_r, L_{r1} and L_{r2} is insignificant and hence is ignored during this mode.

7) Mode VII ($t_5 - t_6$): In this mode, S_2 is turned ON with ZVS. This is a transition mode where the extra energy stored in the L_{r1} and L_{r2} is dumped into the output capacitor. During this mode, i_{Lr2} is increased and i_{Lr1} is decreased quickly with linear slopes of $\pm V_o/(2L_r)$, respectively. i_{Lr2} increases linearly until it reaches i_L, while i_{Lr1} reaches exactly zero at this time. As soon as i_{Lr1} reaches zero next mode starts because body-diode of S_1 becomes reverse bias.

8) Mode VIII ($t_6 - t_7$): During this mode S_2 is on while both S_1 and S_{aux} are OFF. During this mode, a resonant circuit is formed between C_{oss}, L_{r1} and L_{r2} and the current through L_{r2} is increased beyond i_L while i_{Lr1} reverses its direction and charges the capacitor C_{oss} of S_1. The equations of this mode are given below:

$$v_{DS1}(t) = V_o(1 - \cos(\omega_1 t)) \quad (12)$$

$$i_{Lr1}(t) = -\omega_1 C_{oss} V_o \sin(\omega_1 t) \quad (13)$$

$$i_{Lr2}(t) = i_L + \omega_1 C_{oss} V_o \sin(\omega_1 t). \quad (14)$$

9) Mode IX ($t_7 - t_8$): During this mode, status of the switches remains same. This mode starts when C_{oss} of S_1 is charged to V_o. At this point, the current in L_{r1} and L_{r2} begins to discharge through the capacitor C_r by forming a resonance circuit. The voltage across C_r increases and can be found by solving a resonance circuit formed in this mode

$$v_{cr}(t) = \sqrt{\frac{C_{oss}}{C_r}} V_o \sin(\omega_r t). \quad (15)$$

During this mode, the voltage across S_1 is given as $v_{DS1} = V_o + v_{cr}$.

$$v_{DS1}(t) = V_o\left(1 + \sqrt{\frac{C_{oss}}{C_r}}\sin(\omega_r t)\right). \quad (16)$$

When i_{Lr2} reaches i_L, i_{Lr1} reaches zero and body diode of S_{aux} reverse biases and stops conducting. At the end of this mode the following happens.

1) C_r is charged to $\sqrt{(C_{oss})/C_r}V_o$.
2) v_{cr} will remain constant until the next mode and the energy stored in C_r is given by

$$E_{cr} = \frac{1}{2}C_{oss}V_o^2. \quad (17)$$

B. Control Strategy

The used control algorithm is the same as the traditional one for TP PFC converter operated in CCM with an outer voltage control loop for voltage regulation, and an inner average current mode control loop for input current shaping [15]. The only difference is the inclusion of the signal of the auxiliary FET. To ensure proper operation of the converter, a constant turn-ON time ($T_{ON,aux}$) corresponding to a constant duty cycle is utilized for the turn-ON of S_{aux}. This is due to the fact that the ω_r remains consistent throughout the converter's operation. This signal has to be synchronized carefully such that S_{aux} is turned ON for $T_{ON,aux}$ prior to the turn-OFF of the synchronous FET. In practice, this can be achieved by using a left-aligned pulsewidth modulation (PWM) counter for the main FET and generating a complimentary signal for the synchronous FET, while a right aligned PWM counter is configured to drive the S_{aux} with a duty cycle corresponding to $T_{ON,aux}$. The control algorithm and SSC logic for this topology is already explained in detail in [31].

C. Design and Optimization of L_r and C_r

The design of the SSC includes calculation of the optimum values of L_r and C_r at a given switching frequency. The proposed converter achieves full soft-switching for the main switches within a specific range of ac line cycle. The main FET begins to achieve full ZVS turn-ON from a determined input voltage $v_{g,min}$, corresponding to a duty cycle, $d(t_{min})$. The ω_r of the soft-switching tank is given in (5), constraining the values of L_r and C_r by $d(t_{min})$. Smaller value of L_r increases the ω_r, expanding the full soft-switching range; however, there may be insufficient ZVS time to discharge the C_{oss} of the main FET. On the other hand, a higher value of L_r stores sufficient energy to extend ZVS time and results in lower current stress

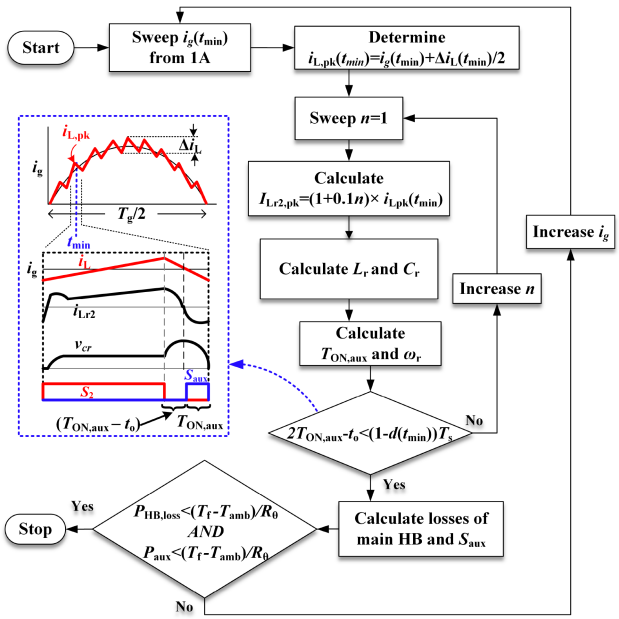

Fig. 4. Flowchart of the SSC optimization framework.

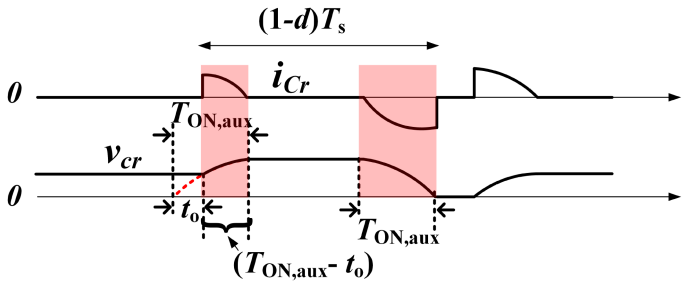

Fig. 5. Determination of $T_{ON,aux}$.

on the L_r and S_{aux}, but narrows the full soft-switching operation region. Partial soft-switching may cause significant power loss, potentially leading to FET temperatures exceeding the maximum operational temperature limits. Therefore, it is critical to optimize the SSC for the desired switching frequency (f_{sw}), taking into account the power losses that may arise due to the partial soft-switching region. The flowchart of the optimized L_r and C_r design is given in Fig. 4 and its steps are summarized as below.

1) In the design of L_r for a specific L and f_{sw} at a given power level, a crucial factor to consider is the peak value of the resonance inductor current ($I_{Lr2,pk}$), at the moment of auxiliary switch turn-OFF. This value, which is consistently greater than $i_{L,pk}$ across the soft-switching range, is essential to determine the optimal L_r. Moreover, achieving full soft-switching necessitates a minimum peak current, given by $i_{L,pk}(t_{min})=i_g(t_{min})+\Delta i_L(t_{min})/2$. The optimization process begins with an outer-loop sweeping of the average input current, i_g at t_{min}, starting from 1 A. Next, $I_{Lr2,pk}$ is derived using $I_{Lr2,pk}=(1+0.1n)\cdot i_{L,pk}(t_{min})$, by sweeping n in the inner-loop. Ultimately, L_r is computed utilizing the following:

$$L_r=\frac{(V_o^2C_{oss})}{2(I_{Lr2,pk}^2-i_{L,pk}^2(t_{min}))}. \tag{18}$$

The above equation is derived from the energy conservation principle between resonance elements. The value of $i_{Lr2,pk}$ depends on L_r, which should be chosen carefully. Specifically, L_r should not be excessively high, as this would compromise the soft switching range while driving up the size and cost of the resonance inductor. Conversely, it should not be too low, as this could introduce high current stress on the switches due to high resonance current peak.

2) Once L_r is determined, the corresponding C_r is calculated using (19) and limiting the maximum voltage stress on auxiliary switch such that $V_{DS,max}>V_o+V_{cr,max}+V_{margin}$. For GaN FETs $V_{DS,max}$ usually is 650 V and V_{margin} must at least be 100 V for safe operation

$$V_{cr,max}=\sqrt{\frac{2L_ri_{L,max,pk}^2+C_{oss}V_o^2}{C_r}}. \tag{19}$$

Note that $i_{L,max,pk}$ in (19) is the peak of the inductor current at the maximum power level.

3) Once C_r and L_r are determined, the timing condition is checked in every loop. If the condition is satisfied, the next step is executed; if not, n is increased, and the process is repeated until the timing constraints are met. The turn-ON time of S_{aux} is critical, as it is an important factor in determining the overall efficiency of the converter. Consequently, the timing condition is established by calculating the resonance frequency once L_r and C_r have been computed, as provided in (20)

$$\omega_r=\frac{1}{\sqrt{2L_rC_r}}. \tag{20}$$

The turn-ON time of the auxiliary switch can be calculated using the minimum possible turn-ON time of the synchronous FET, which is actually limited by the maximum duty cycle of the main switch. This timing constraint is illustrated in Fig. 5 and is given as $T_{ON,aux}-t_o+T_{ON,aux}\leq(1-d(t_{min}))$. Hence

$$2\cdot T_{ON,aux}-t_o\leq(1-d(t_{min}))T_s. \tag{21}$$

Here, t_o can be determined utilizing (4) and is given as

$$t_o=\frac{1}{\omega_r}\dot{\cos}^{-1}\left(\sqrt{\frac{C_{oss}V_o^2}{(2L_ri_{L,pk}^2+C_{oss}V_o^2)}}\right). \tag{22}$$

For the proper operation of soft switched circuit and ensuring v_{cr} to reach zero in every switching cycle, the turn-ON time of auxiliary switch must be one quarter of the resonant period

$$T_{ON,aux}=\frac{T_r}{4}=\frac{\pi}{2\omega_r}. \tag{23}$$

4) After timing constraints are met, the total power loss of auxiliary switch is estimated using the switch-loss model provided in [32].

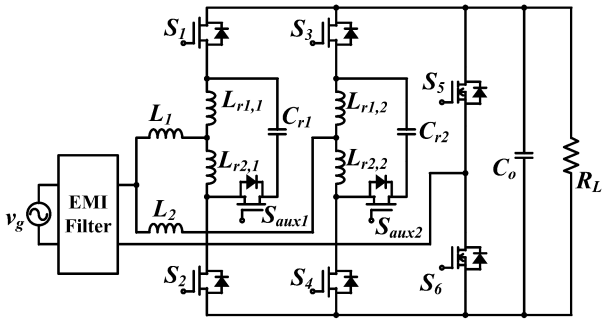

Fig. 6. Proposed topology for 3.7 kW application.

TABLE I
SPECIFICATIONS OF THE DESIGNED CONVERTER

Output power (P_o)	3.7 kW
Output voltage (V_o)	400 V
Switching frequency (f_{sw})	200 kHz
Input voltage (V_{in})	220 V_{rms}
Input inductor (L_1, L_2)	80 μH
Resonance inductor ($L_{r1,1}$, $L_{r2,1}$,$L_{r1,2}$, $L_{r2,2}$)	0.69 μH
Resonance capacitor (C_{r1}, C_{r2})	18 nF

5) Once the total power loss on auxiliary switch is estimated, it is determined whether the FET's junction temperature is with in allowed limit or not, if it is with in limit, the SSC is optimally designed. If it is not, i_g is increased and steps from 1 to 5 are followed again in the same manner as explained above.

III. Results and Discussions

Fig. 6 shows the two-phase interleaved version of the proposed topology for 3700 W front-end PFC converter. To achieve high efficiency and high power density, the proposed converter has been optimized according to the framework presented in [32], which has suggested adopting a f_{sw} of 200 kHz together with input inductances L_1 and L_2 of 80 μH. This makes the input current ripple frequency 400 kHz that reduces the size of the DM filter [33]. The $L_{r1,1}$, $L_{r1,2}$, C_{r1}, and C_{r2} of the interleaving converter are optimized by the algorithm presented in Section II-C. According to the results, the optimum starting current level of soft-switching is found as 4 A, while $i_{Lr,pk} = 2 \cdot i_{L,pk}(t_{min})$ is selected. This design specification provides a good tradeoff between required L_r value and power switch losses due to partial soft-switching. Using (18) and (19), L_r and C_r are found as 0.69 μH and 18 nF, respectively.

A. Simulation Results

The operation of the converter is verified by simulations with the specifications given in Table I, and the results are provided in Fig. 7. The simulation results show that the converter achieves high power factor with low input current total harmonic distortion (THD). The main FETs are ZVS turned ON when $i_g > i_{g,min}$. Here, $i_{g,min}$ corresponds to the current at t_{min}, which

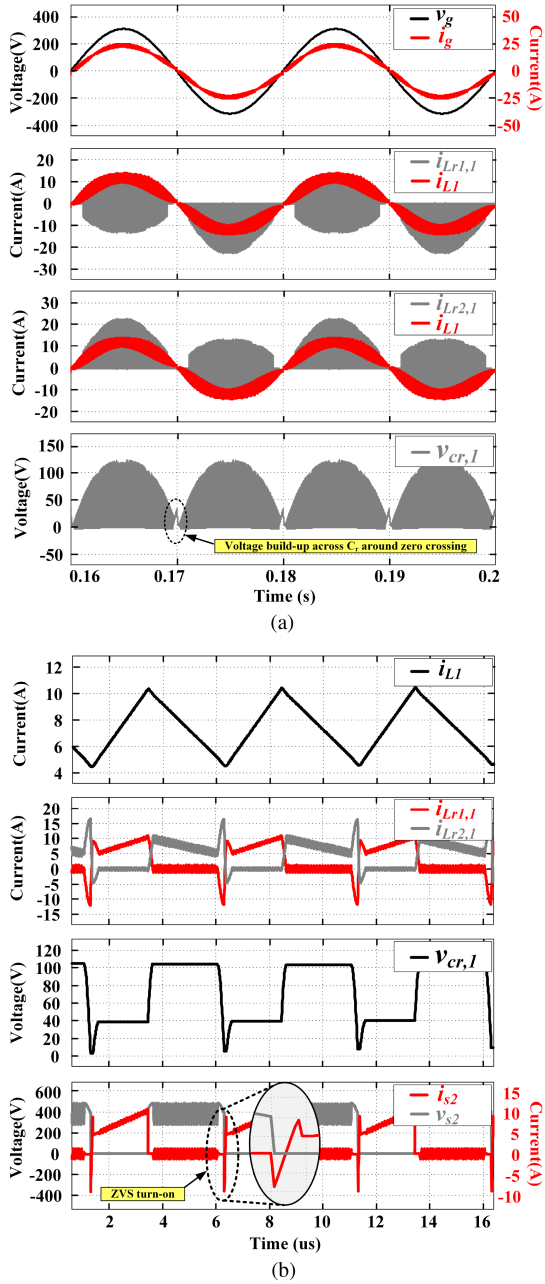

Fig. 7. Simulation results for (a) line frequency and (b) switching characteristics when $v_g > 0$.

is the time when the converter enters the ZVS region within an ac line cycle. Prior to this determined time, the main FETs are turned ON at switch node voltages less than the dc-bus voltage, which provides partial soft-switching. It is important to note that v_{cr} does not discharge completely to zero, as S_{aux} is only turned ON for $t_{ON,aux}$, which is not sufficient to discharge v_{cr} to zero i.e., $t_{ON,aux} < T_r/4$. Consequently, the voltage across C_r starts to build up during this time period, as shown in Fig. 7(a). Fig. 8(a) also illustrates the voltage buildup phenomenon in the ideal simulation case where there is no zero-crossing blanking time. It can be observed that this voltage buildup is more pronounced in this scenario [see Fig. 9(a)] than in the case where blanking time

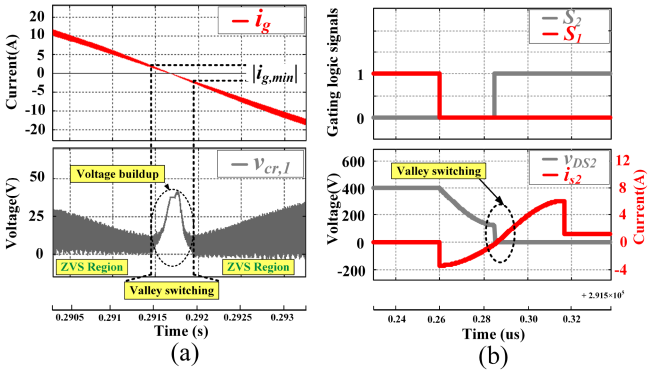

Fig. 8. When $i_g < i_{g,\min}$ (a) voltage build-up phenomena across C_r and (b) valley switching operation.

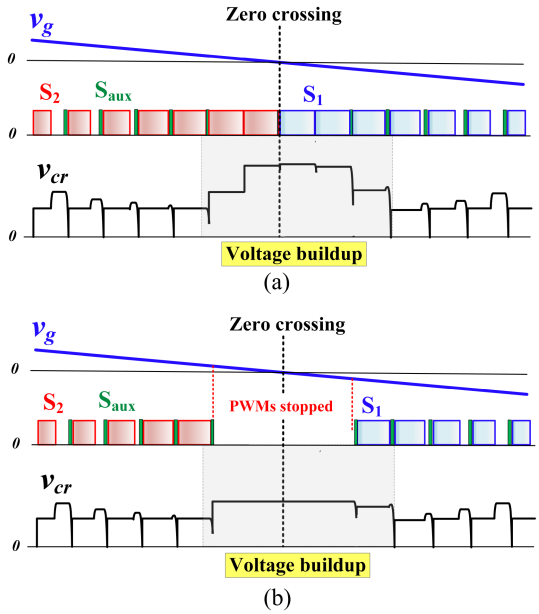

Fig. 9. Key figures showing voltage buildup across C_r near zero crossing (a) without blanking time and (b) with blanking time.

is introduced and PWMs are stopped [see Fig. 9(b)]. In the latter case, the voltage initially rises but remains constant thereafter, as there is no switching and thus no charge or discharge of $C_{\rm r}$. During the voltage buildup just before stopping all the PWMs, the converter does not enter into full hard-switching mode, as the $C_{\rm r}$ still stores some energy even when $i_g < i_{\rm g,min}$. This energy is partially transferred into $L_{\rm r}$ in each switching cycle during this period. This process helps to achieve valley switching operation of the main switch, even during the non-ZVS region, as illustrated in Fig. 8(b).The switch turning ON with reduced voltage leads to a decrease in turn-ON loss and an improvement in overall efficiency. This phenomenon can be explained by considering (5) and (6). As a result, a generalized expression of $v_{\rm DS2}$ that incorporates the non-ZVS region can be provided

$$v_{\rm DS2}(t) = V_o - K \times \sqrt{\frac{2L_{\rm r}i_{\rm L,pk}^2 + C_{\rm oss}V_o^2}{C_{\rm oss}}}\sin(\omega_1 t) \qquad (24)$$

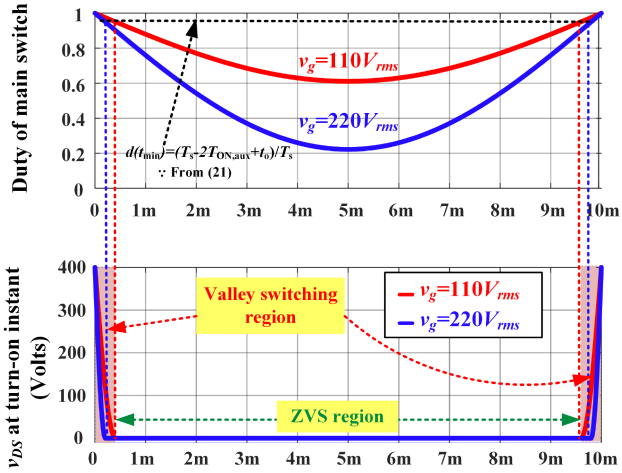

Fig. 10. Illustration of ZVS range over half-line cycle.

$$K = \begin{cases} 1 & \text{if } t_{\rm ON,aux} = \frac{T_{\rm r}}{4} \\ \sin\left(\frac{2\pi t_{\rm ON,aux}}{T_{\rm r}}\right) & \text{if } t_{\rm ON,aux} < \frac{T_{\rm r}}{4}. \end{cases} \qquad (25)$$

It can be seen from (24) that second term of the equation is scaled down by a factor K, where, $0 < K \leq 1$ and it takes on the values based on the condition of $t_{\rm ON,aux}$ as provided in (25). These two equations also state that partial soft-switching or valley switching becomes inevitable once $t_{\rm ON,aux}$ is less than one quarter of the resonance period T_r, which happens only near zero-crossings of line voltage where the duty cycle of the main FET reaches to maximum, while that of synchronous switch becomes too low. Since, turn-ON of the auxiliary FET is aligned with synchronous FET, the ZVS range of the converter is primarily determined by the duty cycle limitation of the synchronous FET. Indirectly, this limitation is also influenced by v_g as the duty cycle is related to v_g. It is important to note, however, that in theory, this ZVS range remains independent of the load conditions.

The parameters to determine the range of ZVS can be determined using (24) and (25). In this analysis, $i_{L,\rm pk}$ is assumed to be zero as the ZVS is independent of load. A graph is then plotted to illustrate the relationship between $v_{\rm DS}$ of the main switch at the turn-ON instant, and the corresponding time during one half cycle of operation as shown in Fig. 10.

It can be observed that as long as (21) is satisfied, the voltage across the $v_{\rm DS}$ of the main switch during the turn-ON instant is zero, indicating that the converter is within the ZVS range. Conversely, when (21) is not satisfied, nonzero $v_{\rm DS}$ values begin to appear at the turn-ON instant, indicating the onset of the valley switching region. It must be noted that during valley switching region the converter still exhibits turn-ON losses that mainly include IV-overlap loss and capacitive turn-ON loss but this loss is lower than typical hard-switched turn-ON loss.

B. Experimental Verification

The experimental prototype has been developed as shown in the Fig. 11, 50 mΩ TI GaN LMG3425R050 is chosen for main GaN FET half-bridge and 150 mΩ TI GaN LMG3410R150 is chosen as the auxiliary switch. Two parallel Si FETs are used

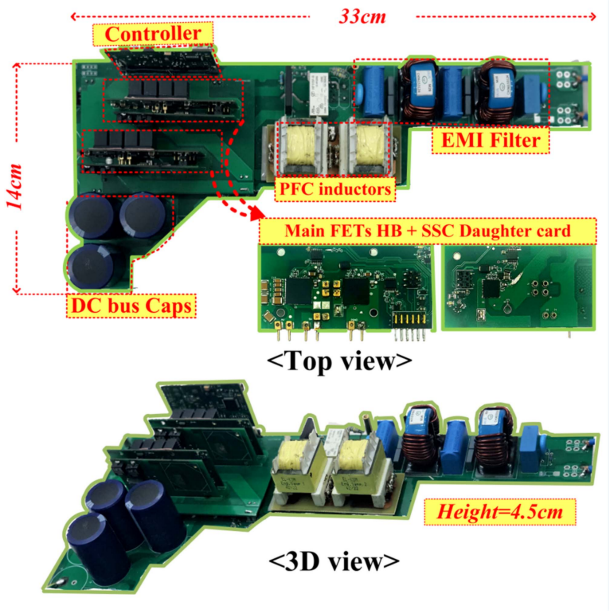

Fig. 11. 3.7 kW experimental prototype.

for rectifying leg switches. Ferroxcube E-cores 3F3-341409 are selected and stacked together to form the single core for each input inductor. The inductor is designed to give 80 μH inductance with 0.683 mm air-gap and 19 turns with AWG 14 wire. 470 μF $\times$ 3 capacitors are used as bulk DC-bus capacitors. Off-the-shelf inductors from Würth Electronik (744325072) are selected to be used as resonance inductors. These inductors are chosen for their high saturation current capability and excellent performance at high frequencies, aiming to minimize associated core losses.

The experimental results during an AC line cycle are given in Fig. 12(a). i_{L1} and i_{L2} can also be shown to have a very low zero crossing distortion due to implementation of maximum duty limit to 0.98 and giving enough blanking time i.e., stop all PWMs during this time and also implementing soft-start. Fig. 12(b) shows the zoomed-in experimental waveforms of i_{L1}, $i_{Lr1,1}$, and v_{cr} in a grid period. Please note that waveform of v_{cr} shows voltage buildup but this voltage buildup is not as pronounced as in case of simulations, which is due to the inserted blanking time and soft-start at zero crossing. Similarly, Fig. 12(c) shows switching waveform of all the inductors current and Fig. 12(d) shows waveform of v_{DS2}, i_{s2}, i_{cr1}, v_{cr1} of the converter. In addition, Fig. 13(a) shows the experimental waveform of the ZVS operation of the main switch, while Fig. 13(b) and (c) illustrate the switching characteristics of the synchronous and auxiliary FETs, respectively. It is worth noting that the auxiliary FET turns ON at ZCS and does not exhibit any Q_{oss} loss since it is not used in half-bridge configuration.

The zoomed-in waveforms of the proposed converter at two extreme duty cycles are also provided in Fig. 14 to validate the ZVS range of the proposed converter. Fig. 14(a) presents the zoomed-in waveforms of v_{DS2} and i_{s2} along with v_{cr} and i_{cr} at a very low duty cycle of 0.25. Similarly, experimental results at a very high duty cycle of 0.97 are provided in Fig. 14(b).

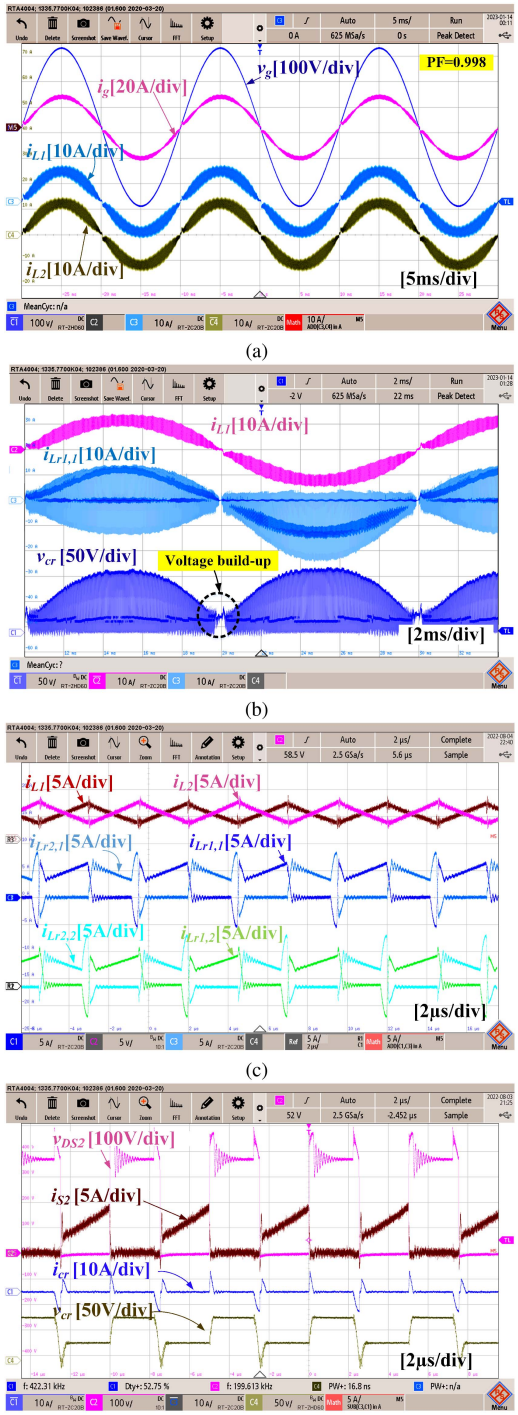

Fig. 12. Experimental waveforms; (a) v_g, i_g, i_{L1}, and i_{L2} for grid period, (b) i_{L1}, i_{Lr}, and v_{cr} for grid period, (c) all inductors currents for f_{sw}, (d) S_2 and C_r voltage and current for f_{sw}.

It is clearly shown that the converter operates under full ZVS operation during the low duty cycle, while it loses its ZVS operation and enters the valley-switching region during the very high duty cycle which also corresponds to near zero-crossing region. Moreover, during the vicinity of zero-crossing, the current is at an extremely low level, and the duty cycle is exceptionally high. During this period, the turn-ON of S_{aux} is synchronized

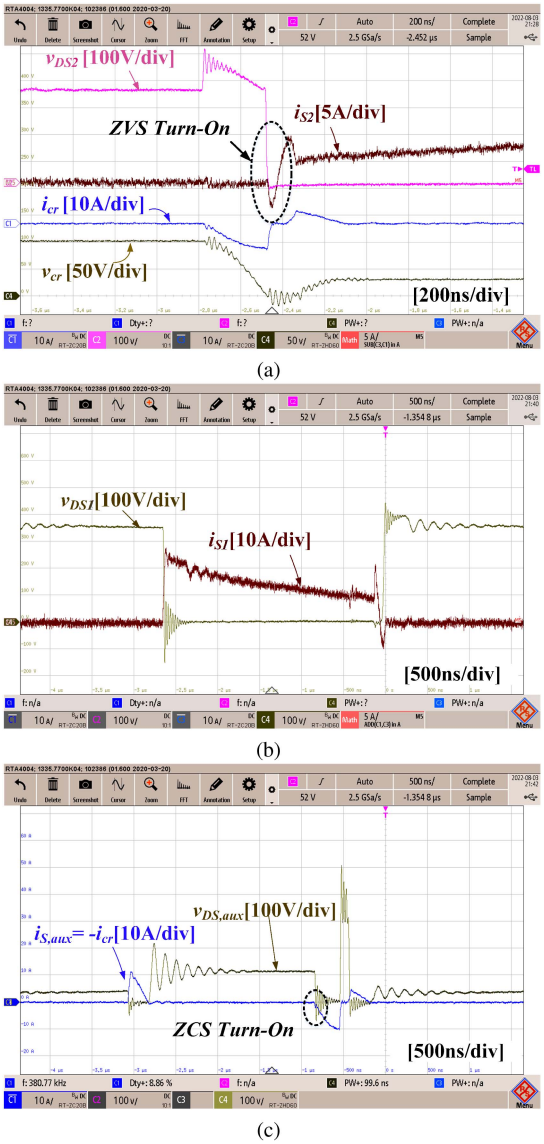

Fig. 13. Experimental waveform of the switching characeristics of (a) Main FET with ZVS turn-ON, (b) sync FET, and (c) auxiliary FET with ZCS turn-ON.

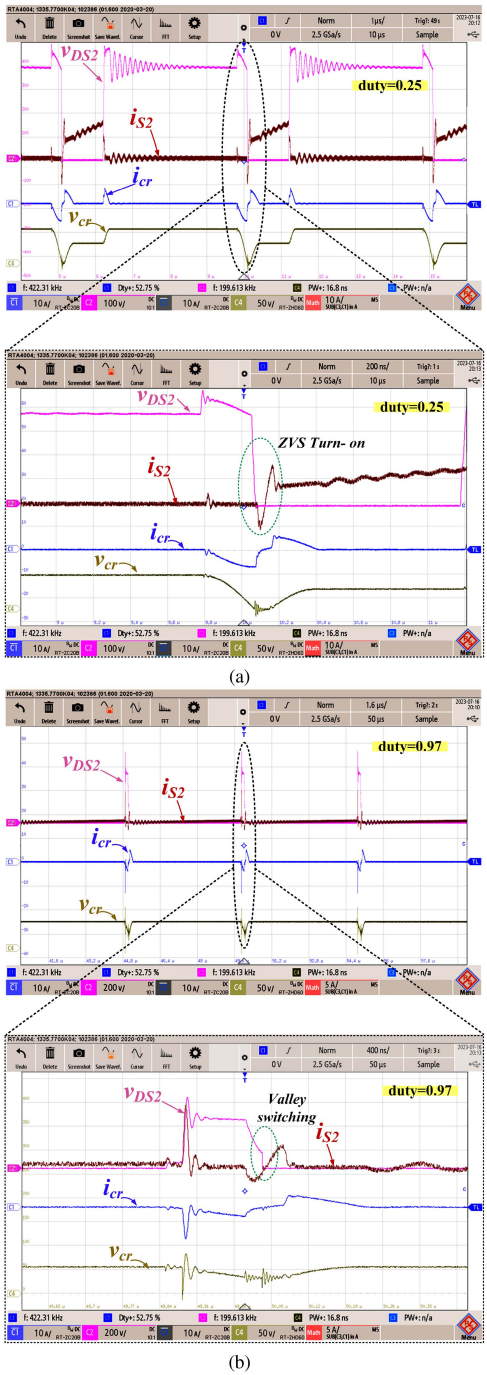

Fig. 14. Zoomed-in experimental waveforms. (a) When $d = 0.25$ and (b) $d = 0.97$.

with the turn-ON of the synchronous FET. If S_{aux} is turned ON before the voltage transition on the main FET is complete, a high voltage equal to v_{cr}+V_o is applied across the C_{oss} of the main FET, while its voltage is less than v_{cr}+V_o. This results in a high current that rapidly charges the C_{oss} of the main FET, as illustrated in Fig. 14(b). Apart from circulating current loss, there is no switching loss on the main FET during this period since the channel of the GaN FET has already been turned OFF earlier.

C. Efficiency Analysis

The proposed converter has been designed with a focus on achieving high overall efficiency at 3.7 kW. It has shown to have peak efficiency of 99.14% at 1.4 kW and an efficiency of 98.71% at 3.7 kW with a 220 V_{rms} line voltage. In addition, it is able to achieve an efficiency of 97.76% at 1.8 kW and a peak efficiency of 98.05% during low line (110 V_{rms}) operation, as shown in Fig. 15. Furthermore, the efficiency of the proposed converter is shown to be very high even at a switching frequency of 200 kHz due to the use of soft-switching technique to achieve ZVS turn-ON for all of the main GaN FETs. This technique reduces switching losses for most of the line cycle, however at non-ZVS region it still exhibits better performance than that of a conventional hard switched converter due to valley switching, resulting in improved overall efficiency and making the converter suitable for high-frequency applications. Moreover, THD

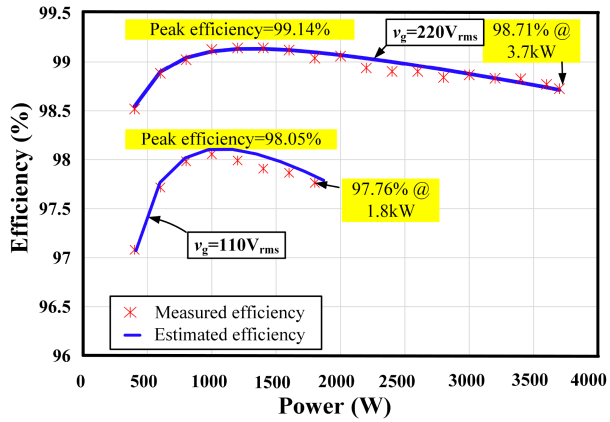

Fig. 15. Measured and estimated efficiencies under tested conditions for low and high AC line.

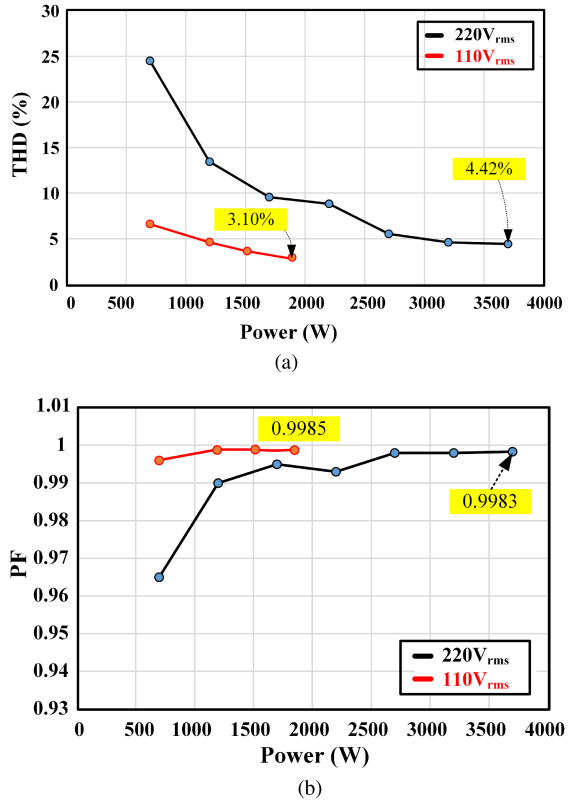

Fig. 16. THD and PF curves for low and high AC line voltages at different loads.

and PF of the proposed converter is measured across different input voltages and load currents and the results are provided in the form of curves in Fig. 16.

Thermal measurements were also conducted under different load conditions, and the temperatures of the FETs and PFC inductors were recorded. The junction-to-ambient temperature rise (ΔT) values are plotted in Fig. 17, with an ambient temperature of 27 °C. At low load, the Δ T on the main FET was measured at 11.31 °C, while that of the aux FET was 13.46 °C. The ΔT on the PFC inductor was recorded as 9.2 °C. Similarly, at full

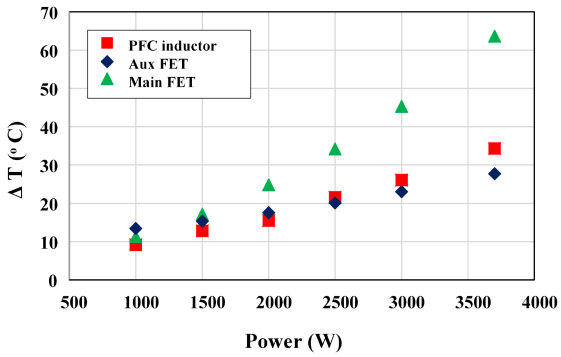

Fig. 17. Temperature measurement of FETs and PFC inductor at different loads.

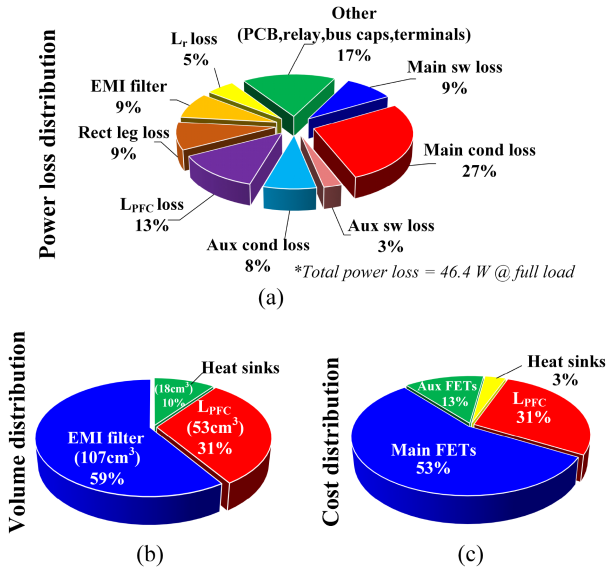

Fig. 18. Pie chart illustrations for the proposed converter's estimated breakdown of (a) total power loss, (b) volume, and (c) cost.

load, the ΔT on the main FET increased to 63.7 °C, the aux FET reached 27.75 °C, and the PFC inductor showed a temperature rise of 34.32 °C.

The increase in the temperature of the main FET from low load to maximum load is attributed to the heightened conduction losses of the main FET. On the other hand, the increase in the temperature of the aux FET is less pronounced, as the current through the auxiliary circuit only changes slightly, allowing for the use of smaller heatsink.

D. Analysis of Power Loss, Volume, and Cost

The losses of the converter are mainly due to the main FETs, aux FETs, input inductors, and EMI CM chokes. These losses are illustrated in the pie chart in Fig. 18(a). It can be seen that the switching losses of the main FETs of the proposed converter are low i.e., 9% of the overall power losses, compared with conduction losses of 27% associated with the same FETs. The other major contributors to the overall power loss of the proposed converter are the rectifying leg loss (9%) and the PFC

TABLE II
COMPARISON OF PROPOSED CONVERTER WITH OTHER SOFT-SWITCHING TP PFCS

Reference		Proposed	[28]	[29]	[30]
Output power		3.7 kW	3 kW	1.6 kW	5 kW
Switching frequency		200 kHz	300 kHz	200 kHz	75 k-1.2 MHz
High frequency switch count		4×GaN 650V / 50 mΩ 2×GaN 650V / 150 mΩ	3×2 paralleled GaN 650V / 70 mΩ	4×GaN 650V / 60 mΩ	4×GaN 650 V / 30 mΩ
FET cost (p·u·) normalized to $R_{ds,on}$		0.70	0.64	0.50	1
Normalized FET cost (p·u·) / kW		0.60	0.68	1	0.64
Full load efficiency (%)		98.7	98	98.05	98.7
Main FET	**Turn-ON**	ZVS	ZVS	ZVS	ZVS
	Turn-OFF	Hard	Hard	Hard	Hard
Aux. FET	**Turn-ON**	ZCS	ZVS	-	-
	Turn-OFF	Hard	Hard	-	-
ZVS range		Wide (duty cycle dependent)	Medium (load current dependent)	Medium (excessive circulating current)	Wide (requires negative inductor current)
Current mode		CCM	CCM	CCM	iTCM
Control complexity		Low (constant $t_{ON,aux}$ aligned with sync FET)	Medium (adaptive duty of auxiliary FET)	Medium (additional phase-shifting control)	High (Variable frequency, ZVD implementation, phase-sync)
Aux. inductor		0.7 μH / 25 A × 4	40 μH / 32 A × 1	50 μH / 10 A × 1	14 μH / 33 A × 2
Normalized (pu) energy capacity($L_{aux}I^2$)		0.043	1	0.12	0.74
Aux. capacitor		18 nF × 2	2.2 μF × 1	-	1.5 μF × 1
Switch voltage stress		$V_o + V_{cr}$	$V_o + V_{cr}$	V_o	V_o

input inductors (13%). The use of an SSC circuit reduces the overall power loss; however, the auxiliary switch also has some switching losses, particularly during turn-OFF operation, the loss distribution chart shows a 3% contribution from switching losses and a 8% contribution from conduction losses of auxiliary switches. Apart from these losses, L_r, EMI filter, dc link capacitor, PCB, relay and terminal losses also contribute significantly to overall efficiency. Also note that there is a voltage ringing on FETs during the normal boost mode operation, which is damped to zero due to dissipation in parasitics of the power loop in every switching period. However, its contribution to overall power loss can be shown to be as low as 4.6%, which is already included in "L_r" and "Other" losses in the loss distribution chart. The volume approximation of the proposed converter is done based on volume of EMI filter, input inductor and the heatsinks used since they are the major contributors to overall volume of any PFC converter. The EMI filter has a volume of 107 cm^3, the boost inductors 53 cm^3, heat-sinks 10 cm^3, as shown in Fig. 18(b). The cost analysis of the converter is based on the costs of 3 main components of the converter; input inductors, heat sinks and FETs. The cost of the components is determined using the model presented in [32] and [34], and the cost distribution of the proposed converter is illustrated in Fig. 18(c).

E. Comparison With Recent TP PFCs in Literature

1) Comparison With Soft-Switching TP PFCs: The comparison of the proposed converter has been conducted with three different soft-switching TP PFCs, and the results are tabulated in Table II. To ensure a fair comparison, several parameters, such as FET cost normalized to $R_{ds,on}$ and normalized FET cost [per unit (p.u.)] per kW for each topology, have been determined. From the provided results in the Table II, it is evident that the proposed converter outperforms all other topologies in terms of normalized FET cost (p.u.) per kW, with a value of 0.60 p.u. Among the compared topologies, the proposed converter and [30] exhibit superior efficiency mainly attributed to their wide ZVS ranges, reaching 98.7% at peak load, while [28] and [29] have comparatively lower efficiencies of 98% each. In the case of [28], the load-dependent ZVS range and high auxiliary FET current restrict its efficiency to approximately 98%. Similarly, for [29], achieving full ZVS requires a significant increase in the auxiliary inductor current, leading to a substantial increase in conduction losses and thus reducing the overall efficiency.

Regarding the complexity of the controller, the proposed converter surpasses its counterparts due to its simple conventional control algorithm, where a right-aligned PWM counter with a

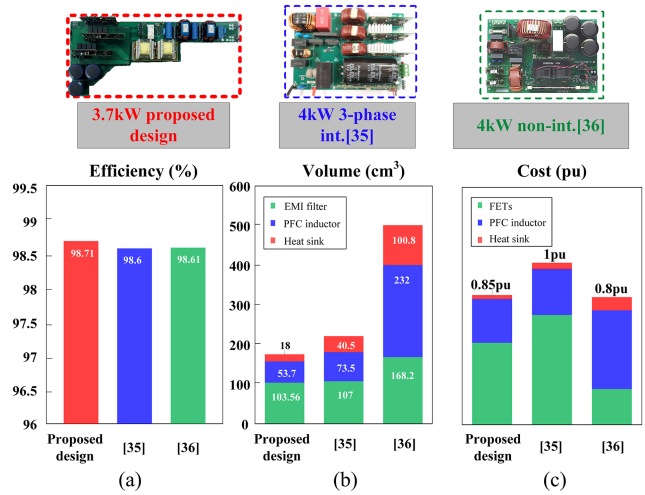

Fig. 19. Comparison of the proposed design with 4 kW three-phase [35] and single-phase [36] reference designs in terms of (a) efficiency, (b) volume, and (c) cost.

fixed duty cycle value is needed to turn-ON the auxiliary FET. In [28] and [29] have a moderate level of control complexity, while Park et al. [30] exhibited high control complexity due to its variable switching frequency control, similar to CrM TP PFCs. Moreover, accurately implementing zero-voltage detection (ZVD) and phase synchronization in interleaved structure at high frequencies can be challenging.

The sizes of the auxiliary inductors are also evaluated and compared among all the topologies. In order to make a fair comparison, a figure-of-merit parameter is defined based on the normalized (p.u.) energy capacity ($L_{\text{aux}}I^2$). This parameter provides insightful information about the sizes of the inductors in terms of their energy storage capabilities. It is evident that despite having four auxiliary inductors, the proposed auxiliary inductors are significantly smaller. Specifically, they are 20 times smaller than the one in [28], 2.5 times smaller than the one in [29], and 16 times smaller than the one in [30].

It can be seen that the proposed converter surpasses the other soft-switching TP PFCs across all performance matrices and therefore can be considered as a viable alternative to its counterparts.

2) Comparison With Conventional Hard-Switching TP PFCs: In addition, the proposed topology was also compared with two hard-switched reference designs: a 4 kW three-phase interleaved [35] and a 4 kW noninterleaving TP PFC converters [36]. The comparison was carried out in terms of power loss, boxed volume, and cost of each design, and the results were presented in the form of bar charts in Fig. 19. A full load efficiency of 98.71% was achieved by the proposed converter, while the efficiencies of [35] and [36] were 98.6% and 98.61%, respectively. The proposed design showed a slight improvement in terms of efficiency, while in terms of volume, the improvement was quite significant. Specifically, the proposed design achieved a boxed component volume of 175 cm^3, which was significantly smaller compared with the volumes of [35] and [36], which were 225 cm^3 and 594 cm^3, respectively. Moreover, in terms of cost, the proposed design outperformed the design in [35], which had a maximum cost taken as 1 p.u.), mainly due to the use of three 50 mΩ GaN FETs half-bridges and three heatsinks. In contrast, the proposed design used only two half-bridges with heatsinks, resulting in a lower cost of approximately 0.85 p.u. The cost of the design in [36] was approximately 0.8 p.u., which was also close to the proposed design's cost. The design in [36] incurred a significant cost due to the bulky single input inductor and the additional DM filter inductor used.

IV. Conclusion

In this article, a new TP PFC converter with SSC for GaN applications is proposed to increase the effective switching frequency up to 400 kHz at which the EMI filter and input inductor size get smaller compared with hard-switched TP PFCs operated below 150 kHz. The primary advantage of the topology are twofolds; the simple TP PFC structure and low components count of SSC circuit as well as the ability to apply CCM control method. Applying soft-switching technique to the FETs across a wide range of the ac line cycle, coupled with partial soft-switching during the remaining cycle, offers the potential to significantly reduce the dimensions of the magnetic components.

In the content of this article, the operation principle of the converter is discussed and verified by simulation and experimental results. The design procedure of ZVS cell is also included and different parameters, which affect the design of the soft-switching cell, are discussed. A 3700 W two-phase interleaved version of the proposed converter has been built. The designed prototype achieved a peak efficiency of 99.14% and a full load efficiency of 98.71%. Analysis results demonstrate that this topology is a promising alternative to traditional hard-switched TP PFC topologies that operate under CCM in high power application.

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