A Design of Boost Converter With Time-Domain MPPT and Digital Self-Tracking ZCD for Thermoelectric Energy Harvesting Applications

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Abstract—This article presents a dc–dc boost converter for energy harvesting. The time-domain maximum power point tracking (MPPT) technique implements to maximize the source's energy harvesting performance with no additional switch and time slot. Furthermore, it is implementing digital self-tracking zero current detectors for high efficiency. This dc–dc boost converter fabricates with a 180-nm CMOS process. The input voltage of the boost converter ranges from 0.2 to 0.7 V and generates an output voltage of 1.2 V. The total area of this converter with the MPPT operation is 600 μm $\times$ 475 μm. The measured power conversion efficiency of this dc–dc boost converter is 85.5%.

Index Terms—DC–DC boost converter, digital self-tracking zero current detector (ST-ZCD), energy harvesting, time-domain maximum power point tracking (MPPT).

I. INTRODUCTION

THESE days, energy harvesting from ultralow power sources is more important because wearable electronics or wireless sensors are more popular. Especially the wireless sensor is essential for the Internet of Things (IoT) and drawing more attention [1], [2]. The energy sources used in these systems are meager, so maximizing energy harvesting is essential.

The maximum power point tracking (MPPT) operation is essential to maximum the energy harvesting performance from a source. An energy harvesting boost converter extracts maximum power from energy sources, such as solar or thermoelectric generators (TEGs), according to MPPT operation. This article presents a method that requires a reference voltage among various methods for MPPT operation, and this reference voltage is made by using the open-circuit input voltage [3], [4], [5]. The open-circuit input voltage is the boost converter's input voltage when the current does not flow through the energy source. The reference voltage of MPPT is some ratio of open-circuit input voltage, such as half of input voltage. The reference voltage of MPPT is compared with the input voltage at every switch. The conventional boost converter sensed the open-circuit input voltage by setting up the additional OFF-timing slot [6], [7], [8], [9]. Fig. 1(b) shows the conventional MPPT operation timing diagram. An OFF-time slot is used periodically to sense the open-circuit input voltage of the boost converter. At the OFF time, the S3 switch is open, and the current is not flowing through R_{TEG}. Therefore, the pure open-circuit V_{IN} voltage without any resistive voltage drop can be sensed in this way. Conventional MPPT circuits of energy harvesting had added a series switch to the boost converter, as shown in Fig. 1(a). The series switch's resistance must be minimal to reduce the conduction loss of the boost converter. This means that the size of this additional switch should be considerable. Moreover, the time slot's period is from millisecond to the second scale. So, to generate this periodical OFF-time slot, an internal clock and additional frequency dividing circuit are needed regardless of the boost converter's control. These additional blocks occupy the area and increase the quiescent current of the dc–dc boost converter. So, if the MPPT concept is changed, the additional series switch will not be required to perform the MPPT operation. Furthermore, the oscillator and frequency dividing circuit can be removed. This article proposes the time-domain MPPT concept with no additional huge series switch and other circuitry related to the time slot.
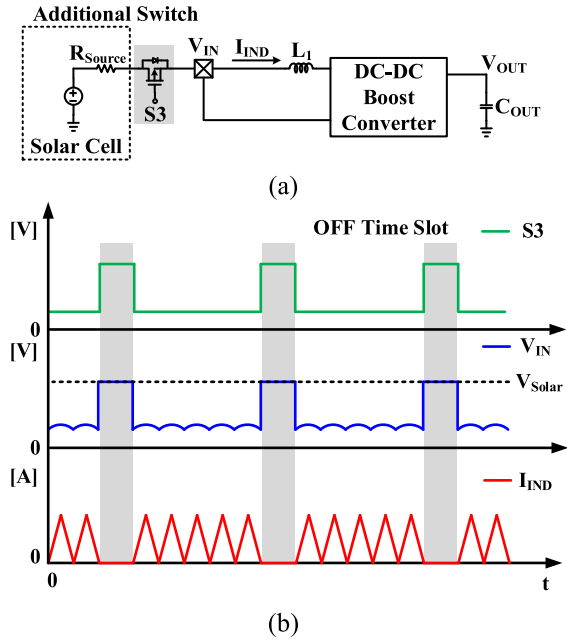
Fig. 1. (a) Structure of conventional MPPT. (b) Operation of conventional MPPT.
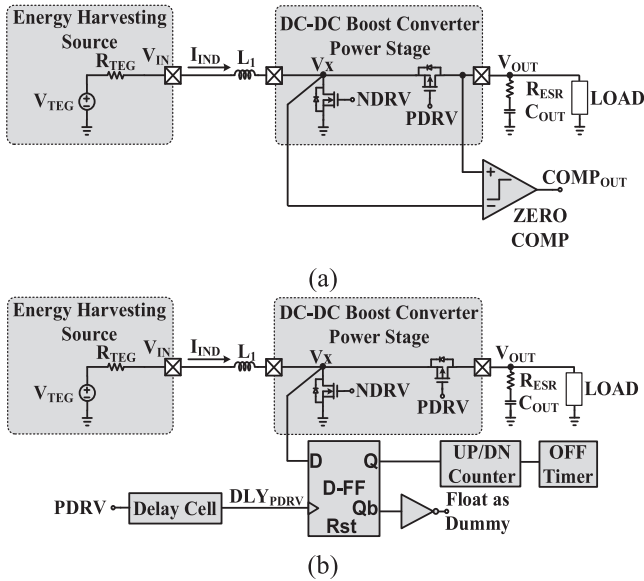

Fig. 2. (a) Conventional ZCD concept using comparator. (b) Conventional ZCD concept using D-flip flop.

To enhance the efficiency of the boost converter in energy harvesting applications, the accurate and low-power operation of the zero current detectors (ZCDs) is required for blocking reverse current from V_{OUT} to V_X. The conventional ZCD compares the V_X node voltage with the V_{OUT} voltage level [10], [11], [12], [13] when the inductor current flows through the PMOS switch, as shown in Fig. 2(a). This concept is very intuitive, but it is easy to be affected by the characteristics of the comparator. Furthermore, since the resistance of the PMOS pass transistor is minimal, the difference voltage between V_X node and V_{OUT} node is incomparably small when the current flowing through
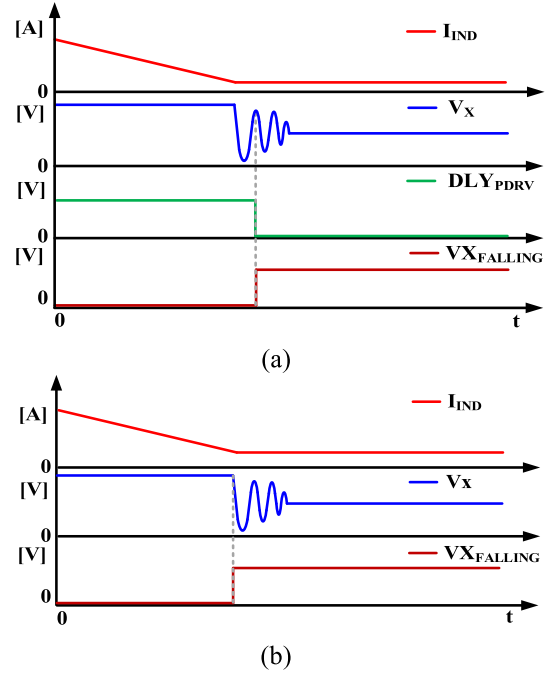

Fig. 3. (a) Abnormal operation of the conventional ZCD using D-flip flop. (b) Normal operation of the proposed ZCD.

the PMOS switch is almost zero. Therefore, this concept is easily affected by the comparator's offset voltage or delay time. The comparator for detecting zero current will be designed in large size to minimize the comparator's offset. Also, to reduce the comparator's delay time, this comparator will consume a large amount of current, which may reduce the efficiency of the dc–dc boost converter, especially all light load conditions. Second, how to track the fall time of the V_X node is also used in [14], [15], [16], [17], and [18] to find the zero current point, as shown in Fig. 2(b).

Compared to the previous one, the advantage of this concept is that comparator is not used for detecting the zero current of the inductor. Therefore, the ZCD design is simple and not affected by the comparator property. Nevertheless, the ringing of VX node voltage can cause the abnormal operation of zero current detecting. During the PMOS switch-OFF time, the inductor current flow path abruptly blocks the energy stored in the inductor, and parasitic capacitance can create a resonance phenomenon. For this reason, the V_X voltage ringing is generated inherently. DLY$_{PRDV}$ is the delay time of the PDRV signal driving signal of the PMOS switch. VX$_{FALLING}$ is V_X node voltages at free-wheeling operation boost converter. DLY$_{PRDV}$ and VX$_{FALLING}$ can cause the abnormal operation of ZCDs, as shown in Fig. 3(a). In this case, the falling of the V_X node is not sensed, and ZCD could not function normally. The proposed boost converter is not affected by the comparator's properties and is robust for ringing of V_X node voltage.

The rest of this article is organized as follows. Section II presents the architecture of the proposed energy harvesting boost converter. The overall structure of this boost converter is shown in this section. After that, the details of the building blocks are presented in Section III. The circuit and operation of each block
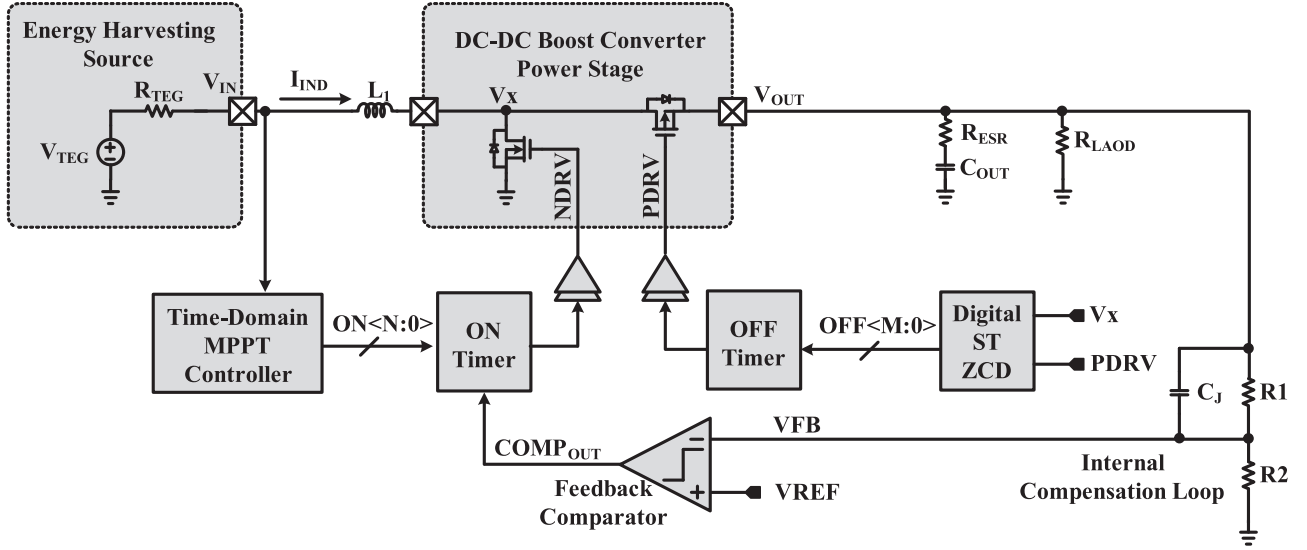
Fig. 4.   Top diagram of the proposed boost converter for energy harvesting system.
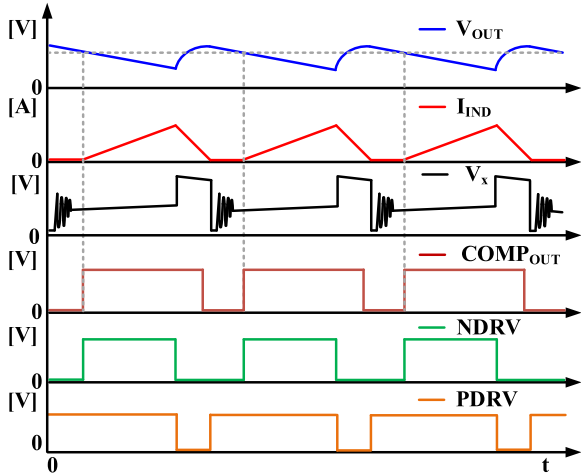

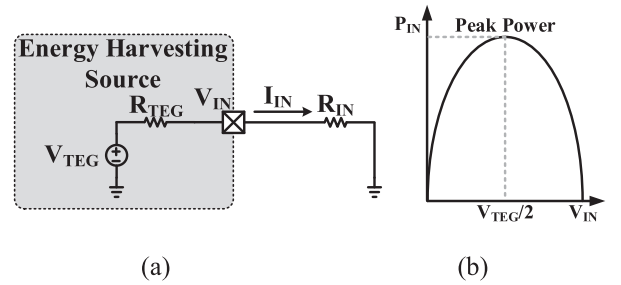Fig. 5.   Operation of the proposed boost converter.

Fig. 6.   (a) Model of TEG. (b) Relationship between input voltage and input voltage.

OFF time control and the zero current level of the inductor current are tracked. The OFF time control code is input to the OFF timer, and the OFF time pulse is generated proportional to OFF[M:0].

III. BUILDING BLOCKS

A. Time-Domain MPPT

Fig. 6(a) shows a modeled TEG with a voltage source (V_{TEG}) and internal resistance (R_{TEG}) [19], [20], [21].

When the boost converter is connected to the TEG, R_{IN} means the input impedance of the dc–dc boost converter. In this model, the input current of the boost converter is calculated by

$$I_{\text{IN}} = \frac{V_{\text{TEG}} - V_{\text{IN}}}{R_{\text{TEG}}}. \tag{1}$$

So, the input power of boost converter is shown as follows:

$$P_{\text{IN}} = V_{\text{IN}} \times I_{\text{IN}} = V_{\text{IN}} \times \frac{V_{\text{TEG}} - V_{\text{IN}}}{R_{\text{TEG}}}. \tag{2}$$

To find the maximum power point of TEG, the derivative equation of (2) is equal to 0, as shown in Fig. 6(b)

$$\frac{\partial P_{\text{IN}}}{\partial V_{\text{IN}}} = \frac{V_{\text{TEG}}}{R_{\text{TEG}}} - \frac{2V_{\text{IN}}}{R_{\text{TEG}}} = 0 \tag{3}$$

will be illustrated in this section. In Section IV, the experimental results are discussed. Finally, Section V concludes this article.

II. ARCHITECTURE OF THE PROPOSED BOOST CONVERTER

Fig. 4 shows the structure of the proposed boost converter. This boost converter consists of an ON timer, OFF timer, feedback comparator, the time-domain MPPT block, and the digital self-tracking ZCD (ST-ZCD). Fig. 5 shows the operation of the proposed dc–dc boost converter. The feedback comparator sets the switching timing. The feedback comparator compares the feedback voltage (VFB) divided by resistors with the reference voltage (VREF). The ON time duration of this converter is generated by ON timer. The ON time control by MPPT operation. The time-domain MPPT block selects the switching frequency for maximum efficiency. The digital ST-ZCD block decides the OFF time of this boost converter. The digital ST-ZCD block monitors the V_{X} node voltage and generates the OFF time control code OFF[M:0]. By controlling capacitor value in OFF timer, the
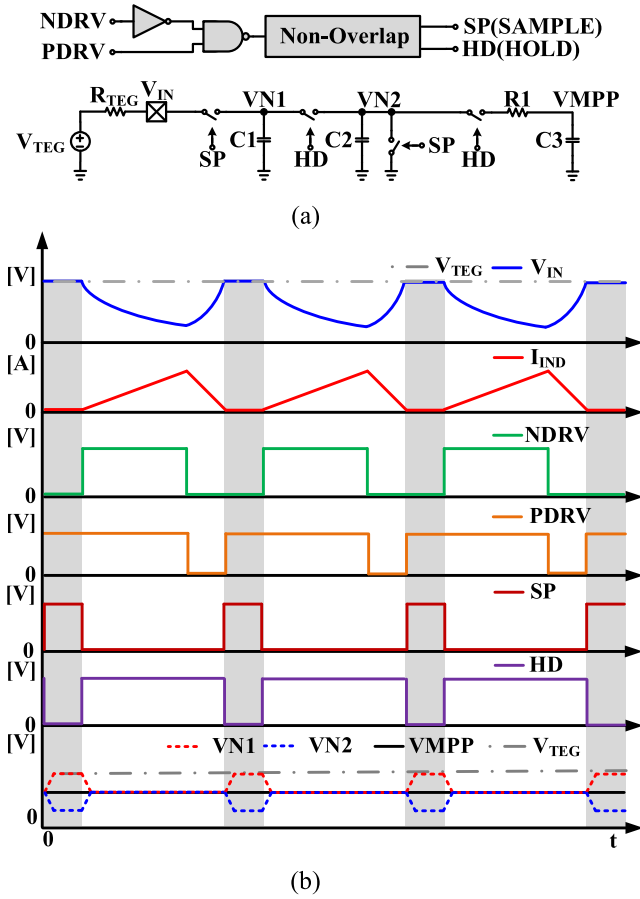
Fig. 7. (a) Structure of the proposed open-circuit VIN sensing. (b) Operation of the proposed open-circuit VIN sensing.

$$V_{\text{IN}} = \frac{V_{\text{TEG}}}{2}. \tag{4}$$

As (4) indicates, the input voltage should be half of the voltage of the open-circuit voltage to maximize the power of energy harvesting [22]. In order to meet this condition, the input voltage is compared with $V_{\text{TEG}}/2$ voltage, and adjusts the boost converter's time to control the boost converter's input voltage. To compare the input voltage, the open-circuit voltage needs the sense to generate the half of this voltage. In the proposed time-domain MPPT algorithm, by increasing the ON time control bit, the boost converter regulates half of the V_{IN} for maximum efficiency.

Fig. 7(a) and (b) show the proposed open-circuit V_{IN} voltage sensing structure and operation, respectively. The additional large series switch and OFF-time control are unnecessary. The boost converter operates in discontinuous current mode (DCM), and dead time between switching generates inherently. Furthermore, this dead time using for open-circuit input voltage sensing instead of an additional OFF-time slot. Because the input current does not flow from the energy source at this time, the voltage of the input source can make sense without a resistive voltage drop. This means that the artificial OFF-time slot does not need it because of using the boost converter's normal operation. Therefore, the oscillator and frequency dividing circuit are also
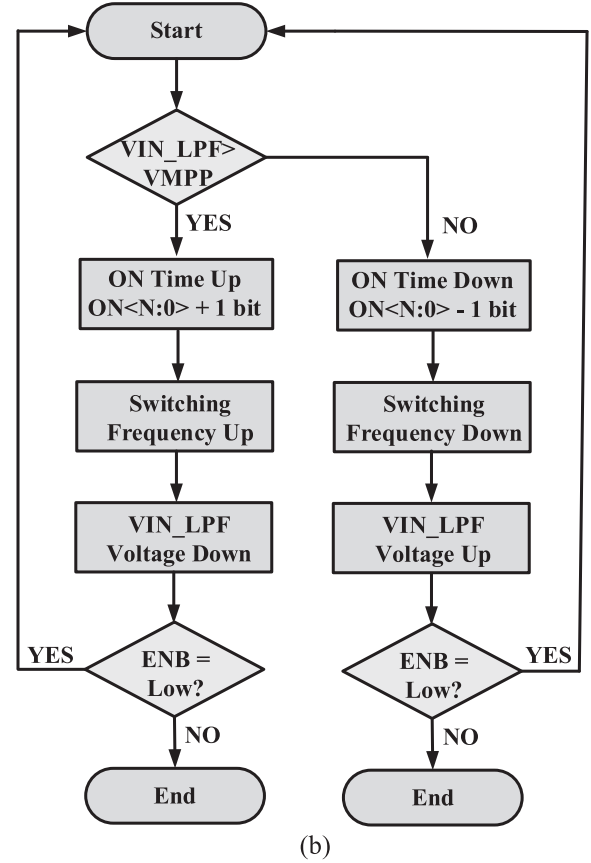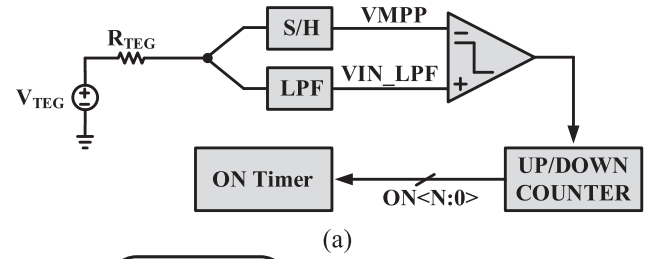

Fig. 8. (a) Structure of the proposed time-domain MPPT. (b) Operation of the proposed time-domain MPPT.

not needed. Furthermore, the other large switch series connects to the boost converter, and the internal clock frequency does not even use.

The reference voltage (VMPP) of the time-domain MPPT function is generated by the sampling and holding circuit. The input voltage is sampled at the dead time between switching. The sample (SP) and hold (HD) signals can generate using NDRV and PDRV power switch drive signals. At the dead time, the input voltage of the boost converter is sampled and stored in the sampling capacitor (C1). In the hold status, the sample voltage divides by x0.5 or x0.8 of the input voltage by charge sharing with capacitor C2. This VMPP node voltage compares with the low-pass filtered input voltage (VIN_LPF), and the ON time is determined by the compared result, as shown in Fig. 8(a).

The VMPP voltage is compared with the VIN_LPF voltage, which determines whether to increase or decrease the ON time, as shown in Fig. 8(b). If the VIN_LPF voltage is larger than
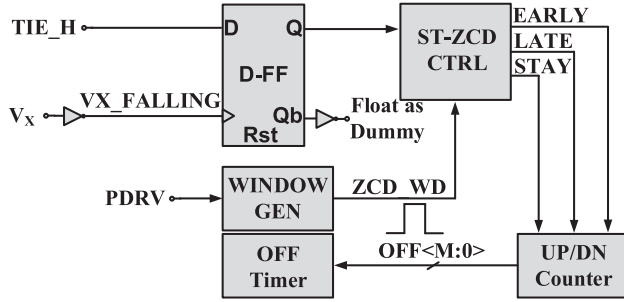
Fig. 9.   Proposed ZCD concept.

the reference voltage of the MPPT (VMPP), the timing of the boost converter should increase. Then, the VIN_LPF voltage is lowered. In contrast, if VIN_LPF is lower than the VMPP voltage, the timing of the boost converter should be reduced, and the VIN_LPF voltage will increase. By adjusting the time of the boost converter, the VIN_LPF voltage tracks the VMPP voltage, and the MPPT operation performs automatically.
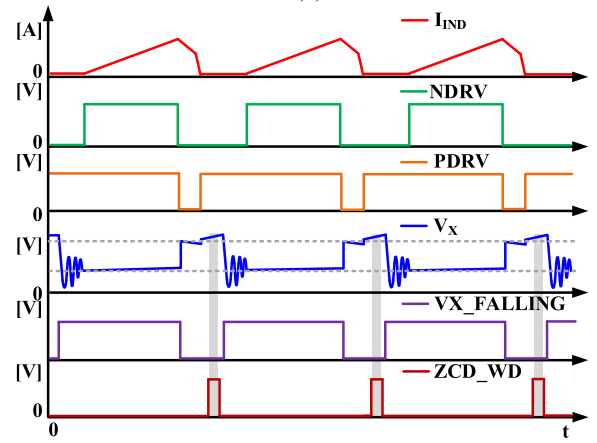
B. Digital ST-ZCD

In the case of conventional ZCD design, comparator is used to compare V_X and V_{OUT}, conventional ZCD design is depended on the comparator's offset and delay performance. The proposed digital ST-ZCD can detect zero current with low power consumption without depending on comparator performance, because of digital self-track V_X node, as shown in Fig. 9. First, the V_X node voltage's falling timing is monitored and detected using a D-flip flop. Because the comparator does not operate monitoring of $_{VX}$ node voltage, the performance of ZCD is not affected by the comparator's properties, such as offset and delay. The difference between the proposed concept and the work in [12], [13], [14], [15], and [16] is that the V_X node voltage's falling timing is detected by the D-flip flop's clock, which reacts to the edge of the signal. This concept's advantage is that the V_X node ringing caused by PMOS/NMOS power switch-OFF does not affect the ZCD operation, as shown in Fig. 3(b). The D-flip flop outputs the VX_FALLING signal once a switching, regardless of the V_X node's ringing. Because the ringing cannot affect the output of the D-flip flop, it is robust compared to the previous concept.

The VX_FALLING signal generated by the D-flip flop is compared with target V_X node falling time. The target time of the V_X node is the time at which the value of the inductor current is zero. Digital ST-ZCD CTRL controls UP/DN Counter using output of the WINDOW GEN for obtaining the target time. To prevent the OFF<M:0> code cycle in a steady state, the VX_FALLING signal time is compared with the target timing window (ZCD_WD), as shown in Fig. 10. After comparing the timing of VX_FALLING with ZCD_WD, the ST-ZCD CTRL determines whether the PMOS is required. The power switches OFF earlier or later than the target time. To start with, if the PMOS power switch OFF time is earlier than the target time, the OFF time of the boost converter should be greater than that shown in Fig. 10(b). In contrast, if the PMOS power is switched OFF
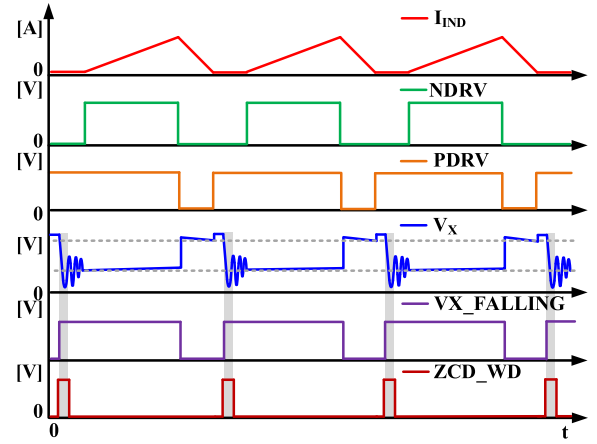
(a)

(b)
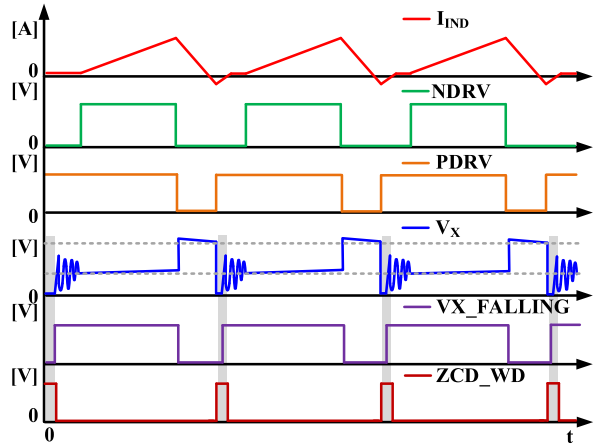
(c)

Fig. 10.   Timing diagram of digital ST-ZCD at (a) STAY status, (b) EARLY status, and (c) LATE status.

longer than the target time, the OFF time of the boost converter should be shorter, as shown in Fig. 10(c). If the rising edge of the VX_FALLING signal's is within the ZCD_WD signal, the OFF<M: 0> code is neither increment nor decremented. Therefore, by deciding whether the PMOS power switches OFF earlier or later, the OFF time of the boost converter can be controlled to meet zero inductor current.
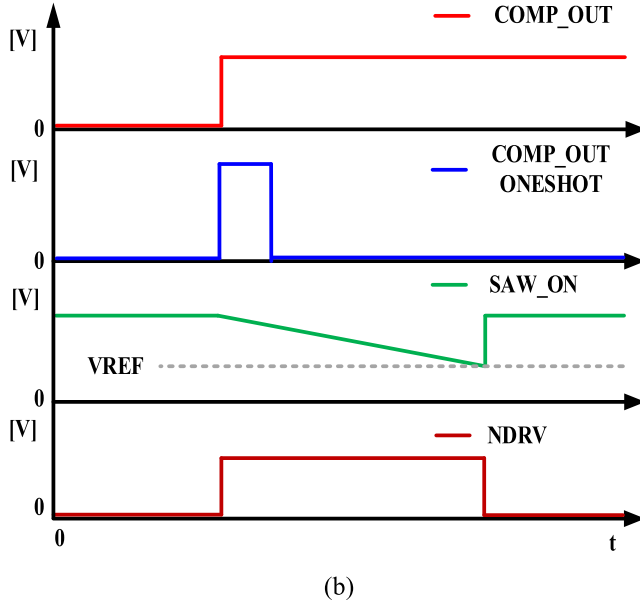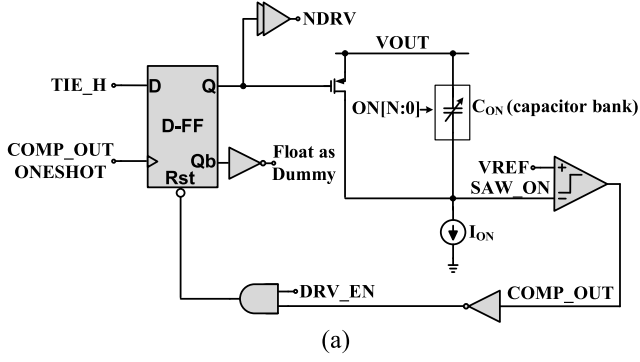
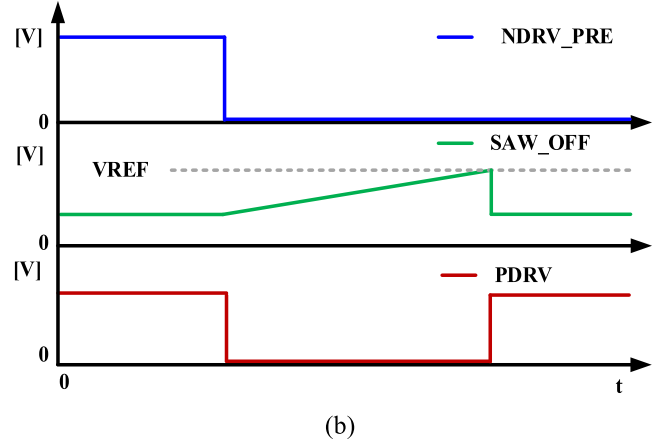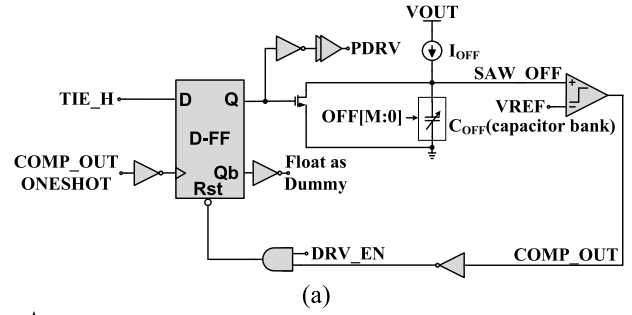Fig. 11.　(a) Structure of ON timer. (b) Operation of ON timer.

Fig. 12.　(a) Structure of OFF timer. (b) Operation of OFF timer.

Similar to the ON timer, the OFF time determines the charging of the capacitor C_{OFF} with a constant bias current I_{OFF} as shown Fig. 12(a). When the NMOS power switch is OFF, the PMOS power switch is ON, and if the VREF voltage is lower than the SAW_OFF node voltage, the D-flip flop is reset, and the PMOS power switch is OFF as shown Fig. 12(b).

IV. EXPERIMENTAL RESULTS

Fig. 13 shows the chip microphotograph. This chip fabricates with a 180-nm CMOS process, and the die area of the energy harvesting boost converter is 600 μm × 475 μm.

Fig. 14 shows the chip measurement board of the proposed dc–dc boost converter. This board comprises IC, an external inductor, and several ports for chip testing. There is a VDD and GND port for chip operation and V_{IN} and V_{OUT} pins of the dc–dc boost converter. To control the boost converter, the SPI control ports are used too.

Fig. 15 shows the simulation results of the time-domain MPPT operation. The reference voltage of MPPT (VMPP) is generated using dead times between switching. The low-pass filtered V_{IN} voltage (VIN_LPF) is compared with the VMPP voltage, and the ON time of the boost converter is adjusted by controlling the ON<4:0> code.

Fig. 16 shows the simulation waveform of the digital ST-ZCD operation. According to the timing of VX_FALLING, the EARLY, LATE, or STAY signals are generated and the OFF time of the boost converter is controlled by adding or subtracting the OFF<5:0> code.

The UP/DN counter generates the OFF-time control code OFF[M:0] by adding or subtracting one code from the earlier code. The adding or subtracting of OFF<M:0> decides the PMOS power switch's OFF timing. By adding one code to the OFF[M:0] stored in advance, the OFF time of the boost converter is longer. In contrast, subtracting the OFF[M:0] code reduces the OFF time of the boost converter.

C. ON/OFF Timer

The time-domain MPPT and digital ST-ZCD control blocks generate the ON/OFF time control code. Each code is input to ON/OFF timer blocks for control capacitor bank. Fig. 11(a) shows the proposed ON timer structure. The control code of ON time and real ON time of the boost converter is proportional. The ON time starts when the COMP_OUT triggers from low to high. C_{ON} discharge constant bias current I_{ON} and the SAW_ON node voltage is decreased with a constant slope decided by C_{ON} and I_{ON} as shown Fig. 11(b). The ON[N:0] code is decided in advance by the MPPT operation. When the SAW_ON node voltage is lower than the VREF voltage, the comparator in the ON timer is triggered, and the D-flip flop resets. The boost converter decides when to terminate the NDRV pulse and reset the D-flip flop.

Fig. 13.   Chip microphotograph of the proposed DC–DC boost converter.
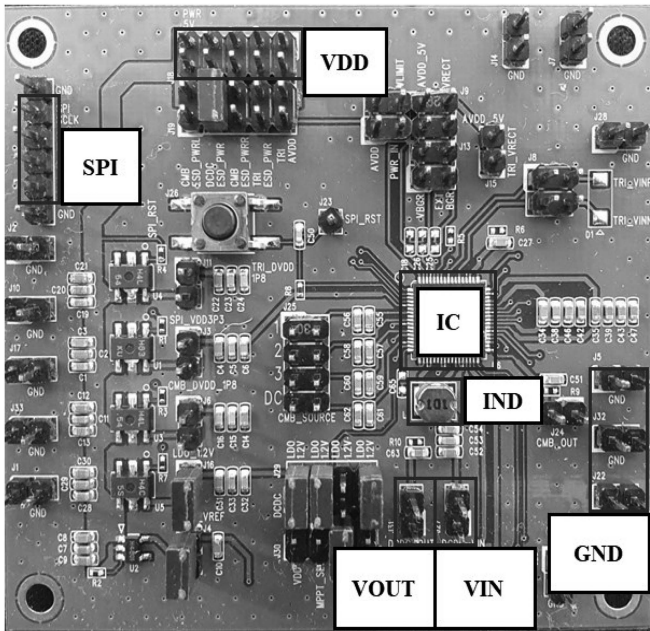
Fig. 14.   Measurement board of the DC–DC boost converter.

Fig. 15.   Time-domain MPPT simulation results of the boost converter.
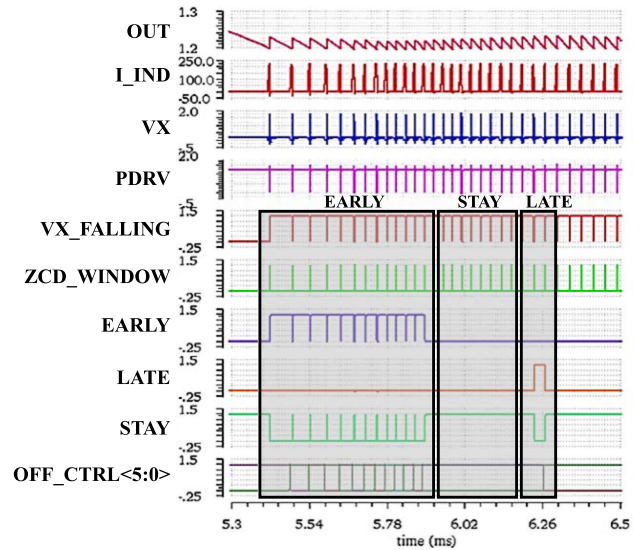
Fig. 16.   Digital ST-ZCD simulation results of the boost converter.
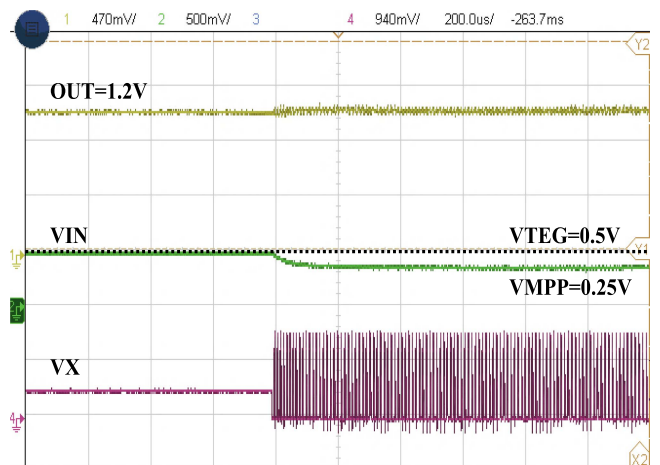
Fig. 17.   Measured waveform of the time-domain MPPT operation.

Fig. 17 shows the measured waveform of the energy harvesting boost converter. When the boost converter is operating, the input voltage of boost converter is controlled to MPPT target voltage (VMPP), such as the waveform of the time-domain MPPT operation simulation result. By observing the V_{IN} voltage regulation, the VMPP voltage also can be found out indirectly. The ON time of boost converter is also controlled to meet the MPPT target voltage. Finally, the operation of generating the MPPT reference voltage and controlling the ON time code, the V_{IN} voltage of boost converter is regulated to the MPPT target voltage and the maximum power tracking is functioned.

TABLE I
PERFORMANCE COMPARISON OF THE ENERGY HARVESTING BOOST CONVERTER WITH PRIOR WORKS

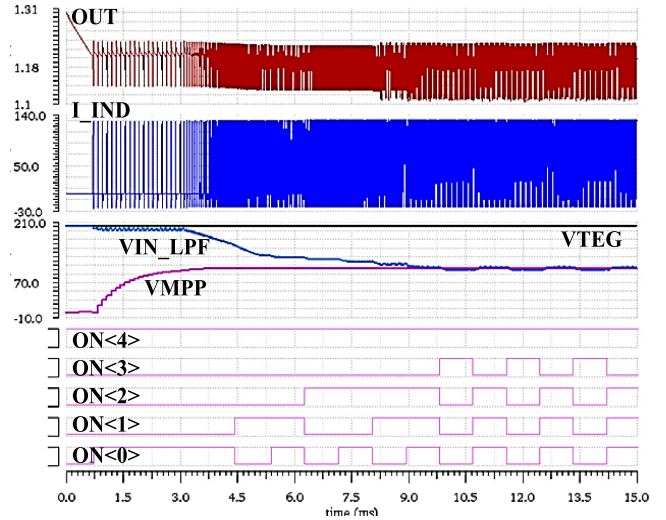| Reference		[9]	[10]	[15]	[18]	[23]	[24]	**This Works**
Process	nm	130	350	65	180	180	180	**180**
Application	-	Thermoelectric Energy Harvesting	Thermoelectric Energy Harvesting	Thermal Energy Harvesting	Autonomous Body-Heat Energy Harvesting	Thermal Energy Harvesting	Thermoelectric Energy Harvesting	**Thermoelectric generator Energy Harvesting**
MPPT	-	YES	YES	NO	YES	NO	YES	**YES**
Input Voltage Range	mV	$80-300$	$70-600$	$50-200$	$15-200$	$60-460$	$25-300$	**$200-700$**
Output Voltage	V	0.3	$3-5.8$	1.2	1.2	$1-1.8$	$25-300$	**1.2**
Load Current	mA	0.1	1	-	-	$0-1.3$	0.225	**$0.1-1$**
Input Inductor	μH	22	22	27	100	22	82 (transformer)	**100**
Output Capacitor	μF	4.7	10	1	1	0.05	-	**1**
Peak Efficiency	%	72.1	72.2	73	82	78.55	84	**85.5**
Die Area	mm^2	1.16	1.90	0.99	1.02	0.5292	1.6	**0.29**
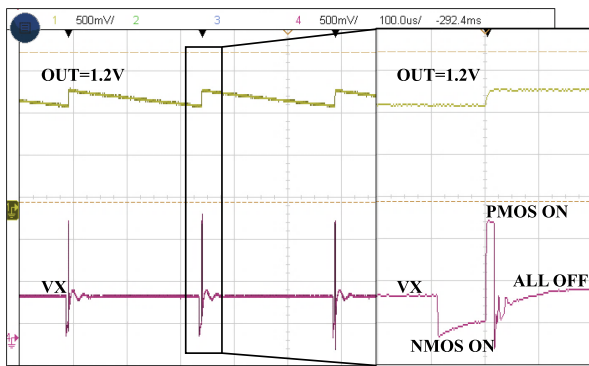
Fig. 18. Measured waveform of the digital ST-ZCD operation.
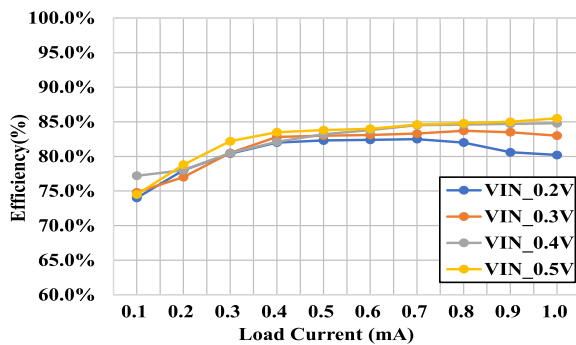
Fig. 19. Measured efficiency of the proposed energy harvesting boost converter.

Fig. 20. Measured quiescent current of the proposed energy harvesting boost converter at 0.1-mA load condition.

Fig. 18 shows the measured digital ST-ZCD waveform. After the PMOS is switched-OFF, no diode conduction loss detects in this waveform. By measuring the waveform of V_X node voltage, the steady-state condition is in STAY operation, and the ST-ZCD function is also operating.

Fig. 19 shows the measured efficiency of the proposed boost converter. Efficiency is measured when the proposed boost converter output voltage regulated 1.2 V. The peak efficiency is 85.5% at input voltage 0.5 V and the load current upper 1 mA.

Table I shows the performance comparison of the proposed energy harvesting boost converter with prior works of the low-voltage boost converter. This chip is fabricated with a 0.18-μm process. The proposed energy harvesting boost converter has
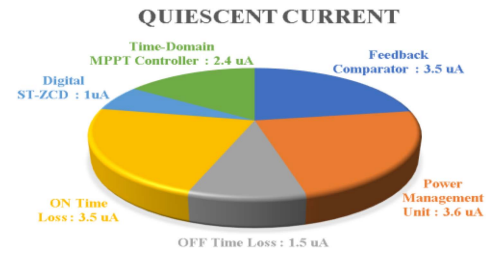
inductor size as 100 μH to minimize the conduction loss that can occur in metal routing and PCB parasitic, inductor size of 100 μH improves conduction loss on minimizing the inductor current slope. The proposed energy harvesting boost converter output capacitor is selected as 1-μF capacitor to drive an IoT device has operating current that 1 μA in several milliseconds. The proposed energy harvesting boost converter has wide input voltage and high efficiency by using time-domain MPPT and digital ST-ZCD. The proposed energy harvesting boost converter is an output voltage of 1.2 V and a current load range from 0.1 to 1 mA while supporting a wide input range from 0.2 to 0.7 V. This work has 0.29-mm^2 small die area using the proposed digital ST-ZCD that removes input PMOS switch. Furthermore, using the concept of the time-domain MPPT, the peak efficiency of the proposed energy harvesting boost converter is 85.5%. When using the proposed energy harvesting boost converter, an efficiency improvement of 1.5% to 13.4% is achieved when using the proposed concept compared to prior work. The power loss distributions consist of fixed internal power consumption in the internal block, inductor R_{on} loss, power transistor conduction loss, and power transistor switching loss. Fixed power consumption is consisting of internal operating block, total quiescent current is 15.5 μA at 0.1-mA load condition, as shown Fig. 20. The power loss of almost 10% is estimated from the inductor R_{on} and power transistor conduction loss and switching loss.

V. CONCLUSION

This article proposed a boost converter with the digital ST-ZCD for TEG energy harvesting applications. The proposed

method implements the time-domain MPPT concept using the dead time between switching in DCM mode, so additional series switching is unnecessary. This concept also does not require the additional time slot for MPPT generating slot used in open-circuit input voltage sensing. Because the input current does not flow from the energy source at this MPPT generating time using boost converter dead time. In this article, the digital ST-ZCD is proposed to operate with high efficiency. In this concept, the operation of the digital ST-ZCD is not affected by comparator performance and operated low power consumption due to not using a comparator. Also, by using the D-flip flop's clock, the detection of the V_X node falling edge is robust for the ringing of V_X node voltage. This chip fabricates with a 180-nm CMOS process. The area of the die is 600 μm $\times$ 475 μm. The measured peak efficiency of the energy harvesting boost converter is 85.5%.

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