Motor Overvoltage Mitigation by Active Cancellation of Reflections Using Parallel SiC Devices With a Coupled Inductor

Tim Lackie, *Student Member, IEEE*, Yunlei Jiang, *Member, IEEE*, Luke Shillaber, *Student Member, IEEE*, and Teng Long, *Member, IEEE*

***Abstract*—Employing high-switching-speed wide-bandgap devices improves the efficiency of industrial drive inverters but can result in motor overvoltages for shorter lengths of cable between the inverter and the motor. These overvoltages are caused by high-frequency impedance mismatches resulting in reflection of the voltage pulse edges of the inverter output. Forward and backward traveling reflections interfere and, in the worst case, cause double the dc-link voltage to appear across the motor terminals. In this article, this doubling of the motor voltage stress is observed with only a 10-m-long cable. To mitigate the motor overvoltage, a novel method using a differential-mode coupled inductor between the paralleled half-bridges and the phase output is proposed. By adding a delay time between the half-bridges at every switching event, a quasi-three-level output is produced that can actively cancel reflected voltage waves, eliminating the cause of motor overvoltages. The method can be utilized for three-phase inverters and, when using independently driven paralleled devices, only requires one additional inductor per phase. A design process for the coupled inductors is given, which aims to minimize the circulating current between the half-bridges and, therefore, give minimal increase in conduction losses due to imbalanced current sharing. These additional conduction losses and other limitations of the proposed method are analyzed. An inverter utilizing this proposed method is implemented and compared to a passive filter designed for overvoltage mitigation. The novel method achieves near perfect overvoltage mitigation with much smaller additional volume and much lower losses than that of the filter. Furthermore, the losses when using the active mitigation method are very similar to when using the inverter with no overvoltage mitigation.**

***Index Terms*—Circulating current, coupled inductors, industrial drive, inverter-driven motor, long cable, motor overvoltage, parallel devices, quasi-three-level, reflection cancellation, SiC MOSFETs, wide bandgap (WBG).**

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I. Introduction

PERFORMANCE metrics of switching power electronic converters can be substantially improved by utilizing wide-bandgap (WBG) devices. These new types of device, including SiC MOSFETs and GaN high-electron-mobility transistors, have significantly shorter switching times than those of Si devices. Converter switching losses can, therefore, be reduced, improving efficiency. Alternatively, the switching frequency can be increased without increasing the switching losses, and this allows physically smaller filters to be used, improving the power density [1]. However, depending on the application of the power converter, the shorter switching time can worsen the existing problems or introduce new problems.

One application, where the advantages and disadvantages of shorter switching times can be observed, is the use of dc–ac inverters to drive motors through a long cable [1], [2], [3], [4]. This includes variable-speed drives (VSDs) used in industrial settings. A system-level overview of an industrial drive inverter with a long cable is shown in Fig. 1 . The use of cables can cause the reflections of pulsewidth modulation (PWM) pulse edges to occur at the motor termination of the cable where there is a mismatch of high-frequency impedance. The reflections occur when the rise/fall time of the voltage pulse is of similar duration to the propagation time of the cable. This can be considered to impose a maximum dv/dt on the inverter pulse edge before reflections occur. Higher dv/dt values result in reflections on shorter cables because the propagation time of a cable is proportional to its length. With fast switching SiC MOSFETs, these reflections can occur with cable lengths as short as 3 m [5]. The reflected voltage edges will superimpose to cause significant overvoltages to appear at the motor terminals. This leads to greater than intended voltage stress on the winding insulation of the motor, with the overvoltage commonly having double the magnitude of the switching edge [1], [2], [3], [4]. In some cases, the magnitude can be even larger, such as when pulses are frequent enough that oscillations from previous pulses do not have time to decay before a new pulse arrives at the motor [3]. Overvoltages pose a problem for the insulation of motor windings, even if they have been designed in accordance to some insulation standards

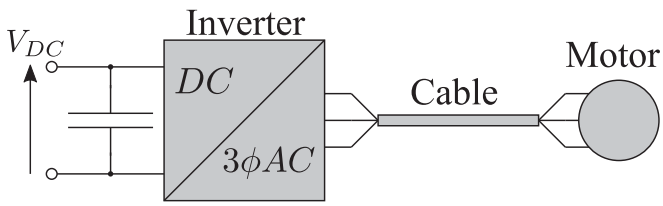


Fig. 1. System overview of the drive side inverter and cable connection for an industrial drive system.

specifically intended for inverter-fed applications [4]. Since the adoption of SiC MOSFETs means that these problems will occur with shorter cables, it is desirable to be able to mitigate these new occurrences of overvoltages. The main focus of this article is, therefore, to explore overvoltage mitigation methods for shorter cable lengths while retaining the benefits of SiC MOSFETs.

Increasing the rating of winding insulation cannot be considered a universal solution for all the applications that would be exposed to overvoltages, especially for retroactive upgrades of grid-connected motors to use VSDs. Other methods to mitigate these overvoltages have been proposed. These methods include passive and active approaches. Passive methods can utilize filters at the inverter output to either reduce the high dv/dt edges of the PWM waveforms [5], [6], [7], [8], [9], [10] or remove all high-frequency content from the waveforms to leave an approximately sinusoidal voltage output [11]. In either case, the overvoltages at the motor termination of the long cable can be effectively mitigated [4]. Alternatively, passive filters located at the motor terminals seek to match the impedance of the motor to the impedance of the cable removing the cause of reflections [6], [7], [10]. The implemented filters can be either first- or second-order filters. First-order filters can have high values of passive components and large volumes, whereas second-order filters introduce resonances that must be carefully placed in the frequency domain and damped by additional resistors [7]. In [5], an integrated *LC* filter is demonstrated to mitigate overvoltages. The volume of *LC* filters can be minimized by placing their resonant frequency above the switching frequency, as they only need to attenuate the high-frequency content, which contributes to sharp switching edges [9]. Losses in the damping resistances of passive filters, however, can be large and present significant barriers to achieving high efficiencies [8]. One proposed alternative is to use diodes to clamp the filter output voltages to the dc-link voltages, while the *LC* filter reduces the maximum dv/dt of the switching edge [12]. This method does not eliminate the damping losses and requires the addition of two diodes per phase. Overall, passive filters can be considered relatively simple and robust methods to mitigate overvoltages primarily by limiting the maximum dv/dt during switching events; however, they introduce additional volume and losses to the system.

In addition to passive methods, active methods of mitigating overvoltages caused by long cables exist and have been shown to be effective [13], [14]. These methods involve alternative control strategies [15], [16] often using additional or auxiliary switching devices [17] and/or some additional passive components [18], [19], [20], [21]. While many active techniques specifically intended for the mitigation of overvoltages exist and will be discussed here, it is worth noting that techniques with other primary objectives can sometimes help to at least partially mitigate overvoltages. This includes multilevel inverter topologies, where the voltage magnitude of each switching edge is reduced compared to a two-level inverter. As a result, the magnitude of reflected voltages is reduced, for example, limiting the magnitude of the overvoltage at the motor terminals to one and a half times the dc-link voltage when using a three-level converter compared to two times the dc-link voltage for a two-level converter [13]. An alternative method of utilizing a three-level PWM waveform is to insert a carefully timed mid-level pulse, which cancels out the reflected voltage wave and effectively removes overvoltages at the motor terminals [16], [17]. This technique is referred to as a quasi-three-level output. This has been demonstrated using a T-type three-level converter in [17] and using a single-phase full-bridge converter with a single-phase motor in [16]. Other methods have been proposed, which also seek to utilize a mid-level dwell time in the output voltage waveform to achieve reflection cancellation, and this can be achieved using coupled inductors connected to a low-voltage full bridge [21] or a network of passive components and auxiliary switching devices [20]. In both of these cases, a significant number of additional devices and passive components are required per phase.

Alternatively, active methods can be used in conjunction with a passive filter to reduce the dv/dt of the inverter output waveforms [19]. Doing so achieves similar results to a second-order passive filter without the damping losses; however, it introduces significant control complexity and will affect the conduction and switching losses of the semiconductor devices. Similar results can be obtained by using a soft switching technique with a switching duration carefully selected in a similar manner to the mid-level dwell time [18]. An auxiliary resonant commutated pole inverter is used in [18] to achieve the soft switching, which will reduce the switching losses of the main switching devices while achieving the mitigation of motor terminal overvoltage. However, the additional passive components, auxiliary switching devices and associated losses, and significant control complexities somewhat offset the benefits of this method. Furthermore, the elongation of the switching times negates one of the main benefits of using WBG devices. Finally, a method to mitigate any overvoltage events with greater than two times the switching edge voltage magnitude purely by using an adjusted PWM technique is given in [15]. This strategy does not only have any additional components or devices but also has limited utility as it has no effect on overvoltages less than two times the switching edge magnitude.

In summary, a variety of active techniques have been shown to effectively mitigate overvoltages due to voltage reflections on long cables, many of which utilize a mid-level dwell time in their voltage output waveforms. This article proposes and describes a new technique to utilize paralleled switching devices connected through a coupled inductor in each phase to synthesize a mid-level dwell time, with a straightforward control technique and no added resonances. This technique is independently proposed in [22]. Achieving this mid-level dwell time for each phase leg allows this novel method to be used for three-phase inverters,

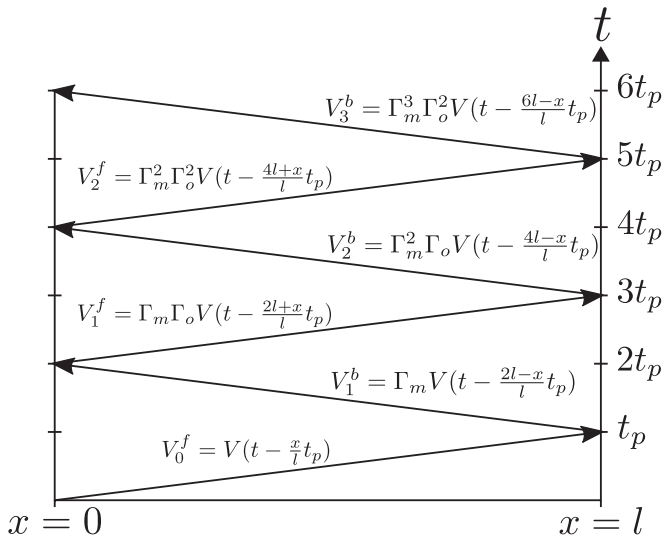


Fig. 2. Bounce diagram for an inverter connected to a motor through a long cable. $V(t)$ is the time-domain representation of an incident voltage pulse at $x = 0$, the common form of which is given in (1).

such as those in common industrial VSDs and those shown in Fig. 1. Furthermore, the novel method retains the high switching speeds and, hence, low switching losses of WBG devices.

The rest of this article introduces the proposed method, explains its principles of operation, details its design, and provides a comparison of its performance to an *LC* dv/dt filter implementation. Section II provides an explanation of the occurrence of overvoltages and how a mid-level dwell time can be used to cancel voltage reflections. Section III details the operation of the proposed overvoltage mitigation technique. Section IV compares its design to a passive filter. Section V presents and explores experimental results to assess the suitability and performance of the novel method. Finally, Section VI concludes this article.

II. Occurrence of Overvoltages

The cause of overvoltages at the load termination of long cables is well understood and presented in the literature [2], [3], [17]. A summary of the relevant mechanisms and important results will be given here.

The root cause of overvoltages is the occurrence of voltage reflections due to high-frequency impedance mismatches at both the terminations of the cable. There is significant high-frequency content associated with the fast rising voltage pulse edges of an inverter output voltage [1], and it is the content that undergoes reflections. These voltage edges are modeled as a function of time (t) in (1) with a linear rise time of t_r and a final value equal to the dc-link voltage (V_{DC})

$$V(t) = \begin{cases} \frac{V_{\text{DC}}}{t_r} t, & 0 \le t \le t_r \\ V_{\text{DC}}, & t > t_r \end{cases}. \tag{1}$$

By considering the cable as a transmission line, the forward and backward traveling reflections, denoted as V^f and V^b, respectively, can be modeled using a bounce diagram [17], as in Fig. 2. The important parameters for understanding the voltage reflections are the cable length l, propagation time t_p, reflection coefficient between cable and motor Γ_m, and the reflection coefficient between cable and inverter Γ_o. A cable's propagation time is dependent upon the cable length as well as the velocity of electromagnetic waves in the cable v, with the following relations:

$$t_p = \frac{l}{v} \tag{2}$$

$$v = \frac{1}{\sqrt{LC}}. \tag{3}$$

It is defined that L is the cable inductance per meter, and C is the cable capacitance per meter. The characteristic impedance of the cable Z_c is defined as follows:

$$Z_c = \sqrt{\frac{L}{C}}. \tag{4}$$

Using the characteristic impedance, as well as the motor and inverter impedances, Z_m and Z_o, seen by the cable, the reflection coefficients at each termination are derived as follows:

$$\Gamma_o = \frac{Z_o - Z_c}{Z_o + Z_c} \tag{5}$$

$$\Gamma_m = \frac{Z_m - Z_c}{Z_m + Z_c}. \tag{6}$$

The values of Z_m and Z_c can be found for real cables and motors using the techniques detailed in [23] and [24]. However, in the high frequency range of interest, Z_m will usually be large compared to Z_c, as it is dominated by the inductances of the motor [2], [7], [8], [9]. Furthermore, the impedance looking into the inverter terminals cannot be straightforwardly measured, and therefore, it must be assumed that since a voltage-source inverter is being used, then Z_o will be very small compared to Z_c [7]. As a result, the approximations of (7) and (8) can be usefully employed

$$\Gamma_o \approx \frac{-Z_c}{Z_c} = -1 \tag{7}$$

$$\Gamma_m \approx \frac{Z_m}{Z_m} = 1. \tag{8}$$

These reflection coefficients can be used in conjunction with the bounce diagram of Fig. 2 to create theoretical time-domain waveforms for the inverter voltage (V_o) and motor terminal voltages (V_m). To model the inverter voltage pulse, it is defined that $V_o = V(t)$ from (1). The result is shown in Fig. 3, where it can be seen that the frequency of voltage oscillations at the motor terminals f_{Osc} is determined entirely by the propagation time of the cable t_p [3], as follows:

$$f_{\text{Osc}} = \frac{1}{4t_p}. \tag{9}$$

Oscillations of the cable current and voltage due to reflections will appear as resonances in the impedance response of the cable in the frequency domain. Therefore, by measuring the cable impedance and observing the series resonant frequency, the propagation time can be inferred [2]. Fig. 4 shows the measured differential-mode (DM) line–line impedance of the

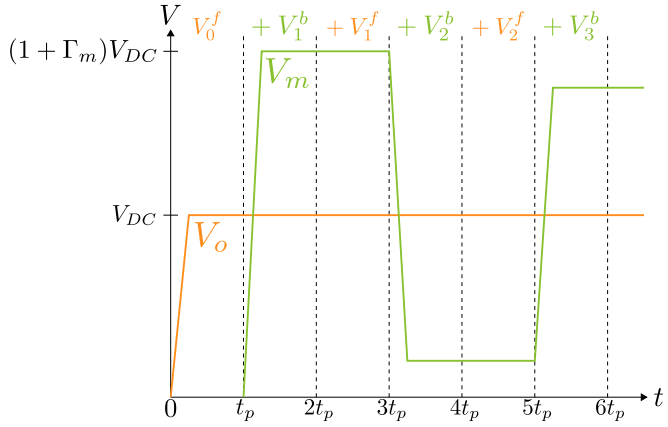


Fig. 3. Theoretical representation of the time-domain voltage waveforms at the motor and inverter terminals.

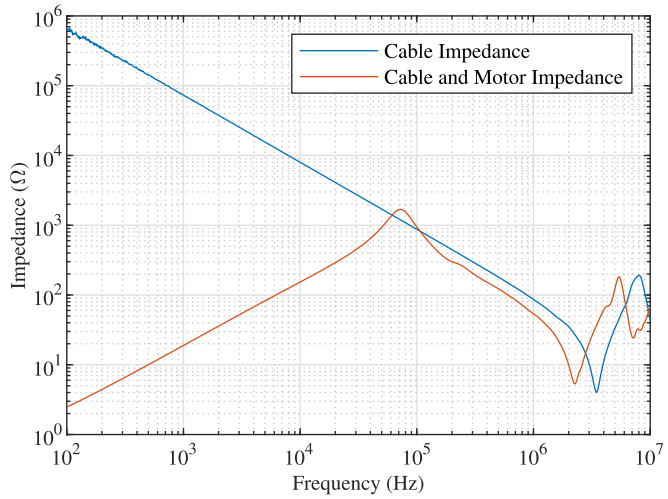


Fig. 4. Measured DM impedance of the cable and the cable connected to the motor. The 10-m-long 5× 40 mm^2 core cable and three-phase induction motor detailed in Table I are used. The low-frequency DM inductance of the motor is 3.7 mH.

cable terminated in an open circuit as in [23] and the DM line–line impedance of the cable terminated by an induction motor. The series resonant frequency in these two cases is different, with the open-circuit termination giving a resonant frequency of 3.469 MHz and the motor termination giving 1.995 MHz. As a result, the effective propagation time in each case will be different with 72 ns predicted by the open-load measurements and 125 ns predicted for the motor terminated measurement. By observing the motor terminal overvoltage with the same experimental configuration, shown in Fig. 5, the observed frequency of oscillations is 1.97 MHz. It can be seen that the observed oscillation frequency matches well with the resonant frequency of the cable terminated by the motor. Since this gives a significantly different value of effective propagation time when compared to using the open-circuit cable, the impedance response of the cable terminated by the motor should be used to infer the propagation time, which will occur in the real system.

While the oscillation frequency of the reflected voltages depends only upon the cable propagation time, the magnitude of

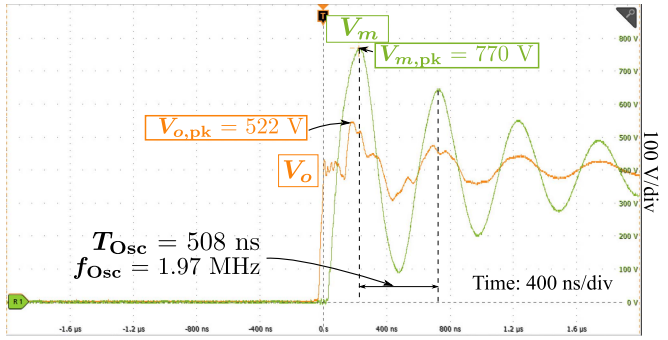


Fig. 5. Experimental measurement of the line–line voltages at the inverter output (V_o) and at the motor terminals (V_m). The rise time (t_r) of V_o is 20 ns. A 10-m-long cable with five cores of 4-mm^2 stranded copper conductors is used, which has a propagation time of 125 ns. This cable is terminated by a three-phase induction motor. Details of the inverter, cable, and motor are given in Table I.

overvoltage at the load terminals depends upon both the inverter rise time and the cable propagation time. When the application of only one pulse is being considered, the magnitude of the motor terminal voltage can never be greater than twice the dc-link voltage V_{DC}. This is evident from the fact that $|\Gamma_m| \leq 1$ when only passive impedances are considered ($Z_m, Z_c > 0$) [17]. If the pulse rise time (t_r) of the inverter is less than $2t_p$, then this worst case 100% overvoltage will be observed at the motor terminals for times t, where $t_r + t_p < t < 3t_p$. This is shown in Fig. 3. If instead the rise time is greater than $2t_p$, then, by referring to Fig. 2, the peak motor voltage will be achieved at $3t_p$ just before the V_1^f wave reflected from the inverter reaches the motor. Therefore, the peak motor voltage will be observed in both the cases at a time of $3t_p$. The magnitude of this peak voltage is, therefore, given in the following equation, derived for the pulse edge given in (1):

$$\begin{aligned} V_m(3t_p) &= V_0^f(3t_p) + V_1^b(3t_p) \\ &= V(2t_p) + \Gamma_m V(2t_p) \\ &= (1+\Gamma_m)\frac{2V_{\mathrm{DC}}t_p}{t_r}. \end{aligned} \tag{10}$$

For cases where $t_r > 4t_p$, the true peak voltage may not be achieved until sometime after $5t_p$, and the peak voltage will then be less than twice V_{DC}[18]. As such, the worst case overvoltage can be seen to occur when $t_r \leq 2t_p$, and the maximum observed motor voltage is $(1+\Gamma_m)V_{\mathrm{DC}}$. This results in effectively double the peak voltage being applied across the motor terminals compared to the output of the inverter.

Experimental waveforms for an inverter driving a motor with no overvoltage mitigation are shown in Fig. 5, and the observed time-domain behavior of the motor voltage can be seen to agree with the waveforms in Fig. 3. In this case, the motor voltage matches the predicted behavior when $t_r < 2t_p$. One difference is the presence of voltage oscillations at the inverter output, which results in a 36% overvoltage to occur here. These oscillations occur due to a real-world nonzero value of Z_o. In this article, the measurement point of the output voltage for a phase leg is positioned at the common connection point of two parallel half-bridges. The common connection was made using

the lengths of wire for experimental flexibility. These wires introduce parasitic inductance, giving a nonzero value of Z_o at high frequencies. Reflections observed at this measurement point are not considered to be disadvantageous and are instead a result of experimental limitations. At the motor terminals, a 92.5% overvoltage is observed. This is also due to a nonideal reflection coefficient at the motor termination. The theoretical description of the motor overvoltage phenomenon can, therefore, be seen to be a useful tool to predict peak motor overvoltages, especially in the worst cases where the inverter rise time is much shorter than the cable propagation time.

III. Proposed Method to Mitigate Motor Overvoltages

This section will outline the theory behind the insertion of a mid-level voltage dwell time to actively cancel voltage reflections caused by the long cable. Inverters that utilize this method are said to have a quasi-three-level output. A new control technique and inverter circuit design to implement this mitigation method will be proposed. The use of this technique for overvoltage mitigation is independently proposed in [22]. Beyond proposing the new technique, in this article, it will be described and analyzed, which will be used to detail a design methodology to implement it. Finally, the implications of this novel design will be explored, including the effect on achievable modulation indices and on the conduction losses.

A. Use of a Mid-Level Voltage Dwell Time to Cancel Reflections

Inserting a mid-level voltage dwell time into the voltage pulse edges can be used to cancel out voltage reflections on long cables [13], [16], [17], [20]. This will split the pulse edge into two voltage pulses each of half the magnitude, and with a time delay between them. By setting this time delay to be twice the propagation time of the cable, the reflections of the first half-pulse edge at the motor will always be 180° out of phase with the reflections from the subsequent half-pulse edge. This is shown in the theoretical time-domain waveforms of Fig. 6, where the reflections caused by each of the two half-pulse edges are shown separately, as well as their resulting superposition [17]. The addition of an A subscript denotes the contributions of the first half-pulse, and the addition of a B subscript denotes the contributions of the delayed half-pulse. The time-domain representation of voltage contribution at the inverter for the first half-pulse is denoted as $V_{o,A}(t)$ and given in (11), and for the delayed half-pulse, the contribution to the inverter voltage is $V_{o,B}(t)$ and given in (12). Both of these representations are defined relative to the standard pulse edge given in (1). The superposition of both the half-pulses gives the complete behavior of the inverter voltage, as given in (13), and of the motor voltage given in (14)

$$V_{o,A}(t) = \frac{1}{2}V(t) \tag{11}$$

$$V_{o,B}(t) = \frac{1}{2}V(t - 2t_p) \tag{12}$$

$$V_o(t) = V_{o,A}(t) + V_{o,B}(t) \tag{13}$$

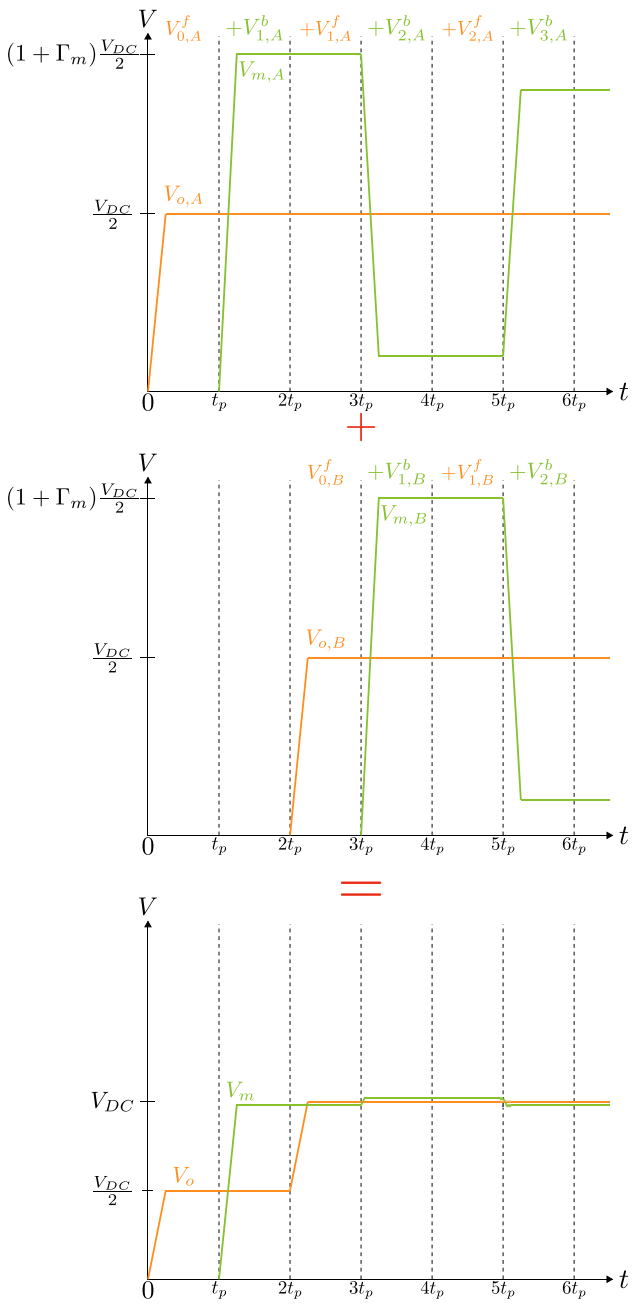


Fig. 6. Expected waveforms for a pulse edge with a mid-level dwell time set at $2t_p - t_r$, showing how this can be seen as the superposition of two half-level pulses with a time delay of $2t_p$ between them.

$$V_m(t) = V_{m,A}(t) + V_{m,B}(t). \tag{14}$$

By considering Fig. 6, it can be seen that the peak motor voltage will appear by a time of $5t_p$ when $t_r < 2t_p$. Using the bounce diagram of Fig. 2 to consider the reflections of both the half-pulses using (11) and (12), the peak voltage at the motor terminals can be found analytically using (14) and is given in (15). When $\Gamma_m \approx 1$ and $\Gamma_o \approx -1$, then the resultant peak motor voltage is approximately V_{DC}. Thus, the motor overvoltage can be effectively mitigated using this method

$$V_m(5t_p) = V^f_{0,A}(5t_p) + V^b_{1,A}(5t_p) + V^f_{1,A}(5t_p)\ldots$$

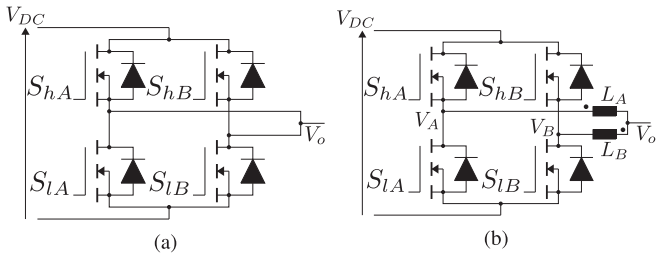


Fig. 7. (a) Circuit diagram for a single phase leg of directly connected parallel half-bridges. (b) Single phase leg of the proposed coupled parallel half-bridges.

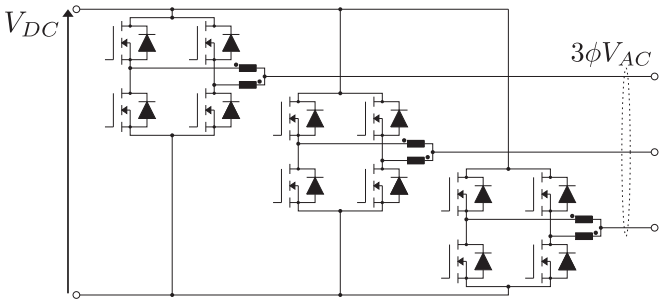


Fig. 8. Circuit diagram for a three-phase inverter utilizing the proposed coupled parallel half-bridges.

$$
\begin{aligned}
&+ V^b_{2,A}(5t_p) + V^f_{0,B}(5t_p) + V^b_{1,B}(5t_p) \\
&= \frac{1}{2}\big((1+\Gamma_m)V(4t_p) + (1+\Gamma_m+\Gamma_m\Gamma_o\ldots \\
&\quad + \Gamma_m^2\Gamma_o)V(2t_p)\big) \\
&= \frac{V_{\text{DC}}}{2}\left(2+2\Gamma_m+\Gamma_m\Gamma_o+\Gamma_m^2\Gamma_o\right). \qquad (15)
\end{aligned}
$$

Previously, the circuit topologies used to implement a mid-level voltage dwell time have T-type phase legs in [13] and [17], a single-phase full bridge in [16], and half-bridge phase legs each with an auxiliary circuit in [20]. In the following sections, a new implementation will be discussed, which utilizes paralleled half-bridge legs with a coupled inductor per phase output to produce the mid-level dwell time [22], [25], [26]. This circuit is shown in Fig. 7(b) for one phase leg, which can be repeated to give as many phases as needed. A three-phase inverter using this overvoltage mitigation method is therefore possible, and its schematic is shown in Fig. 8. Using a simple time-delay control strategy, the dwell time can be controlled to equal $2t_p - t_r$ [16]. The delay time duration to achieve this is $2t_p$. In applications where paralleled devices are used to meet power requirements, this only requires the addition of one passive component per phase, while having an easily implemented control strategy. As a result, the new paralleled device implementation presents a novel method to mitigate motor overvoltages due to long cables with minimal system-level tradeoffs.

B. Reflection Cancellation Using Paralleled Half-Bridges

In applications requiring output currents that are large enough to cause the conduction losses in a single half-bridge phase leg to be prohibitively large, two or more half-bridges are connected in parallel per phase leg. The structure of a single phase leg connected in this way is shown in Fig. 7(a). Doing this will share the current approximately equally between the half-bridges, reducing the effective ON state resistance ($R_{\text{DS,on}}$). It is assumed that there are four devices per phase leg in this article, although each of these devices can itself be made of several devices in parallel. Traditionally, the high-side devices, denoted S_{hA} and S_{hB}, can be driven by a single gate driver. This also applies for the lower devices, denoted S_{lA} and S_{lB}.

Alternatively, the paralleled half-bridges can be connected together through inductances L_A and L_B, as shown in Fig. 7(b). These inductances can be uncoupled, or they can be DM coupled as shown in Fig. 7(b). Using coupled inductors is the preferable option. It is assumed that the DM coupling coefficient, k, is close to 1. It is also assumed that the self-inductances of both the windings, L_A and L_B, are approximately equal, and therefore, the DM inductance seen by any voltage difference between the two half-bridges in the phase leg, denoted by L_{cir}, is given in as follows:

$$
\begin{aligned}
L_{\text{cir}} &= L_A + L_B + 2k\sqrt{L_A L_B} \\
L_{\text{cir}} &\approx 4L_A = 4L_B. \qquad (16)
\end{aligned}
$$

In addition to the inductor coupling, each of these half-bridges in parallel is controlled by an independent gate drive signal. Therefore, the system will gain an additional degree of freedom, equivalent to a quasi-three-level output [25], [26]. To achieve the third voltage levels, the two half-bridges (S_{hA}, S_{lA} and S_{hB}, S_{lB}) must be switched asynchronously. One of the half-bridges will be driven with a time-delay relative to the other half-bridge, and this will be the lagging half-bridge, which will be half-bridge B in this article. Bridge A is, therefore, the leading half-bridge and, therefore, receives the drive signals first.

During the dwell time period, the relation between the half-bridge currents i_A and i_B and the output and circulating currents i_o and i_{cir}, which are all shown in Fig. 9, is given in (17)–(20). The currents i_A and i_B can be split into DM and common-mode (CM) components from the perspective of the two half-bridges. This means that the CM currents are those which flow exclusively onto the output line, and DM currents flow only between the half-bridges. From this viewpoint, i_o is the sum of the CM currents from both the half-bridges and i_{cir} is the DM component of i_A and i_B

$$
\begin{aligned}
i_{\text{cir}} &= \frac{i_A - i_B}{2} \qquad (17) \\
i_o &= i_A + i_B \qquad (18) \\
i_A &= \frac{i_o}{2} + i_{\text{cir}} \qquad (19) \\
i_B &= \frac{i_o}{2} - i_{\text{cir}}. \qquad (20)
\end{aligned}
$$

The DM currents are caused by voltage differences between half-bridges, which are dropped across the DM inductance L_{cir} between them, which is summarized as follows:

$$
v_A - v_B = L_{\text{cir}}\frac{di_{\text{cir}}}{dt}. \qquad (21)
$$

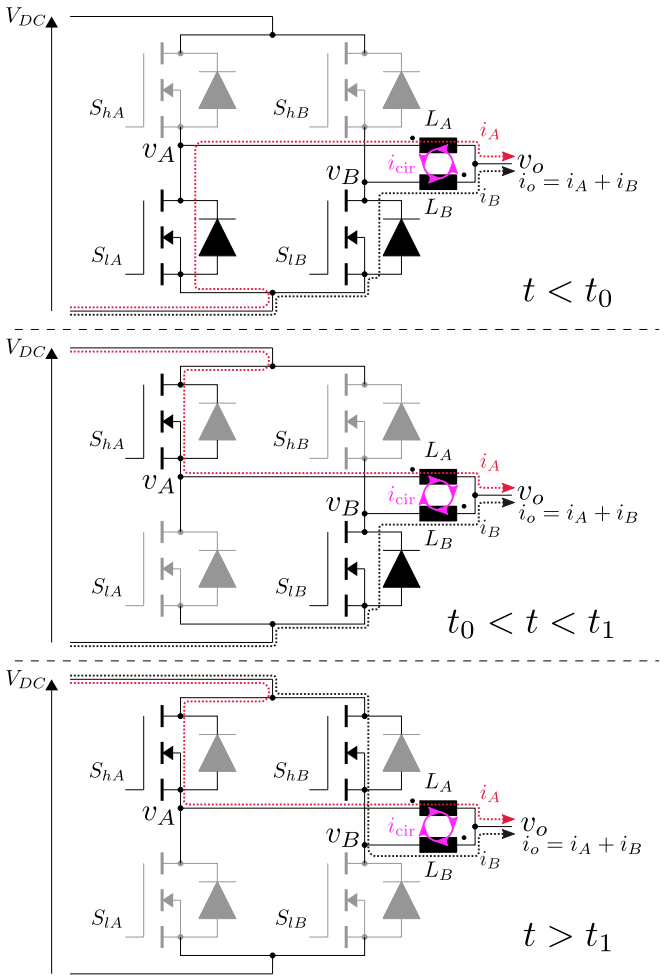


Fig. 9. Circuit diagrams showing three different stages involved in the complete switching of the output voltage state.

The sequence of device switching states to synthesize the mid-level dwell time for a rising edge voltage output is shown in Fig. 9. This operation can be split into three time periods: $t < t_0$, $t_0 \leq t < t_1$, and $t \geq t_1$, as shown in Fig. 10.

1) First Time Period, $t < t_0$: Initially, both the half-bridges are in the same state, and they will share the output current i_o. The current will not be shared equally, so while $i_A + i_B = i_o$, $i_A \neq i_B$. In Fig. 9, it is assumed that initially, $V_o = 0$, and therefore, both the low-side MOSFETs S_{lA} and S_{lB} are reverse conducting. During this initial period, the channel resistances of the MOSFETs, $R_{\text{DS,on}}$, will actually result in a small voltage difference between the half-bridges, which is given as follows:

$$v_A - v_B = -R_{DS,\text{on}}(i_A - i_B). \tag{22}$$

This voltage is dropped across the DM inductance between the half-bridges, denoted here as L_{cir}, and therefore, this will result in a slow rate of change in the circulating current, i_{cir}, which is given in (23). The magnitude of this current change will, however, be small and so will be neglected for this analysis

$$\frac{di_{\text{cir}}}{dt} = -\frac{R_{DS,\text{on}}(i_A - i_B)}{L_{\text{cir}}}. \tag{23}$$

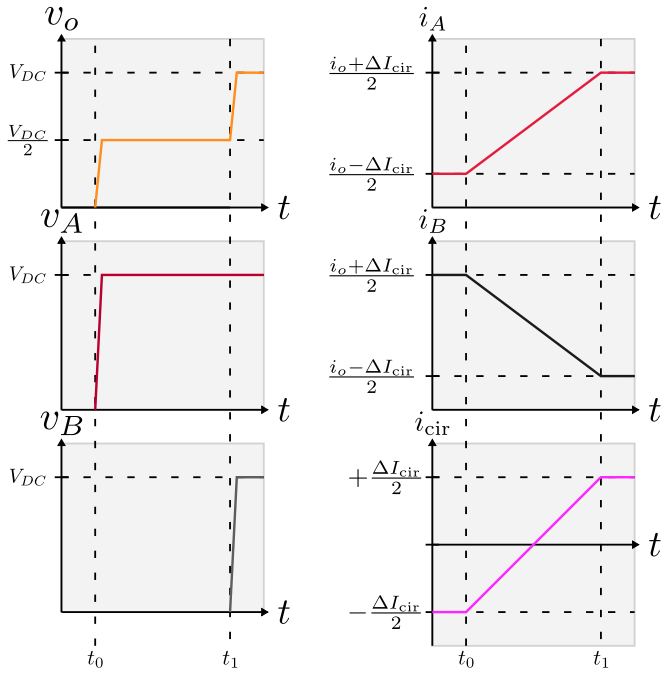


Fig. 10. Waveforms showing how the currents i_A, i_B, and i_{cir} and the voltages v_A, v_B, and v_o vary over the duration of one rising edge transition of the phase output.

2) Second Time Period, $t_0 \leq t < t_1$: At the beginning of the state transition, first, S_{lA} is turned OFF and then S_{hA} is turned ON with the current i_A commutating to the upper device. During this period, the circulating current will begin to change quickly, which will change the values of i_A and i_B, while i_o remains approximately constant, as it is set by the output circuit. In this state, the voltage difference between the half-bridges, and hence the voltage drop across the DM inductance, is given as follows:

$$v_A - v_B = V_{\text{DC}}. \tag{24}$$

Since the voltage applied across the circulating inductance during this period is V_{DC}, there will be a constant rate of change of circulating current over this period. As identified in Section III-A, it is desirable to set the duration of this period to $2t_p$, which will cancel the voltage reflections and mitigate motor overvoltage. As a result, the change in circulating current during the dwell time, ΔI_{cir}, can be found by using the following:

$$\Delta I_{\text{cir}} = \frac{2V_{\text{DC}}t_p}{L_{\text{cir}}}. \tag{25}$$

The output voltage v_o is the CM component of the half-bridge voltages; therefore, during the dwell period, the output voltage is given as follows:

$$v_o = \frac{v_A + v_B}{2} = \frac{V_{\text{DC}}}{2}. \tag{26}$$

3) Final Time Period, $t \geq t_1$: Once the $2t_p$ duration dwell period is finished, the second half-bridge will change state. Switch S_{lB} will be turned OFF, and then, S_{hB} will be turned ON so that the current i_B is now being sourced from the positive terminal of the dc link. After this time, the voltage difference between the outputs of the two half-bridges will be the same as that defined in

(23), and therefore, there is negligible change in the circulating current. Furthermore, the output of the phase leg will now be V_{DC}, and therefore, both the output voltage and the circulating current will be approximately constant until the next change of state of the phase.

For the falling edge transition, the same analysis can be performed, and the result will be similar, but ΔI_{cir} will have the opposite sign but the same magnitude as the value found with (25). The result of this is that the circulating current will change direction every time, and the phase changes state with no dc component of the circulating current. The waveforms for the voltages v_A, v_B, and v_o and the currents i_A, i_B, and i_{cir} for a rising edge of the phase output are shown in Fig. 10.

C. Implications of the Parallel Device Active Reflection Cancellation Method

Implementing a modulation method for a converter requires only that a time delay can be inserted between the gate drives of the two half-bridges . Since each of the half-bridges has to have independent gate drive signals, it is required that there must be double the number of gate driver circuits. This will present additional costs and complexity and could impact reliability. Most common types of modulation would be suitable with the leading half-bridge of each phase being modulated as normal and the lagging half-bridge having the same gate drive signals but delayed by $2t_p$. It must be ensured that a dead time is still inserted for each half-bridge, and this must be shorter than the dwell time. This can be done straightforwardly in software.

The introduction of the dwell time will present a limit on the range of duty cycles, which are valid. For a switching period of T_{sw}, the minimum and maximum possible duty cycles, D_{min} and D_{max}, are given by

$$D_{\text{min}} = \frac{2t_p}{T_{\text{sw}}} \tag{27}$$

$$D_{\text{max}} = \frac{T_{\text{sw}} - 2t_p}{T_{\text{sw}}}. \tag{28}$$

Because of this limited range of duty cycles, when used in an inverter, the range of modulation index, M, will also be constrained. The maximum valid modulation index, M_{max}, is given as follows:

$$M_{\text{max}} = 1 - 2D_{\text{min}} = 1 - 4f_{\text{sw}}t_p. \tag{29}$$

In this equation, it is clear that the modulation index is limited by both the propagation time of the cable being used, t_p, and the switching frequency of the converter, f_{sw}. To give the widest range of modulation index, both of these values should be kept small; however, t_p is set by the cable, and therefore, only the switching frequency can be adjusted. For very long cable lengths, t_p could become large enough to result in a limiting value of maximum modulation index. This would limit the suitability of the proposed mitigation method if it were to be applied for high switching frequencies and long cables. The proposed technique is, therefore, suitable for applications, where WBG inverters could result in the occurrence of voltage reflections that would not occur with slower switching speed

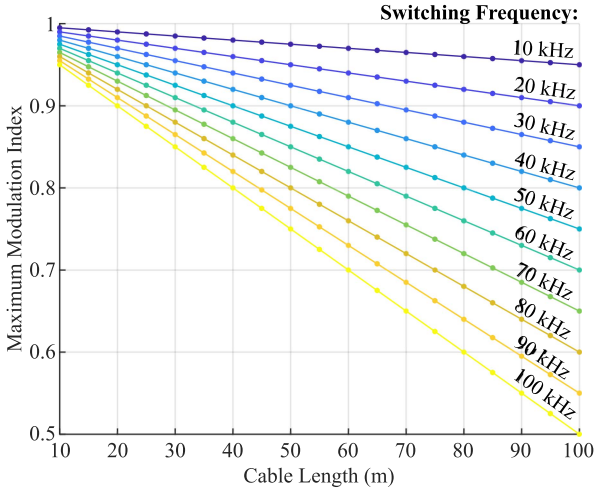


Fig. 11. Achievable maximum value of the modulation index (M_{max}) for varying switching frequencies and varying cable lengths. The per-meter propagation time is set based on the cable parameters specified in Table I.

inverters. In these applications, the WBG devices still switch at high speeds keeping hard switching losses low and, hence, retaining a major benefit of WBG devices. The effect of the cable length and switching frequency on the achievable modulation index is shown in Fig. 11.

The circulating current that is introduced between the half-bridges of each phase will result in one of the half-bridges carrying more current than the other at every point in time. It means that the conduction losses in each phase are greater than they would be if each half-bridge carried an equal share of the current. The power losses due to conduction in each phase ($P_{\text{Con,Ph}}$) are given in (30), where I_o is the amplitude of the fundamental component of the phase output current, and ω_0 is the fundamental angular frequency

$$\begin{aligned} P_{\text{Con,Ph}} &= \frac{\omega_0 R_{\text{DS,on}}}{2\pi} \int_0^{\frac{2\pi}{\omega_0}} \left(\left(\frac{I_o}{2}\cos(\omega_0 t) + \frac{\Delta I_{\text{cir}}}{2} \right)^2 \dots \right. \\ &\quad \left. + \left(\frac{I_o}{2}\cos(\omega_0 t) - \frac{\Delta I_{\text{cir}}}{2} \right)^2 \right) dt \\ &= R_{\text{DS,on}} \left(\frac{I_o^2}{4} + \frac{\Delta I_{\text{cir}}^2}{2} \right). \end{aligned} \tag{30}$$

Large magnitudes of circulating current will, therefore, increase the conduction losses in the inverter. Furthermore, over one fundamental cycle, it is possible that the leading half-bridge will carry a higher magnitude of current for a larger proportion of the time. This will depend upon the power factor ($\cos(\phi)$) of the load and also upon the modulation index (M). At low frequency, the currents in the leading half-bridge ($i_A(t)$) and in the lagging half-bridge ($i_B(t)$) are given in (31) and (32), respectively. Simulated waveforms for these half-bridge currents are shown in Fig. 12:

$$i_A(t) = \frac{1}{4}\left(1 + M\cos\left(\omega_0 t\right)\right)\left(I_o\cos\left(\omega_0 t + \phi\right) + \Delta I_{\text{cir}}\right) \tag{31}$$

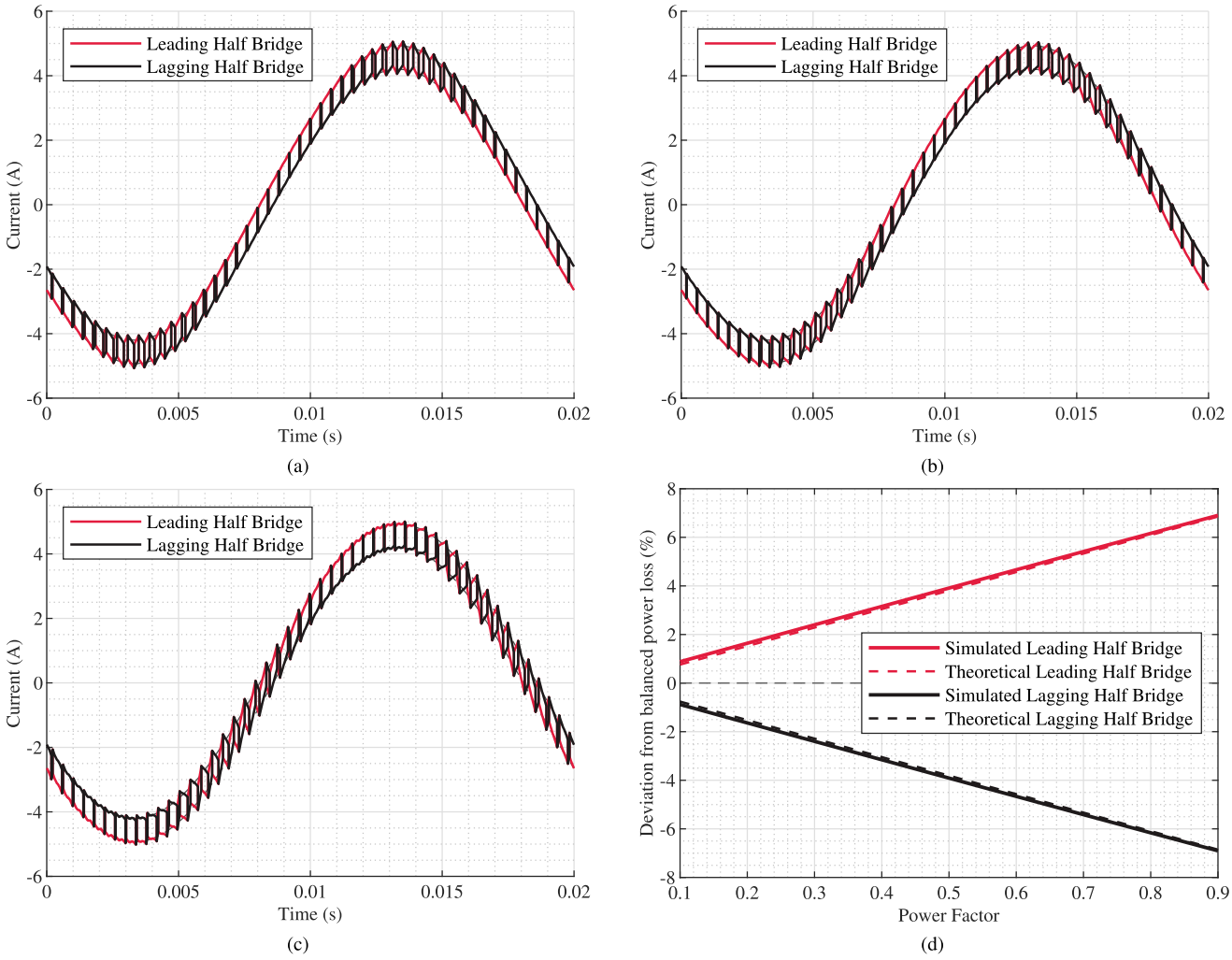


Fig. 12. Currents in the leading and lagging half-bridges of one phase of the proposed inverter, which were simulated in MATLAB for a power factor of 0.1 in (a), 0.5 in (b), and 0.9 in (c). These simulations use a load impedance with a constant magnitude of 20 Ω at a fundamental frequency of $f_0 = 50$ Hz, $L_{\text{Cir}} = 136\ \mu$H, $M = 0.913$, $f_{\text{sw}} = 2.5$ kHz, and $t_p = 125$ ns. In (d), the percentage difference of the half-bridge conduction losses relative to half of the total conduction losses of the phase ($\pm\Delta P_{\text{Con,AB}}/P_{\text{Con,Ph}}$) is shown with the power factor, both using MATLAB simulations and the theoretical equations in (30), (34), and (35).

$$i_B(t) = \frac{1}{4}\left(1 - M\cos\left(\omega_0 t\right)\right)\left(I_o\cos\left(\omega_0 t + \phi\right) - \Delta I_{\text{cir}}\right). \tag{32}$$

The resulting difference in conduction losses between the leading and lagging half-bridges of one phase is denoted as $\Delta P_{\text{Con,AB}}$ and given as follows:

$$\begin{aligned}\Delta P_{\text{Con,AB}} &= \frac{\omega_0 R_{DS,\text{on}}}{2\pi}\int_0^{\frac{2\pi}{\omega_0}} i_A(t)^2 - i_B(t)^2\, dt \\ &= R_{DS,\text{on}}\frac{M I_o \Delta I_{\text{cir}}\cos(\phi)}{2}.\end{aligned} \tag{33}$$

Finally, the conduction losses in the leading half-bridge is denoted as $P_{\text{Con,A}}$ and in the lagging half-bridge as $P_{\text{Con,B}}$. These are given as follows:

$$P_{\text{Con,A}}(t) = \frac{1}{2}\left(P_{\text{Con,Ph}} + \Delta P_{\text{Con,AB}}\right) \tag{34}$$

$$P_{\text{Con,B}}(t) = \frac{1}{2}\left(P_{\text{Con,Ph}} - \Delta P_{\text{Con,AB}}\right). \tag{35}$$

The percentage difference between conduction losses in each half-bridge compared to evenly shared conduction losses ($\pm\Delta P_{\text{Con,AB}}/P_{\text{Con,Ph}}$) is shown in Fig. 12(d) for varying power factors. This is performed using MATLAB simulations as well as the theoretical method above, which both show good agreement. Differences between the simulated and theoretical values are due to the inclusion of ripple current in the simulations. Power factors close to unity result in less even sharing of the conduction losses between leading and lagging half-bridges. This can be understood by observing how the proportion of time that the leading half-bridge has a greater magnitude of current varies across Fig. 12(a)–(c).

To overcome this unequal loss distribution, an active method to ensure equal power sharing over short time scales is detailed in [26]. Over long time scales, equal power sharing can be achieved by changing which half-bridges are leading/lagging every fundamental cycle. In the rest of this article, applications with both the nonunity power factor and the low modulation index will be considered, and therefore, the unequal losses are considered to be small enough to not need compensating for.

D. Design Process for the Coupled Inductor Used for Active Overvoltage Mitigation

The performance of the circulating inductor is central to the operation of the proposed inverter. For minimal system-level impact, the coupled inductor must limit the magnitude of the peak to peak circulating current, ΔI_{cir}, as given in (25). This will minimize conduction losses in the converter, as given in (30), and the copper losses in the inductor windings. Furthermore, this should be achieved with a volume no larger than necessary. These parameters need to be split into design objectives and design constraints.

The design equations for the coupled inductors are given in (36)–(39), where $\Re$ is the total reluctance of the core, including any air gaps, in H $^{-1}$, l_e is the effective length of the core in meters, l_g is the length of the air gaps in meters, μ_0 is the permeability of free space in H$\cdot$ m^{-1}, μ_r is the relative permeability of the magnetic core material, μ_e is the effective relative permeability of the whole magnetic path, A_e is the effective area of the core in m^2, N is the number of turns in each winding, and k is the differential-mode coupling coefficient between the windings

$$\mu_e = \frac{\mu_r l_e}{l_e + \mu_r l_g} \tag{36}$$

$$\Re = \frac{l_e}{\mu_e \mu_0 A_e} \tag{37}$$

$$L_{\text{cir}} = 2(1+k)\frac{N^2}{\Re} \tag{38}$$

$$\Delta B = (1+k)\frac{N\Delta I_{\text{cir}}}{\Re A_e}. \tag{39}$$

By substituting (25) into (38) and (39), alternative representations for the flux density and change in circulating current can be found, which are given as follows:

$$\Delta I_{\text{cir}} = \frac{2V_{\text{DC}} t_p \Re}{2(1+k)N^2} \tag{40}$$

$$\Delta B = \frac{2V_{\text{DC}} t_p}{2NA_e}. \tag{41}$$

The inductor core loss depends upon the magnetic flux density (ΔB), and the losses of the MOSFETs depend upon ΔI_{cir}, as described in (30). It would, therefore, be beneficial to reduce both of these values, which from (40) and (41) can be achieved simultaneously by increasing the number of turns in the coils N. However, to keep the resistance (R) of the coil the same, the effective cross-sectional area of the coil wire must, therefore, be increased due to the larger number of turns resulting in a longer length of wire (l_w). This relation is given as

$$R = \frac{4\rho_{\text{Cu}} N l_M}{\pi d_w^2}. \tag{42}$$

where ρ_{Cu} is the resistivity of copper, d_w is the diameter of the wire, and l_M is the mean length of wire per turn.

When the magnitude of I_o is less than the magnitude of ΔI_{cir}, the circulating current causes the direction of the MOSFET current to reverse, which will enable zero-voltage switching turn-ON for all the switching devices [27], [28]. This can result in reductions of switching losses when the line current is close to zero; however, this effect is not a primary design goal and, therefore, is not considered when designing the circulating inductor.

In this article, the design objectives are to minimize both core flux and circulating current. The design is constrained by a selected core, which defines all l_e, A_e, μ_r, and l_M. The wire diameter (d_w), upper limits on the winding resistances (R_{Max}), and the core peak flux density (B_{pk}) are also all constrained. The values of these constraints are given in Table II. An example of the feasible range of ΔI_{cir} and the core flux ($\Delta\phi$) for inductors subjected to the listed design constraints is shown in Fig. 13.

TABLE I
DESIGN SPECIFICATIONS FOR THE EXPERIMENTALLY IMPLEMENTED INVERTER AND MOTOR SYSTEM

	Design Parameter	Value
Inverter	Inverter Power Rating, S_{Rated} (kVA)	5
	Number of phases	3
	Half-bridges per phase	2
	DC-link Voltage, V_{DC} (V)	400
	Power supply model	Magnapower TS 4U
	Fundamental frequency range, f_0 (Hz)	0-50
	Switching frequency, f_{sw} (kHz)	10
	Switching devices	IMZA65R048M1H
	Rise time, t_r (ns)	20
	Modulation technique	Sinusoidal PWM
	DSP model	Texas Instruments TMS320F28379D controlCARD
	FPGA model	Terasic DE0-Nano Altera Cyclone IV
Cable	Cable model	4-mm^2 SY 5 core
	Cable length (m)	10
	Cable propagation time, t_p (ns)	125
Motor	Induction motor model	Brook Crompton 160A419219
	Motor connection	3ϕ, Delta connection
	Motor rated voltage (V)	400
	Motor rated current (A)	33
	Motor rated frequency, f_0 (Hz)	50
	Motor rated power (kW)	18.5
	Motor DM Inductance, L_{DM} (mH)	3.7

TABLE II
DESIGN PARAMETERS FOR THE EXPERIMENTALLY IMPLEMENTED COUPLED INDUCTORS

Design Parameter	Value
Self-Inductance, L_A/L_B (μH)	34.2
Inductor core geometry	PQ26/20
Effective magnetic path length, l_e (mm)	46.3
Effective magnetic area, A_e (mm^2)	119
Relative permeability, μ_r	3300
Peak magnetic flux density, B_{pk} (mT)	200
Number of turns per coil, N	7
Number of coupled coils	2
DM coupling coefficient	1
Air gap length, l_g (mm)	0.2
Maximum resistance per coil, R_{Max} (mΩ)	5
Wire diameter, d_w (mm)	1

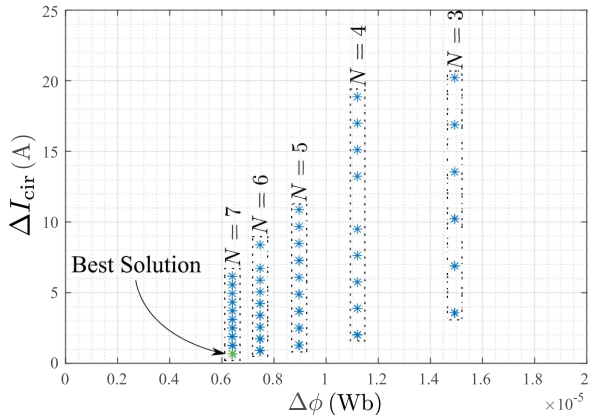


Fig. 13. Plot of the achievable values of circulating current and core flux for different inductor designs, indicating the location of the best inductor design. The design constraints are applied from Table II, which also lists the design parameters corresponding to the best solution marked in the figure.

In order to achieve the design objectives, a two-stage design process is used. First, the number of turns in each coil (N) is maximized. This is done using (42) and subject to the constraint that $R < R_{\text{Max}}$. An additional constraint must be added to ensure that the number of turns of the specified wire can physically fit into the available window area of the selected magnetic core. In this article, the packing arrangement of the wire turns was modeled in MATLAB and compared against the window area. The largest value of N that satisfies both of these constraints is selected. Second, the value of $\Re$ should be minimized to keep ΔI_{cir} as small as possible. This is done by selecting the smallest value of the air gap length l_g. The lower boundary on the value of l_g is constrained by the core flux due to the CM current in each coil and the imperfect differential-mode coupling between coils. This additional core flux must be kept low enough to ensure that the total magnetic flux density in the core never exceeds B_{pk}.

The inductor design process is applied for a drive system with the specifications provided in Table I. For this case, the circulating current and core flux for the selected solution are shown in Fig. 13. The selected parameters for the implemented coupled inductors are shown in Table II.

IV. Comparison of the Proposed Active Method to a Passive *LC* dv/dt Filter

To compare overvoltage mitigation methods, a dv/dt filter is designed to meet the specifications in Table I. An inverter output *LC* filter is selected, as shown in Fig. 14(a). The design processes from [8] and [9] are employed to limit the peak motor line–line voltage to less than 20% over the dc-link voltage. Equations (43)–(45) are from [8] and [9], where the peak permissible motor line–line voltage is given as $V_{m,l-l,\text{pk}}$ in volts, the critical rise time of the pulse edges is given as $t_{r,\text{crit}}$ in seconds, the filter inductance (L_f) is in henries, and the filter capacitance (C_f) is in farads. The losses of a given filter design (P_{loss}) are estimated as described in [8] with the damping resistor losses considered

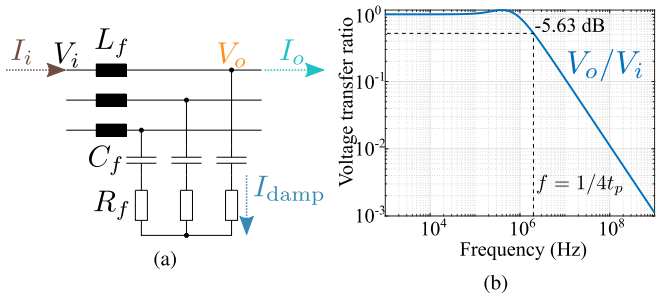


Fig. 14. (a) Passive dv/dt filter circuit. (b) Frequency-domain transfer response between input voltage and output voltage.

TABLE III
Design Parameters for the Experimentally Implemented *LC* dv/dt Filter

Design Parameter	Value
Inductance, L_f (μH)	8
Inductor core geometry	PQ26/20
Effective magnetic path length, l_e (mm)	46.3
Effective magnetic area, A_e (mm^2)	119
Relative permeability, μ_r	3300
Peak magnetic flux density, B_{pk} (mT)	200
Number of turns per coil, N	9
Number of coils	1
Air gap length, l_g (mm)	1.4
Maximum resistance per coil, R_{Max} (mΩ)	10
Wire diameter, d_w (mm)	1
Capacitance, C_f (nF)	10
Damping Resistance, R_f (Ω)	56
Power dissipation (W)	20

as dominant and given in (46)

$$V_{m,l-l,\text{pk}} = \left(\frac{3t_p\Gamma_m}{t_{r,\text{crit}}} + 1\right) V_{\text{DC}} \tag{43}$$

$$t_{r,\text{crit}} \leq \sqrt{L_f C_f} \tag{44}$$

$$R_f = 2\sqrt{\frac{L_f}{C_f}} \tag{45}$$

$$P_{\text{loss}} = \frac{12 f_{\text{sw}} V_{\text{DC}}^2 C_f}{\pi^2} \tag{46}$$

These equations are applied to the design parameters of Table I. Importantly, (46) shows that the losses in the dv/dt filter are actually independent of the value of damping resistance chosen and instead depend upon the amount of energy transferred into the filter capacitance [12], [14], [29]. Therefore, a value of 10 nF for C_f is selected, which is small enough to limit losses, but large enough that the filter inductance can be implemented using the same magnetic core as the coupled inductor of Table II. The required value of L_f is 8 μH. A damping resistance (R_f) of 56 Ω is required, and this can be freely selected to meet damping requirements without appreciably increasing the losses. The finalized filter design parameters are given in Table III, and the voltage transfer function for the filter is shown in Fig. 14(b). A slightly underdamped response is achieved with -5.63-dB attenuation by the resonant frequency of the cable.

The losses in the resistors require them to be mounted on a heat sink, which is selected for forced convection air cooling

using a fan. This gives a reasonable compromise between system volume and cooling complexity.

The power losses of the different methods of overvoltage mitigation are simulated in MATLAB for the inverter with specifications given in Table I. To utilize publicly available switching energy data, however, SCTWA35N65G2 SiC MOSFETs are used for the device modeling [30]. The inverter operation was simulated when using no overvoltage mitigation, the proposed active overvoltage mitigation using the L_{Cir} of Table II, and the passive overvoltage mitigation method using the filter specified in Table III. To do this, the desired apparent power and effective inductance seen by the inverter at the fundamental frequency are used to calculate the modulation index and fundamental component of the load current. Then, the output voltages of the inverter half-bridges are created in the time domain by using a software-defined sinusoidal PWM modulator. These voltages are decomposed into DM and CM components from the perspective of both the three-phase output and the parallel half-bridges of each phase. The effective inductances seen at the switching frequency in each of these modes are used to calculate the output ripple currents and any circulating currents. These can be combined with the fundamental output current to define the full piecewise linear representation of the half-bridge currents. Examples of how these currents combine to define the half-bridge currents when using the proposed active mitigation method are shown in Fig. 12. Switching device losses can be calculated from these currents, as can be the losses in any passive components, P_{Pass}. For the filter, the losses due to damping are calculated as described in [14]. Magnetic core losses are not included in the simulations.

The results of these simulations are given in Fig. 15. In Fig. 15(a), the total losses as a percentage of the supplied apparent power are given for all the three considered mitigation methods. It can be seen that the passive mitigation method shows much greater losses than those of the active mitigation method. Furthermore, the power losses from the active mitigation method are similar to when no mitigation method is used. This is shown in more detail in Fig. 15(b) where particularly at light loads the active method reduces turn-ON losses. However, as the load apparent power increases, the additional conduction losses and losses in the coupled inductor contribute to slightly increased overall losses compared to when no mitigation method is used.

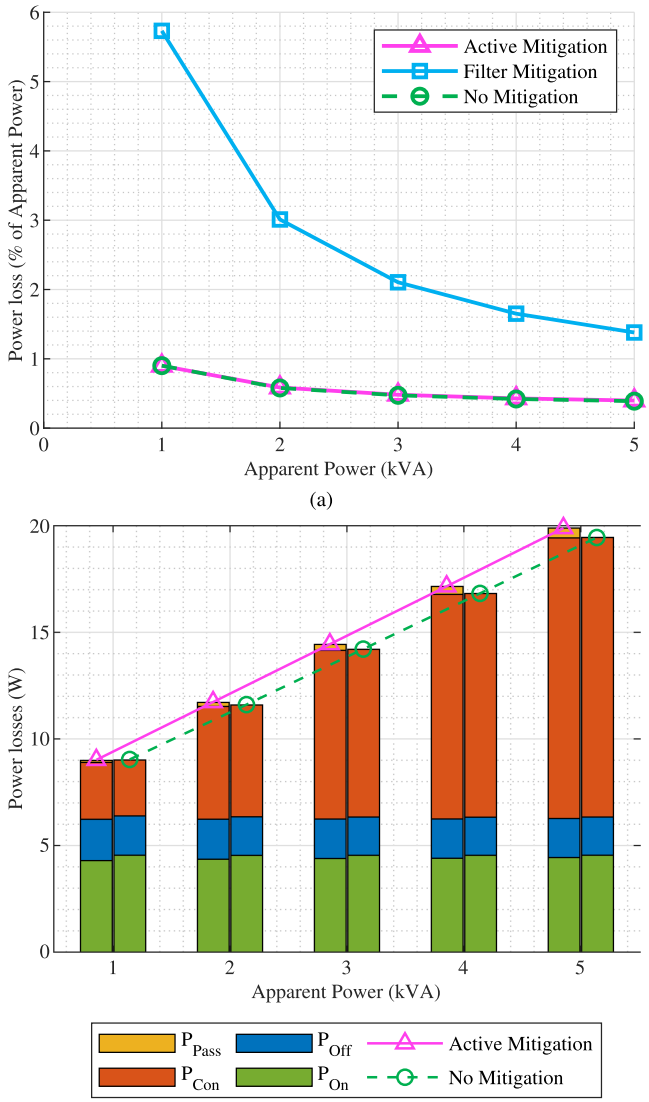


Fig. 15. Predicted converter losses for a 5-kVA rated three-phase inverter with two half-bridges per phase, a 400-V DC-link voltage, $f_{\text{sw}} = 10$ kHz, and fundamental frequency of $f_0 = 50$-Hz driving a "wye" connected load with power factor of 0.15 and constant inductance of $L_{\text{load}} = 33$ mH. The passive mitigation method uses $L_f = 8\,\mu$H, $C_f = 10$ nF, and $R_f = 56\,\Omega$, as described in Table III. The active mitigation method assumes a propagation time of $t_p = 125$ ns and $L_{\text{cir}} = 136\,\mu$H. In (a), the simulated losses are compared for the inverter using no overvoltage mitigation, the proposed active mitigation method, and the described passive mitigation method. Simulations are performed in MATLAB. In (b), the causes of power losses are shown for the active mitigation method, and when no mitigation method is employed. P_{ON}, P_{OFF}, and P_{Con} describe the total turn-ON, turn-OFF, and conduction losses, respectively, for all the devices. P_{Pass} describes the total power losses in any passive components in the system (excluding the load).

V. Experimental Results and Discussion

The design specification of the system used for experimental validation is given in Table I. The inductor design for the novel overvoltage mitigation technique is shown in Table II, and for the dv/dt filter, it is shown in Table III. The inverter in all the cases utilizes two parallel half-bridges per phase leg, for a total of six half-bridges for a three-phase output, and is shown in Fig. 16. Unless stated otherwise, a 10-m-long cable is used to connect the inverter to the motor. A constant V/f control method is used to drive the motor, with voltage boosting applied when necessary to ensure that the currents remain stable. The inverter output is controlled in the frequency range of 0–10 Hz. A three-phase synchronous machine connected to a resistive load is used to mechanically load the induction motor in the experiments. The experimental setup is shown in Fig. 17, where the variac is used for fine adjustments of the load apparent power. In addition, the cable in Fig. 17 is shown coiled; however, in experiments, it is stretched out to minimize the coupling of the cable inductances.

A hard-switched traditional inverter implementation with no delay time and no inductor between half-bridges [see Fig. 7(a)]

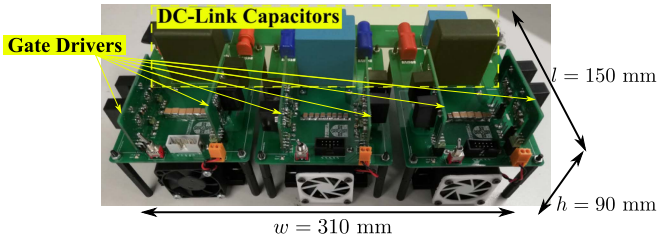


Fig. 16. Implemented three-phase paralleled half-bridge inverter with integrated dc-link capacitors.

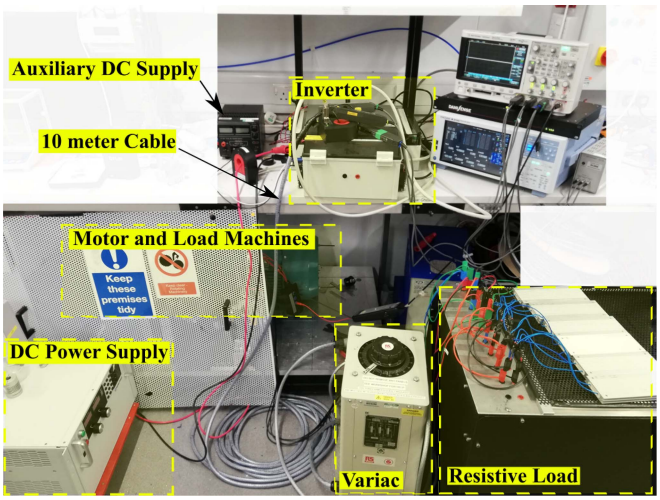


Fig. 17. Implemented experimental setup.

is used as a reference point, and the observed voltages and currents are shown in Fig. 18. This shows that the expected severe overvoltages are experienced, which is notable as it occurs with only 10-m-long cable due to the use of fast-switching SiC MOSFETs. For an individual line–line voltage pulse, a 96% overvoltage compared to the dc-link voltage is seen at the motor terminals. Over the course of a whole fundamental period (200 ms), the peak motor line–line overvoltage seen is actually 106% and is caused by the double-pulsing phenomenon [3]. The increase in magnitudes of reflected voltages seen close to the voltage polarity reversals in Fig. 18 is also attributed to the double-pulsing phenomenon since the width of voltage pulses will be very short in these regions [3].

In contrast, Fig. 19 shows the performance of the quasi-three-level parallel half-bridge active overvoltage mitigation technique. From these waveforms, it can clearly be seen that this active mitigation technique successfully limits motor overvoltage to 10% compared to the dc link, which is also observed at the inverter output. Over the entire fundamental period, the peak overvoltage is limited to 13%, eliminating the effects of double pulsing. Also shown are the currents I_A and I_B, which with reference to Fig. 7(b) describe the currents from each of the two coupled half-bridges in one phase. By computing the difference of these currents, it can be seen that the circulating current behaves as predicted in Fig. 10. Over the course of the fundamental period, the circulating current varies such that ΔI_{cir} remains consistent, but this current change is not always symmetrical about 0 A. This is partially due to the presence of

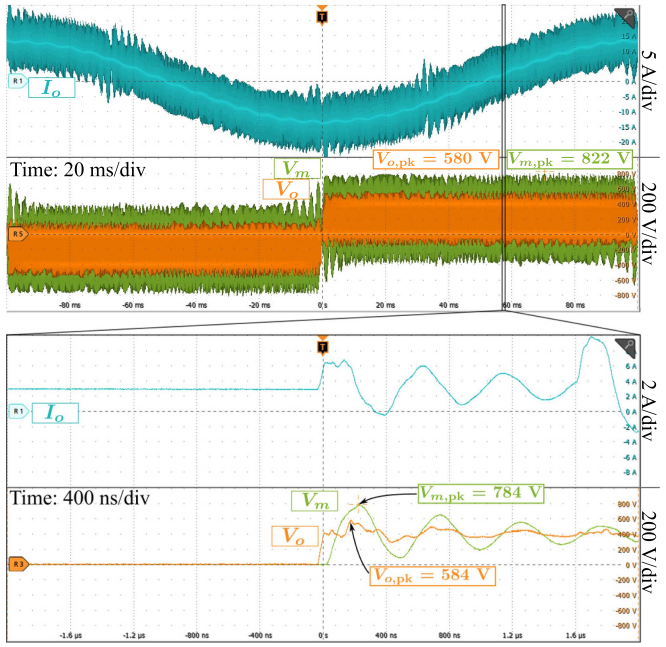


Fig. 18. Experimental results for the waveforms at the inverter and the motor when no overvoltage mitigation is employed. The peak inverter output voltage $V_{o,\text{pk}} = 580$ V and the peak motor voltage $V_{m,\text{pk}} = 822$ V.

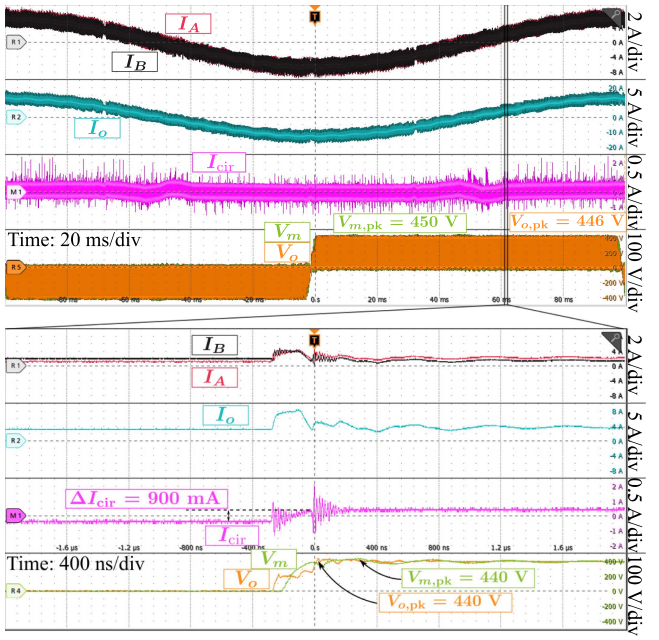


Fig. 19. Experimental results for the waveforms at the inverter and the motor when the proposed active overvoltage mitigation method is employed. The peak inverter output voltage $V_{o,\text{pk}} = 446$ V and the peak motor voltage $V_{m,\text{pk}} = 450$ V. The change in circulating current $\Delta I_{\text{cir}} = 900$ mA.

small changes of circulating current when both the half-bridges are in the same state, caused by the unequal voltage drop across the devices carrying different magnitudes of current. Beyond this, there is a significant change in the low-frequency value of the circulating current when the output current (I_o) is close to zero. During this time, the current in the devices can reverse, which enables soft switching and will significantly affect the

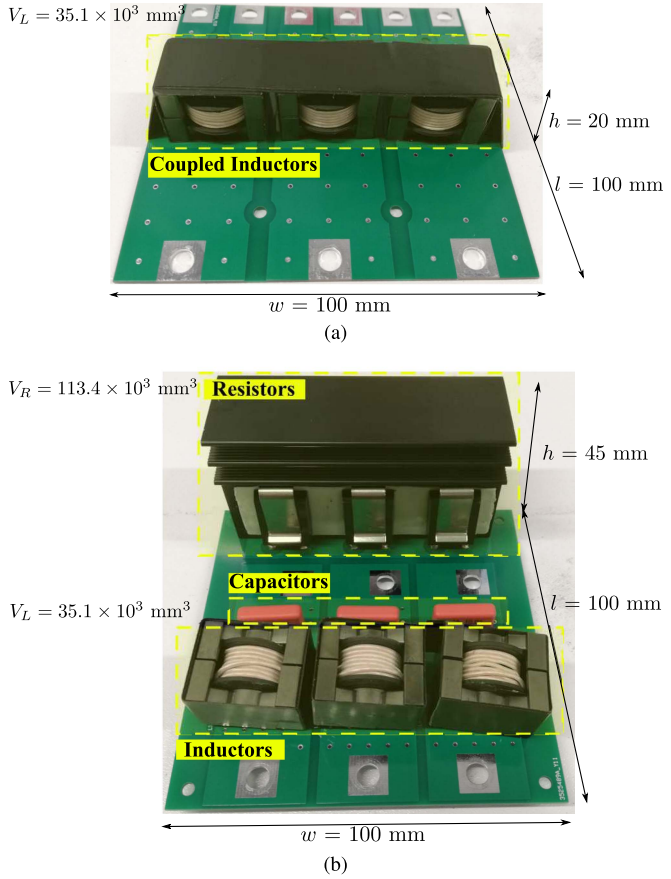


Fig. 20. Implemented passive components for (a) the active mitigation method and (b) the passive mitigation method.

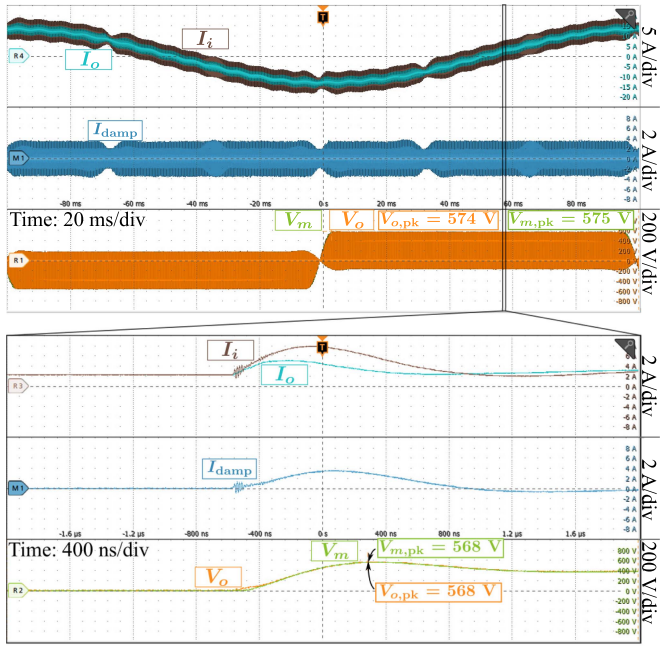


Fig. 21. Experimental results for the waveforms at the inverter and the motor when a passive-filter-based overvoltage mitigation method is employed. The peak inverter output voltage $V_{o,\mathrm{pk}} = 574$ V and the peak motor voltage $V_{m,\mathrm{pk}} = 575$ V.

behavior of switching transients [27], [28]. Since achieving soft switching is not an objective of this piece of research, its presence has not been directly confirmed nor will it be considered further.

In addition, the value of I_o for both the active mitigation technique and the traditional unmitigated operation displays overshoot after switching events, which is caused by the capacitance of the cable [31]. The capacitance causes a significant charging current due to the high voltage slew rate at the switching edge. In the case of the active mitigation technique, however, the current falls back toward the original value of I_o as soon as the second half-bridge begins its dead time. This can be seen in Fig. 19. After this, the cancellation of reflections means that no more oscillating current will flow. The same phenomenon occurs for I_o using traditional directly paralleled half-bridges, as shown in Fig. 18; however, owing to the presence of much larger voltage oscillations on the cable, the magnitude of the currents caused by these oscillations is larger.

In this article, an alternative overvoltage mitigation method using the dv/dt filter shown in Fig. 20(b) is compared with the proposed active method. Comparing the implemented filter to Fig. 20(a), it can be seen that the total volume of the filter is 323% greater than the volume of the coupled inductors due to the damping resistance and heat sink of the filter. Fig. 21 shows the waveforms of relevant quantities for the passive filter on the time scale of a pulse edge and the fundamental time period. Using the filter, the motor overvoltage observed is limited to 42% of the dc-link voltage on the scale of an individual pulse and a worst case overvoltage of 45% over the fundamental period. While this is a significant reduction from the peak overvoltage of 106% seen without any overvoltage mitigation, it does not meet the intended 20% limit used to design the filter in Section IV. Some deviations in the suggested filter design calculations exist between [8] and [9]. In particular, (43) is not thoroughly derived in [9] and can be compared with (10) given in Section II. With reference to V_o in Fig. 21, an approximate value of $t_r \approx 400$ ns can be used. Using (43), it is predicted that $V_{m,l-l,\mathrm{pk}} = 775$ V, whereas by using (10) a value of $V_{m,l-l,\mathrm{pk}} = 500$ V is predicted. Furthermore, by including the 16% output voltage overshoot for the filter shown in Fig. 14(b), it would be predicted that $V_{m,l-l,\mathrm{pk}} = 580$ V. This value is closer to the observed value of 568 V than that obtained using (43). Despite this, the filter does perform the expected function, increasing the rise time of the voltage edge seen by the inverter-side termination of the cable, as seen in Fig. 21.

Despite being partially effective at mitigating motor overvoltage, the filter introduces high losses. This can be seen in Fig. 22. Across all the values of apparent power demanded from the inverter, the filter has the highest losses, by at least 0.8% of the magnitude of the apparent power being delivered. This efficiency penalty is even worse at light apparent loading, where the penalty is approximately 4.5%. This is because of the losses in the damping resistance, which absorbs a pulse current (shown by I_{Damp} in Fig. 21) at every switching event, with no dependence on the load current. At light loading where conduction losses are minimal, this damping loss will, therefore, dominate.

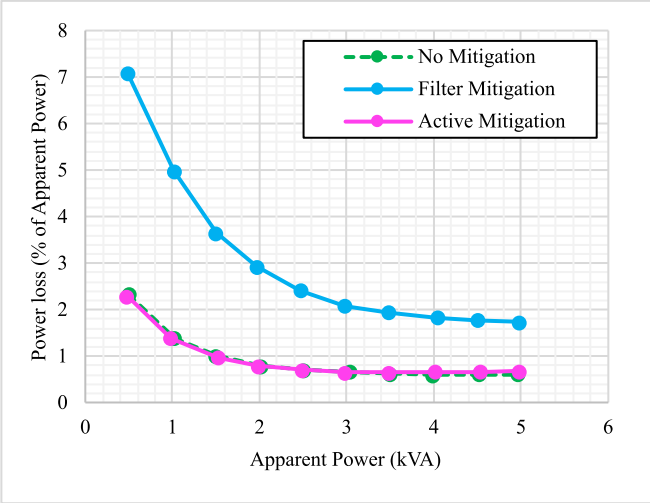


Fig. 22. Experimentally obtained losses at various levels of apparent power load experienced by the inverter when using the different mitigation methods in this article. The specifications of Tables I–III are used.

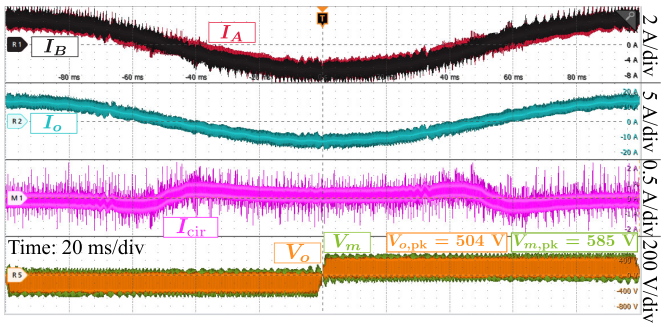
In contrast to the passive method using the dv/dt filter, the proposed active method using parallel half-bridges has notably better performance across most measures. Primary among these are the system losses. In Fig. 22, the losses caused by the active mitigation technique can be seen to closely resemble the losses when no mitigation is performed. This means that the additional losses introduced by the coupled inductors and delay time between the parallel half-bridges are minimal compared to a traditional unmitigated inverter. From the perspective of system efficiency, this allows overvoltage mitigation to be achieved without a large penalty. Fig. 22 shows that the light-load losses are reduced by inserting the delay time between parallel half-bridges, which aligns with the findings in [27] and the analytical predictions in Fig. 15(b). This reduction in losses is, however, minimal and not considered to have a significant effect. At high loads, the opposite trend is realized, where the active mitigation technique increases losses compared to the system with no mitigation applied. The difference is small, within 0.2%, and therefore, the impact of this loss increase is minimal, as desired. Observations of experimental power losses at higher apparent loading, therefore, agree with the predicted trends from Fig. 15(b). As stated in Section IV, these additional losses are caused by unequal current sharing between devices caused by the circulating current, as well as the copper and core losses of the coupled inductors, which are not present for the inverter with no mitigation.

By implementing the active mitigation technique with an increase of losses at load of less than 0.2% when compared to the inverter with no mitigation, it can be seen that the primary goal of achieving overvoltage mitigation with minimal increase of losses has been achieved. Simultaneously, this is achieved with a minimal volume penalty from the coupled inductors, which are shown in Fig. 20(a), which is at least 113.4×10^3 mm^3 less than the volume penalty of the filter shown in Fig. 20(b). It can, therefore, be seen that the active overvoltage mitigation method proposed in this article achieves lower losses with a smaller volume than a dv/dt filter, while also achieving more complete mitigation of the motor overvoltage.

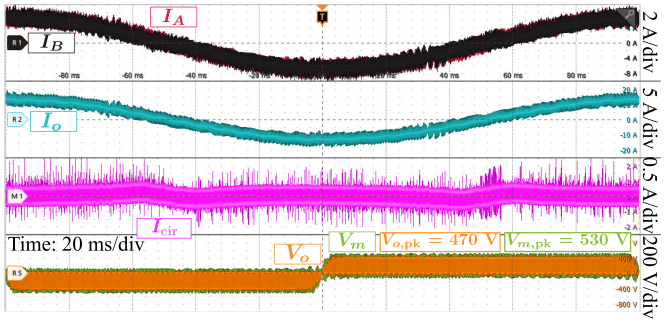
A. *Effect of Nonideal Delay Times*

While the implemented delay time set at $2t_p$ is shown to nearly eliminate the voltage reflections, which cause motor overvoltages, the effect of a delay time that is not equal to $2t_p$ must also be considered. If the real t_p of the cable connected to the inverter is different from the predicted value used to set the delay time, then a nonideal dwell time will result. One cause of this is that t_p is a function of the cable temperature [32], [33]. Changes in the temperature of the cable due to power losses or changes in the ambient temperature will, therefore, result in different values of t_p. In [33], it is observed that for a 40 K change in temperature, there is a 6% change in the propagation time. To model cases where nonideal dwell time occurs, both shorter and longer than ideal delay times are considered. In both the cases, the same 10-m cable and coupled inductors are used, and the only change made is to adjust the delay time within the control software of the inverter.

Changes of $\pm25\%$ were made to the applied delay time to model expected changes of t_p with generous margin. Since the volume of the system is unchanged, the performance metrics to be observed are the power loss of the inverter system and the peak motor overvoltage observed. With 75% of the ideal delay time, the peak motor overvoltage is 46% of the dc link, as seen in Fig. 23(a). In this case, a very similar overvoltage is achieved as when the passive filter is used. Similarly, with 125% of the ideal delay time, the peak motor overvoltage is 32% of the dc link, which is shown in Fig. 23(b). This is lower than the overvoltage obtained with the filter. However, both the cases have worse motor overvoltage than when the ideal delay time setting is used. Fig. 24 shows how the losses of the different lengths of delay time vary with the apparent power loading of the inverter. Both of the delay times that deviate from the ideal show greater losses across the range of test loads, with the shorter than ideal time giving the worst losses. For the longer than ideal delay time, the greater magnitude of circulating current, evident from I_{cir} in Fig. 23(b), will also contribute to greater conduction losses as from (30). In both the cases, the presence of reflected waves will cause an oscillating current in the cable. This presents additional conduction losses in the devices and coupled inductor when compared to the ideal delay time. The additional losses caused by nonideal delay times would result in only a 0.1% reduction in efficiency at 3 kVA. Therefore, even with a $\pm25\%$ error in the delay time setting, a similar level of overvoltage mitigation is achieved when compared to a dv/dt filter, but still with significantly reduced losses when compared to the filter. In particular, this is useful in applications where an accurate propagation time of the cable cannot be measured or where the effective propagation time may vary substantially during use due to temperature changes or other effects. These observations support the use of the proposed active overvoltage mitigation technique in an open-loop manner where the dwell time is set using a nominal cable propagation time. Even if the



(a)



(b)

Fig. 23. Experimental waveforms when using nonideal delay time settings. In (a), 75% of the ideal delay time is used. The peak inverter output voltage $V_{o,\text{pk}} = 504$ V and the peak motor voltage $V_{m,\text{pk}} = 585$ V. In (b), 125% of the ideal value is used. In this case, the peak inverter output voltage $V_{o,\text{pk}} = 470$ V and the peak motor voltage $V_{m,\text{pk}} = 530$ V. The cable specified in Table I is used in all the cases.

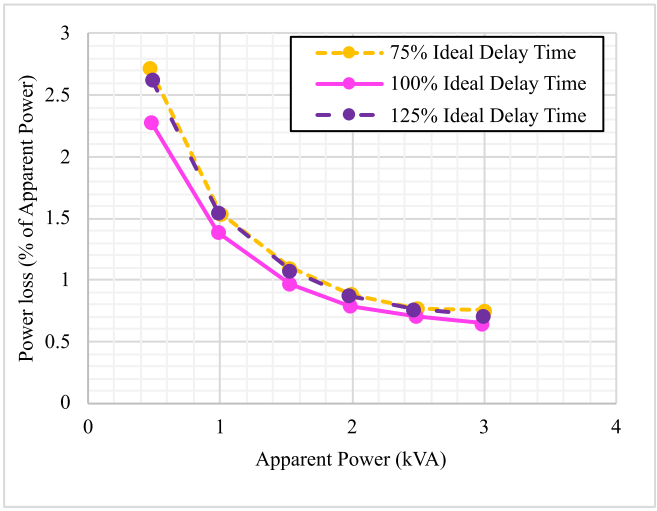


Fig. 24. Experimentally obtained losses at various levels of apparent power load experienced by the inverter when the delay time between parallel half-bridges is varied.

real cable propagation time drifts from the nominal value, partial overvoltage mitigation will still be achieved.

VI. Conclusion

This article reported a novel technique to actively cancel the reflected voltage of an inverter connected through a long cable to a motor. The novel method utilized parallel-connected SiC power devices to achieve voltage reflection cancellation without additional power devices. To achieve this, the parallel half-bridges per phase leg were connected to the phase output through a coupled inductor. The half-bridges were driven with the same PWM signals, but with a delay time between them. The resulting output from the inductor was a staggered voltage edge, which dwells at the mid-level voltage for the set delay time minus the inverter rise time. A method to design the coupled inductors between the half-bridges was outlined, which limits the impact of the circulating current during the dwell time. The designed inductor was implemented for use with an inverter-fed drive system with a 10-m-long cable, which was experimentally tested. When implemented, the performance of the novel active overvoltage mitigation technique aligns well with theoretical predictions. The motor overvoltage was reduced to the point where it was no larger than the output voltage of the coupled inductors. This was achieved with a minimal increase in power losses when compared to a traditional paralleled inverter with no overvoltage mitigation under the same loading conditions.

Furthermore, when compared to a passive dv/dt filter, the active mitigation technique simultaneously achieved better overvoltage reduction, significantly reduced power losses, and a lower volume of passive components. In addition, the active mitigation technique showed tolerance to deviations between the implemented delay time and the real propagation time, still achieving similar overvoltage reduction to the dv/dt filter while maintaining its power loss advantage. The minimal impact of the active mitigation technique on the performance of the inverter supported the inductor design technique, which was given for this application. It was demonstrated that the proposed active mitigation method effectively eliminates the motor overvoltage while still utilizing the high-speed switching of SiC MOSFETs and the efficiency benefits this entails. The technique is suitable for implementation in n-phase inverters.

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