An Approach for Online Estimation of On-State Resistance in SiC MOSFETs Without Current Measurement

Furkan Karakaya, *Student Member, IEEE*, Anuj Maheshwari, *Student Member, IEEE*, Arijit Banerjee, *Senior Member, IEEE*, and John S. Donnal, *Senior Member, IEEE*

***Abstract*—While silicon carbide power MOSFETs have significantly superior figures-of-merit in comparison to conventional silicon devices, they have seen relatively limited adoption in high-power applications due to intrinsic reliability concerns. One of the most consistent precursors of early device failure is increased on-state resistance (R_{ds-on}). This article presents the design of a nonintrusive health monitoring circuit (HMC) that can be embedded within the power converter to measure this resistance during operation. The HMC does not require load current information or any interaction with the gate driver. It is experimentally validated for a range of voltage and current levels including continuous operation in a buck converter and provides estimates of R_{ds-on} within $\pm 5\%$ of the true value for all cases.**

***Index Terms*—Health monitoring, junction temperature, MOSFETs, on-state resistance, reliability, silicon carbide (SiC).**

I. Introduction

Wide bandgap semiconductors are required to efficiently scale electronic power converters to the voltages and power levels needed in many emerging applications, such as electric transportation and renewable energy resources. In particular, silicon carbide's (SiC) low conduction loss, high switching frequency, and high blocking voltage make it an ideal candidate to replace the Si IGBTs and MOSFETs currently used in these applications. However, the reliability of SiC MOSFETs remains a significant concern [1] and has so far made it difficult to integrate these switches in the high-power applications where they provide the most benefit. Therefore, tracking early signs of device fatigue is critical to their wider adoption. SiC devices can fail for a variety of reasons, but one of the most consistent precursors regardless of fault type is an increase in the on-state resistance [1], [2], [3].

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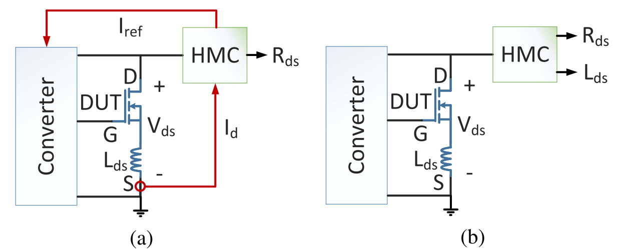

Fig. 1. In-situ measurement of on-state resistance in SiC MOSFETs. On-state resistance is an increasing function of junction temperature and can indicate early signs of device failure. (a) Conventional methods. (b) Proposed method.

Tracking R_{ds-on} *online*, i.e., during an active converter operation, is challenging due to the high blocking voltage when the device is not conducting and sensor synchronization for the submillisecond periods when the device is conducting. There are several well-established methods to isolate R_{ds-on} measurement circuits from the high blocking voltage [4], [5] but synchronizing the current and voltage measurements during device conduction is a much more challenging problem [6]. Even with high bandwidth current sensors, the package inductance introduces a phase offset that can corrupt the resistance measurement, especially at high switching frequencies. Therefore, previously proposed in-situ measurement circuits are either offline [3], that is they can only be used when the converter is not operational, or require additional synchronization with the health monitoring circuit [7], [8], as shown on the left-hand side of Fig. 1. Even if these constraints are satisfactory, the additional high bandwidth measurement of load current [3], [8], [9] introduces significant cost and complexity.

This article proposes an in-situ *online* R_{ds-on} estimation that requires no current measurement or coordination with the controller, as shown on the right-hand side of Fig. 1. Rather than directly measuring the current and voltage across the SiC device under test (DUT), the circuit injects a high-frequency current in parallel with the load current using a voltage-controlled current source. The differential voltage created on the DUT by the injected current is measured by an analog circuit that produces a continuous voltage proportional to the device impedance.

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After initial calibration, both L_{ds} and R_{ds-on} can be recovered from this impedance measurement. Any variation in impedance during converter operation can be attributed to R_{ds-on} since L_{ds} is a function of package geometry and considered constant. This approach eliminates the need for a high bandwidth current measurement and any synchronization with the controller. Results confirm a correct estimation of on-state resistance with a ±5% error. The circuit's measurement performance is demonstrated up to a 100% increase in the on-state resistance. The entire operation is proved in a range of converter current from 0 to 10 A and converter voltage between 0 and 500 V.

The rest of this article is organized as follows. Section II discusses the physics of on-state resistance and experimental results showing its correlation to device health. Section III discusses the estimation error introduced by a current sensor and package inductance. Section IV explains the theoretical background of the proposed method. Section V presents the experimental verification of the proposed technique. Finally, Section VI concludes this article.

II. On-State Resistance in SiC MOSFETs

The on-state resistance in SiC MOSFETs is formed by the series combination of the channel resistance $(R_{\rm ch})$, JFET region resistance $(R_{\rm JFET})$, drift layer resistance $(R_{\rm D})$, and total contact resistance $(R_{\rm package})$ [10]

$$R_{ds-\rm on} = R_{\rm ch} + R_{\rm JFET} + R_D + R_{\rm package}. \tag{1}$$

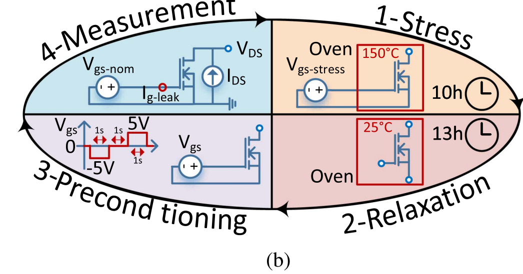
The on-state resistance is particularly useful for condition monitoring because both chip and package level faults cause an increase in this value prior to device failure. The high trap concentration in the gate-oxide generated by the SiC/SiO_2 interface [11] can lead to gate-oxide breakdown [12], which increases the channel resistance. Similarly, bond wire or solder layer defects due to mismatched thermal characteristics increase the package resistance [13]. The physics of SiC make it unlikely that these types of faults can be designed out of MOSFETs, instead, converters must assume such device failures are possible and alert users to early signs of degradation so the converter can be repaired or replaced.

A. Gate-Oxide Degradation

Among all SiC fault types, gate-oxide failure is the most widely studied in the literature [14]. Traps in the oxide cause the threshold voltage to increase, as given in (2) [15] where Q_{ot} is the oxide trap-charge, Q_{it} is the near-interface trap-charge, C_{ox} is gate-oxide capacitance, and V_{th0} is ideal threshold voltage without a trap. A positive shift in the threshold voltage as a result of accumulating interface trap density results in a gradual increase in the channel resistance $(R_{\rm ch})$, as shown in (3) where L_{ch} is the length of the channel, W_{ch} is the width of the channel, μ_n is the surface electron mobility, and V_{GS} is the gate-source bias level

$$V_{\rm th} = V_{\rm th0} - \frac{Q_{\rm ot}}{C_{\rm ox}} + \frac{Q_{\rm it}}{C_{\rm ox}} \tag{2}$$

(a)



(b)

Fig. 2. High-temperature gate bias (HTGB) experimental test setup and cycle. (a) HTGB test setup including an oven for thermal stress, a measurement board for parameter characterization, precise source-meters for stress and characterization. (b) HTGB daily test cycle.

$$R_{\rm ch} = \frac{L_{\rm ch}}{W_{\rm ch}\mu_n C_{\rm ox}(V_{\rm GS} - V_{\rm th})}. \tag{3}$$

To evaluate the effect of gate-oxide condition on R_{ds-on} and device health, a series of SiC MOSFETs were degraded until failure. Devices were deemed operational until the gate leakage current exceeded the capability of the gate driver meaning the transistor could no longer be controlled. The aging process was accelerated using high-temperature gate bias (HTGB), a widely accepted technique to simulate operational fatigue [12], [14], [16], [17]. HTGB applies the maximum junction temperature and a high electric field across the gate to form traps in the oxide. Left unchecked, this configuration quickly leads to device failure. To measure the rate of progression in R_{ds-on} as a function of oxide health the DUT is periodically switched between HTGB and rest conditions. Five SiC MOSFETs from three different batches were tested with periodic HTGB using the experimental setup shown in Fig. 2(a). The test cycle consists of the four steps shown in Fig. 2(b). During the stress phase, a large gate-source bias is applied inside an oven at maximum junction temperature. After 10 h the device is removed from the oven and unbiased for 13 h. Before measuring the parameters a preconditioning sequence of alternating gate-source voltages is applied to return the gate-oxide to a typical operational state [18]. This process is repeated until device failure. Results of this test are shown in Fig 3. An abrupt increase in gate leakage current indicates device failure, at which point the device is removed from the test process. Results show an increase in the on-state resistance from 15% to 125% prior to failure indicating on-state resistance is a reliable metric of oxide health.

It is important to note that in addition to device health, on-state resistance is also a function of junction temperature. The next section discusses the sources of error in typical R_{ds-on}

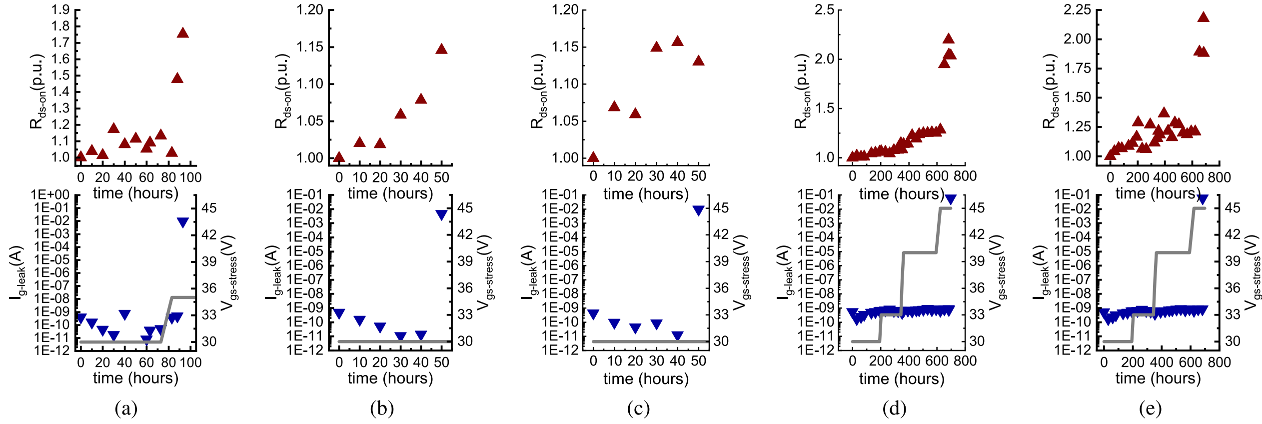


Fig. 3. Results show the recorded per-unit on-state resistance and gate leakage current of nine samples from three groups of SiC MOSFET. Group A has 1200 V_{ds-max} / 22 A_{ds-max} / 15 V_{gs-nom}, group B has 650 V_{ds-max} / 22 A_{ds-max} / 15 V_{gs-nom}, group C has 1200 V_{ds-max} / 20 A_{ds-max} / 20 V_{gs-nom} ratings. The gate-source stress voltage level increases in steps to accelerate the aging further. All on-state resistance and gate leakage current values are measured at nominal gate-source bias of each device. (a) Sample A1. (b) Sample A2. (c) Sample B1. (d) Sample C1. (e) Sample C2.

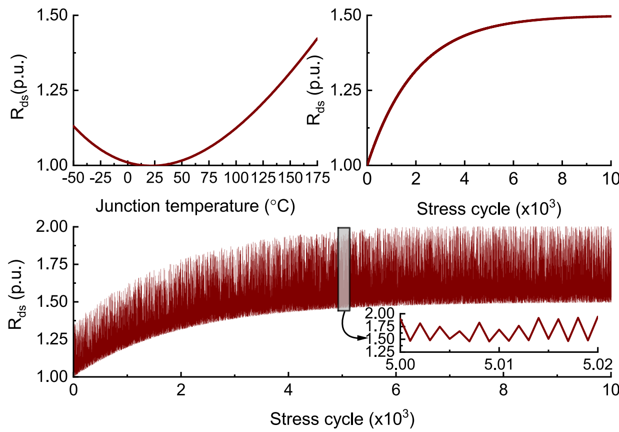


Fig. 4. Artificially generated R_{ds-on} profile including the variation due to temperature and aging. The per-unit R_{ds-on} is given with respect to the junction temperature and stress cycle number. Each cycle refers to an operating temperature where heating or cooling is performed, reflecting the converter ON and OFF cases. The achieved junction temperature is randomly picked between 80° C and 160° C for heating and between 25° C and 65° C for cooling so that triangular cycle variation can be obtained. In the meantime, the operational stress on the DUT slowly degrades the gate-oxide such that the on-state resistance increases exponentially.

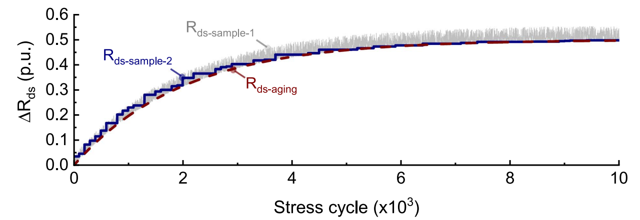


Fig. 5. Change in the on-state resistance due to the aging ($R_{ds-aging}$) can be isolated by applying varying sampling techniques. Two sampling examples are presented in this figure: $R_{ds-sample-1}$ is obtained by sampling the on-state resistance only if the junction temperature is less than 75° C, so this technique has to be assisted by a temperature sensor. Contrary to $R_{ds-sample-1}$, $R_{ds-sample-2}$ does not require a temperature sensor and is obtained by taking one sample once every 100 cycles. Each data that is larger than any following data is removed so that a nondecreasing trend can be obtained.

measurement circuits motivating the need for an alternative design to make a truly online measurement.

B. Junction Temperature

The on-state resistance is not only a function of oxide health; it is also strongly correlated with junction temperature—a relationship that is typically specified in manufacturer datasheets. This temperature dependence complicates the use of R_{ds} as an aging precursor [19]. However, because a healthy device typically undergoes thousands of thermal stress cycles before failure [20], the cyclic effect of temperature can be easily decoupled from the monotonic effect of device aging. This is illustrated by simulation in Fig. 4. The top portion of the figure shows the relationship of R_{ds} to junction temperature (left) and device health (right). Applying these effects simultaneously over the expected lifetime of a device produces an exponential envelope, as shown at the bottom of the figure.

Various sampling techniques can be applied to isolate the degradation in the on-state resistance by omitting temperature-dependent variation or vice versa. If the converter state can be controlled, a comparison of R_{ds} during idle and active operation can be used to estimate junction temperature [21]. However control or even knowledge of converter state is not required to differentiate between aging and temperature effects on R_{ds}. Two such techniques are shown in Fig. 5. The first method requires a temperature sensor and is performed by restricting on-state resistance measurements to periods when the junction temperature is less than 75 °C. This limits the temperature dependent variation to no more than 6% for the C3M0120100 K SiC industrial MOSFET [22]. The second sampling technique does not require a temperature sensor. Instead, R_{ds-on} is sampled at fixed intervals (every 100 stress cycles in this simulation), and only samples that show a constant or increasing resistance from the prior measurement are retained. The resulting nondecreasing trend follows the monotonic aging component of the on-state resistance ($R_{ds-aging}$). The only constraint on the aging profile

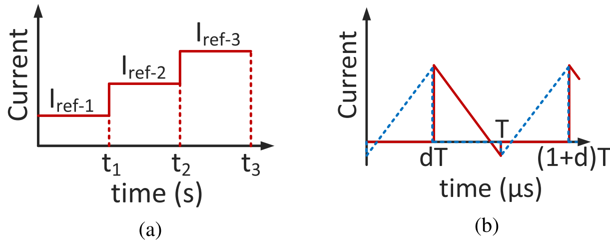


Fig. 6. Estimating R_{ds-on} as V_{ds}/I_{ds} requires a separate DC current injection and cannot be performed during converter operation. (a) Injected I_{ds} as in [7], [8]. (b) Operational I_{ds}.

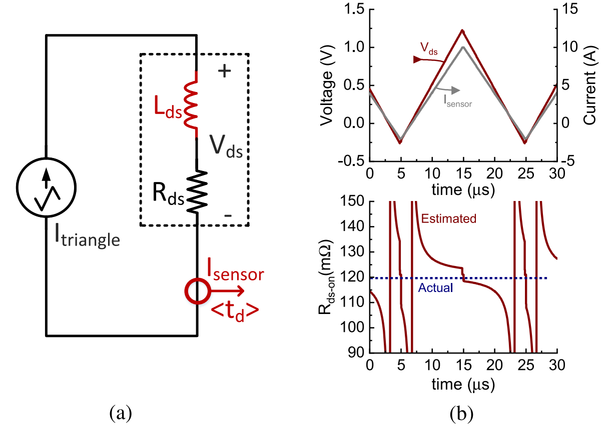


Fig. 7. Analysis of estimation error for on-state resistance with an inductive impedance model and a current sensor delay. (a) Simulation circuit. (b) Estimation result.

is that it is nondecreasing and lasts longer than one temperature cycle. Another approach given in [21] is tracking the degradation related deviations when the power converter is IDLE, and then using that measurement as a base value for temperature estimation when power converter is ON.

III. Challenges in Measuring On-State Resistance

The typical approach to measure R_{ds}, or any resistance, is to measure the ratio of voltage to current at steady state [23]. This requires electrically isolating the MOSFET and injecting a known current from drain to source. Approaches for in-situ estimation, such as [7], [8] offer an improvement by utilizing the load current for measurement, but this requires maintaining a fixed load current at multiple levels for several seconds, as shown Fig. 6(a). This is not practical for online use as typical load currents may vary arbitrarily depending on environmental parameters, such as torque on an electric motor. Since the power converter's operation is constrained during measurement such techniques are only considered quasionline [24]. A truly online estimation of R_{ds} cannot assume steady state load current and instead must measure the rapidly changing current levels in an operational converter, as shown in Fig. 6(b). This particular waveform is typical of zero-voltage-switching (ZVS) converters, which require negative current flow through the MOSFET to discharge the parasitic output capacitance [25], [26]. Under these conditions, the package inductance of the MOSFET and dynamics of the current sensor create a phase shift (φ) between measured current and voltage. A straightforward application of Ohm's law, in the following, leads to significant error in the resistance estimate:

$$R^e_{ds-\text{on}}(t) = \frac{\widehat{V}_{ds}\sin(\omega t + \varphi)}{\widehat{I}_{ds}\sin(\omega t)}. \tag{4}$$

The effect of this phase shift on the estimation is illustrated by simulation using an inductive impedance MOSFET model with a 50 kHz triangular current waveform resembling a ZVS converter, as shown in Fig 7(a). The current sensor dynamics are modeled as a 50 ns time delay, the package inductance is 15 nH and the on-state resistance is 120 mΩ. The resulting voltage (V_{ds}) and measured current (I_{sensor}) are plotted in Fig. 7(b). The ratio of these waveforms is no longer constant and cannot be used to accurately estimate $R_{ds-\text{on}}$.

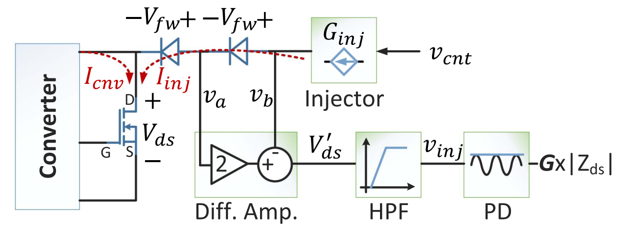


Fig. 8. Proposed on-state impedance measurement circuit.

One technique to eliminate this error is to sample the current and voltage waveforms at or above the Nyquist frequency and use a ratio of RMS values to compute the resistance instead. While technically possible, the complexity of such a measurement would require lab instrumentation or be prohibitively expensive to embed in a typical power converter. This article proposes an alternative approach that avoids this phase shift sensitivity without the need for high bandwidth sampling.

IV. Proposed Online Measurement of $R_{ds-\text{on}}$

Rather than using the load current, this article proposes an approach that exploits the small signal linearity of $R_{ds-\text{on}}$ to make an online measurement that is independent of the converter dynamics. During conduction, a known high-frequency current is injected in parallel with the unknown load current. The resulting V_{ds} waveform is a linear combination of both currents. By passing this waveform through an appropriately tuned filter, the effect of the injected current can be isolated and used to compute a highly accurate estimate of the on-state resistance.

A. Theory of Operation

A block diagram of the proposed $R_{ds-\text{on}}$ measurement circuit is presented in Fig. 8. A voltage-controlled current-injection circuit generates a high-frequency sinusoidal current (I_{inj}) that is superimposed on the unknown load current (I_{cnv}). The combined currents produce a voltage (V_{ds}) across the device described by Ohm's law. Some care must be taken when measuring this

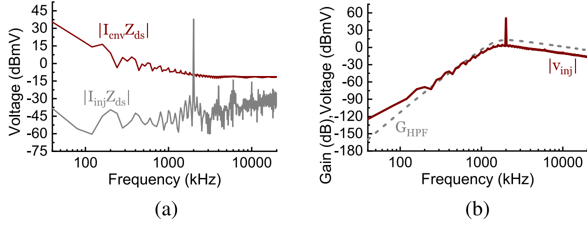


Fig. 9. Principles of converter current elimination with a HPF. (a) Input of HPF unit. (b) Output of HPF unit.

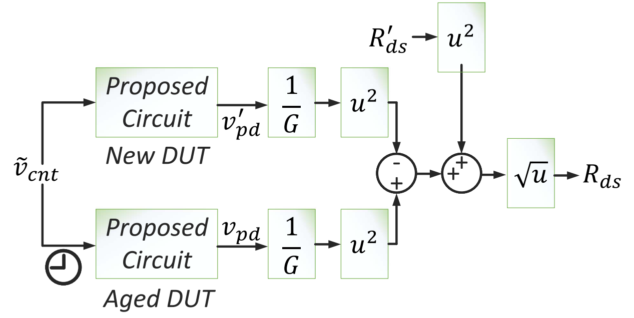


Fig. 10. Block diagram for R_{ds} extraction.

value in-situ since the on-state voltage is much smaller than the typical blocking voltage, which can be up to 10 kV or higher for SiC MOSFETs. Placing a diode between the drain and the current injector protects the measurement circuit but introduces a potential source of error due to the forward voltage drop of the diode. Although some studies rely on precalibrated forward voltage drop of the blocking diode [27], [28], a more reliable solution is eliminating the voltage drop by using a double diode configuration and an appropriately scaled subtraction amplifier, as proposed in [4]. The measured voltage V'_{ds} is then fed to a high-pass filter (HPF), which eliminates the voltage produced by the load current leaving only the voltage produced by the injected current (v_{inj}). The final stage is a peak detection circuit that converts the high-frequency signal to a dc value that can be easily measured using a unipolar, low-bandwidth analog-to-digital converter. This signal is proportional to the on-state impedance ($Z_{\text{ds}}(\omega_{\text{cnt}})$) by a scalar gain coefficient G, which can be derived as follows.

A sinusoidal voltage source with a known amplitude $\hat{v}_{\text{cnt}}$ creates an injected current i_{inj}

$$v_{\text{cnt}}(t) = \hat{v}_{\text{cnt}}\sin(\omega_{\text{cnt}}t)$$
$$i_{\text{inj}}(t) = G_{\text{inj}}v_{\text{cnt}}(t). \tag{5}$$

This injected current in combination with the load current creates a voltage v_{ds} across the MOSFET

$$v_{ds} = Z_{ds}(i_{\text{load}} + i_{\text{inj}}). \tag{6}$$

By making a differential measurement across v_a and v_b the effect of the protection diode's forward voltage drop can be eliminated

$$v_a = v_{ds} + v_{fw}$$
$$v_b = v_{ds} + 2v_{fw}$$
$$v_{ds'} = 2v_a - v_b$$
$$v_{ds'} = 2(v_{ds} + v_{fw}) - v_{ds} + 2v_{fw}$$
$$v_{ds'} = v_{ds}. \tag{7}$$

The voltage $v_{ds'}$ can be described as a Fourier series with the lower frequency terms determined by the load current and a single high-frequency term determined by the injected current. An HPF with a cutoff frequency $\omega_c \gg \omega_{\text{cnv}}$ removes the lower frequencies leaving only the voltage induced by the injector. The effect of this filter is described visually in Fig. 9

$$v_{ds'}(t) = \sum_{\omega=0}^{\infty} Z_{ds}(\omega)i_{ds}(\omega t)$$
$$v_{hf}(t) = (H_{\text{HP}} * v_{ds'})(t)$$
$$v_{hf}(t) = Z_{ds}(\omega_{\text{cnt}})i_{\text{inj}}(t). \tag{8}$$

A peak follower circuit effectively tracks the magnitude of this frequency component eliminating the effect of the phase offset between current and voltage

$$v_{pd} = \max_t(v_{hf}(t))$$
$$v_{pd} = |Z_{ds}(\omega_{\text{cnt}})|G_{\text{inj}}\hat{v}_{\text{cnt}}. \tag{9}$$

The impedance Z_{ds} includes both the on-state resistance as well the package inductance. At the injection frequency, this inductance is on the same order of magnitude as the resistance leading to the following equation for R_{ds} as a function of the measured voltage v_{pd}:

$$\sqrt{R_{ds}^2 + (\omega_{\text{cnt}}L_{ds})^2} = \frac{v_{pd}}{G_{\text{inj}}\hat{v}_{\text{cnt}}}. \tag{10}$$

For health monitoring applications where the specific value of R_{ds} is not as important as its rate of change, the package inductance can be ignored and v_{pd} itself can be used as the diagnostic metric since it is an increasing function of R_{ds} and L_{ds} is a constant.

If the particular value of R_{ds} is required, a simple calibration procedure can be used to decouple it from the inductance. The output v_{pd} is measured once during commissioning when the MOSFET is in a known good condition and its operational parameters including R_{ds} match the datasheet values. This baseline value can then be used to recover R_{ds} from an online measurement taken at any point in the future. The computation is illustrated in Fig. 10. The baseline measurement (v'_{pd}) and new measurement (v_{pd}) are scaled to Z_{ds} and squared so that their difference cancels L_{ds}, which is independent of device condition

$$\left(\frac{v_{pd}}{G}\right)^2 - \left(\frac{v_{pd'}}{G}\right)^2 = R_{ds}^2 - R_{ds}'^2. \tag{11}$$

The $R_{\text{ds-on}}$ for a healthy device is known from the datasheet and can be added to this result to recover the current value of $R_{\text{ds-on}}$, as shown in the final step of Fig. 10. After calculating

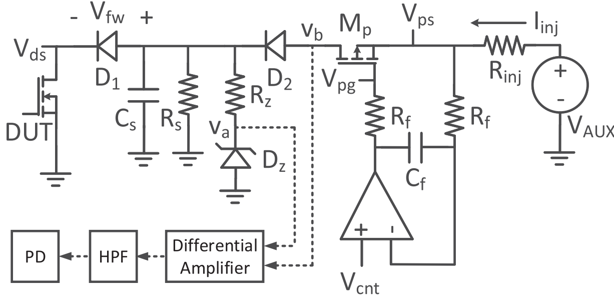


Fig. 11. Current injection circuit: The source terminal voltage of P-MOS (V_{ps}) is adjusted to the same value with the control signal (V_{cnt}) by the op-amp regulator such that the injected current (I_{inj}) can be controlled.

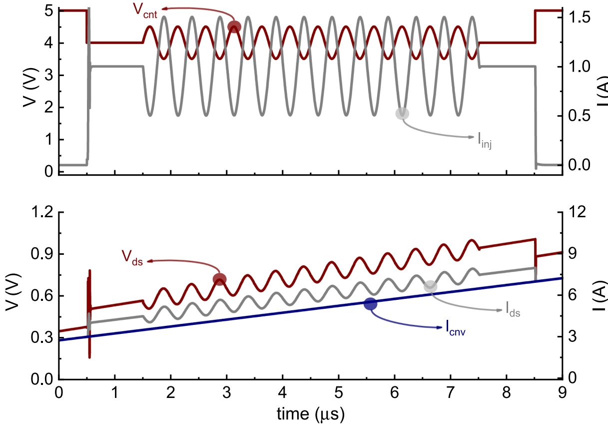


Fig. 12. Simulation results visualize the injection concept. An external current is injected to the DUT while an inductive converter current flows across the same device. The control signal has a 1 V_{pp} amplitude and 2 MHz of frequency resulting a 1 A_{pp} injection current due to the 1 Ω series injection resistor.

$R_{\text{ds-on}}$, L_{ds} can be computed from Z_{ds} using the known injection frequency ω_{cnt}.

B. Implementation

The schematic for the current injection and protection diodes are shown in Fig. 11. Nodes v_a and v_b connect to the differential amplifier, which leads to the rest of the measurement circuit. Negative feedback through the operational amplifier keeps the source (v_{ps}) of the MOSFET equal to the control voltage as long as v_{cnt} is less than V_{AUX}. The injected current is then

$$I_{\text{inj}} = \frac{V_{\text{AUX}} - V_{\text{cnt}}}{R_{\text{inj}}}. \tag{12}$$

Fig. 12 shows a visualization of these waveforms. The dc component of I_{ds} is removed by the HPF, so neither V_{AUX} nor the average value of v_{cnt} effect the measurement result. Only the high-frequency ac component of the injection current is significant

$$\hat{i}_{\text{inj}} = \frac{\hat{v}_{\text{cnt}}}{R_{\text{inj}}}. \tag{13}$$

A low-pass filter formed by R_f and C_f stabilizes the transient response of the amplifier. The diode protection circuit also has a filter formed by C_s, R_s to suppress the switching transients produced by the DUT. Without this filter, the additional impedance introduced by D_1's parasitic capacitance creates a voltage spike during switching events that interferes with the operation of the measurement circuit. To maximize this filter's effectiveness, capacitor C_s should be placed as close as possible to D_1 to maintain a low impedance return path for transient currents. Finally, R_z and D_z clamp any excessive voltage and provide a path to ground for the injected current when the DUT is not conducting. These filters do not modify the functionality of the circuit as discussed in Section IV-A, and the specific values are flexible. Table I lists the critical components of the injection circuit and reasons for their selection.

TABLE I
CRITICAL COMPONENTS IN THE INJECTION CIRCUIT

Component	Model	Advantages
Operational amplifier	LT1809	• Rail-to-rail input common mode voltage range • Rail-to-rail output swings • 180 MHZ gain-bandwidth product • 350V/μs slew rate
P-channel MOSFET	DMP2078LCA3	• 1.1 nC gate charge • 13 A pulsed drain current • Small footprint
Blocking diode	S1FLM-M	• 1 kV dc blocking voltage • 4 pF parasitic capacitance • Small footprint

The differential amplifier, HPF, and peak detection circuits are standard analog circuit blocks and can be implemented using a variety of well-known topologies. However, some care should be taken when choosing the injection frequency and cutoff frequency of the HPF. If the injection frequency cannot be placed well above the converter frequency, a high-order filter is required to fully attenuate the converter harmonics while keeping the injected frequency in the pass band. The drain-source current is the combination of both the load and injected current. Therefore, the DUT voltage can be divided into two components: $V_{ds-\text{cnv}}$ and $V_{ds-\text{inj}}$, each attenuated by HPF based on their frequency. Thus, the output of the HPF includes two signals whose division gives the signal-to-noise ratio (SNR) where G_{hpf} is the gain of HPF, and n is the filter order

$$\text{SNR} = \frac{G_{\text{hpf}}(f_{\text{inj}})V_{ds-\text{inj}}}{G_{\text{hpf}}(f_{\text{cnv}})V_{ds-\text{cnv}}}$$

$$\text{SNR} = \frac{G_{\text{hpf}}(f_{\text{inj}})(|Z_{ds}(f_{\text{inj}})|I_{\text{inj}})}{G_{\text{hpf}}(f_{\text{cnv}})R_{ds}I_{\text{cnv}}}$$

$$\text{SNR} = 10^{\frac{n}{10}\frac{f_{\text{inj}}}{f_{\text{cnv}}}}\frac{|Z_{ds}(f_{\text{inj}})|I_{\text{inj}}}{R_{ds}I_{\text{cnv}}}. \tag{14}$$

The SNR can be improved by increasing the injection frequency, injection magnitude, or filter order. While R_{ds} does affect SNR, the impact of small R_{ds} values is limited by the package inductance, which sets a lower bound on the overall impedance, Z_{ds}. Several SNR curves for various values of these parameters are

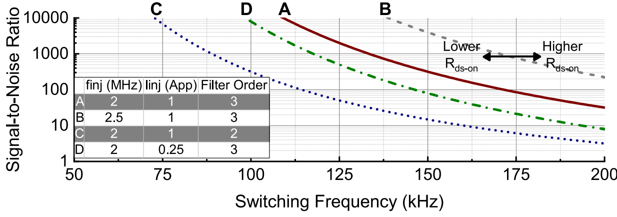


Fig. 13. Signal-to-noise ratio (SNR) curves show how design parameters affect the signal quality. Increasing the filter order, current injection, and injection frequency each improves the SNR for a given switching frequency. Lower values of R_{ds} decrease the SNR but the effect is minimal since the impedance is dominated by the package inductance at the injection frequency.

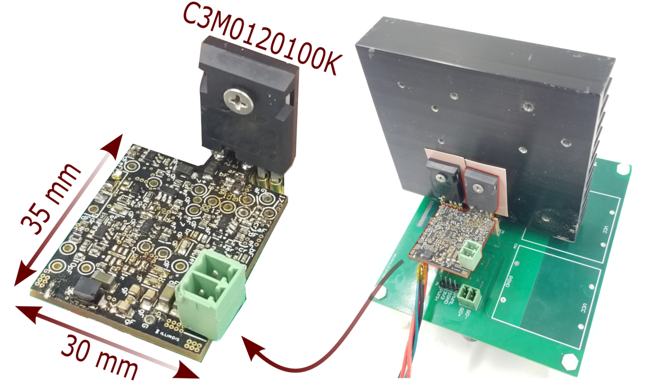


Fig. 14. Proposed circuit is connected to an SiC MOSFET, and the DUT is connected to a half-bridge to perform in-situ and online measurements.

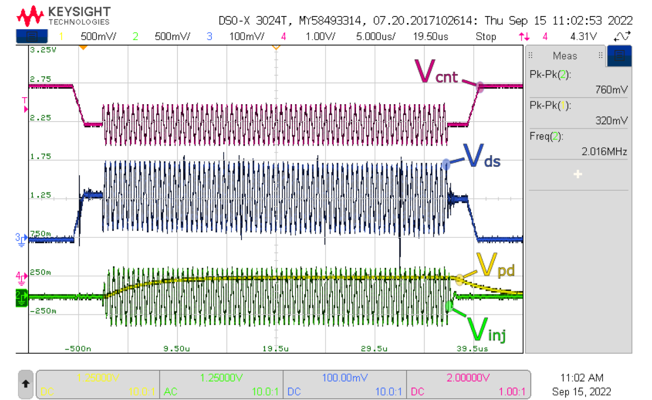


Fig. 15. Oscilloscope screenshot shows the voltage waveforms of the control-signal (V_{cnt}—CH4: 1 V/div), the actual device on-state voltage (V_{ds}—CH3: 100 mV/div), HPF output voltage (V_{inj}—CH2: 500 mV/div), and output voltage of the PD unit (V_{pd}—CH1: 500 mV/div). When the control signal gets lower than the auxiliary supply level, the injection current starts to flow. The sinusoidal modulation causes a high-frequency AC signal on the on-state voltage. HPF successfully removes the low-frequency components, and PD tracks the peak value.

shown in Fig. 13 to illustrate this design intuition. Curves are computed based on 10 nH package inductance and 2 V $V_{ds-\mathrm{cnv}}$.

The proposed measurement circuit, regardless of the design parameters chosen for optimal SNR, has no impact on the operation of the power converter itself. Since the injected current is much higher than the switching frequency, it is well outside the bandwidth of the controller and does not affect stability or control. Since current is injected only when the DUT is conducting, the injected current only flows from drain to source and does not affect the load current or the output voltage. The circuit is also compatible with common protection techniques that use drain-to-source voltage measurement, such as desaturation detectors, as the injected current is well below what would be expected in a short circuit fault. For example, the device we used has a rated current of 30 A, and a properly designed desaturation detector would be used to trigger a fault around 2 times the rated current (60 A), or more [29]. In comparison, our injected current is 0.5 A, which is less by orders of magnitude. Finally, because there is no Ohmic connection to the gate, there is no impact on the gate driver or associated protection circuitry (e.g., miller-clamps).

V. Experimental Results

Experimental verification of the proposed circuit was performed using an SiC MOSFET controlled by a MAX22701E [30], a typical gate driver unit, on the custom-printed circuit board shown in Fig. 14. The HPF is a fifth-order design built from cascaded Sallen–Key R-C filters [31] with 1 kΩ and 100 pF passive values resulting in a 1.6 MHz corner frequency. Note that in most applications this provides more attenuation than strictly necessary and could be reduced to a lower order filter while still meeting SNR requirements, as shown in Fig. 13. The waveforms in Fig. 15 show the operation of the current injector and analog circuitry without a load current. The output of the circuit is the steady state voltage of the peak detector v_{pd}, which is directly proportional to Z_{ds}. The transfer function in (9) is an ideal relationship that assumes each circuit block in the measurement path has unity gain. Accounting for the frequency-dependent scale factors introduced by each block in the measurement path results in an effective gain of

$$\boldsymbol{G} = G_{pd}(\omega_{\mathrm{cnt}}) \times G_{\mathrm{hpf}}(\omega_{\mathrm{cnt}}) \times G_{\mathrm{diff}}(\omega_{\mathrm{cnt}}) \times (\hat{v}_{\mathrm{cnt}} g_{\mathrm{inj}}). \quad (15)$$

The terms in this equation can be determined by calibration. Fig. 16 shows the experimental input/output relationships of each circuit block over a wide range of injection frequencies. All of the relationships are highly linear, which means the effective gain at a particular injection frequency ω_{cnt} is characterized by a single scalar coefficient

$$|Z_{ds}(\omega_{\mathrm{cnt}})| = v_{pd}/\boldsymbol{G}(\omega_{\mathrm{cnt}}). \quad (16)$$

A. Estimation Error

The injection frequency must be high enough to avoid interference from harmonics of the load current but low enough to avoid attenuation by bandwidth limits of the injection and measurement circuitry. Fig. 17 shows the experimental accuracy of the circuit across a range of injection frequencies and resistances. The estimation error (ε), is calculated as

$$\varepsilon(\%) = \frac{|R_{ds_{\mathrm{estimated}}} - R_{ds_{\mathrm{actual}}}|}{R_{ds_{\mathrm{actual}}}} \times 100. \quad (17)$$

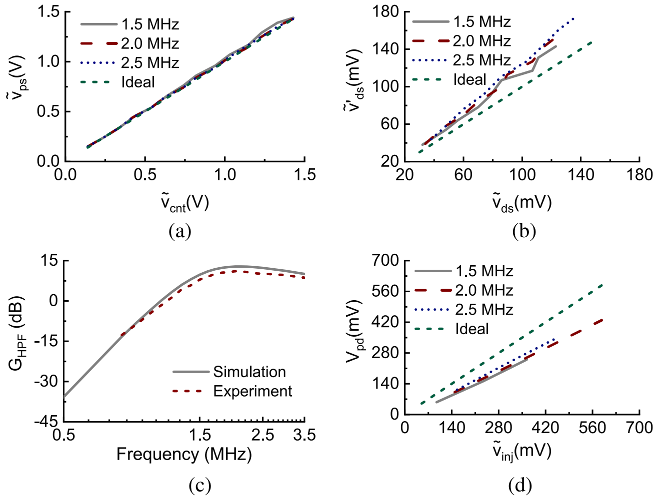


Fig. 16. Calibration results for all sub-units: injection unit requires a calibration from the control signal ($\hat{v}_{\rm cnt}$) amplitude to source node voltage of P-MOS ($\hat{v}_{\rm ps}$) amplitude, subtraction amplifier unit requires a calibration from the actual on-state voltage ($\hat{v}_{\rm ds}$) to a calculated on-state voltage ($\hat{v}'_{\rm ds}$), HPF unit requires a calibration of the gain, and peak detection unit requires calibration from its output level ($v_{\rm pd}$) to its input voltage peak level ($\hat{v}_{\rm inj}$). (a) Injection unit. (b) Subtraction amplifier. (c) HPF unit. (d) Peak detection unit.

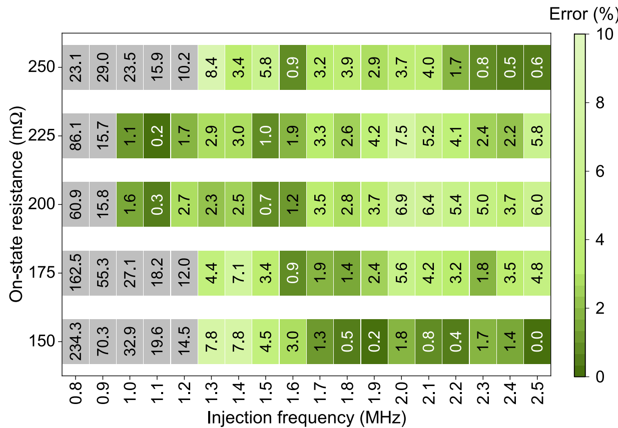


Fig. 17. Estimation error for varying on-state resistance and injection frequency. The healthy device has 120 mΩ resistance. To mimic the increase in the $\rm R_{ds-on}$ (as in aging), the gate-source bias level is adjusted to reach different on-state resistance values. The actual value of the resistance is measured by a source-meter and given on the vertical axis. Then, the $\rm R_{ds-on}$ is estimated by the proposed circuit. Each square shows the estimation error for a pair of resistance and injection frequencies. The results show that the estimation error is below 10% for all frequencies above 1.3 MHz.

All injection frequencies above 1.3 MHz produce less than 10% error across the typical range of $\rm R_{ds}$ in SiC MOSFET's. This error bound assumes the initial on-state resistance [used in (11)] is accurate. This value can be obtained by measuring the DUT prior to use, but using the nominal value provided by the manufacturer eliminates the need for per-device calibration. While the actual initial value may differ from the datasheet, the effect of this error on the measurement result is minimal. Fig. 18 evaluates two cases where the true initial resistance is 20% higher or lower than the nominal value. Estimation results show that the error is bounded by 20% and in fact decreases as the device ages.

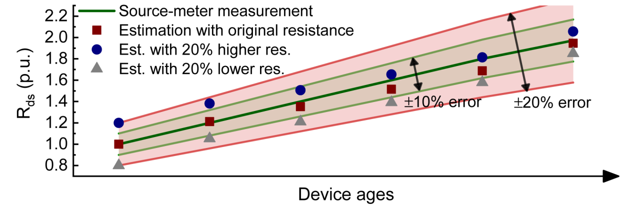


Fig. 18. Sensitivity to initial conditions. Any error in the initial R_{ds} value has a limited impact on the measurement result, and the effect of this error decreases as the device ages.

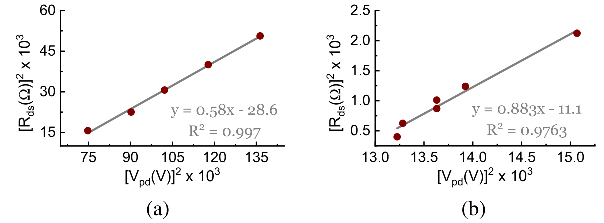


Fig. 19. Computing the gain term G for (11) using end-to-end calibration. Since R_{ds}^2 is directly proportional to V_{pd}^2, the slope of the least squares fit line is equal to G^2. For devices with high initial R_{ds} values (left), the signal voltages are large enough that the op-amps are essentially ideal and $G \approx$ (15). For much lower values (right), the effective G also reflects the nonidealities of the op-amps. In both cases, the high $\rm R^2$ values indicate the linear model of the circuit is accurate. (a) 120 mΩ device. (b) 20 mΩ device.

As built, when the R_{ds} value is above approximately 50 mΩ, the op-amps can be considered ideal and the effective gain G in (11) is accurately described by the analytic expression in (15). Smaller R_{ds} values generate low signal levels in the circuit and the op-amp nonidealities cannot be ignored. Rather than deriving a full analytic expression, the gain term can be directly determined from an end-to-end calibration, as shown in Fig. 19. The slope of the best-fit line is the circuit gain. The high R^2 values for both conditions (high and low R_{ds} values) confirm the validity of a linear model for this circuit.

B. Online Measurement

The online performance of the proposed circuit is demonstrated with two different topologies: a double pulse test (DPT) circuit and a buck converter. The DPT is performed in two different configurations to measure the effect of both load current and converter voltage on the $\rm R_{ds}$ estimation. In the first configuration, the converter current is increased from 0 to 10 A by adjusting the DPT voltage. In the second configuration, the converter current is kept below 2.5 A, and the converter voltage is varied from 50 to 500 V. At each voltage and current level, the output value of the proposed circuit is recorded, and the on-state resistance is calculated. The results are presented in Fig. 20. The gradual increase in on-state resistance with load current is expected and in agreement with the datasheet. In both sets of measurements, the measurement error is within ±5%. Fig. 21 shows oscilloscope screenshots for DPT configurations at maximum current (left) and voltage (right). These results

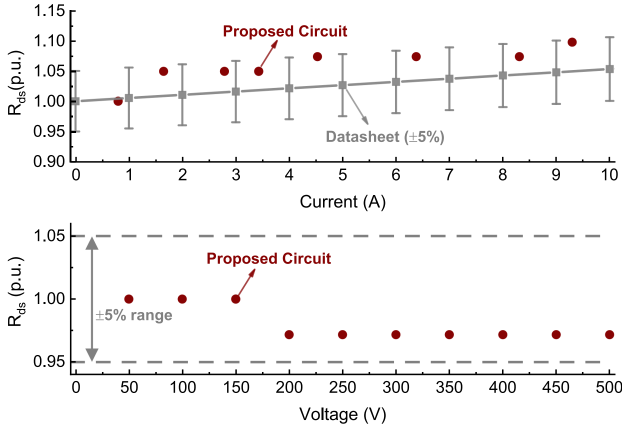


Fig. 20. Estimation results of DPT test for varying current and voltage levels. Each test shows an estimation error below ±5%.

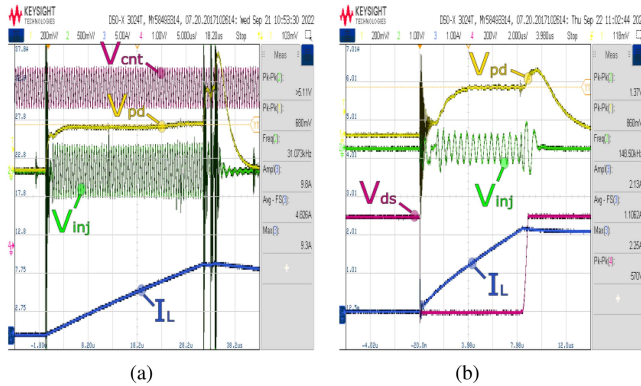


Fig. 21. Oscilloscope screenshots for two DPTs: CH1 shows the output voltage of the PD unit (V_{pd}—200 mV/div), CH2 shows the HPF output voltage [V_{inj}—500 mV/div for (a) 1 V/div for (b)], CH3 shows the power inductor current [I_L—5 A/div for (a) 1 A/div for (b)], and CH4 shows the control signal (V_{cnt}—1 V/div) for (a), drain-to-source voltage of the DUT (V_{ds}—200 V/div) for (b). The left figure shows the captured waveforms for 10 A of load current, and the right figure shows the captured waveforms under 500 V supply level. In consecutive DPT tests, the output voltage of the peak-detection circuit (V_{pd}) is captured while the load current is swept from 1 to 10 A or the supply level is increased from 50 to 500 V. (a) DPT result at 10 A. (b) DPT result at 500 V.

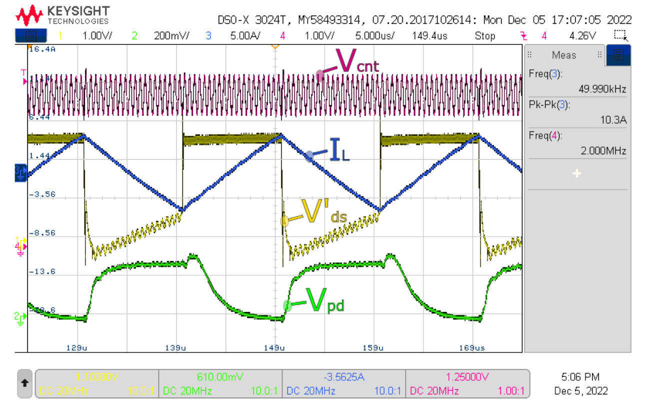


Fig. 22. Oscilloscope screenshot shows the voltage waveforms of the control signal (V_{cnt}—CH4: 1 V/div), the power inductor current (I_L—CH3: 5 A/div), differential amplifier output voltage (V'_{ds}—CH1: 1 V/div), and output voltage of the PD unit (V_{pd}—CH2: 200 mV/div). The control signal is generated at 2 MHz of injection frequency. The injection is performed only if the DUT is turned on and a control signal is applied. The output value of the PD unit is the same with the no-load case proving the elimination of the converter/load effect.

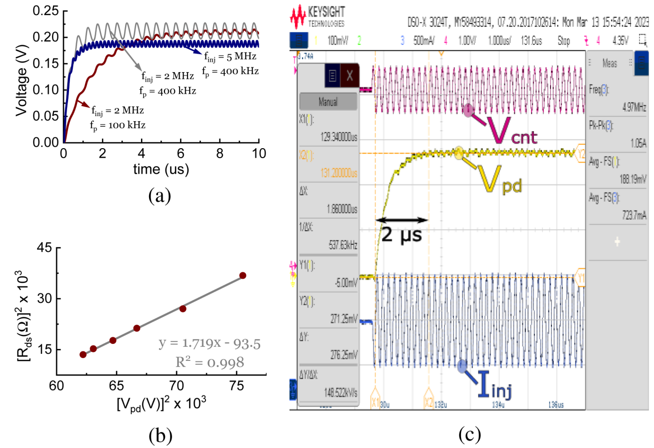


Fig. 23. Measurement output is valid after the peak detector (PD) settles, which is a function of the injection frequency and PD pole location: (a) shows PD response for various values of these parameters, (b) gives the experimental calibration of the proposed circuit at 5 MHz injection frequency, and (c) shows the measured waveforms confirming a 2 μs settling time when the injection frequency is 5 MHz. (a) Simulation results. (b) Calibration line at 5 MHz. (c) Experimental result at 5 MHz.

confirm that the output of the measurement circuit, v_{pd}, is unaffected by either converter current or voltage.

The proposed circuit was then used with the same SiC MOSFET in a buck converter to evaluate the measurement accuracy under continuous switching. Oscilloscope waveforms for the significant voltages and currents are shown in Fig. 22. The peak detector (PD) output quickly settles to the same steady state value as the isolated (no load current) setup shown in Fig. 15 indicating the R_{ds} measurement is unaffected by converter operation. The large triangular current through the inductor, I_L, is an extreme scenario in a typical Buck converter. The typical ripple would be much lower leading to even less harmonic content from the load current and potentially an even higher accuracy result.

The peak detection output is valid after approximately 4 μs, as shown in Fig. 22. This is sufficient for most common topologies and switching frequencies. However, at particularly high switching frequencies or low duty cycles, this settling time can occupy a significant portion of the available injection window (device conduction) and impact the accuracy of the R_{ds} measurement. In these cases, the settling time of the PD can be reduced by increasing both the injection frequency (f_{inj}) and the low pass filter corner frequency (f_p), as illustrated in Fig 23(a). For example, increasing the injection to 5 MHz and the low pass filter pole to 400 KHz reduces the settling time to 2 μs. It is important to note that this can be a tradeoff, as increasing the injection frequency may decrease the amplitude of the injected current due to the gain-bandwidth limitation of the injection op-amp.

A final consideration is the circuit's susceptibility to conducted and radiated EMI given the sharp voltage transients in high-frequency switching converters. Such frequency

oscillations are clearly visible during the turn-ON and turn-OFFtransients of the DUT in Fig. 21. While visually significant these do not affect the accuracy of the measurement since the PD is only sampled during device conduction after the output has stabilized. However, additional care must be taken in more complex converters where switching transients of other components can occur during the conduction period of the DUT. These effects can be minimized using typical EMI mitigation techniques such as choke filters, ESD diodes, and device shielding.

VI. Conclusion

This study proposes an in-situ, online R_{ds-on} measurement technique for SiC MOSFETs. The proposed technique does not require any measurement of or synchronization with the load current and is unaffected by the converter voltage. The R_{ds} measurement is experimentally verified to be within $\pm 5\%$ of the true value for the full range of expected resistances. The immunity of the measurement to online conditions is verified with DPT and buck-converter configurations. This measurement circuit provides a flexible in-situ solution for continuously monitoring the health of SiC MOSFETs and therefore helps mitigate the risks of integrating wide bandgap devices into high-power converters.

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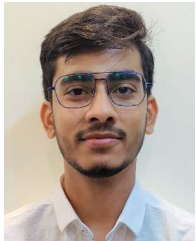

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