A New Simplified Method and Design Guidelines for the Optimization of Push–Pull Class Φ_2 Converters for Wireless Power Transfer Applications

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***Abstract*—The complicated resonant operations of class Φ_2 topology bring challenges for accurate design and performance optimization, hindering the full utilization potential of converters. Considering the narrow design freedom in traditional methods with almost fixed duty cycle D, this article widens the design options of push–pull class Φ_2 converters through frequency-harmonic analysis. A full selection freedom of $D \in (0, 0.5)$ is discussed analytically, providing ample space for optimization based on any required performance indices. From 1.98E5 analytical results, we found six numerical equations that fully decouple the interconnected relations between each circuit parameter and D. The proposed numerical method allows rapid circuit design and component selection with a high accuracy regardless of the system power or load voltage. Parasitic effects are discussed and incorporated into the design approach as correction steps. Finally, we introduce performance analysis based on an example wireless power transfer (WPT) system, providing in-depth studies on the optimization regarding efficiency, power output capability, and component selection. Experimental results validate the accuracy and efficiency of the proposed design method based on a 100-W WPT system at 6.78 MHz frequency. Both inverter and rectifier present load-independent soft-switching operations, with converter efficiency over 93%. The system provides 83% dc–dc efficiency at full load.**

***Index Terms*—MHz, resonant power converters, wireless power transfer (WPT), zero-voltage switching (ZVS), zero-voltage-derivative switching (ZDS).**

I. Introduction

WIRELESS power transfer (WPT) is increasingly becoming a popular technique for diverse applications including electric vehicles, consumer electronics, and industrial applications [1], [2]. WPT systems working at multi-MHz frequencies have the advantage of realizing high efficiency at weak coupling, and more compact systems at higher power density [3] (defined as $\frac{\text{converter power}}{\text{converter volume}}$). Especially, air-core transmitter and receiver coils become possible at MHz operating frequencies [4], removing the need of bulky, fragile, and costly ferrite cores [5]. However, challenges are also introduced to the corresponding dc–ac and ac–dc converters regarding control and losses. The switching loss grows proportionally with the frequency and becomes dominant at MHz. Soft-switching techniques are critical for multi-MHz WPT converters. The conventional full-bridge topology become less suitable due to significantly high switching losses and challenges in high-side driving brought by high dv/dt [6]. Therefore, more studies are focusing on resonant topologies including class E [7], [8], class EF(E/F)$_n$ [8], [9], [10], and class Φ_n [11], [12], [13]. Zero-voltage switching (ZVS) is usually reached in these converters by fully discharging the capacitor in parallel with the switch and bringing its drain–source voltage to zero before turning-ON. During this process, the parasitic output capacitance C_{oss} of the switch is absorbed as a part of the resonance component [14], [15], [16], which sets the lower boundary for capacitance design. With high-order harmonic optimization, the waveform (voltage across, or current through the power switch) can be engineered [17] to reach desired characteristics such as lower voltage or current stress.

Among the resonant converter topologies, class EF$_2$ or class Φ_2 connect resonance branch in parallel with the power switch to remove second harmonic component from the drain–source voltage waveform. The power switches in such topologies greatly benefit from reduced voltage stress (around two times of the input voltage $V_{\text{DC,s}}$) comparing to almost $3.6V_{\text{DC,s}}$ in traditional class E converters [18]. Rather than having large efficiency drop at low $V_{\text{DC,s}}$ for the class E topology, class Φ_2 can maintain relatively constant efficiency over a broad input range [14]. Furthermore, class Φ converters use small-value input inductors as part of the resonance network [19], getting rid of large choke inductors in its class EF counterpart, which is helpful for converter size reduction. The T-network in push–pull topologies (PPT) creates an additional inductive differential branch [20], no more residual inductance or dc block capacitance is required at the ac side. Therefore, the WPT coil can be directly tuned to its resonant frequency, and the PPT class Φ converters have intrinsically load-independent operations among a wide load variation range, compared with traditional resonant converters that only achieve soft switching at the designed nominal load [10], [21].

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Considering the waveform shaping for soft-switching and voltage stress reduction, the resonance network designs are similar in the topologies of class EF_2, class Φ_2, or PPT class Φ_2. However, designs are not straightforward due to the complexity of multiresonance operations. Current approaches mainly focus on the analysis at a particular operation point, which narrows down the applicable range and limits the room for optimization. Assumptions are commonly used during the design process [20], [22], but they are valid within very limited design criteria. Other works design the resonance network only targeting at minimal voltage stress [15] or maximal power output capability (c_{p}) [5], [23], [24], resulting in narrow design possibilities as well. Zero-voltage-derivative switching (ZDS) condition is easily abandoned during the design for simplicity, even ZVS may get lost when optimizing the duty cycle D for better performance [16]. For more general application requirements, rigorous modeling and parameter design methods are still missing. The practical design process is usually carried out by using either simulation-based optimizations [25] or trial-and-error-based design approaches. Such design methods hinder the full potential of the converter, as the operating points are usually suboptimal. The benefits brought by free duty cycle selection [16] have not been investigated yet. Optimizations are greatly time-consuming or even impossible.

Moreover, the parasitic resistance and capacitance are no longer negligible for inductors at MHz frequencies [26], they may shift the resonance, affect soft-switching operations, or even destroy the designed working conditions. Tuning algorithms are developed to eliminate the negative effects from parasitics [16]. However, due to interconnections among the parameters, the required iterations make the process time-consuming. Proper compensation methods or parameter decouple relations are still in urgent demand.

In this article, a harmonic-based approach is introduced for modeling of PPT class Φ_2 converters. We propose a fully analytical parameter design process at first, with the goal to realize the soft-switching criteria including both ZVS and ZDS. Compared with conventional methods where converters are designed based on a fixed angle between the resistive and inductive parts of the differential current[1] $\alpha = 0.26\pi$ [20] and adjusted within a narrow range close to $D = 0.3$ [8], [10], the proposed analytical method expands the design freedom to a much wider range, with the optimization parameter $D \in (0, 0.5)$. The proposed method is unified to all power levels and load resistance, which helps to freely design and optimize the system within the duty range according to given specifications and expected features. With properly designed ZDS characteristics, converters can operate with adjusted power while maintain ZDS soft-switching as long as the components are within their rated operating conditions. Such operation is greatly beneficial, as the absence of ZDS drops the efficiency when $V_{\mathrm{DC,s}}$ increases [16], while our method ensures a maintained high system efficiency when adjusting the rated power. Further, based on 1.98E5 results calculated with the analytical method, we have found six equations describing straightforward relations between each parameter and the optimization parameter D. We propose a simplified numerical design method based on these fully decoupled relations, which provides full freedom for fast and robust system design starting with any given specifications. Accurate tests of the numerical method have shown 95.9% reduction in optimization time compared with the analytical approach. Two correction steps are introduced to the design process for higher accuracy and robustness regarding parasitic effects. In the end, we also discuss the performance of the designed test system and provide guidelines for further developments.

The main contributions of this article are summarized as follows:

1) a fully analytical circuit design method valid for a wide design parameter range;
2) decoupled equations between design parameters;
3) a compact numerical design approach robust to parasitics;
4) system-level performance discussion and guidelines for optimization.

The rest of this article is organized as follows. In Section II, we propose the analytical method of push–pull class Φ_2 converter design. The parameter-decoupled relations are discussed in Section III. Further, we introduce the numerical approach with greatly simplified calculation and accelerated process for optimization. The two-step design correction for parasitic effects is also presented in this section. Based on special case studies, system performances are discussed in Section IV, providing guidelines for component selection and system-level optimization. Section V presents an experimental implementation of a 6.78 MHz WPT system. The test results confirm good validity of the performed analysis and proposed design methods. Finally, Section VI concludes this article.

II. Design Based on a Fully Analytical Model

This section introduces the design of a WPT system with PPT class Φ_2 converters in a systematic way. The operations of the converter are analyzed and fully analytic relations are developed for achieving both ZVS and ZDS directly for the nominal load. The following notations are used throughout this article for easier explanations:

1) subscript "$_n$" represents the nth harmonic of voltage/current component ($n = 1, 2, 3, \ldots$);
2) subscript "$_{\mathrm{a,b}}$" represents the component on the leg-a or leg-b of the circuit, cf., Fig. 10;
3) superscript "$'$" represents the component after the correction of the parasitic effects;
4) current or voltage with
   a) *upper case* (I, V)*:* dc component or amplitude;
   b) *lower case* (i, v)*:* ac component;
   c) *bold characters* $(\mathbf{i}, \mathbf{v})$*:* vector form.

Since the inverter and rectifier have similar operations, we will explain the design process focusing on the inverter side. The analytical design is fully based on the switching harmonic analysis, which is valid regardless of duty cycle selection, and the design solutions ensure direct ZDS operations.

[1] Differential branch inductive angle, see (11).

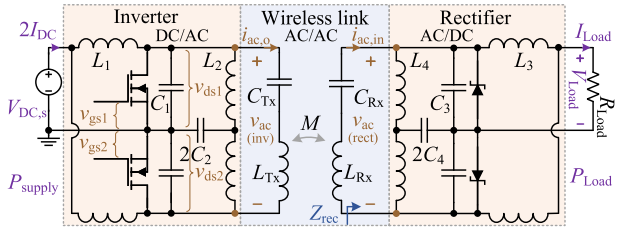

Fig. 1. System structure block diagram of a WPT system using the class Φ_2 inverter and rectifier with T-network filters.

A. System Modeling and Analysis

The schematic of a WPT system including an inverter, a rectifier, and the WPT link is depicted in Fig. 1. The series–series (SS) compensation network is used for transmitter (Tx) and receiver (Rx) coils. Since the PPT class Φ_2 converter has a fixed operating frequency f_s, the WPT branches $L_{Tx} - C_{Tx}$ and $L_{Rx} - C_{Rx}$ are tuned to the resonance at f_s, and, therefore, always show zero phase angle to the converters. The system is analyzed based on the following assumptions:

1) the on-resistance of the switching device $R_{ds(on)}$ is always negligibly small compared with dc- or ac-side equivalent resistance, i.e., $R_{ds(on)} \ll R_{DC}$ and $R_{ds(on)} \ll R_{AC}$;
2) the Tx and Rx coils as well as their series load or input branches have a high quality factor Q, i.e., the currents in Tx and Rx branches are assumed to be sinusoidal;
3) due to the push–pull operation, duty cycle $D \in (0, 0.5)$.

The rectifier input is equivalent to a voltage-control current source, $\mathbf{i}_{ac,in}$, and the inverter has equivalent load impedance Z_{inv} [2], shown as

$$\mathbf{i}_{ac,in} = -\mathrm{j}\frac{\mathbf{v}_{ac}}{\omega_s M}, \quad Z_{inv} = \frac{\omega_s^2 M^2}{Z_{rec}}. \tag{1}$$

Since the dc load (e.g., a battery charger) is always represented as resistive, the input impedance of the rectifier Z_{rec} is also resistive. Therefore, the output impedance seen by the inverter can be simplified as purely resistive: $Z_{inv} = 2R_{AC,o}$.

The four working modes of the PPT class Φ_2 topology are introduced in [20]. To avoid repetitions, we show the main waveforms in Fig. 2. The proposed parameter design method is based on the switching frequency harmonic analysis $(n \cdot \omega_s t)$, where we divide the circuit operations into a differential mode that contains all the odd harmonics $(n = 1, 3, 5, \ldots)$, and a common mode that contains dc and all even harmonic components $(n = 0, 2, 4, \ldots)$. The differential and common mode equivalent circuits of the inverter are given in Fig. 3. The differential currents can be viewed as circulating from the upper leg (leg-a) to the lower leg (leg-b), as shown in Fig. 3(a). Therefore, the two legs are considered as connected in series in differential-mode analysis. The differential currents flowing through the three loops are defined as i_{L1odd}, i_{ac}, and i_{L2odd} [cf., Fig. 3(a)]. They return back together through the $Q_{1,2} \parallel C_1$ differential branch, forming the total differential current i_{diff}. The differential currents result in differential voltages at the corresponding nodes on each leg. At any particular moment, these voltages always have the opposite signs referring to the 0 V "ground" in the middle.

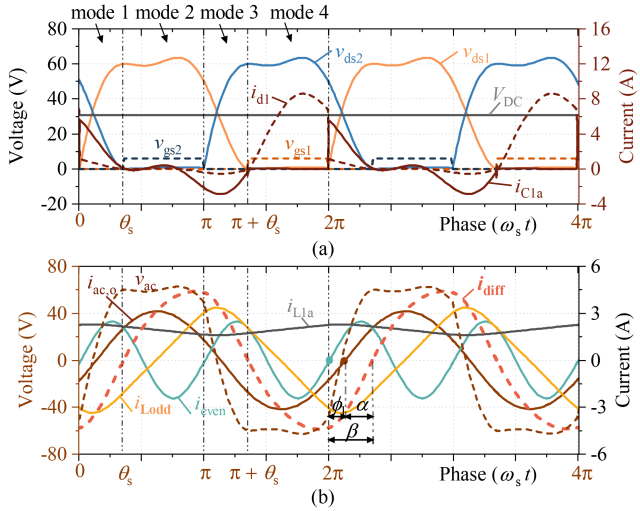

Fig. 2. Main operation modes and waveforms for the PPT class Φ_2 topology. (a) v_{ds} and related currents, (b) phase relations. Voltage and current variables are defined in Figs. 3 and 10(a).

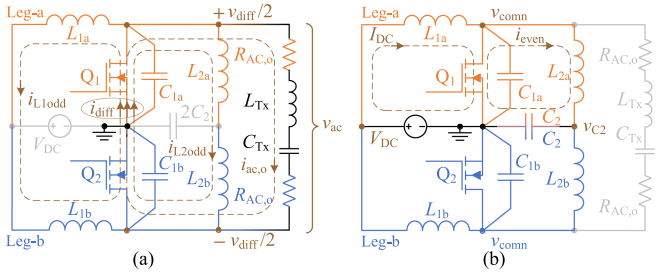

Fig. 3. Equivalent circuit of (a) differential mode and (b) common mode.

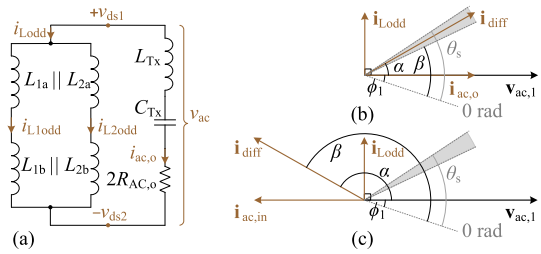

Fig. 4. AC-side differential branch, (a) the equivalent circuit diagram, and corresponding phasor relations of the fundamental frequency components of voltages and currents in (b) the inverter side and (c) the rectifier side. Reference angle (i.e., 0 rad) refers to the time instant when switch Q_1 turns OFF cf., $\omega_s t = 0$ in Fig. 2.

In the differential-mode equivalent circuit, two parallel inductive branches can be simplified into one, with equivalent inductance represented by

$$2L_{eq} = 2L_1 \parallel 2L_2. \tag{2}$$

As illustrated in Fig. 4(a), the total inductive current flowing through this equivalent branch i_{Lodd} is calculated as

$$i_{Lodd}(\omega_s t) = i_{L1odd}(\omega_s t) + i_{L2odd}(\omega_s t). \tag{3}$$

For the fundamental component of the output voltage $\mathbf{v}_{ac,1}$ with phase ϕ_1 and amplitude $V_{AC,1}$ (also represent as V_{AC}), the output

branch current $\mathbf{i}_{\mathrm{ac,o}}$ is approximated to contain only the fundamental component (due to a high-Q filter) and stays in phase with the voltage $\mathbf{v}_{\mathrm{ac},1}$. The equivalent inductive branch connected in parallel with the output branch shares the same voltage but has a 90° lagging inductive current $\mathbf{i}_{\mathrm{Lodd}}$. The corresponding time-domain equations are defined as

$$i_{\mathrm{ac,o}}\left(\omega_{\mathrm{s}}t\right) = I_{\mathrm{AC,o}}\sin\left(\omega_{\mathrm{s}}t-\phi_1\right) \tag{4}$$

$$\begin{aligned} i_{\mathrm{Lodd},1}\left(\omega_{\mathrm{s}}t\right) &= \frac{1}{\omega_{\mathrm{s}}2L_{\mathrm{eq}}}\int v_{\mathrm{ac}}\left(\omega_{\mathrm{s}}t\right)\mathrm{d}\left(\omega_{\mathrm{s}}t\right) \\ &= -I_{\mathrm{Lodd}}\cos\left(\omega_{\mathrm{s}}t-\phi_1\right) \end{aligned} \tag{5}$$

where

$$I_{\mathrm{AC,o}} = \frac{V_{\mathrm{AC}}}{2R_{\mathrm{AC,o}}} \tag{6}$$

$$I_{\mathrm{Lodd}} = \frac{V_{\mathrm{AC}}}{2\omega_{\mathrm{s}}L_{\mathrm{eq}}}. \tag{7}$$

In this section, we consider a lossless circuit where the total ac-side resistive current $I_{\mathrm{AC}} = I_{\mathrm{AC,o}}$ and inductive current $i_{\mathrm{odd}} = i_{\mathrm{Lodd}}$. The total differential current is defined as the sum of i_{ac} and i_{odd}, and its fundamental component is shown as

$$i_{\mathrm{diff},1}\left(\omega_{\mathrm{s}}t\right) = I_{\mathrm{diff}}\sin\left(\omega_{\mathrm{s}}t-\beta\right) \tag{8}$$

where

$$I_{\mathrm{diff}} = \sqrt{I_{\mathrm{AC}}^2 + I_{\mathrm{odd}}^2} \tag{9}$$

$$\beta = \phi_1 + \alpha, \tag{10}$$

$$\alpha = \arctan\left(\frac{I_{\mathrm{odd}}}{I_{\mathrm{AC}}}\right). \tag{11}$$

The vector relations of these currents are illustrated in Fig. 4(b), whereas Fig. 2(b) reveals their relationships in time domain. Here, we note that the phase of the total differential current β and the phase representing the switching moment θ_{s} are two independent variables, and they are not necessarily equal. The former one is obtained in Fig. 4 from the sum of two differential currents, while the latter one depends on the switch duty cycle D, as shown in Fig. 2. By considering θ_{s} and β as two distinct variables, the proposed method can provide expanded design freedom from a fixed T-network resonance point at only $2f_{\mathrm{s}}$ to a wider range of resonance frequencies.

Apart from the fundamental component I_{Lodd}, high-order odd harmonic currents in L_{eq} contribute to the differential current as $i_{\mathrm{diff},n} = i_{\mathrm{odd},n}$, which should be added into consideration if we want to analyze the circuit more rigorously. As the harmonic number increases, its amplitude goes down rapidly. An nth harmonic inductive current is defined in a similar way as its fundamental counterpart in (5), as

$$i_{\mathrm{odd},n}\left(\omega_{\mathrm{s}}t\right) = -I_n\cos\left(n\cdot\omega_{\mathrm{s}}t-\phi_n\right) \tag{12}$$

where amplitudes of the harmonic currents and the corresponding voltage components are related as

$$I_n = \frac{V_{\mathrm{AC},n}}{2n\cdot\omega_{\mathrm{s}}L_{\mathrm{eq}}}. \tag{13}$$

In contrast, the common-mode currents generated by the common dc source $(2I_{\mathrm{DC}})$ or the common $2C_2$ branch in the T-network $(2i_{\mathrm{even}})$ are divided at the forks and flow to the components in two legs simultaneously. The current flowing through C_2 is represented by its amplitude I_2 and phase ϕ_2

$$i_{\mathrm{even}}\left(\omega_{\mathrm{s}}t\right) = I_2\sin\left(2\omega_{\mathrm{s}}t-\phi_2\right). \tag{14}$$

Such symmetric currents result in common voltages at the corresponding nodes on each leg, which have the same signs referring to the circuit ground. Thus, the working principle for the dc and all even harmonics are described by a single-ended common-mode equivalent circuit, shown in Fig. 3(b), where leg-a and leg-b show a parallel equivalence connection.

Thus, by combining the analysis for Fig. 3(a) and (b), the total currents flowing through each circuit component are represented as

$$i_{\mathrm{C1a,b}}\left(\omega_{\mathrm{s}}t\right) = I_{\mathrm{DC}} - i_{\mathrm{even}}\left(\omega_{\mathrm{s}}t\right) \mp i_{\mathrm{diff}}\left(\omega_{\mathrm{s}}t\right), \tag{15}$$

$$i_{\mathrm{L1a,b}}\left(\omega_{\mathrm{s}}t\right) = I_{\mathrm{DC}} \mp i_{\mathrm{L1odd}}\left(\omega_{\mathrm{s}}t\right), \tag{16}$$

$$i_{\mathrm{L2a,b}}\left(\omega_{\mathrm{s}}t\right) = +i_{\mathrm{even}}\left(\omega_{\mathrm{s}}t\right) \pm i_{\mathrm{L2odd}}\left(\omega_{\mathrm{s}}t\right). \tag{17}$$

Since $\mathrm{Q}_{1,2}$ are connected in parallel with $C_{\mathrm{1a,b}}$, the currents in (15) flow through the capacitors only when $\mathrm{Q}_{1,2}$ are OFF. At the ON modes (mode 4 for Q_1, mode 2 for Q_2 as shown in Fig. 2), the same currents switch to the switching component branches and force v_{ds} to be 0. The Q-ON mode duration is represented by D

$$D = \frac{\pi-\theta_{\mathrm{s}}}{2\pi} = 0.5 - D_\delta \tag{18}$$

where θ_{s} and D_δ represent the phase and duty ratio when both gate signals are low, shown as modes 1 and 3 in Fig. 2. By integrating the capacitor current with time, the voltage components across the switches are calculated as

$$\begin{aligned} v_{\mathrm{dsa}}\left(\omega_{\mathrm{s}}t\right) &= \frac{1}{\omega_{\mathrm{s}}C_1}\int i_{\mathrm{C1a}}\left(\omega_{\mathrm{s}}t\right)\mathrm{d}\left(\omega_{\mathrm{s}}t\right), \omega_{\mathrm{s}}t\in\left[0,\pi+\theta_{\mathrm{s}}\right] \\ v_{\mathrm{dsb}}\left(\omega_{\mathrm{s}}t\right) &= \frac{1}{\omega_{\mathrm{s}}C_1}\int i_{\mathrm{C1b}}\left(\omega_{\mathrm{s}}t\right)\mathrm{d}\left(\omega_{\mathrm{s}}t\right), \omega_{\mathrm{s}}t\in\left[0,\theta_{\mathrm{s}}\right]\cup\left(\pi,2\pi\right]. \end{aligned} \tag{19}$$

Thus, the output voltage of the inverter is obtained as

$$v_{\mathrm{ac}}\left(\omega_{\mathrm{s}}t\right) = v_{\mathrm{dsa}}\left(\omega_{\mathrm{s}}t\right) - v_{\mathrm{dsb}}\left(\omega_{\mathrm{s}}t\right). \tag{20}$$

The rectifier has similar working modes as its inverter counterpart. We can analyze the rectifier in the same way as inverters with two modifications: the dc load in rectifiers corresponding to the dc input at the inverter side, and the ac source for the rectifier corresponds to the ac output of the inverter. Considering the power dissipation of a source and a passive load, if the voltage and current direction definitions are kept the same as in the inverter model, the phase relations in the rectifier are shown in Fig. 4(c).

B. Parameter Design Method

This section presents detailed design steps for class Φ_2 inverters using the fully analytical model. The specifications of the

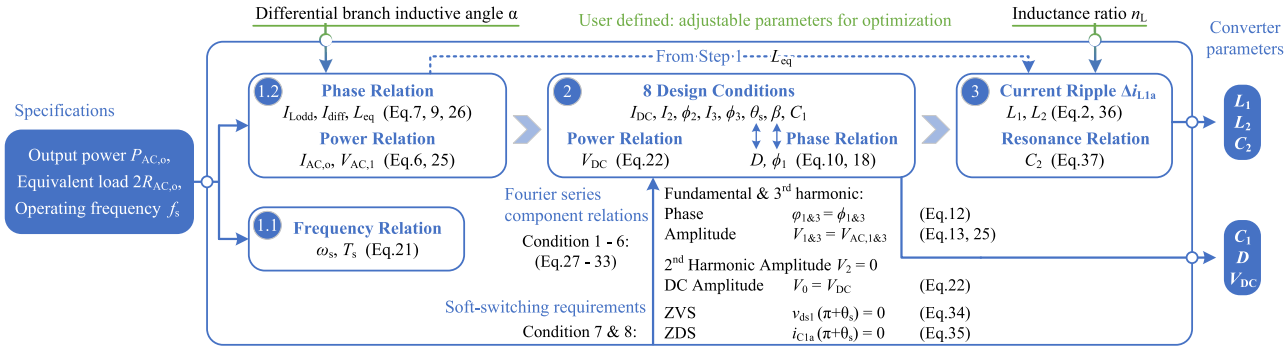

Fig. 5. Parameter design steps flowchart for the proposed analytical method.

WPT system that are defined based on the application requirements are taken as the input to the proposed design approach. In addition to the specifications, the user-defined adjustable parameters are specified based on the optimization criteria. The design flowchart in Fig. 5 summarizes the calculation process for the converter parameters as the output of the design process in three steps.

Determined by the application criteria, the system specifications are defined first, including the rated power at the full load, the equivalent load resistance, and a fixed working frequency (cf., *specifications* block in Fig. 5). The design process comprises three main steps, as described in the following.

1) Step 1: First, the angular switching frequency ω_s and the period T_s can be obtained through

$$\omega_s = 2\pi f_s = \frac{2\pi}{T_s}. \tag{21}$$

The input- and output-side power, the equivalent impedance, and the current and voltage are related as

$$P_{DC} = 2I_{DC} \cdot V_{DC} = (2I_{DC})^2 \cdot R_{DC} \tag{22}$$

$$P_{AC,o} = \frac{I_{AC,o} V_{AC}}{2} = \left(\frac{I_{AC,o}}{\sqrt{2}}\right)^2 2R_{AC,o} = \left(\frac{V_{AC}}{\sqrt{2}}\right)^2 \frac{1}{2R_{AC,o}} \tag{23}$$

$$P_{DC} = P_{AC} = P_{AC,o}. \tag{24}$$

As the whole system is assumed to be lossless at this initial stage of parameter design, the ac power P_{AC} contribute completely to the final output $P_{AC,o}$, and we consider system input voltage $V_{DC,s} = V_{DC}$ [cf., Fig. 10(b)]. Combining the power-related equations (22)–(24), the fundamental component of inverter ac voltage is calculated as

$$V_{AC,1} = V_{AC} = \sqrt{4P_{AC,o}R_{AC,o}} \tag{25}$$

and further the output current is obtained from (6).

Then, different selections of the optimization parameter α define the proportion of inductive current within the total differential current, which is closely related to soft-switching capacitance C_1. Thus, the freedom for choosing α provides a possibility to optimize the system performance parameters, such as the voltage and current stress, power output capability, and efficiency. In Step 2, we always find a design equation set providing one-to-one relation between α and D. According to the available range we set the value of $D \in (0, 0.5)$, while the initial value of α is chosen within the practical range $(0.32, 1.54)$, and then a recursive optimization is implemented to finally determine the α value considering the required performance criteria. We will discuss the optimization based on numerical case studies in Section IV.

At the fundamental frequency, amplitudes of the inductive current I_{odd} and the total differential current I_{diff} are obtained through (7) and (9) based on the chosen value of α. Using (6) and (7), we also calculate the total equivalent inductance $2L_{eq}$ that has the following relation with the inverter equivalent load $2R_{AC,o}$ and α:

$$L_{eq} = \frac{R_{AC,o}}{\omega_s \tan\alpha}. \tag{26}$$

$$v_{diff} = v_{dsa} - v_{dsb} = a_1\cos(\omega_s t) + b_1\sin(\omega_s t) + a_3\cos(3\omega_s t) + b_3\sin(3\omega_s t) + \cdots \tag{27}$$
$$= \underline{V_1}\sin(\omega_s t - \underline{\varphi_1}) + \underline{V_3}\sin(3\omega_s t - \underline{\varphi_3}) + \cdots$$

$$v_{ac} = v_{dsa} - v_{dsb} = \underline{V_{AC,1}}\sin(\omega_s t - \underline{\phi_1}) + \underline{V_{AC,3}}\sin(3\omega_s t - \underline{\phi_3}) + \cdots \tag{28}$$

$$v_{comn} = \frac{v_{dsa} + v_{dsb}}{2} = \frac{a_0}{2} + a_2\cos(2\omega_s t) + b_2\sin(2\omega_s t) + a_4\cos(4\omega_s t) + b_4\sin(4\omega_s t) + \cdots \tag{29}$$
$$= \underline{V_0} + \underline{V_2}\sin(2\omega_s t - \varphi_2) + V_4\sin(4\omega_s t - \varphi_4) + \cdots$$

$$v_{avg} = \frac{v_{dsa} + v_{dsb}}{2} = \underline{V_{DC}} + \underline{0} + V_{avg,4}\sin(4\omega_s t - \phi_4) + \cdots \tag{30}$$

2) Step 2: So far, we dealt with the circuit description equations in Section II-A. At Step 2, we calculate eleven variables: $V_{\rm DC}$, ϕ_1, D, $I_{\rm DC}$, I_2, ϕ_2, I_3, ϕ_3, $\theta_{\rm s}$, β, and C_1. Some of them have relationships that we have already discussed; however, they are not sufficient to find these eleven parameters. We find 1) six hard conditions (Conditions 1–6) describing the current and voltage relationships according to the switching frequency harmonic relations, and 2) two optimization conditions (Conditions 7 and 8) regarding ZVS and ZDS soft switching. Satisfying these eight conditions allows us to find numerical solutions for the abovementioned eight parameters that are underlined. Then the remaining three variables $V_{\rm DC}, \phi_1, D$ are obtained based on the relations given in Section II-A.

Condition 1–6: The Fourier series expansions of $v_{\rm diff}$ and $v_{\rm comn}$ are written as (27) and (29), where a_n and b_n are the Fourier coefficients, and the amplitude and phase of Fourier components

$$V_n = \sqrt{a_n^2 + b_n^2}, \qquad \varphi_n = -\arctan\left(\frac{a_n}{b_n}\right) \tag{31}$$

are the expressions of the eight underlined variables according to (19). On the other hand, voltage $V_{{\rm AC},n}$ and phase ϕ_n of the switching frequency harmonic components in (28) and (30) are already defined through (12)–(14) and (25). Since $v_{\rm diff} = v_{\rm ac}$ and $v_{\rm comn} = v_{\rm avg}$, Conditions 1–6 should satisfy the corresponding phase and amplitude relations in (27)–(30) shown at the bottom of the previous page, i.e.,

$$V_n = \begin{cases} V_{{\rm AC},n}, & n = 1,3,5,\cdots \\ V_{{\rm avg},n}, & n = 0,2,4,6,\cdots \end{cases} \tag{32}$$

$$\varphi_n = \phi_n, \qquad n = 0,1,2,3,\cdots \quad . \tag{33}$$

Since the dc voltage drop across the inductor L_1 is always zero, $V_{{\rm avg},0} = V_{\rm DC}$. The T-network removes the second harmonic voltage from $v_{\rm ds}$ that makes $V_{{\rm avg},2} = 0$.

These conditions describing frequency harmonic relations can be further expanded to include higher order harmonic components with $n \geq 4$. In total, two more variables I_n and ϕ_n will be introduced once we bring in one more harmonic component of $n\omega_{\rm s}$ for analysis, which also provides two more conditions to be satisfied. Thus, including more harmonics to analysis makes the condition set more complete but more complicated as well. In order to take a balance between accuracy and simplicity, including the $v_{\rm diff}$ and $v_{\rm comn}$ components with $n = 0,1,2,3$, is accurate enough for the design.

After describing the harmonic phase and amplitude relationships as six abovementioned conditions, we set the requirement on switching conditions as follows.

Condition 7: Taking a single-ended side (e.g., leg-a) of the push–pull circuit, conditions of ZVS on power switch Q_1 shown in Fig. 2 can be written as

$$v_{\rm dsa}(\pi + \theta_{\rm s}) = 0. \tag{34}$$

Condition 8: In order to achieve ZDS, the current through the parallel capacitor at the switching moment should be zero

$$i_{\rm C1a}(\pi + \theta_{\rm s}) = 0. \tag{35}$$

Therefore, by satisfying the eight design conditions together, we can directly find numeric values of $I_{\rm DC}$, I_2, ϕ_2, I_3, ϕ_3, $\theta_{\rm s}$, β, and C_1. Among the remained variables, the input voltage is calculated through the dc-side power relation (22), whereas the phase relations (10) and (18) determine ϕ_1 and D.

At Step 2, we found eight intermediate variables describing the converter operations and three output parameters required for converter implementation, the input voltage $V_{\rm DC}$, the duty cycle D, and the parallel capacitance C_1, as depicted in Fig. 5.

3) Step 3: During Step 3, all the unknown variables are found by considering practical implementation aspects. First, we introduce an adjustable parameter $n_{\rm L} = L_1/L_2$ to describe the inductance ratio. Combined with (2), the value of each inductor is obtained as $L_1 = (n_{\rm L}+1)L_{\rm eq}$ and $L_2 = (n_{\rm L}+1)L_{\rm eq}/n_{\rm L}$. Considering the input inductor current ripple limitation, the current ripple level on L_1 is calculated as

$$\Delta i_{\rm L1a} = \frac{V_{\rm DC}}{L_1} \cdot DT_{\rm s} < r_{\rm I} I_{\rm DC} \tag{36}$$

where $r_{\rm I}$ is the maximum ratio between the current ripple $\Delta i_{\rm L1a}$ and the input dc current $I_{\rm DC}$. The criteria for determining the value of $n_{\rm L}$ to optimize the dc current ripple and the converter efficiency is discussed in Section IV. Once $n_{\rm L}$ is defined, we obtain the values for L_1 and L_2.

With resonance frequency of $2f_{\rm s}$ in the T-network, the value of C_2 can be calculated from

$$C_2 = \frac{1}{(2\omega_{\rm s})^2 L_2}. \tag{37}$$

So far, the remained component values for converter implementation, L_1, L_2, and C_2, are obtained at Step 3. At the output of the design process in Fig. 5, we have all the parameters required for building an inverter.

C. Parameter Design of Rectifier

Working principles of the rectifier are similar to the inverter, with an alternation of the input and output sides. Therefore, all the voltage-related equations on the rectifier side are the same as for the inverter. Only the phase of ac current $i_{\rm ac,in}$ is half-cycle shifted, and the value of final output dc current $I_{\rm Load}$ changes from positive to negative, as shown in Fig. 4(c).

Therefore, *Conditions 1–6* describing component internal current and voltage relations are still valid for the rectifier. The rectifier-side switching components are expected to operate with zero-current turn-OFF and zero-voltage turn-ON. In the case of soft-switching requirements, *Condition 7* for ZVS-ON is still valid, while *Condition 8* changes into ZCS-OFF condition

$$i_{\rm C1a}(0) = 0. \tag{38}$$

As a result, the same parameter design steps shown in Fig. 5 can also be applied to the rectifier, and all the parameters in the WPT system can be calculated analytically.

TABLE I
DESIGN AND EVALUATION PARAMETERS

Specifications		Opt. parameter	Perform.	Constr.
Load / SPLY	WPT stage			
power voltage current resistance	$L_{\mathrm{Tx}}, L_{\mathrm{Rx}}$ M k f_{r}	D or α n_{L}	$\eta_{\mathrm{Inv,Rec,WPT}}$ η_{tot} c_p Δi_{L1}	C_{oss} Δi_{L1} $V_{\mathrm{ds(pk)}}$ $I_{\mathrm{d(pk)}}$

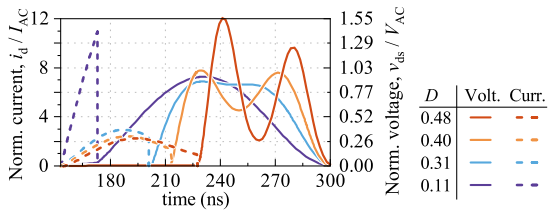

Fig. 6. v_{ds} and i_{d} waveform with respect to D variation (normalized to AC voltage and current). Specifications for the example case study: 100 W rated power, the input DC voltage is 30 V, and the output DC voltage is 28 V.

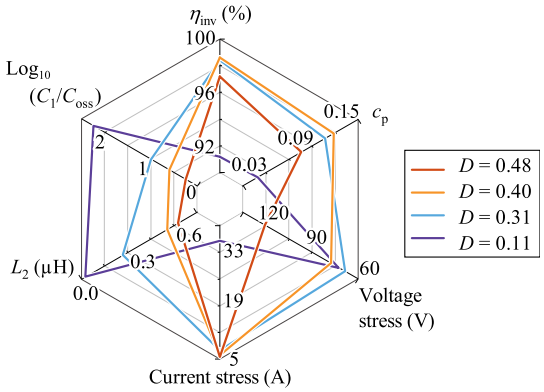

Fig. 7. Converter performance and implement parameters with respect to D variation. Specifications for the example case study: 100 W rated power, the input dc voltage is 30 V, and the output dc voltage is 28 V cf., Fig. 6 for the voltage and current waveforms corresponding to different D.

D. Characterization of the Design and Performance Parameters

Table I classifies all the discussed parameters into four categories: specifications, optimization parameters, performance indices, and practical constraints. System power and voltages are usually defined by applications, whereas the WPT stage parameters (i.e., coil self-inductances L_{Tx}, L_{Rx} and self-resonance frequency $f_{\mathrm{r}} = r f_{\mathrm{s}}$) are specified by the coil design. The coupling coefficient k or mutual inductance M can be adjusted within a limited range, but little space is left for optimization on these parameters.

On the other hand, changing the optimization parameter D, as shown in Fig. 6, may have significant effects on system performance even with fixed design specifications. The inductor current ripple, and voltage and current stresses are closely related to D. Converter efficiency and power output capability c_{p} are affected accordingly. As an example, Fig. 7 shows performance parameters (η_{Inv} and c_{p}), components for implementation (C_1/C_{oss} and L_2), and restrictions (voltage and current stresses). It shows that a relatively high duty cycle $D = 0.4$ is greatly beneficial for performance, whereas a smaller $D = 0.1$ tends to provide easier selection for components. However, when D gets even higher and close to 0.5, the voltage stress increases rapidly and brings down the converter performance. A similar concern for the current stress appears when D is close to the other boundary $D \to 0$. In comparison, the assumptions used in the conventional method [20] are only valid for a limited range of D around 0.3. The choice of such duty cycle is a balance between performance and implementation simplicity, but it does not provide the full scale for system performance optimization.

Therefore, designs can be optimized by considering different optimization goals depending on the application criteria. For example, the optimization objective can be given as follows:

1) the optimal efficiency or maximal power output capability c_{p} by selecting a suitable optimization parameter D or α;
2) or based on the dc-side inductor current ripple $\Delta i_{\mathrm{L1}}/I_{\mathrm{DC}}$ considering EMI requirement.

The practicality of any implementation should always be considered during the optimization process, and here, we list the following most important limitations.

1) The total parallel capacitance C_1 for soft-switching should be able to include parasitic output capacitance C_{oss} of the selected power switch, i.e., $C_1 > C_{\mathrm{oss}}$.
2) Current and voltage stress should always stay within the range of the device limits $V_{\mathrm{ds(pk)}}$ and $I_{\mathrm{d(pk)}}$.
3) Current flowing through the dc-side inductors is always positive, i.e., $r_{\mathrm{I}} = \Delta i_{\mathrm{L1}}/I_{\mathrm{DC}} < 200\%$.

III. SIMPLIFIED DESIGN METHOD

With full design freedom provided by the analytical method, the increased choice of the optimization parameters allows selections of the optimal design that optimizes converter performance. However, the analytical design method involves solving multiple nonlinear equations, where numerical solvers need to be used. Such complicated processes are very resource intensive and time demanding. In particular, for the purpose of optimization, we have to solve the whole equation set at many different design points.

In this section, we propose an alternative simplified numerical method for the design and optimization of class Φ_2 converters. To this end, we have analyzed 1.98×10^5 design solutions obtained through the analytical method, with varying specifications $P_{\mathrm{Load}} \in [10, 3000]$ W, $R_{\mathrm{Load}} \in [1, 1000]\,\Omega$, and the optimization parameter $D \in (0, 0.5)$. It was possible to reveal decoupled relations of design parameters, as shown in Fig. 8, where the dependence between the intermediate variables is eliminated. By analyzing these decoupled relations, we find numerical trends showing straightforward relations between the design variables and the duty cycle D. In the following, we introduce a two-step correction to account for parasitic effects. Combining with the steps for correction and optimization, the numerical approach provides a fast, simplified, and robust design tool for any WPT

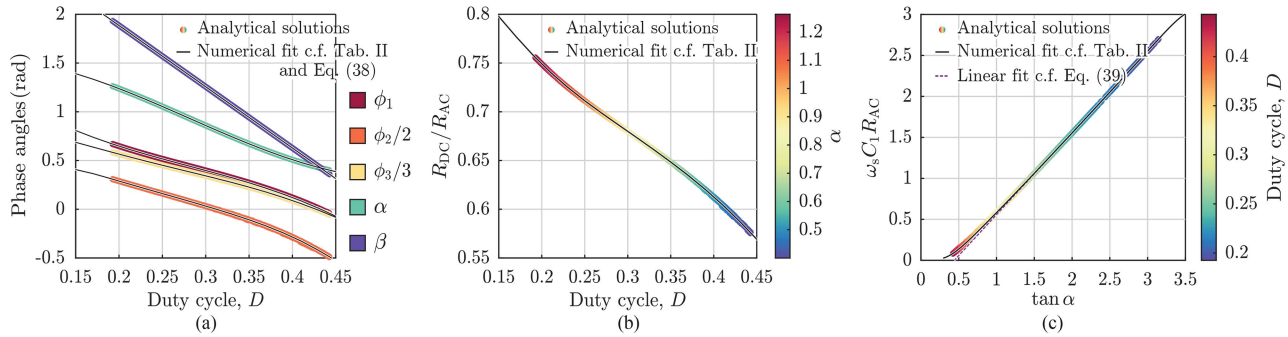

Fig. 8. Parameter decouple relations between (a) phases and duty cycle. (b) Ratio of input and output resistances versus duty cycle. (c) $\omega_s C_1 R_{AC}$ versus tan α. Contains 1.98×10^5 data points with power $P_{Load} \in [10, 3000]$ W and load resistance up to 1000 Ω. The design equations are derived from the numerical curve fitting as given in Table III and (39)–(40).

TABLE II
COMPARISON BETWEEN THE PROPOSED METHOD AND THE EXISTING DESIGN APPROACHES

		Existing works	The proposed method
Design	Accuracy	Suboptimal operating points due to the trial-and-error-based design approach [19], [25]	ZVS and ZDS operations are guaranteed through the proposed design equations
		The components are assumed sumed to be ideal	Parasitic effects correction is included as part of the design process
	Valid range	Only valid at fixed point when $D \approx 0.3$ [10], [20], [22]	Valid for full duty cycle selection range $D \in (0, 0.5)$
	Simplicity	Solve analytical resonance equations with coupled parameters [9], [15]	Six fully decoupled numerical equations [cf., Table III and Eq. (39)–(40)]
Optimization	Freedom	Specific performance target, e.g., minimum voltage stress [15], maximum power output capability [5],[23],[24]	Full freedom for optimizing any performance criteria
	Speed	Slow, due to the coupled parameters in analytical equations [9], [15]	Fast, 95.9 % reduction in optimization time compared to the analytical approach in the design example

TABLE III
DESIGN EQUATIONS FOR PARAMETERS α, $\phi_{1,2,3}$, INPUT–OUTPUT RESISTANCE RATIO R_{DC}/R_{AC}, AND $\omega_s C_1 R_{AC}$

function	$y = f(x) = a_0 + \sum_{i=1}^{3} [a_i \cos(i \cdot wx) + b_i \sin(i \cdot wx)]$				
x	D				$\tan\alpha$
y	α	ϕ_2	ϕ_3	R_{DC}/R_{AC}	$\omega_s C_1 R_{AC}$
a_0	0.9312	-57.71	0.1841	0.6753	0.6819
a_1	0.617	71.05	2.279	0.06411	-0.6067
b_1	0.1173	31.62	1.224	0.1365	-0.3214
a_2	—	-12.11	0.2865	0.03997	-0.07078
b_2	—	-15.34	-0.5491	0.03509	0.05524
a_3	—	—	—	0.007978	—
b_3	—	—	—	0.003402	—
w	6.246	2.039	5.499	8.779	1.871
RMSE*	0.0003	0.001	9.3e-5	0.0001	0.0003

*RMSE is used to evaluate the fitting accuracy.

system with PPT class Φ_2 converters. The proposed design process ensures direct realization of both ZVS and ZDS even with practical tolerances and parasitic effects. A compact comparison between the existing and the proposed design approaches is provided in Table II, showing the advantages of the proposed method in the aspects of design efficiency and optimization freedom.

A. Parameter Decoupling

1) Between Phases α, β, ϕ_n, and the Duty Cycle D: Analyzing Fig. 8(a), we have found that all the phase parameters (i.e., α, β, and $\phi_{1,2,3}$) can be found as functions of D, and these functions do not depend on specifications. This means that now that the data points for a large number of designs have been properly analyzed, one can use these simple decoupled relations to design converters with any required performance parameters. Note that Fig. 8 includes data points for all 1.98×10^5 designs.

The numerical relation between two optimization parameters, $\alpha = f(D)$, is easily found as the fitted curve in black, Table III tabulates the coefficients of $f(D)$. Similarly, other phases ϕ_n and β can also be expressed as functions of D only, with the corresponding coefficients given in Table III.The result reveals that when the T-network resonates at $2f_s$, the relation $\beta = \theta_s$ is valid for any duty cycle. Therefore, ϕ_1 can be found as

$$\phi_1 = \beta - \alpha = \pi - 2\pi D - \alpha. \tag{39}$$

The numerical equations given in Table III give straightforward and direct relations between each phase angle and the duty cycle D for all possible designs at any specification.

2) Between Resistance Ratio R_{DC}/R_{AC} and D: Similarly, the ratio between the converter input and output resistances is also obtained as a function of D, with the coefficients given in Table III. Fig. 8(b) presents the datapoint distribution and a fitted curve for the decoupled relation. This straightforward relationship between R_{DC} and R_{AC} provides full freedom for converter design from either the supply side or the load side. Fast design is reached for any given specification.

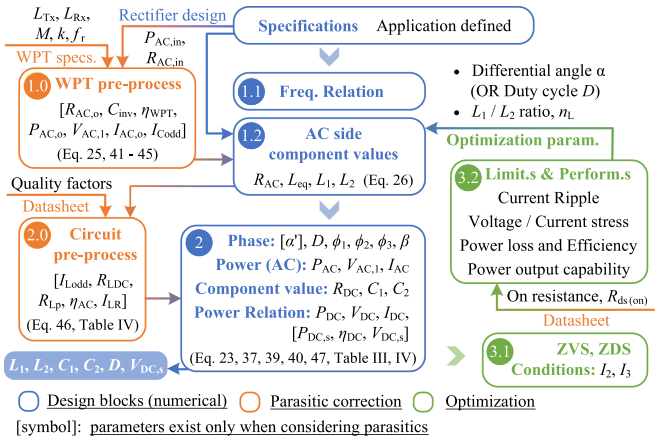

Fig. 9. Flowchart explaining the proposed simplified design method including the correction steps to incorporate parasitic effects and optimization steps for performance improvements.

3) Between α and $\omega_s C_1 R_{AC}$: The solution for capacitance C_1 can also be decoupled from the other dependencies and found as a function of R_{AC} and α. As shown in Fig. 8(c), the $\omega_s C_1 R_{AC}$–$\tan\alpha$ dependency is fitted nicely by a linear function in (40) when $\tan\alpha \geq 1.5$, showing only 0.001 root-mean-square error (RMSE). To get a similar level of accuracy for $\tan\alpha < 1.5$, the $\omega_s C_1 R_{AC}$–$\tan\alpha$ relation is fitted as $\omega_s C_1 R_{AC} = f(\tan\alpha)$ using the function and coefficients given in Table III, which also provides good accuracy of $\mathrm{RMSE} = 0.0003$. Therefore, the decoupled relation during full α variation range is expressed as

$$\omega_s C_1 R_{AC} = \begin{cases} 0.9976\tan\alpha - 0.4402, & \tan\alpha \geq 1.5 \\ f(\tan\alpha), & \tan\alpha < 1.5. \end{cases} \tag{40}$$

From Fig. 8(c), we found that the rated power and voltage do not affect the value of C_1. It reveals that soft-switching features are independent from the system power or voltage. Once the designed converter operates at a fixed duty cycle, its ZVS and ZDS will not be destroyed when changing $V_{DC,s}$. Only the operating power may change with this variation, providing flexible adjustment of the output voltage or current.

B. Numerical Design Method

Due to decoupling of the expressions for phase relation, R_{DC}/R_{AC}, $\omega_s C_1 R_{AC}$, and D, design equations (32)–(33) in the analytical design flowchart can be replaced by simplified numerical relations defined in Table III and (39)–(40). The analytical design method presented in Fig. 5 is also simplified to a numerical version, as shown in Fig. 9. When parasitic effects are not considered, the converter design goes through all the blue-outlined boxes from Steps 1 to 2. Due to the straightforward relation between D and α, the numerical design can start from either one of the optimization parameters, with $D \in (0, 0.5)$ or $\alpha \in (0.32, 1.54)$. Then, the load-side parameters R_{AC} and L_{eq} are calculated at Step 1.2 according to the same equation as in the analytical approach. Similarly, the inductance ratio $n_L = L_1/L_2$ is also defined at the beginning and can be later optimized. At Step 2, all the phase values, as well as C_1 and R_{DC}, are calculated based on Table III. Following the lossless-case equations in Table IV, the power-related parameters are obtained. Until Step 2, we gathered all the parameters $L_{1,2}, C_{1,2}, D$, and $V_{DC,s}$ required for the design.

The numerical method allows us to avoid solving complex equation sets, greatly simplifies the design and optimization, maintaining high accuracy during the process. The proposed numerical method gives the component values almost identical to the results of the fully analytical method, as compared in Fig. 8. Table III also presents the RMSEs of comparison between the results of numerical and analytical calculations. The errors are negligibly small (always smaller than 0.001). Furthermore, the time taken for calculating the component values of 1.98×10^5 design points using the analytical method was 1248 min, whereas it took only 50.8 min for the design based on the simplified numerical method, showing more than 95.9% time saved for the optimization process.

C. Design Correction to Compensate Parasitic Effects

In practical implementations, the components are not ideal, and possess parasitic resistances and reactances, especially for the inductors. Parasitic resistance is connected in series with the inductor, which is usually represented by the quality factor in the datasheet. The WPT coils should also be considered including losses measured by the quality factor Q. In addition, the effect of the parasitic capacitance becomes dominant when the self-resonance frequency of WPT coils f_r gets close to the switching frequency (i.e., r gets closer to 1). The equivalent parasitic components and connections are revealed in the blue outline on top of the lossless model in Fig. 10(a).

Therefore, we introduce two preprocessing steps for corrections due to effects of inductor parasitic resistances and capacitances. The additional prepossessing steps are added to the parameter design flow chart as Step $x.0$ before each step, shown as the orange-outlined boxes in Fig. 9.

1) Step 1.0. WPT Preprocess: The equivalent circuit considering parasitics is introduced in Fig. 10(b), where losses in inductors are represented by the equivalent parallel resistance R_{Lp} in the differential mode and by R_{LDC} in the common mode. Therefore, the dc inductors are modeled as chokes, and the series-compensated Tx coil is modeled as an ideal filter. The parasitics in WPT stage may lead to a slight change in the equivalent resistance R_{inv}, and bring in additional capacitive load C_{inv} connected in parallel. These two parameters are calculated as

$$C_{inv} = \frac{A_0 k \left[B_2^2 R_{rec}^2 + r^4 \left(B_3^2 - \frac{A_1^4}{A_0^4} R_{rec}^2\right)\right]}{\omega_s r^2 \omega_s M \left(B_2^2 R_{rec}^2 + r^4 B_3^2\right)} \tag{41}$$

$$R_{inv}{}' = 2R_{AC,o} = \frac{\omega_s M \left(B_2^2 R_{rec}^2 + r^4 B_3^2\right)}{A_1 \left(A_0^2 k^2 B_1 R_{rec}^2 + r^4 A_2 B_3\right)} \tag{42}$$

where

$$A_0 = (r^2 - 1)/r^2, \quad A_1 = A_0^2 kQ, \quad A_2 = A_1 R_{rec} + \omega_s M$$

TABLE IV
(COL. 1) DESIGN EQUATIONS AS DEFINITIONS, (COL. 2) EQUATIONS VALID FOR THE LOSSLESS CASE, AND (COL. 3) REVISED EQUATIONS CONSIDERING PARASITIC EFFECTS

	Column 1: Definitions	**Column 2:** Lossless case	**Column 3:** Lossy case consider parasitic effects
Row 1	$i_{\text{diff}} = i_{\text{ac}} + i_{\text{odd}}$	$i_{\text{ac}} = i_{\text{ac,o}}$ $i_{\text{odd}} = i_{\text{Lodd}}$	$i_{\text{ac}} = i_{\text{ac,o}} + i_{\text{LR}}$ $i_{\text{odd}} = i_{\text{Lodd}} - i_{\text{Codd}} = i_{\text{L1odd}} + i_{\text{L2odd}} - i_{\text{Codd}}$
Row 2	$V_{\text{AC},n} = I_{\text{odd},n} \cdot X_{\text{eq},n}$ $I_{\text{diff}}^2 = I_{\text{AC}}^2 + I_{\text{odd}}^2$ $I_{\text{odd}} = I_{\text{AC}} \cdot \tan\alpha$	$I_n = I_{\text{odd},n} = I_{\text{Lodd},n}$ $X_{\text{eq},1} = \omega_s L_{\text{eq}}$	$I_n = I_{\text{odd},n} = I_{\text{Lodd},n} - I_{\text{Codd},n}$ $X_{\text{eq},1} = \omega_s L_{\text{eq}} \parallel -\dfrac{1}{\omega_s 2C_{\text{inv}}}$
Row 3	$R_{\text{AC}} = \dfrac{V_{\text{AC}}}{2I_{\text{AC}}}$, $P_{\text{AC}} = \dfrac{V_{\text{AC}} I_{\text{AC}}}{2}$ $R_{\text{DC}} = \dfrac{V_{\text{DC}}}{2I_{\text{DC}}}$, $P_{\text{DC}} = 2V_{\text{DC}} I_{\text{DC}}$	$I_{\text{AC}} = I_{\text{AC,o}}$, $V_{\text{DC,s}} = V_{\text{DC}}$ $R_{\text{AC}} = R_{\text{AC,o}}$, $R_{\text{DC,s}} = R_{\text{DC}}$	$I_{\text{AC}} = I_{\text{AC,o}} + I_{\text{LR}}$, $V_{\text{DC,s}} = V_{\text{DC}} + V_{\text{LDC}}$ $R_{\text{AC}} = R_{\text{AC,o}} \parallel R_{\text{Lp}}$, $R_{\text{DC,s}} = R_{\text{DC}} + \dfrac{R_{\text{LDC}}}{2}$
	$\eta_{\text{AC}} = \dfrac{P_{\text{AC,o}}}{P_{\text{AC}}}$, $\eta_{\text{DC}} = \dfrac{P_{\text{DC}}}{P_{\text{DC,s}}}$ $\eta_{\text{Inv}} = \eta_{\text{AC}} \cdot \eta_{\text{DC}} \cdot \eta_{\text{loss}}$	$P_{\text{AC}} = P_{\text{AC,o}}$, $P_{\text{DC,s}} = P_{\text{DC}}$ $P_{\text{supply}} = P_{\text{DC,s}} = P_{\text{DC}} = P_{\text{AC}} = P_{\text{AC,o}}$	$P_{\text{AC}} = P_{\text{AC,o}} + P_{\text{LR}}$, $P_{\text{DC,s}} = P_{\text{DC}} + P_{\text{LDC}}$ $P_{\text{supply}} = P_{\text{DC,s}} + P_{\text{cond}}$
		$\eta_{\text{AC}} = 1$, $\eta_{\text{DC}} = 1$	$\eta_{\text{AC}} = \dfrac{R_{\text{AC}}}{R_{\text{AC,o}}}$, $\eta_{\text{DC}} = \dfrac{R_{\text{DC}}}{R_{\text{DC,s}}}$

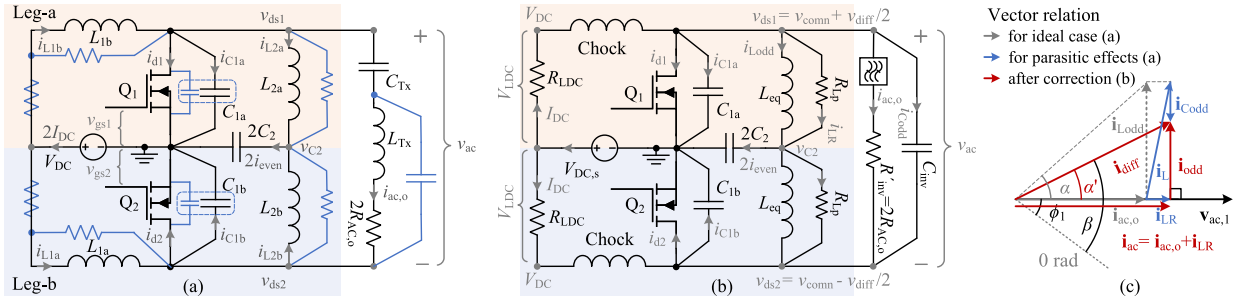

Fig. 10. (a) Inverter circuit illustrating parasitic components (in blue). The lossless ideal circuit can be derived by removing blue-colored components. (b) Equivalent circuit considering the effects of parasitic components. (c) Vector relation of currents/voltages for the ideal case and with parasitic effect correction.

$$B_1 = 1 + k^2 Q^2, \quad B_2 = A_0 k B_1, \quad B_3 = A_1 R_{\text{rec}} + B_1 \omega_s M.$$

Two ac-side equivalent branches share the same voltage $V_{\text{AC},1}$, with currents $i_{\text{ac,o}}$ and i_{Codd}, respectively. Therefore, the reactive current flowing through the equivalent capacitive branch is calculated as

$$I_{\text{Codd}} = V_{\text{AC},1} \cdot \omega_s C_{\text{inv}}. \tag{43}$$

Similarly, the power loss of WPT coils P_{WPT} is calculated through the WPT specifications and the required rectifier input as (44) shown at the bottom of this page. Thus, the WPT stage efficiency can be obtained at this step as

$$\eta_{\text{WPT}} = \frac{P_{\text{AC,rec}}}{P_{\text{AC,inv}}} = \frac{P_{\text{AC,rec}}}{P_{\text{AC,rec}} + P_{\text{WPT}}} \tag{45}$$

and meanwhile, the inverter load power $P_{\text{AC,o}} = P_{\text{AC,inv}}$ is obtained. The remained parameters at this step, $V_{\text{AC},1}$ and $I_{\text{AC,o}}$, are still calculated through (25) and (23).

Next, $R_{\text{AC,o}}$ is fed to Step 1.2, and R_{AC} is revised following the equation for the lossy case in Table IV—Col. 3, Row 1. The calculation for the other parameters at Step 1.2 are kept unaffected.

2) Step 2.0. Circuit Preprocess: Considering the inductor voltage $\mathbf{v}_{\text{ac},1}$ and current $\mathbf{i}_{\text{L}}$ relationship in Fig. 10(c), we can split the inductor current $\mathbf{i}_{\text{L}}$ into resistive part $\mathbf{i}_{\text{LR}}$ and inductive part $\mathbf{i}_{\text{Lodd}}$. Thus, the inductor is equivalent to a resistive branch R_{Lp} and an inductive branch with revised L_{eq}, both connected in parallel with the ac load. The resistive current due to the inductor parasitic resistance is calculated as

$$I_{\text{LR}} = \frac{V_{\text{AC},1}}{2R_{\text{Lp}}} \tag{46}$$

while the inductive current I_{Lodd} still follows (7). The ac-side efficiency of the inverter is defined in Table IV—Col. 1, Row 3, and it can be calculated at this step through the ratio of the ac-side resistances given in Col. 3 of the same table.

3) Corrected Step 2. Corrected Phase and Power: At this step, the predefined parameters are corrected based on the parallel equivalences at Step 2.0. Shown in Table IV—Row 1, the total inductive current i_{odd} is contributed by both i_{Lodd} and i_{Codd}

$$P_{\text{WPT}} = \frac{A_1 \left[k^2 \left(A_0^2 + \dfrac{A_1^2}{A_0^2} \right) R_{\text{rec}}^2 + r^4 \left(A_2^2 + \omega_s^2 M^2 \dfrac{A_1^2}{A_0^4} \right) \right]}{\omega_s M \left(B_2^2 R_{\text{rec}}^2 + r^4 B_3^2 \right)} \frac{V_{\text{AC}}^2}{2}. \tag{44}$$

TABLE V
VOLTAGE AND CURRENT GAINS OF EACH STAGE IN THE SYSTEM

	Voltage gain	Current gain
Rect.	$\frac{V_{\text{Load}}}{V_{\text{AC(rec)}}} = \sqrt{\frac{\eta_{\text{DC}}}{4}\frac{R_{\text{DC}}}{R_{\text{AC}}}}$	$\frac{I_{\text{Load}}}{I_{\text{AC,in}}} = \sqrt{\eta_{\text{AC}}\frac{R_{\text{AC}}}{R_{\text{DC}}}}$
WPT	$\frac{V_{\text{AC(rec)}}}{V_{\text{AC(inv)}}} = G_{\text{WPT}} Z_{\text{rec}}$	$\frac{I_{\text{AC,in}}}{I_{\text{AC,o}}} = G_{\text{WPT}} Z_{\text{inv}}$
Inv.	$\frac{V_{\text{AC(inv)}}}{V_{\text{DC,s}}} = \sqrt{4\eta_{\text{DC}}\frac{R_{\text{AC}}}{R_{\text{DC}}}}$	$\frac{I_{\text{AC,o}}}{I_{\text{DC}}} = \sqrt{\eta_{\text{AC}}\frac{R_{\text{DC}}}{R_{\text{AC}}}}$

after the correction, and the total resistive current i_{ac} becomes $(i_{\text{ac,o}} + i_{\text{LR}})$. Their vector relations are illustrated in Fig. 10(c), with the initial differential angle α revised as

$$\alpha' = \arctan\left(\frac{I_{\text{Lodd,1}} - I_{\text{Codd}}}{I_{\text{AC,o}} + I_{\text{LR}}}\right) = \arctan\left(\frac{R_{\text{AC,o}} \parallel R_{\text{Lp}}}{\omega_{\text{s}} L_{\text{eq}} \parallel -\frac{1}{\omega_{\text{s}} 2C_{\text{inv}}}}\right). \quad (47)$$

The equations describing the circuit operations are summarized in Table IV, where the total ac resistive and inductive currents maintain the same relation with α (i.e., Col. 1, Row 2) regardless of the corrections. The relationships between power, voltage, current, and resistance (i.e., Col. 1, Row 3) are also valid as defined, only the composition of each ac or dc current is changed (i.e., Row 3, Col. 1 for lossless case to Col. 2 for lossy case).

Apart from the dc-side and ac-side resistive losses modeled by η_{DC} and η_{AC}, the converter losses also contain conduction losses caused by the ON-resistance of two power switches, $R_{\text{ds(on)}}$. The conduction loss is found as

$$P_{\text{cond}} = 2 \cdot \frac{1}{2\pi} \int_{(\pi+\theta_{\text{s}})}^{2\pi} i_{\text{d}}^2(\omega_{\text{s}} t)\, R_{\text{ds(on)}}\, \text{d}(\omega_{\text{s}} t). \quad (48)$$

The switching loss is negligibly small due to the soft-switching operations. Thus, the inverter efficiency is calculated as is shown in Table IV, Row 3, where η_{loss} is the efficiency factor due to losses on the power switches, calculated as

$$\eta_{\text{loss}} = \frac{P_{\text{DC,s}}}{P_{\text{supply}}} = \frac{P_{\text{DC,s}}}{P_{\text{DC,s}} + P_{\text{cond}}}. \quad (49)$$

D. Optimization Steps Based on Performance and Constraints

Finally, in Fig. 9, the steps for optimization are given in the green-outlined boxes. By iterating within Steps 1.2–3.2, the design is optimized toward the target performance within the set limitations, until a proper duty cycle D and inductance ratio n_{L} are selected. The detailed performance analysis according to the optimization is discussed in Section IV.

Further, precise voltage and current gains for each converter and the WPT link are given in Table V, where all the parasitic effects are considered. G_{WPT} represents the transfer admittance between the WPT output current and WPT input voltage, given by

$$G_{\text{WPT}} = \frac{I_{\text{AC,in}}}{V_{\text{AC(inv)}}} = \frac{k^2 Q^2}{k\left(\frac{1+k^2Q^2}{r^2-1} - \text{j}Q\right) R_{\text{rec}} - \text{j}\omega_{\text{s}} M \frac{(1+k^2Q^2) r^4}{(r^2-1)^2}}. \quad (50)$$

The dc–dc gain of voltage or current can be easily calculated by multiplying the gains of these stages together.

TABLE VI
ELECTRICAL CHARACTERISTICS OF POWER SWITCH MODELS

Model	$R_{\text{ds(on)}}$/mΩ	C_{oss}/pF	$V_{\text{ds(pk)}}$/V	$I_{\text{d(pk)}}$/A
1	80	20	40	4
2	16	100	100	60
3	7	250	100	120
4	100	40	650	30
5	25	126	650	120

*Models 1–5 are EPC8004, GS61004B, GS61008T, GS66504B, and GS66508B.

IV. PERFORMANCE OPTIMIZATION AND CASE STUDY

The design method introduced in the previous section offers full freedom in setting optimization objectives, as appropriate for various applications of the class Φ_2 converter topology. In this section, we present numerical case studies for wireless charging applications based on the discussion of different optimization goals, i.e., each *performance* objective in Table I. To this end, the range of possible designs is discussed in terms of *specifications*, *optimization parameters*, *performance* indices, and practical *constraints*, as characterized in Table I.

To illustrate the general applicability of the proposed method, the *specifications* covers the nominal load R_{Load} ranges from several Ohms to 1000 Ω and a nominal power ranges from 10 to 3000 W. Then, the design results are filtered following the practicalities discussed in Section II-D. As an example, one of five different power switch models is selected for each design point depending on the maximum voltage and current stress of the switch, as given in Table VI (voltage and current stresses are always assumed to be below 80% of the specified maximum rating of the switch).

Thus, we obtain curves showing the relationships between the given *specifications* (power and load), the *performance* objectives (efficiency, voltage stress, current stress, c_{p}), and the *optimization parameter* D (or α). Finally, the selection of optimization parameters D or α is discussed based on the required converter performance or overall system efficiency.

A. Converter Efficiency Optimization

1) For the Optimal Duty Cycle Operation: The power-related parameters at the input or output side include the voltage, current, resistance, and power. Depending on the application criteria, two power-related parameters are usually fixed, and the remaining parameters can be decided accordingly. Since the battery charging applications usually have specified power and

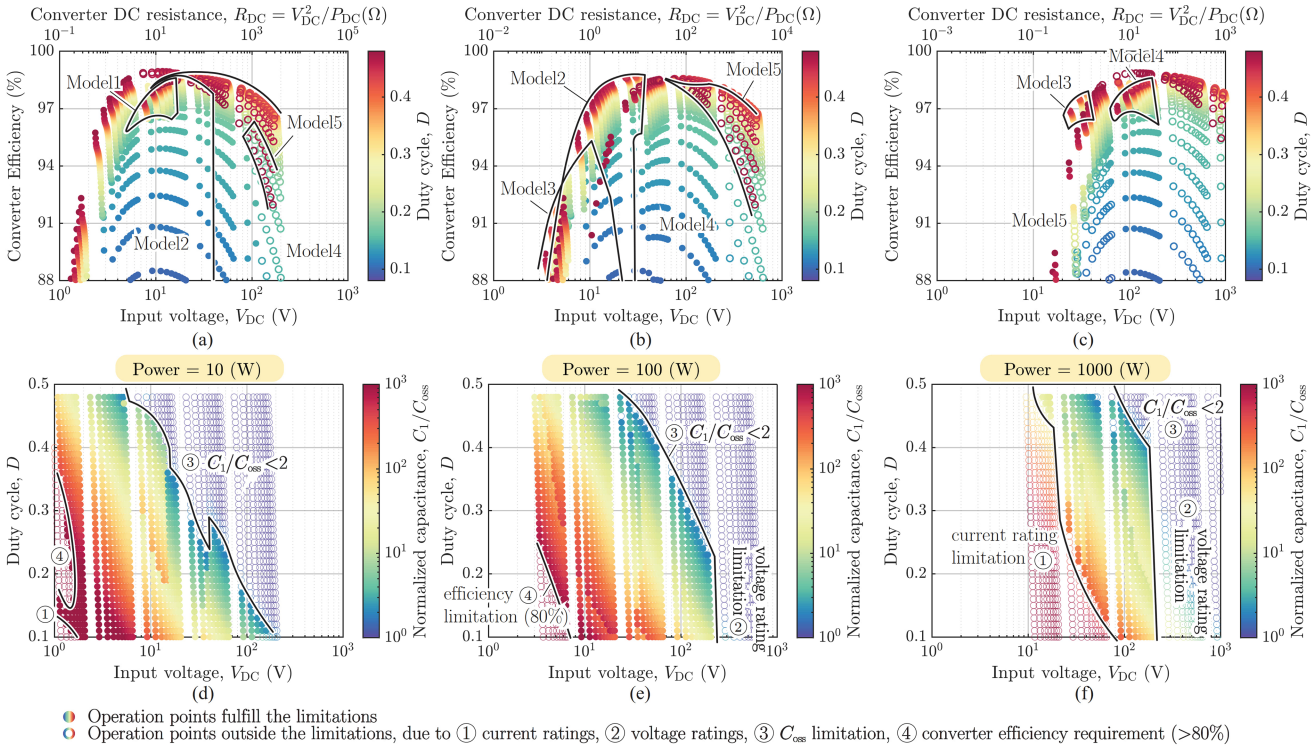

Fig. 11. Inverter efficiency with respect to the variation of duty cycle and DC-side parameters at (a) 10, (b) 100, (c) 1000 W. The black lines indicate the boundaries for design points with different power switch models (cf., Table VI). The valid range for duty cycle with respect to input voltage at (d) 10, (e) 100, (f) 1000 W.

charging current/voltage, converter efficiency can be optimized through selection of duty cycle D.

Fig. 11(a)–(c) show the inverter efficiencies with respect to duty cycles at 10 W, 100 W, and 1 kW load power. Each scatter point in Fig. 11 refers to a possible design point. Similarly to the comparison in Fig. 7, a design with a smaller D is prone to lower efficiency, since the resistive losses are higher due to high currents $I_{d(max)}$ and $i_{L1,2}$. The efficiency drop is especially significant when $D < 0.15$, which should be avoided if the design target has good efficiency. In contrast, much higher inductance is required for L_2 when D gets closer to 0.5, and losses on the corresponding parasitic resistance may also lower down the efficiency with a relatively low $i_{L1,2}$. Low efficiency at the left boundary of each figure is naturally caused by low values of R_{Load}, comparable with $R_{ds(on)}$, which should be avoided, as we discussed in Section II-A. It is noted from Fig. 11(a)–(c) that for any particular design with a predefined power and supply voltage (cf., one vertical line in the figure), we can always find an optimal D providing the highest converter efficiency.

However, the component selection and corresponding parasitics limit the viable range of design. For example, Fig. 11(d)–(f) show the duty cycle variation against the input voltage V_{DC} and the soft-switching capacitance C_1 (normalized to C_{oss}). All the possible designs are marked as filled scatter point in the figure. The invalid operating points (circles without filling color) are filtered out based on the constraints in Table I. Regions ① and ② are excluded based on the current and voltage ratings of the selected power switch. Regarding the limitation $C_1 > C_{oss}$, the boundary for Region ③ is set as 2 times of C_{oss}, due to the consideration of the nonlinearity of C_{oss} with respect to voltage stress. However, it would be better to select designs with C_1 several orders higher than C_{oss} in order to ensure robust operations independent of v_{ds} variation. Further, some designs may also have limitations for the lowest converter efficiency, considering 80% as an example, Region ④ would be then excluded.

Let us consider a design example of battery charging [27] with 100 W power and 28 V output. By comparing the designs at $V_{DC} = 30$ V in Fig. 11(b) and (e), the selection range of D narrows down from $(0, 0.5)$ to [0.1,0.46] after filtering the practically feasible design options according to the selected switch models. The upper boundary of D is usually limited by C_{oss} and voltage stress, whereas the lower boundary is set by the current stress and efficiency requirements. Similarly, with respect to any other given specifications, the viable range of duty cycle will also get reduced. For the designs requiring low power but high dc voltage [e.g., 10 W, 180 V cf., Fig. 11(d)], no duty cycle is valid for designs bound by all constraints.

2) For the Optimal Load Operation: In certain applications, the nominal load or supply voltages are restricted to given specifications; however, when the load or equivalent input resistance can be freely chosen, the converter efficiency will be further improved by optimizing the resistance. As an example, inverter designs starting from the input side are shown in Fig. 11(a)–(c). For each power level, the highest efficiency is reached at the optimal input voltage. As seen from Fig. 11(a)–(c), despite of the variation in power or voltage, the optimal dc resistance for the best efficiency always appears at around 10 Ω. Depending on the applications and the design flow, similar figures can also be plot to find the optimal ac resistance.

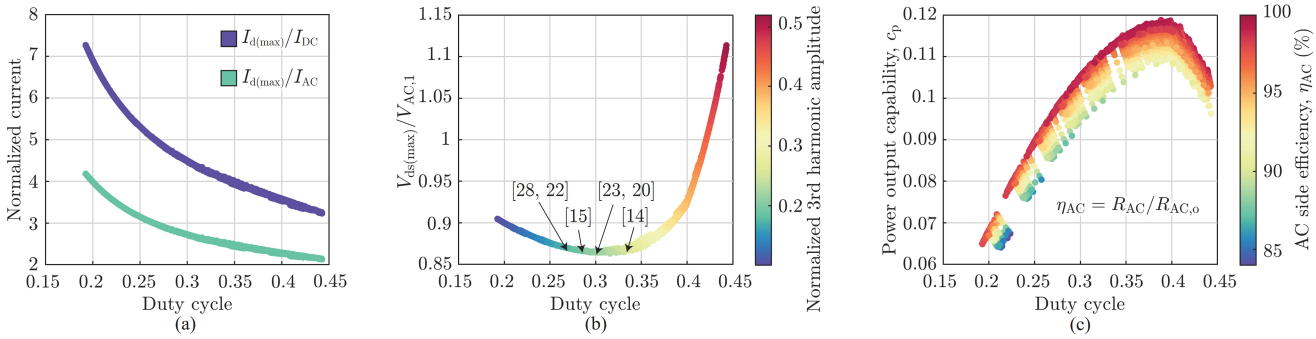

Fig. 12. System performance versus duty cycle. (a) Normalized current stress versus D. (b) Normalized voltage stress versus D. (c) Power output capability versus D. Contains 1.98×10^5 data points with power $P_{Load} \in [10, 3000]$ W and load resistance up to 1000 Ω.

B. Optimization for Low DC Current Ripple

During the circuit design, there is no restriction on the values of L_1 or L_2 because their parallel equivalence L_{eq} [cf., (2)] is used for parameter calculation. However, with respect to device performance, the inductance ratio $n_L = L_1/L_2$ affects the dc current ripple, EMI features, and converter efficiency. A low n_L value also brings the risk of negative i_{L1}, which should be carefully avoided. With the abovementioned considerations, the calculated efficiency always gets higher with higher n_L, but the rate of increase gets slower. Too high n_L also brings difficulty in realizing a large value L_1 and increases the converter volume. Therefore, as a rule of thumb, $n_L \geq 10$ provides a negligible ripple and reasonably high efficiency.

C. Optimization for Minimal Voltage Stress

Fig. 12(a) and (b) show the variation of the normalized current and voltage stresses on power switches with respect to D. The current stress normalized to the input or output current is independent of the rated power and nominal load, which only falls as D increases. On the other hand, the minimum voltage stress appears when $D = 0.3$. The curve remains flat within the range $D \in [0.2, 0.38]$, whereas the normalized voltage stress increases rapidly when D gets higher than 0.38 because of the increased third harmonic amplitude $V_{AC,3}/V_{AC,1}$. The class Φ_2 topology loses its advantage when $D > 0.45$, since the voltage stress becomes similar to that in a class E converter (almost 3.6 times of the input voltage [18]).

D. Optimization for Maximal Power Output Capability

The power output capability is defined as the output power normalized to the maximum voltage $V_{ds(max)}$ and current $I_{d(max)}$ rating of the switch. Due to the push–pull operation, the output power for each power switch is averaged as halved. Therefore, c_p after correction for parasitics is calculated as

$$c_p = \frac{P_{AC} \cdot \eta_{AC}}{2V_{ds(max)} I_{d(max)}} = \frac{R_{AC}}{2R_{AC,o}} \frac{V_{AC,1}}{V_{ds(max)}} \frac{I_{AC}}{I_{d(max)}} \tag{51}$$

revealing relations to both D and η_{AC}.

Fig. 12(c) shows the power output capability changes as a function of D for all the designs calculated for $P_{Load} \in [10, 3000]$ W. c_p reaches its peak value of 0.119 at $D = 0.39$, providing the highest utilization of power switches. The c_p-versus-D curve changes slightly with the resistance ratio $R_{AC,o}/R_{AC}$ because of the inductor parasitic losses. The operation point for design in [20] with fixed $\alpha = 0.26\pi$ (corresponding to $D = 0.31$), the designed working points for [14], [15], [22], [23], [28] are also marked in Fig. 12. Compared with a single operating point, the enlarged design range provides a more flexible optimization of system performance.

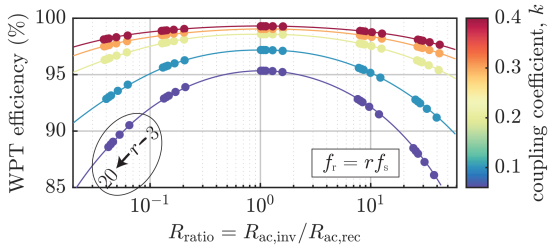

Fig. 13. WPT efficiency with respect to R_{ratio}, k, and $f_r = r f_s$ variation.

E. Optimization and Design Guidelines for the WPT Link

Next, in order to obtain the optimal system performance, optimization of the WPT link is considered. The parameters related to WPT link include the mutual inductance M, coupling coefficient k, and self-resonance frequency of the coils f_r. These parameters are related closely to the WPT efficiency, inverter equivalent load resistance R_{inv}, and parallel capacitance C_{inv}. Proper coil design can help to reduce the negative effects from parasitics [29], but Q and f_r still cannot be infinitely high. The ratio of ac resistance between the inverter side and rectifier side is defined as

$$R_{ratio} = \frac{R'_{inv}}{R_{rec}} \xrightarrow{Q\to\infty, r\to\infty} \left(\frac{\omega_s M}{Z_{rec}}\right)^2. \tag{52}$$

Therefore, the effects of the abovementioned parameters are analyzed for the ranges $k \in [0.1, 0.4]$, $f_r \in [3f_s, \infty]$, and $R_{ratio} \in [1/25, 25]$. Fig. 13 shows the WPT link efficiency curves with respect to the variations of k, f_r, and R_{ratio}. If we focus on the WPT link performance in Fig. 13, a design should always target the highest possible k to optimize the

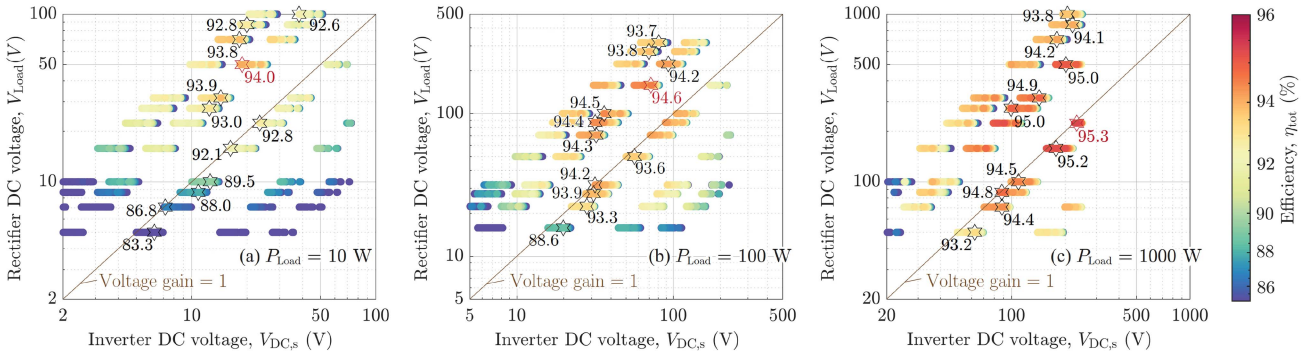

Fig. 14. System input and output DC voltages with respect to DC–DC efficiency at (a) 10, (b) 100, and (c) 1000 W load power.

η_{WPT}. However, the positive effect on η_{WPT} gets smaller as k is increasing. For example, $k = 0.2$ already provides more than 98.5% η_{WPT} compared with 99.3% when $k = 0.4$.

The coil self-resonance frequency is a critical concern for system efficiency and load-independent operations if it is not high enough compared with the switching frequency. A relatively low f_{r} (i.e., higher parasitic capacitance of the WPT coils) easily brings in a comparable capacitive load for the inverter and destroys the load-independent characteristics. However, the efficiency η_{WPT} can be compensated in low f_{r} cases by proper correction steps as proposed in Section III-C (cf., Fig. 9). The circle in Fig. 13 shows a group of datapoints with only r varied [3,20]. We find that with proper design correction, r does not directly affect η_{WPT}; instead, the WPT efficiency is affected by changes of R_{ratio}. From the numerical analysis, we find that self-resonance frequencies $f_{\mathrm{r}} > 10$ are good enough to make the parasitic capacitance small enough and keep as good efficiency as for the coils with higher f_{r}.

On the other hand, identical ac resistances on the inverter and rectifier sides (i.e., $R_{\mathrm{ratio}} = 1$) always provide the highest η_{WPT}, and the negative effect on η_{WPT} from low f_{r} is also minimized, as shown in Fig. 13.

F. System-Level Efficiency Optimization

After we discussed the efficiency for each power stage, the total system dc–dc efficiency η_{tot}, defined as

$$\eta_{\mathrm{tot}} = \eta_{\mathrm{Inv}} \cdot \eta_{\mathrm{WPT}} \cdot \eta_{\mathrm{Rect}} = \frac{P_{\mathrm{Load}}}{P_{\mathrm{supply}}} \tag{53}$$

can be optimized as depicted in Fig. 14. The optimization steps are explained by considering an example of a wireless battery charging application. We set the rated output power of 100 W and 28 V dc output voltage [27] as the design specifications.

1) Step 1. Rectifier Optimization: The rectifier efficiency can only be optimized by selection of D. Considering Fig. 11(b), we find that $D = 0.42$ gives the highest $\eta_{\mathrm{Rect}} = 98.6\%$. Therefore, the rectifier input power and equivalent resistance are obtained (i.e., 101.8 W and 25.6 Ω, respectively), which are later used as the input parameters for WPT link and inverter optimization.

2) Step 2. Optimization for WPT and Inverter Stages: According to Fig. 13, the highest WPT efficiency happens at $R_{\mathrm{ratio}} = 1$. However, the corresponding R'_{inv} might not be the optimal load for the highest η_{Inv}, and vice versa. Therefore, the WPT and inverter stages should be optimized together considering the system efficiency. Fig. 14 shows the η_{tot} of each design point with respect to the system input and output dc voltages. One global maximum point for η_{tot} can always be found for each power level if the dc voltages or mutual inductance is not specified; otherwise, based on any requirement on the voltage value or voltage gain, a local optimal D and R_{ratio} can be selected for the inverter and WPT link. For example, the star points in Fig. 14 reveal the local optimum designs at each specified V_{Load}, where we find that $D = 0.42$ and $R_{\mathrm{ratio}} = 1.29$ provide the highest possible system efficiency of 93.9% for the example design [27].

TABLE VII
PARAMETERS FOR EXPERIMENT

Inverter		Rectifier	
input voltage, $V_{\mathrm{DC,s}}$ (V)	30	power, P_{Load} (W)	100
duty cycle, D (%)	31.4	load, R_{Load} (Ω)	7.5
input inductor, L_1 (μH)	2.7	output inductor, L_3 (μH)	2.7
T-network L_2 (nH)	278	T-network L_4 (nH)	278
T-network $2C_2$ (pF)	992	T-network $2C_4$ (pF)	992
parallel CAP, C_1 (nF)	1.35	parallel CAP, C_3 (nF)	1.35

WPT link	Transmitter (Tx)		Receiver (Rx)	
self-inductance (μH)	L_{Tx}	4.56	L_{Rx}	4.52
self-resonance frequency (MHz)	$f_{\mathrm{r(Tx)}}$	23.5	$f_{\mathrm{r(Rx)}}$	23.8
compensation capacitance (pF)	C_{Tx}	112.4	C_{Rx}	113
Quality factor	Q_{Tx}	472	Q_{Rx}	530

V. Experimental Setup and Measurements

The experimental prototype is built to validate the proposed analysis and design methods. The system specifications are chosen following the WPT battery charging example [27], and one design is selected for experimental implementation among all the discussed design solutions in Section IV. As an example, we select the design case in Fig. 7 based on the considerations of system performance as well as difficulty for implementation, the set-up parameters are given in Table VII.

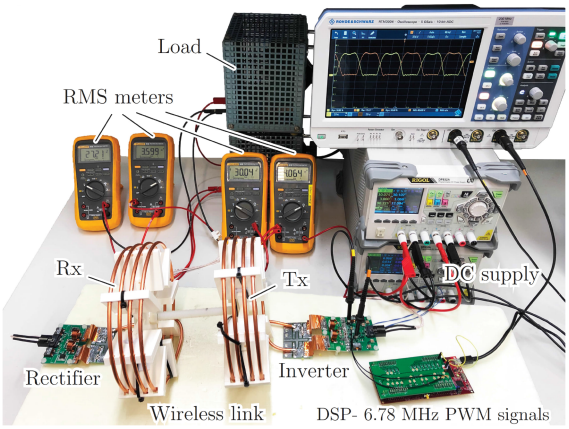

Fig. 15. Experimental setup for the WPT system.

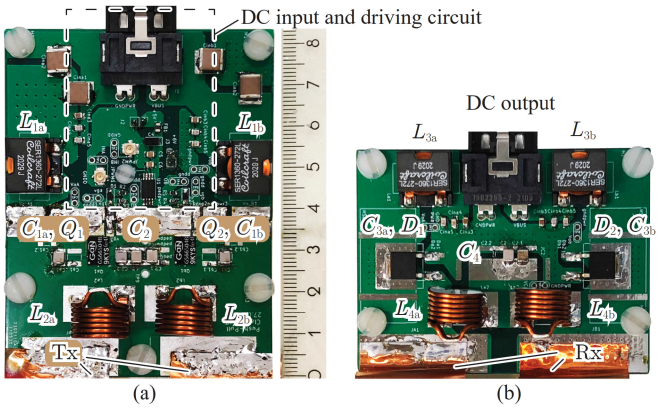

Fig. 16. Photographs of (a) inverter board and (b) rectifier board.

A. Experimental Setup

The experimental setup with a dc power supply, an inverter, a wireless link, a rectifier, and a resistive load is shown in Fig. 15. Control signals are generated by a digital signal processor *TMS320F28379*. All the waveforms are captured by the oscilloscope, and the input and output powers are measured with industrial grade true-rms meters (model *FLUKE 28-II*). The dc–dc efficiency η_{tot} can be calculated in terms of the input and output dc powers following (53).

Fig. 16 presents photographs of the inverter and rectifier boards. In total, two GS66504B GaN FETs from *GaN Systems* are used for the inverter, together with a dual channel gate driver ISL55110. On the rectifier board, the controllable switching components are replaced by two SiC Schottky diodes, C6D10065E, from *CREE*. Considering the skin effect at high frequencies, the transmitter and receiver coils are made with a copper pipe to ensure a good quality factor. The desired mutual inductance can be realized at the nominal transfer distance of 96 mm, which provides $k = 0.12$.

B. Experimental Results

As we know from the theoretical analysis (see Fig. 12), the power switches should have voltage stress around 2.1 times of the input voltage at $D = 0.31$. Fig. 17(a) presents drain–source

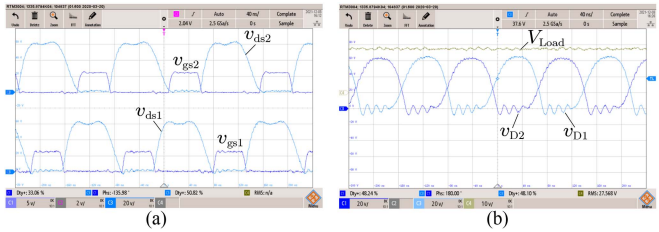

Fig. 17. (a) Inverter control signals and drain–source waveforms. (b) Rectifier voltage waveforms of power diodes and the load.

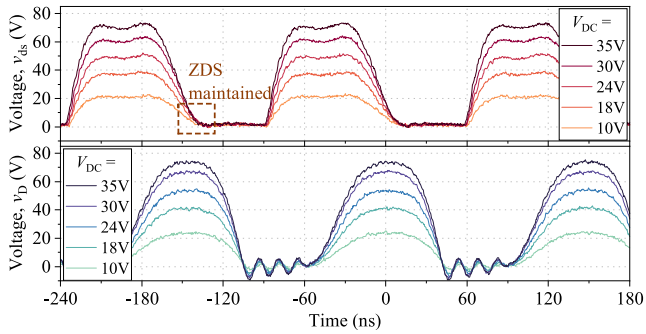

Fig. 18. Inverter drain–source voltage v_{ds} and rectifier diode voltage v_{D} waveforms against input voltage variations.

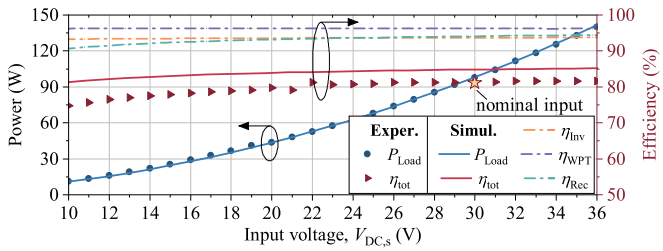

Fig. 19. System efficiency and output power against input voltage variations.

voltage waveforms of two switches in the inverter. Both switches show ZVS and ZDS switchings at the nominal load. Similarly, the rectifier diode voltages v_{D1} and v_{D2} and the output dc voltage V_{Load} are shown in Fig. 17(b). With zero v_{D} derivative at the beginning of turn-OFF period, the diodes have ZCS-OFF and ZVS-ON. The rectifier waveforms also verify an operation duty cycle of 0.31, as designed in Table VII.

Next, we verify that the change in the input dc voltage preserves the soft-switching conditions. Fig. 18 shows the measured v_{ds} and v_{D} waveforms for varying $V_{\text{DC,s}}$, variations of the input voltage do not affect the soft-switching performance, only the input and output powers change during this period, and ZDS is maintained regardless of the power level. Similarly, the voltage curves on both inverter and rectifier sides show the same trend with the variation of input voltage.

From Fig. 19, the input voltage variation hardly affects the inverter efficiency, since the inductive and output powers also change in the same manner together with the system power variation. On the other hand, an increase of the input voltage increases the efficiency of the rectifier mainly because the diode forward voltage drop becomes less dominant at higher powers.

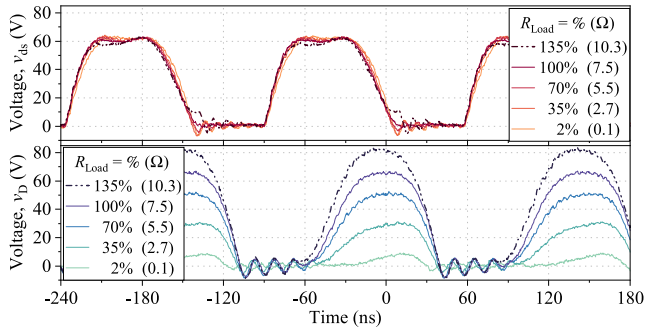

Fig. 20. Inverter drain–source voltage v_{ds} and rectifier diode voltage v_D waveforms against load variations.

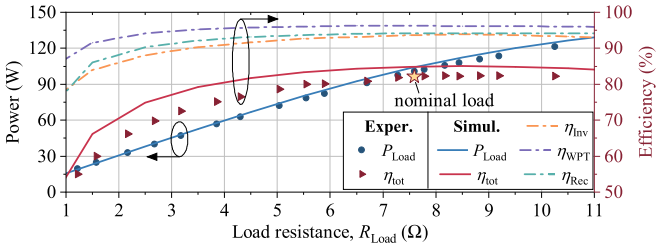

Fig. 21. System efficiency and output power against load variations.

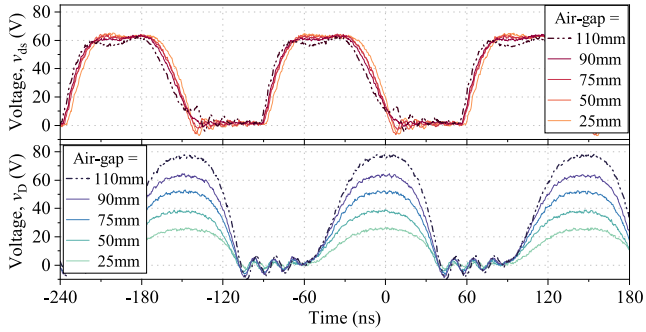

Fig. 22. Inverter drain–source voltage v_{ds} and rectifier diode voltage v_D waveforms against mutual inductance variations.

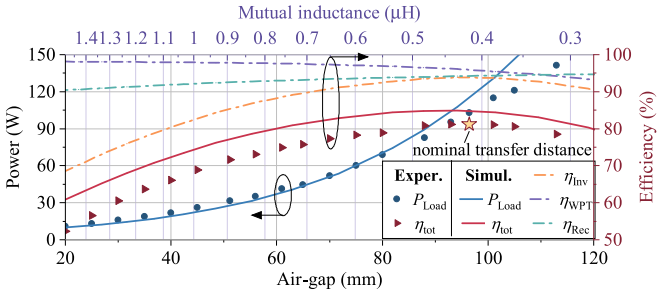

Fig. 23. System efficiency and output power against mutual inductance variations.

Therefore, the proposed design method guarantees higher efficiency with increasing supply voltage provided that all the components work within their rated powers, as shown in Fig. 19. At the nominal operation point, the WPT system shows measured dc–dc efficiency of 83% with the breakdown efficiency around 93% of each converter.

The v_{ds} and v_D waveforms changes against dc load variations are shown in Fig. 20. Within the range from the empty load to the full load, ZVS switching is always maintained in the inverter, as seen in v_{ds} waveforms. The inverter output voltage v_{ac} is almost constant during this variation, which results in a constant input current for the rectifier, according to Li and Mi[2]. The forward voltage drop of body diodes, high dv/dt rating at the switching moment, or lost ZVS, are three main reasons causing small ringing during the Q-ON period. Therefore, ZDS has great importance in eliminating this ringing by forcing the voltage and its derivative to exactly zero before switching. On the other hand, having a load value over 100% will destroy the ZVS; however, that is beyond the load variation range for the designed constant current output system.

With regard to the load variation, the output power and the dc–dc efficiency are given in Fig. 21. It can be noticed that reduction of the load resistance causes power reduction due to the current-source nature at the load. Meanwhile, inductive power becomes dominant as compared with the power delivered to the output load, same for the inductor parasitic losses, which results in the degradation of the system efficiency for light-load situations.

Considering the situations of varied transfer distance or misalignment in WPT systems, variations in the mutual inductance produce similar effects on the inverter as load variations. Due to the SS compensation topology, the mutual inductance greater than its nominal value is equivalent to an increased R_{inv}, resulting in power reduction and loss of ZDS in v_{ds} waveform. In contrast, on the rectifier side, relations (1) reveal a reduced input current with regard to higher M, as well as a reduction of the rectifier power and the diode voltage v_D.

However, the turn-ON period of the diode is not affected by variations of M. According to (26) and the decoupled relations of α versus D and R_{DC}/R_{AC} versus D in Table III, for any working rectifier with fixed L_{eq} value, turn-ON period of the diode D can be expressed as a function related to only R_{DC}. Therefore, v_D waveform always have fixed turn-ON cycle in Fig. 22, compared with the varied turn-ON period in Fig. 20 against load variation.

Similarly, an increase of the mutual inductance from its nominal value also reduces the system efficiency mainly due to reductions of converters efficiency, as seen in Fig. 23.

VI. Conclusion

This article presents a unified modeling and parameter design method for PPT class Φ_2 converters. The proposed analytical method expands the design possibilities to a full duty cycle selection range within (0,0.5), while both ZVS and ZDS soft-switching characteristics are always maintained during the design process. Universal numerical relations for parameter decoupling have been found from the design solutions of the unified analytical method, providing accurate and straightforward links between the circuit parameters and the optimization parameter D. These decoupled equations allow us to introduce a simplified

numerical design approach. Combined with correction steps for parasitic effects and an optimization step for good performance, the proposed numerical method allows accurate, fast, and robust designs of WPT systems with any given specifications. Furthermore, we also provide design guidelines for the selection of optimization parameters D and n_{L}, and system parameters $V_{\mathrm{DC,s}}$, R_{Load}, k, R_{ratio} based on the discussion of system performance indicators. The proposed design method allowed us to design example WPT systems demonstrating excellent performance at different duty cycles, revealing possibilities of reaching 95% system efficiency at kW power, over 98% converter efficiency, power output capability of 0.119 at $D = 0.39$, or low voltage stress around 2.1 times of the input voltage at $D = 0.3$. These performance indicators surpass the state-of-the-art results achieved with the use of existing design approaches. Apart from the application of WPT discussed in this article, the proposed parameter design approach and guidelines for converter optimization can also be used for other applications, such as an RF amplifier/rectifier.

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