Letters

Distributed Input Multiport MMC Based Power Converter for AC and DC Loads

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***Abstract*—A distributed input multiport topology is proposed in this letter based on the use of a modular multilevel converter (MMC). The distributed input modular multilevel converter (DIMMC) is based on the application of an MMC to multiphases systems, such as multiport generators or multiport transformers. The proposed converter is devised for high voltage and high-power applications with distributed inputs such as ship electric propulsion systems or industrial application available for both ac or dc loads. The main claims of the DIMMC are integration, modularity, scalability, and fault tolerance. This letter analyzes the steady state behavior of the converter, fault tolerance, and the advantages/disadvantage of its application.**

***Index Terms*—Aerospace electronics, aircraft propulsion, fault tolerance, multilevel converters, voltage-source converters.**

I. Introduction

HIGH voltage (HV) distribution, in the range of kV, is required in many applications to reduce conduction losses and system volume. Consequently, power converter topologies able to manage HV levels are required. Because of the voltage and current rating limitations of currently switch devices, multilevel topologies provide advantages.

Nowadays, the modular multilevel converter (MMC) topology is well-known as a suitable topology for medium/high-power applications with HV levels. It provides high quality output performance, high modularity, scalability, and low voltage rating switch devices. The MMC has become a popular solution in applications such as HV direct current (HV dc) transmissions lines and industrial variable-speed drivers, integration of low/medium voltage batteries to the grid, power electronic transformers, railway electric traction systems, and ship electric propulsion systems [1].

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Its modularity provides scalability and fault resilience [2], [3]. Not having a physical element connecting the positive and negative terminals reduces the probability of having a fault in the dc link, which may have severe consequences. Current state of the art is looking into improving fault management, volume reduction [4] and cooling size optimization [5].

Another approach reported in the literature for managing HV and high-power conversion, consists of using multiport generators or transformers to connect in series several ac/dc conversion units. In [6], a series-stacked ac–dc conversion architecture integrated with a multiport permanent magnet synchronous generator is proposed. To each of the multiple three-phase systems either an active or a passive rectifier is connected, and the series connection of their outputs form a HV dc bus. Similarly, in [7] and [8], a multiport transformer is used in an industrial application. In the case of [7], a modular converter formed by an H-bridge cells is presented. This uses a multiwinding transformer with several three-phase systems. This modular converter formed a HV ac output with a voltage level depending on the number of series connected H-bridge cells. Each cell is fed from one of the three-phase systems through a six-diode rectifier.

Based on the previous ideas, in the patent presented in [9], a distributed input modular multilevel converter (DIMMC) is presented. The proposed DIMMC topology explores the possibility of feeding the capacitor of each half-bridge cell of a MMC by an ac/dc rectifier with high power factor (PF) connected to one of the multiple three-phase systems (see Fig. 1).

II. DIMMC Topology

Fig. 1 shows a block diagram of the DIMMC topology with a proposal for one of its cells. This is a multiport topology based on an MMC with multiple three-phase systems, an HV dc port and an HV ac port. Each phase is comprised of two arms and each arm is comprised by several cells and an inductor connected in series. The cells proposed are based on a half-bridge and a capacitor, but they could potentially be exchanged for any other [10]. This letter will describe the operation for the half-bridge due to its simplicity. The half bridge capacitor (C_{cell}) voltage is regulated by one of the multiple three-phase systems through an active rectifier. The inherit isolation, provided at the input by the generator or a transformer, between the multiple three-phase systems eliminates the requirement of using isolated cells as in

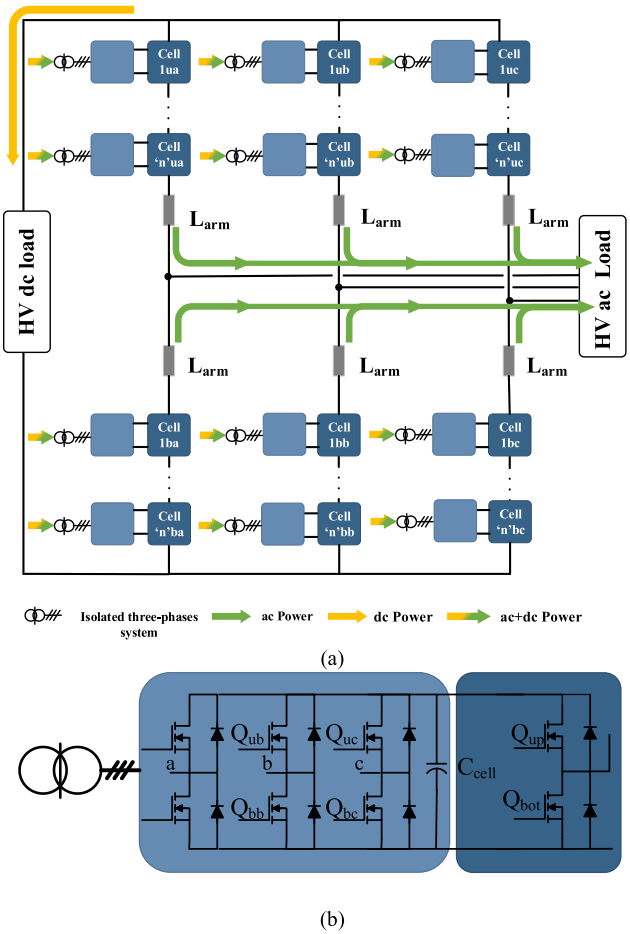

Fig. 1. DIMMC topology. (a) General topology scheme. (b) Details of the DIMMC cell structure.

the case of MMC based power electronics transformers [11]. The active rectifier can be implemented with any nonisolated topology, but in this case a simple two-level rectifier has been chosen for the sake of simplicity. This is controlled to drain ac power with unity PF and to maintain a constant C_{cell} voltage level [12].

Similar to the behavior of an MMC, the DIMMC is controlled to generate an unipolar arm voltage. The homopolar component of the upper and bottom arm voltage, v_{x1} and v_{x2}, respectively, determines the HV dc port voltage level (v_{dc}) as defined in

$$v_{x1} = \frac{v_{dc}}{2} - v_x \tag{1}$$

$$v_{x2} = \frac{v_{dc}}{2} + v_x \tag{2}$$

$$v_{dc} = v_{x1} + v_{x2} \tag{3}$$

where v_x is the phase output voltage, given by

$$v_x = \frac{v_{x1} - v_{x2}}{2}. \tag{4}$$

Fig. 2 illustrates a simplified scheme of the topology and the main voltage waveforms. Assuming both HV dc and HV ac ports are connected to loads, the power flow direction displayed in Fig. 1 is expected. However, this multiport topology could

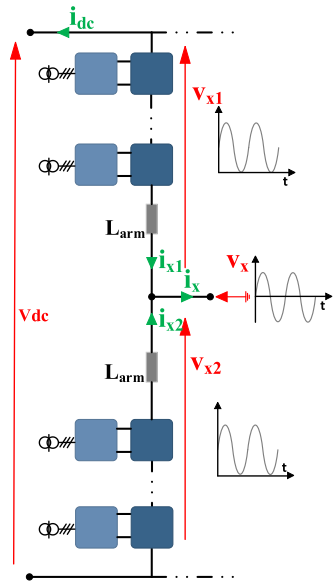

Fig. 2. Simplified representation of the main DIMMC signals. Only one phase represented for the sake of simplicity.

manage other power flow directions. As the cell voltages are fixed by the local control of the active rectifier, the DIMMC central control will be only responsible of guarantee the power balance equation

$$P_{ac} = V_a \cdot i_a + V_b \cdot i_b + V_c \cdot i_c \tag{5}$$

$$P_{dc} = V_{dc} \cdot i_{dc} \tag{6}$$

$$\sum_{n=1}^{N} P_{n,j} = P_{ac} + P_{dc} \tag{7}$$

where $P_{n,j}$ represents the active power provided by the cell n of the phase j, being N the total number of cells.

The arm inductors are designed with a similarly objective to the case of the traditional MMC, as they need to provide high frequency filtering and current limitation features.

The C_{cell} is designed in an MMC to hold its voltage over a minimum value when the cell is activated. This normally yield to a high capacitance value, which penalized the overall specific power of the converter. In the particular case of being used in variable-speed machine drivers, a challenge exists at low motor speed when the C_{cell} voltage ripple become significant higher [13]. In the proposed DIMMC, as the C_{cell} voltage is regulated by an active rectifier, a significant capacitance reduction for a similar voltage level fluctuation is achieved, as has been explored in [12]. Additionally, this suppresses the requirement of cell balancing techniques, such as a sorting method, which increases the number of commutations per cycle of the half-bridge and consequently the switching losses.

The main claims of this new topology are expounded in [9]. The DIMMC has been identified as a promising candidate to be used in ac to ac conversion systems with accessible HV dc bus, in which commonly two conversion stages are implemented, see Fig. 3. The DIMMC is proposed for system in which either

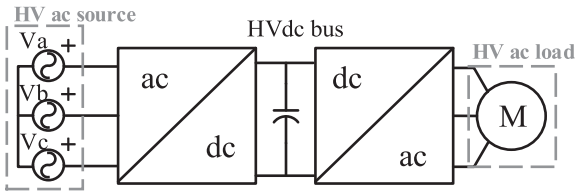

Fig. 3. Back-to-back ac to ac conversion scheme.

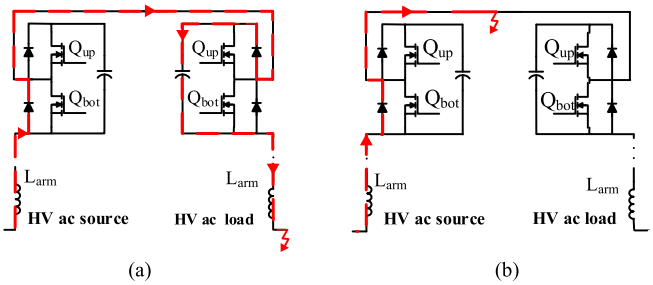

Fig. 4. MMC fault current paths. (a) ac side output short-circuit. (b) dc ports short circuits.

multiwinding generators [6] or multiport transformers [7] are available or part of the architecture.

The main advantage of the DIMMC over the back to back MMC is that in the DIMMC, one MMC stage can be eliminated, and the number of arms inductors and capacitors is halved. Duplication of switches is the price to pay for reducing the volume and weight of the topology as passive elements are the main drivers. This fact, in addition to the capacitance reduction presented previously and developed in [12] and particularized for the DIMMC result in the DIMMC being a more compact topology providing a higher specific power for applications related to transportation electrification under the aforementioned architecture conditions. Therefore, the DIMMC can be of high interest for high power electric mobility applications such as maritime or aerospace, where the weight reduction is one of the main targets when designing power converters [14].

III. Short-Circuit Fault Handling Capability

Another feature of the proposed DIMMC topology is its better short-circuit capability in comparison with the traditional MMC in a back-to-back configuration. Short-circuit capability has been evaluated based on the topology effectiveness in blocking the fault current when the modulation is disabled. No extra fault current control is considered. Two types of short-circuits are analyzed: ac side and dc side short-circuit.

In the situation of suffering a short-circuit at the HV ac load side, both topologies feature a similar performance. The path followed by the fault current from the source to the faulty point is illustrated in Figs. 4(a) and 5(a). After disabling the modulation, the fault current will naturally fade when the cell capacitor voltage is higher than the phase peak voltage and the freewheeling diode is reverse biased [15].

When a short circuit happen in the HV dc bus, the MMC converter that is connected to the HV ac source will further

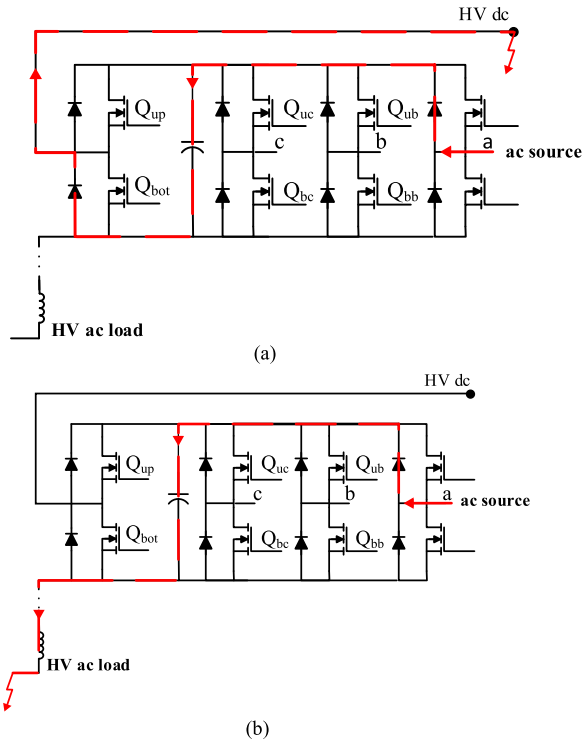

Fig. 5. DIMMC fault current paths. (a) dc side output short circuit. (b) ac ports short circuits.

contribute to the fault, the free-wheeling diodes of the switches will provide a path for the current from the HV ac source to contribute to the short-circuit current [16]. The expected current path is displayed in Fig. 4(b).

With the DIMMC, in case of having a fault in the HV dc port, after disabling the modulation the fault current will flow through C_{cell} until this is charged to the input phase peak voltage and the current is blocked by the freewheeling diode (similar to the case of the short-circuit at the HV ac load side). The current path in this case is illustrated in Fig. 5(b). Only the contribution of one of the ac phases is shown for simplicity.

Therefore, it can be concluded that in terms of short-circuit handling capability the DIMMC topology is superior to a conventional MMC.

IV. Simulation Results

To validate the steady state operation of the DIMMC and the short-circuit fault handling capability a model has been developed in MATLAB/Simulink.

A. Steady State Operation

The steady state operation of the new topology has been tested using a MATLAB/Simulink model. The model is run under the following specifications: seven cells per arm, dc cell voltage of 430 V, dc voltage of 3000 V, three-phase ac voltage peak of 1500 V, ac power of 1 MW, and dc power of 50 kW. These specifications have been chosen as matter of example of a feasible application for this topology.

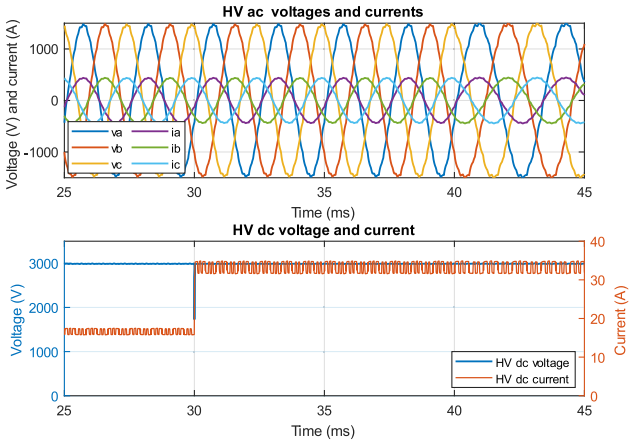

Fig. 6. Steady state output HV ac phase voltages and currents (upper) and steady state output HV dc voltage and current (bottom).

As can be seen in Fig. 6, the HV ac voltage and currents are similar to an equivalent MMC. Similarly, the arm currents will be formed by a dc current component, also known as circulating current, and an ac component equal to half the ac output phase current. If the system is balanced, the dc current through each phase will be 1/3 of the demanded current by the HV dc load. Fig. 6 also displays the HV dc voltage and current, both ac and dc loads are supply simultaneously. At 30 ms a HV dc load step is performed, HV ac output signals remain invariable. Additionally, at 40 ms the HV ac voltage frequency changes from 400 to 300 Hz, the HV dc port signals are not affected.

As has been mentioned in the list of claims in [8], the number of commutations of each cell per grid cycle is significantly lower in the DIMMC, as can be seen in Fig. 7. In Fig. 7(a), the insertion state of one cell is illustrated when a sorting algorithm is used for maintaining the cell voltages balanced in a conventional MMC [17]. The sorting algorithm measures the cell voltage and depending on the arm current direction it inserts first the cells with higher or lower voltage so at the end of the output ac voltage cycle the average voltage of every single cell is the same. Fig. 7(b) illustrates the insertion state of the same cell in the DIMMC. The switching losses at cell level are significantly reduced in the case of DIMMC because as can be seen by comparing Fig. 7(a) and (b), the number of state commutations is significantly reduced.

Additionally, in Fig. 7 is illustrated the main DIMMC feature analyzed in [12]. Thanks to the regulation of the cell voltage, the required capacitance at the cell can be significantly reduced, and therefore, the overall volume and weight of the converter. In the bottom figures of Fig. 7, the voltage level of one cell of a conventional MMC and the DIMMC are shown. In both cases, the converter is operating in steady state at the same operating point. But, in the case of the DIMMC the capacitance value of the cell capacitor is eight times lower. The MMC cell capacitance has been designed following [18], the resulted value is 1.3 mF (0.16 mF in the DIMMC). The maximum cell voltage variation is similar. However, Fig. 7(b) shows high dv/dt at both connection and disconnection of the cell. This might impact EMI compliance and the designer will need to trade energy storage reduction versus EMI performance. The origin of those spikes

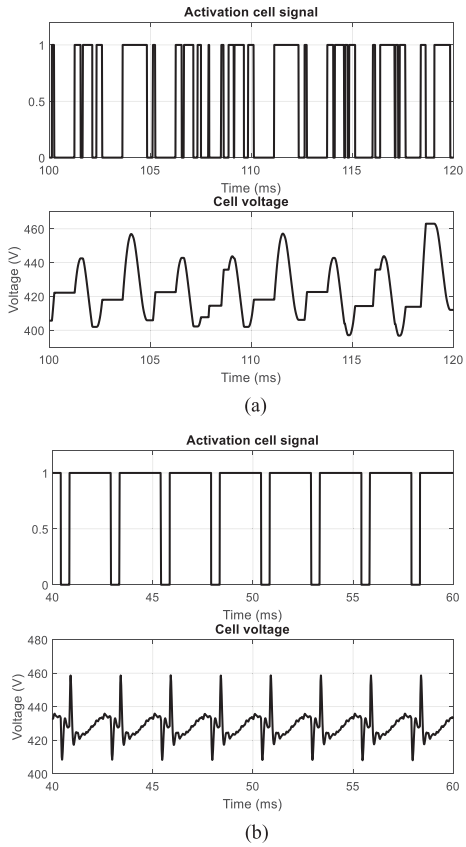

Fig. 7. Cell 1ua activation signal and C_{cell} voltage level. (a) MMC topology with sorting algorithm implemented for cell's voltage balancing. (b) DIMMC (sorting is not needed).

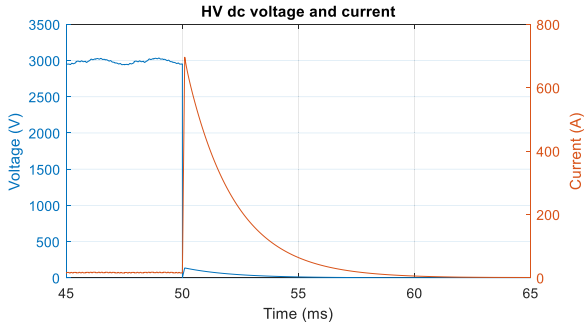

Fig. 8. HV dc port fault simulation. At t = 50 ms a short-circuit occurs and at t = 50.1 ms the modulation is disable.

is the control response of the active rectifier. As it was presented in [12], the control algorithm is a standard dual-loop control tuned for performing the fastest response with the minimum capacitance for a maximum voltage variation constraint.

B. Short-Circuit Fault Handling Capability

The short-circuit fault handling capability of the DIMMC has been tested by simulating a short-circuit at the HV dc port. Fig. 8 illustrates a short-circuit at t = 50 ms, it can be seen how the HV dc voltage decreases to zero. The modulation is disabled at t = 50.1 ms and the short-circuit current automatically disappears. HV side current and voltages are shown in Fig. 9. As

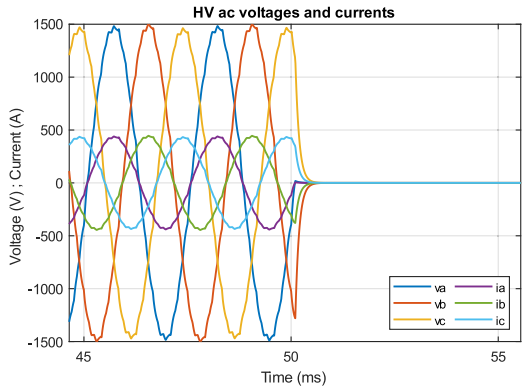

Fig. 9. HV ac output voltages and currents. At t = 50 ms a short-circuit occurs and at t = 50.1 ms the modulation is disable.

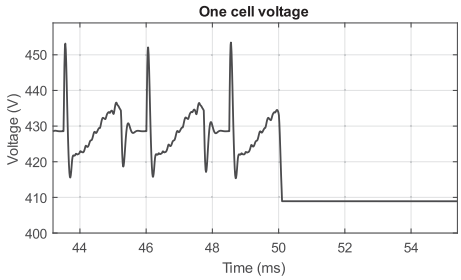

Fig. 10. C_{cell} voltage of one cell. At t = 50 ms a short-circuit occurs and at t = 50.1 ms the modulation is disable.

expected, the HV ac output turns zero when the modulation is disabled.

Additionally, Fig. 10 illustrates what happens at one of the C_{cell}. In normal operation, C_{cell} voltage is higher than the input phase peak voltage. Therefore, if the modulation is disabled the freewheeling diode is reversed bias. In Fig. 10, the voltage of the C_{cell} drops initially, this is because the fault occurs at t = 50 ms and the modulation is disabled at t = 50.1 ms. Once the rectifier switches are open, as the C_{cell} voltage remains higher than the input phase peak voltage the diode blocks the current and the voltage remains constant.

V. Conclusion

The DIMMMC topology presents modularity and scalability features Additionally, it provides cells capacitor volume and weight reduction and better short-circuit current handling capability. It has been shown, how with the DIMMC the cells capacitance value can be reduced eight times for a similar voltage fluctuation. Additionally, the no need of implementing a sorting method for balancing the voltage cells provides a significant reduction of the half bridge commutations and, therefore, switching losses. Furthermore, its better short-circuit handling capability with respect to a common MMC makes possible to fade the short circuit current caused by a HV dc port fault by opening all the switches.

Based on the presented analysis, the DIMMC seems promising for high voltage/high power applications, and in particular for the new challenges of transportation electrification. The DIMMC is a competitive solution in terms of weight/volume and efficiency for working at those voltage and power levels.

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