Integrated Fractional-Turn Planar Transformer for MHz and High-Current Applications

Kangping Wang, *Senior Member, IEEE*, Qingyuan Gao, Gaohao Wei, and Xu Yang, *Senior Member, IEEE*

***Abstract*—In megahertz and high-current applications, planar transformers face problems such as significant winding loss and limited winding current-carrying capacity, which seriously restrict the converter's efficiency and power density improvement. This article proposes a fractional-turn planar transformer structure and embeds key power devices into the transformer. The proposed method can significantly shorten the winding length, thus reducing winding losses. At the same time, the high integration of the transformer and key power devices can effectively reduce the overall volume of the converter and eliminate terminal losses. The analysis and optimization of the proposed integrated fractional-turn transformer are presented in detail. Finally, a 380 V–12 V 1-kW unregulated *LLC* is built with the proposed integrated transformer. The full-load efficiency is 97.7%, and the power density is 99 W/cm^3, both of which are the highest among the state-of-the-art prototypes with similar specifications.**

***Index Terms*—Fractional turn, gallium nitride (GaN), LLC, planar transformer.**

I. Introduction

With the continuous development of aerospace, information technology, electric vehicles, etc., higher requirements are placed on power converters in terms of efficiency, power density, and current capability. Taking the data center as an example, as a basic platform to support the development of new infrastructures such as artificial intelligence, cloud computing, 5G, etc., the electricity consumption of the data center will account for about 4.5% of the electricity consumption of the whole society in 2025 [1]. However, the power supply's efficiency from the power grid to the processor in the data center is only 85% at present [2]. Therefore, improving the power converter's efficiency is significant for saving energy and reducing carbon emissions. At the same time, with the development of data centers, the power consumption of a single rack is as high as 25 kW, about 2100 A@12 V, which poses a greater challenge to improve the power density and current capability of power converters.

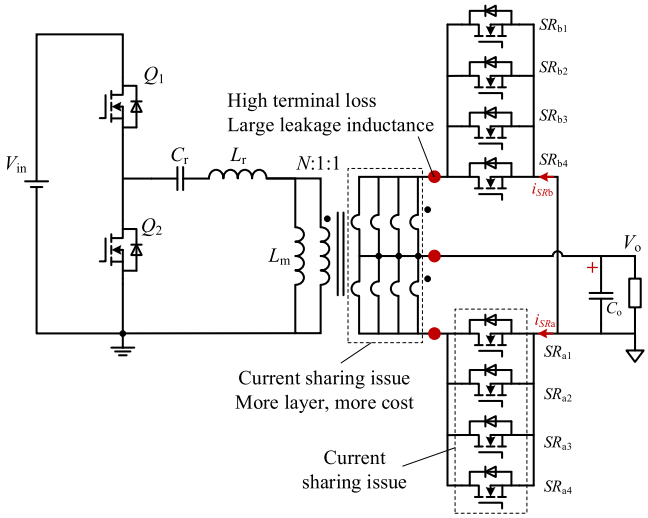

Fig. 1. *LLC* converter with high current output.

In recent years, with the application of wide-bandgap devices and soft-switching technology, the switching frequency has been continuously pushed up to the megahertz (MHz) frequency [3], [4]. At the MHz frequency, planar transformers based on printed circuit board (PCB) windings have been widely studied and applied due to their advantages of high power density, good consistency, and easy interleaving of windings, etc. However, it is very challenging to handle large currents efficiently at MHz frequencies. This is because eddy current effects (including proximity effect and skin effect) become more pronounced as frequency increases, resulting in higher winding resistance and losses. To reduce the eddy current effects, thinner conductors are required. At the same time, more windings need to be paralleled to handle high currents. Taking the *LLC* circuit shown in Fig. 1 as an example, there are the following problems under high frequency and high current [5]: 1) current sharing issues in parallel windings; 2) current sharing issues in parallel synchronous rectifiers (SRs); 3) large terminal loss; 4) large leakage inductance, etc. Therefore, it is not a high-efficiency way to directly parallelize multiple windings in high-frequency and high-current applications.

Matrix transformer has been extensively studied to solve the above problems. The windings and SRs can be dispersed around the core legs by adopting a multileg magnetic core structure to

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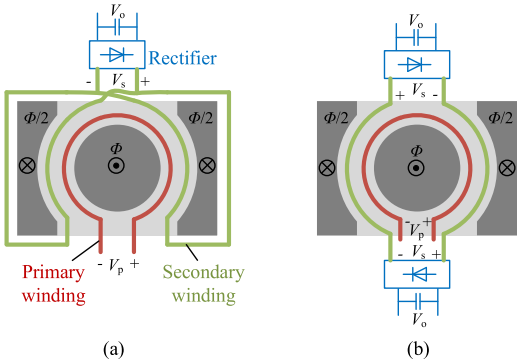


Fig. 2. Fractional-turn transformer. (a) Fractional-flux structure. (b) Fractional-winding structure.

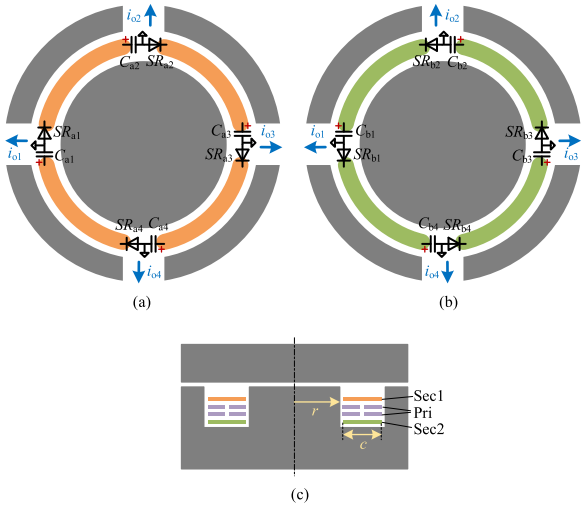


Fig. 3. Proposed integrated fractional-turn transformer structure with rectifiers and output capacitors. (a) Top side. (b) Bottom side. (c) Side view.

reduce PCB layers and terminal losses. Power converters based on MHz matrix planar transformers have been proven to have higher power density and efficiency than the traditional ways with direct parallel windings [6], [7], [8], [9]. However, the research works show that the winding loss of the planar matrix transformer is still dominant [8] and is not easy to reduce further.

Fractional-turn transformers have been proposed for a long time, and they have recently regained attention in high-frequency, high-current, and low-voltage applications. Fractional-turn transformers can be divided into two categories: 1) fractional-flux structure and 2) fractional-winding structure, as shown in Fig. 2. The magnetic core of the fractional-flux structure has multiple side legs, and the fractional turn is achieved by placing the secondary winding around the side post [10], as shown in Fig. 2(a). To further reduce the winding end loss and leakage inductance, the current of each secondary winding is first rectified and then connected in parallel on the dc side [11], [12]. However, the winding length of the fractional flux structure is not significantly shortened, so the reduction of winding loss is limited. The fractional-winding structure achieves the fractional turns by constructing fractional winding lengths. Taking Fig. 2(b) as an example, a whole turn of winding is divided into several segments, and the current in each segment can be equal through a symmetrical structure design. This structure is used for the first time in the application with a wide voltage range, and the equivalent transformer ratio can be changed by configuring the rectifier bridge [13]. Furthermore, 1-MHz *LLC* DCX is built based on the fractional-winding structure and achieves a full-load efficiency of 96.8% [14]. In [15], a 750-kHz, 600-W half-turn structure *LLC* DCX was developed where a Litz wire is used for the primary winding and PCB trace is used for the secondary winding. The full-load efficiency reaches 97.2% (the driving loss is not included). The fractional-turn transformers have great potential for winding loss reduction. However, there is still a gap between converters built with fractional-turn transformers and state-of-the-art converters in terms of efficiency and power density.

This article proposes a highly integrated fractional-turn planar transformer for MHz and high-current applications. The SRs and output capacitors are embedded in the transformer. The proposed transformer has a more compact structure and shorter winding length than the conventional fractional-turn schemes, so the power density and efficiency can be further improved. A 380 V–12 V/1 kW *LLC* DCX is built with the proposed integrated fractional-turn transformer. The experimental results show that the *LLC* DCX achieves a full-load efficiency of 97.7% and a power density of 99 W/cm^3, both of which are the highest among the state-of-the-art prototypes with similar specifications.

II. Proposed Integrated Fractional-Turn Transformer

A. Proposed Schemes and Basic Relationships

The proposed fractional-turn transformer structure is shown in Fig. 3, which integrates the SRs and output capacitors. A full turn of the winding around the central column is equally divided into N segments. Then N groups of SRs and output capacitors are symmetrically placed on the windings. For simplicity, the SRs are replaced by diodes in the figures. The output nodes V_o and GND are connected together outside the transformer. Here, a full-wave rectifier circuit is taken as an example, and the proposed methods are also applicable to full-bridge rectifier circuits and the like.

Fig. 4 shows the working processes of the proposed integrated transformer. In the positive half cycle, SR_{a1}–SR_{a4} are ON, and SR_{b1}–SR_{b4} are OFF. The output capacitors provide a low-impedance path for high-frequency winding currents. Through a symmetrical structure design, the high-frequency current in the secondary winding will flow around the center column. The path of the high-frequency current is the shortest, which can significantly reduce the winding loss and eliminate the terminal loss. For the negative half cycle, SR_{b1}–SR_{b4} are ON, and SR_{a1}–SR_{a4} are OFF. The working process is similar and will not be repeated here.

The voltage on each group of output capacitors is V_o. The voltage on each winding segment is clamped to V_o, which is equal in magnitude and opposite to the output capacitor voltage. So the output capacitors of the N groups are all grounded in

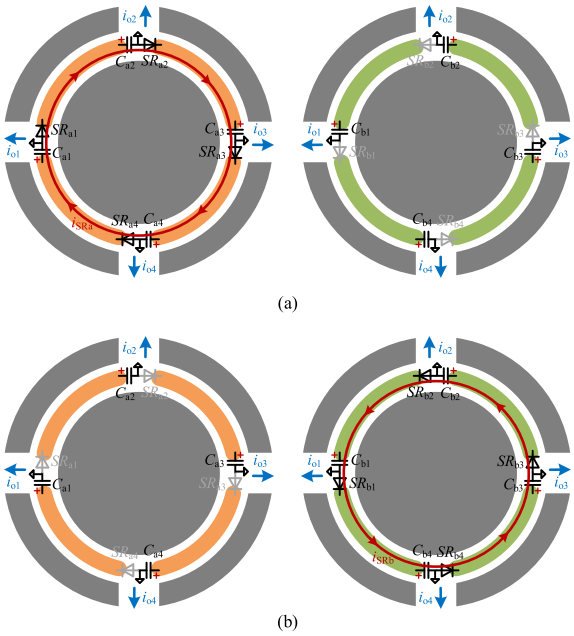


Fig. 4. Working processes. (a) Positive half-cycle. (b) Negative half-cycle.

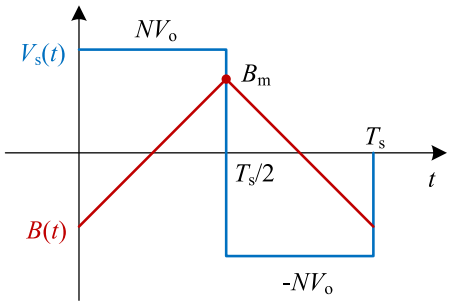


Fig. 5. Magnetic flux density $B(t)$ in the proposed fractional-turn transformer.

common. The voltage on one turn of the winding around the center column is NV_o, which is N times the output voltage V_o, so the equivalent turn of each segment winding is $1/N$.

When the SRs are turned ON, the voltage on one turn of the windings is clamped to NV_o. The magnetic flux density $B(t)$ in the core is shown in Fig. 5. According to Faraday's law, it can be deduced

$$A_e(N) = \frac{NV_oT_s}{4B_m}. \tag{1}$$

If B_m and T_s are kept unchanged, the effective core area A_e is proportional to N. Here, we consider the case where the center column of the magnetic core is circular. The effective core area $A_e = \pi r^2$, so

$$r(N) = \sqrt{\frac{A_e}{\pi}} = \sqrt{\frac{NV_oT_s}{4\pi B_m}} \tag{2}$$

where r is the radius of the central column. The length of each segment in secondary winding l_s is

$$l_s(N) = \frac{2\pi\left(r+\frac{c}{2}\right)}{N} = \left(\sqrt{\frac{\pi V_oT_s}{B_mN}} + \frac{\pi c}{N}\right) \tag{3}$$

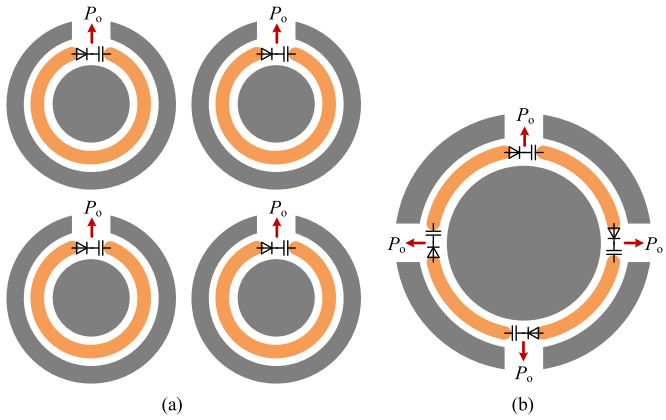


Fig. 6. Comparison of the full-turn transformer (where $N = 1$) and the fractional-turn transformer. (a) Full-turn transformers with an output power $4P_o$. (b) Fractional-turn transformer with an output power $4P_o$.

where c is the winding width. Here, we ignore the distance between windings and cores for simplicity. It can be seen from the above formula that the length of each secondary winding l_s decreases with the increase of N, which means that the resistance of each secondary winding can be reduced by increasing N.

The length of the primary winding is

$$l_p(N) = \frac{N_{p1}}{N}Nl_s(N) = N_{p1}l_s(N) \tag{4}$$

where N_{p1} is the turns of the primary winding when $N = 1$. Likewise, the resistance of the primary winding can be reduced in the same proportion by increasing N.

The volume of the core is

$$V_{Fe}(N) = 2AT_1 + 2A_eT_2 \tag{5}$$

where A and T_1 are the area and thickness of the top and bottom plates, respectively, and T_2 is the height of the central column, which is a fixed value. A and T_1 are calculated by

$$A = \pi(r+c)^2 + \pi r^2 \tag{6}$$

$$T_1 = \frac{A_e}{2\pi\left(r+\frac{c}{2}\right)} = \frac{r^2}{2r+c}. \tag{7}$$

N full-turn transformers are used as a reference for comparison. Fig. 6 shows an example with $N = 4$. The output power of each full-turn transformer is P_o, so the total output power of N full-turn transformers is NP_o, the winding loss is $NP_{Cu}(1)$, and the core loss is $NP_{Fe}(1)$. The full-turn transformer is a special case of a fractional-turn transformer, where $N = 1$. As for the fractional transformers with an output power of NP_o, the winding loss is $P_{Cu}(N)$, and the core loss is $P_{Fe}(N)$. The magnetic loss is proportional to the core volume because the maximum magnetic flux density B_m and the core loss per unit volume P_V are kept the same. The winding losses are proportional to the winding length because the current in the windings is the same and the winding resistance is proportional to the winding length

$$\frac{P_{Fe}(N)}{NP_{Fe}(1)} = \frac{P_vV_{Fe}(N)}{NP_vV_{Fe}(1)} = \frac{V_{Fe}(N)}{NV_{Fe}(1)} \tag{8}$$

$$\frac{P_{Cu}(N)}{NP_{Cu}(1)} = \frac{l_p(N)}{Nl_p(1)} = \frac{l_s(N)}{Nl_s(1)}. \tag{9}$$

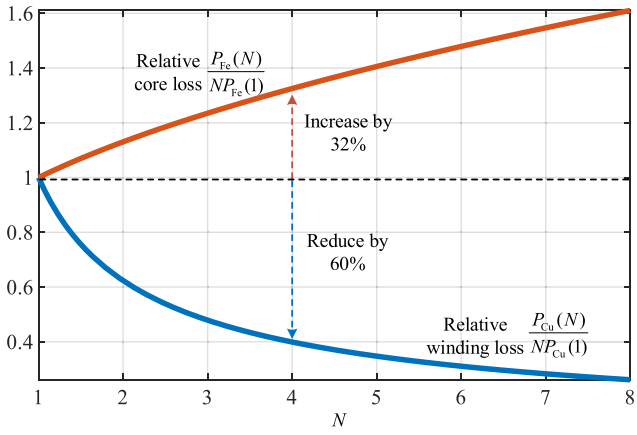


Fig. 7. Relative losses of the fractional-turn transformer to full-turn transformer with the same output power.

Fig. 7 shows the relative variation of fractional-turn transformer losses. It can be seen that the reduction of the winding loss is much greater than the increase of the core loss with the increase of N. The volt–second product is small in the case of low voltage and high frequency, so the loss of the magnetic core is relatively small. At high currents, the winding losses of planar transformers tend to be dominant and much higher than the core loss. Therefore, choosing an appropriate N by weighing the core loss and copper loss can reduce the total loss for applications with high frequency, high current, and low voltage output. In addition, the proposed scheme is highly integrated and is expected to increase the converter's power density further.

B. Equivalent Circuit Modeling

Fig. 8 shows the derivation of an equivalent circuit of the fractional-turn transformer. Here is an example of a one-fourth turn. We assume that the core and winding structures are perfectly symmetrical and ignore external reluctance. Fig. 8(a) shows the simplified core structure with primary and secondary current loops. Fig. 8(b) shows the magnetic circuit derived from Fig. 8(a). R_s is the reluctance of each side leg. R_c is the reluctance of the central leg. R_{lk} is the reluctance corresponding to the leakage inductance of the primary side. R_s and R_c can be expressed as

$$R_s \approx \frac{l_s}{\mu_r \mu_0 A_s} + \frac{l_g}{\mu_0 A_s} \tag{10}$$

$$R_c \approx \frac{l_c}{\mu_r \mu_0 A_c} + \frac{l_g}{\mu_0 A_c} \tag{11}$$

where l_g is the air gap length, l_s and l_c are the magnetic path length of the side column and the center column, respectively, A_s and A_c are the cross-sectional area of the side column and the central column, respectively (where $A_s = A_c/4$), and μ_r is the relative permeability of the core.

The number of turns on the primary side is N_p, so the magnetomotive force of the primary current is $N_p i_p$. The magnetomotive force of the secondary side is i_s. The total reluctance R_m can be obtained by combining the side leg reluctance R_s and the side

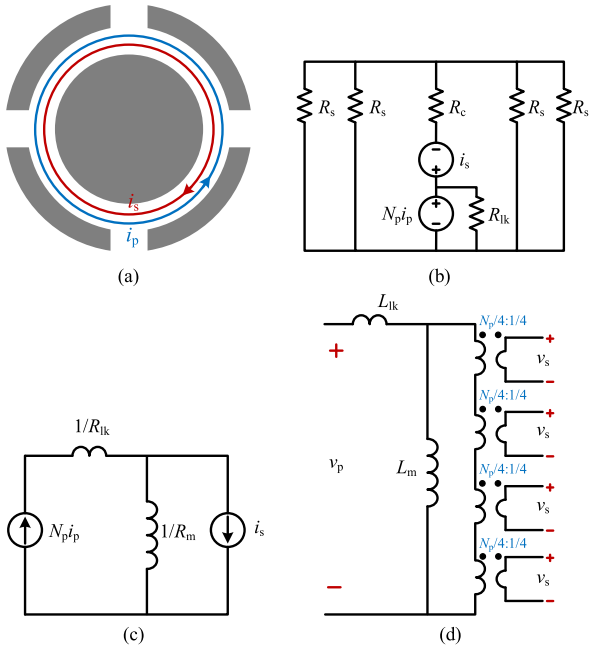


Fig. 8. Derivation of the equivalent circuit. (a) Simplified core structure with current loops. (b) Magnetic circuit. (c) Simplified equivalent circuit. (d) Equivalent circuit of the fractional-turn transformer.

leg reluctance R_c, namely

$$R_m = R_c + \frac{R_s}{4}\,. \tag{12}$$

Then, the magnetic circuit model is transformed into an electric circuit model, as shown in Fig. 8(c). Furthermore, the equivalent circuit of the fractional-turn transformer can be derived as shown in Fig. 8(d). The secondary current i_s is replaced with four ideal transformers considering that the secondary winding has four openings. The turns ratio of each transformer is N_p/4:1/4. The leakage inductance and magnetizing inductance are transformed to the primary side, so

$$L_{\mathrm{lk}} = \frac{N_p^2}{R_{\mathrm{lk}}} \tag{13}$$

$$L_m = \frac{N_p^2}{R_m}. \tag{14}$$

Finally, we can draw a complete *LLC* circuit with other circuit components, as shown in Fig. 9. The proposed fractional-turn transformer is highly integrated, including the transformer, SRs, and output capacitors.

III. Design and Optimization of the Proposed Integrated Transformer

A. Design and Optimization

A 380 V–12 V/1 kW, 1 MHz *LLC* DCX is designed and optimized with the proposed integrated transformer. The magnetic core material is DMR53 from DMEGC company, suitable for 1–3 MHz operating frequency. The primary and secondary windings of the proposed integrated transformer can be simplified into a ring shape, as shown in Fig. 10. Winding losses and core losses are simulated in 2-D Maxwell software. In Fig. 10, r

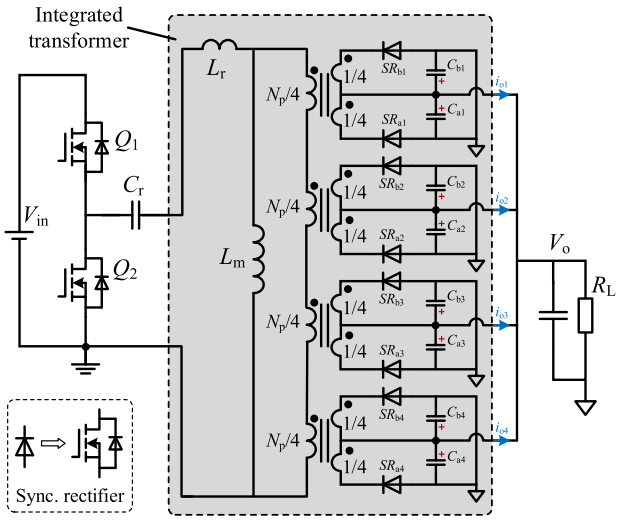


Fig. 9. Integrated fractional-turn transformers in *LLC* converters.

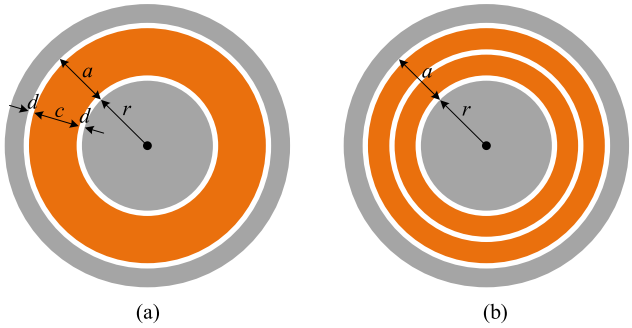


Fig. 10. Winding models. (a) Secondary winding. (b) Primary winding.

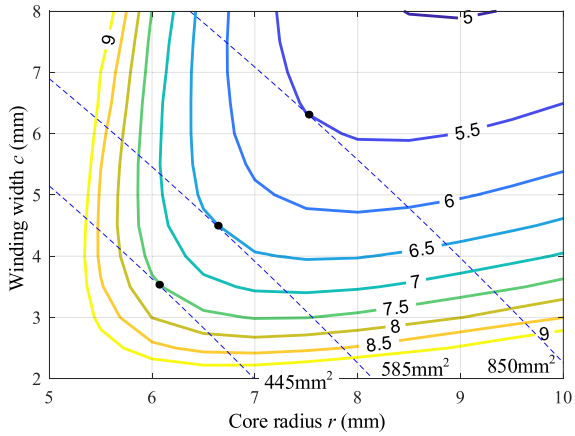


Fig. 11. Transformer loss versus core radius r and winding width c.

is the radius of the central core column, c is the width of the secondary winding, and d is the distance between the winding and the core. The edge distance between the center column and the side column of the magnetic core is $a = c + 2d$.

Fig. 11 plots the contours of the transformer losses as a function of core radius r and winding width c. The numbers

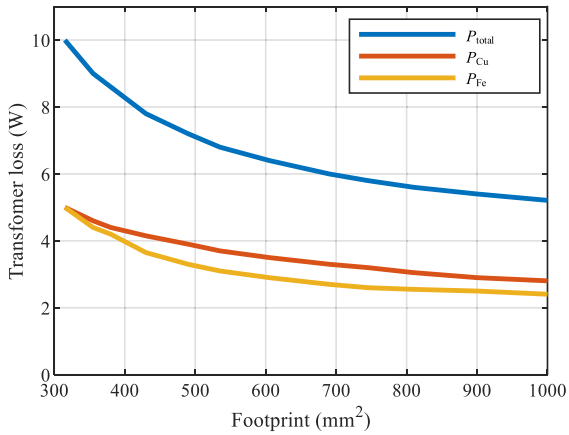


Fig. 12. Transformer loss versus footprint.

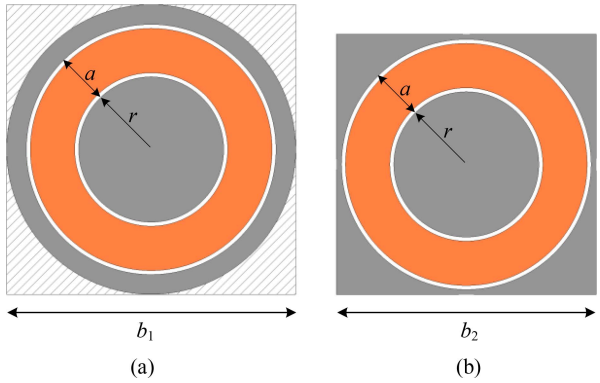


Fig. 13. Core shape optimization. (a) Circular shape. (b) Square shape.

shown on the curves are the transformer losses. The transformer footprint is also related to r and c

$$A = \pi(r + c + 2d)^2 + \pi r^2. \tag{15}$$

Furthermore, the footprint curve of the transformer can be plotted as a function of r and c, as shown by the dotted line in the figure. For given transformer losses, r and c should be chosen to minimize the transformer footprint. The tangent point between the loss curve and the footprint curve is the optimal point where the footprint is the smallest for a given transformer loss. Furthermore, we can find the tangent point under different transformer losses and the corresponding footprint. Finally, the curve of transformer loss with footprint can be drawn, as shown in Fig. 12. The final choice of the transformer footprint is 650 mm^2 as a tradeoff between transformer loss and footprint. The effective core area A_e is selected as 163 mm^2, and the resulting maximum magnetic flux density B_m is 74 mT.

B. Core Shape Optimization

Generally, the shape of the power modules is rectangular. With a circular magnetic core, it is difficult to fully use the corner area, which wastes some PCB area and reduces the converter's power density, as shown in Fig. 13(a). The magnetic

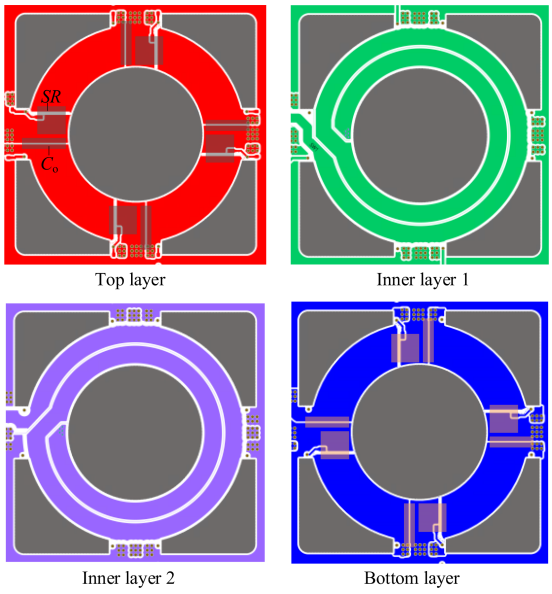


Fig. 14. Layout of the proposed fractional-turn transformer.

core shape is optimized into a rectangular shape to improve the area utilization, as shown in Fig. 13(b). The center leg of the core is optimized as a rectangle with rounded corners. The radius of the rounded corners is r, and the side length of the rectangle is b.

The two cores have the same effective area A_e and winding width c. The core areas of the outer leg and center leg are kept equal. Taking into account the four unused corners, the total footprint of the circular core is

$$A_{s1} = b_1^2 = 4\left((r+a)^2 + r^2\right). \tag{16}$$

For square cores, the total footprint is

$$A_{s2} = b_2^2 = \pi(r+a)^2 + \pi r^2. \tag{17}$$

Then, the area ratio of the two cores is

$$\frac{A_{s2}}{A_{s1}} = \frac{b_2^2}{b_1^2} = \frac{\pi}{4} = 78.5\%. \tag{18}$$

The footprint ratio is 78.5%, which means that square cores can save 22.5% of the board area.

IV. Design Considerations and Simulations

A. Winding Layout

Fig. 14 shows the layout of the proposed fractional-turn transformer windings. The PCB with four copper layers can be used. The top and bottom layers are the secondary windings, which are convenient to connect with the SRs and the output capacitors. The SRs and output capacitors are symmetrically distributed on the secondary winding. The inner two layers are the primary windings with four turns. The turns ratio of the fractional transformer is 4:1/4, which is equivalent to 16:1. It can be seen that the winding area is fully utilized. The overlapping area of the primary and secondary windings is also relatively small, which is only one-third of that of the matrix transformer

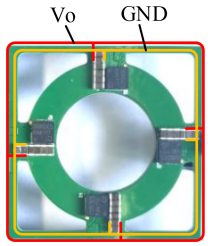


Fig. 15. Connection of the DC outputs.

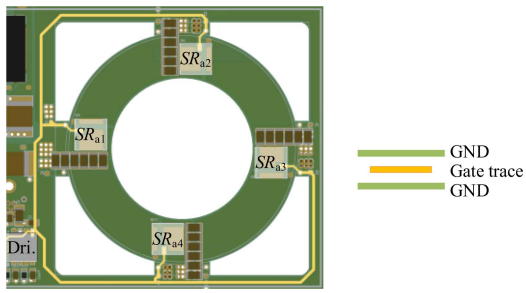


Fig. 16. Gate layout of SRs.

TABLE I
Gate Parasitic Inductance Extracted by Q3D Simulation

	SR_{a1}	SR_{a2}	SR_{a3}	SR_{a4}
L_G (nH)	5.4	13.3	13.8	8.9

[8] due to the reduced winding length and no corners. The parasitic capacitance is proportional to the winding area. That is, the parasitic capacitance between the primary and secondary windings is reduced in the same proportion, which is beneficial to reduce electromagnetic interference (EMI) noise.

Fig. 15 shows the connection of the dc outputs. The GND and V_o of all outputs are connected to the PCB outside the transformer. Since the outputs are direct currents, the inner and outer copper layers of the PCB can be directly connected in parallel.

B. Gate Layout of SRs

One driver is used to drive all SRs to simplify design and reduce cost. Because the SRs are distributed over the windings, minimizing gate inductance and using a symmetrical layout is critical. A sandwich layout structure is adopted, where the gate trace is buried between two ground layers. This sandwich structure can significantly reduce gate parasitic inductance. Fig. 16 shows the gate traces layout from the driver to the SRs. The gate parasitic inductance is extracted using the Q3D simulation, and the results are shown in Table I. Low-voltage Si MOSFETs are used as SRs, and their large input capacitance reduces the sensitivity of gate–source voltage to the gate parasitic inductances [16]. Circuit simulations were performed in LTspice, where the gate parasitic inductances and the coupling between them were considered. The maximum rise/fall time difference of V_{gs} among SRs is only 12 ns, accounting for 1.2% of one cycle with a 1-MHz

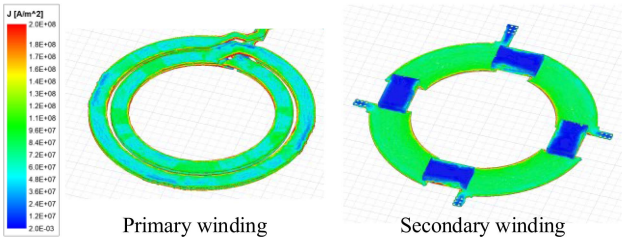


Fig. 17. Simulated current distribution in the windings.

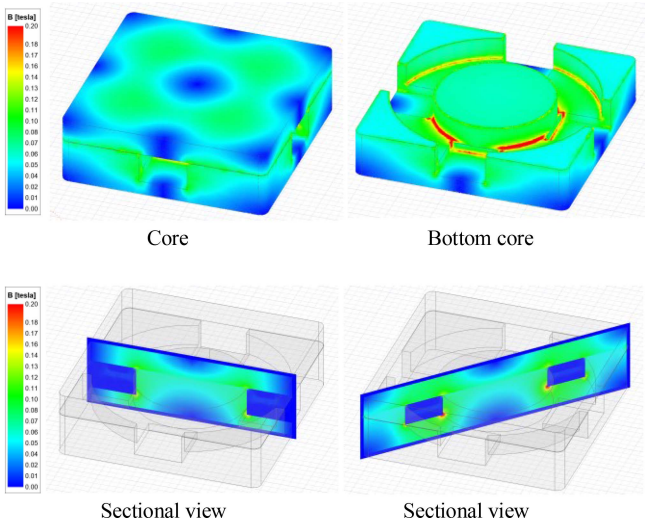


Fig. 18. Simulated flux density in the magnetic cores.

switching frequency. This has little effect on the control of the SRs.

C. Finite-Element Simulations

When the circuit works, the SRs on the same PCB side are turned ON at the same time. The secondary ac current forms a complete loop around the center column. Its working process is the same as that of the traditional full-turn transformer. The proposed transformer is simulated in 3-D Maxwell software. Fig. 17 shows the simulated current distribution in the windings. Fig. 18 shows the simulated flux density in the magnetic cores. The distribution of the winding current and the core flux density are well symmetrical. The air gap should be kept away from the PCB copper layer to reduce the effect of fringing flux on winding losses. The distance from the top plate core to the top PCB copper layer is set as 1.1 mm, which is about 16 times the air gap length.

Furthermore, a simulation is performed to prove that the secondary winding current will not flow through V_o and GND buses. Fig. 19(a) shows the simulation model. The secondary winding is divided into four segments. These segments are connected by a section of insulating material with high permittivity, which is used to simulate the output capacitors C_o. The V_o bus and GND traces are connected to the secondary windings near the output capacitors C_o. A current excitation of 1 A is applied to the

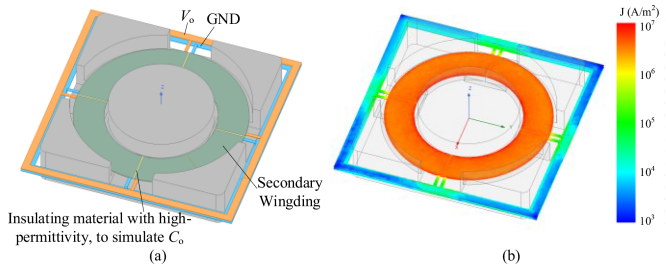


Fig. 19. (a) Simulation model. (b) Simulation results of induced current distribution.

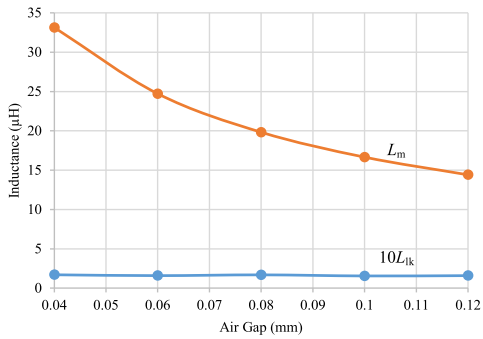


Fig. 20. Effect of the air gap on the magnetizing inductance and leakage inductance.

primary winding (for simplicity, only one turn). Fig. 19(b) shows the induced current distribution on the secondary winding, V_o, and GND traces. The current density on the secondary winding is much higher than the current density on the V_o and GND traces. The currents on V_o and GND traces account for 0.024% and 0.089% of the current on the secondary winding, respectively, which is very small and can be ignored.

Fig. 20 shows the simulation results for the effect of the air gap on the magnetizing inductance and leakage inductance. The magnetizing inductance decreases as the air gap increases. The change of air gap has little effect on primary leakage inductance.

V. Experimental Results

A 380 V–12 V/1 kW *LLC* DCX is built to verify the proposed integrated transformer. The switching frequency is 1 MHz. The switches on the primary side are GaN devices, and the SRs are Si MOSFETs. The PCB has six copper layers, and the copper thickness of each layer is 2 oz. Only four layers are used for windings, and the other two are reserved for EMI shielding. The circuit parameters are shown in Table II. The resonant inductance L_r is the primary leakage inductance with a value of 0.2 μH. The magnetizing inductance L_m is 25 μH. The deadtime T_d is 88 ns. The magnetic core material is DMR53 from DMEGC company, suitable for 1–3 MHz operating frequency. The primary winding turns are 4, and the equivalent turns of the secondary winding are 1/4.

Fig. 21 shows the *LLC* DCX prototype pictures. The size of the *LLC* DCX converter prototype is 29 mm $\times$ 41 mm, and the total thickness is 8.5 mm. The power density of the prototype

TABLE II
CIRCUIT PARAMETERS

Parameters	Types or values	Parameters	Types or values
V_{in}	380 V	Pri. devices	GS66508T
V_o	12 V	Sec. devices	IQE008N03LM5CG
f_s	1 MHz	Pri. driver	2EDF7275KXUMA1
P_o	1 kW	Sec. driver	2EDN7524GXTMA1
Controller	UCD3138RHAT	L_r	0.2 μH
C_r	127 nF	L_m	25 μH
C_o	C1608X5R1E106	T_d	88 ns

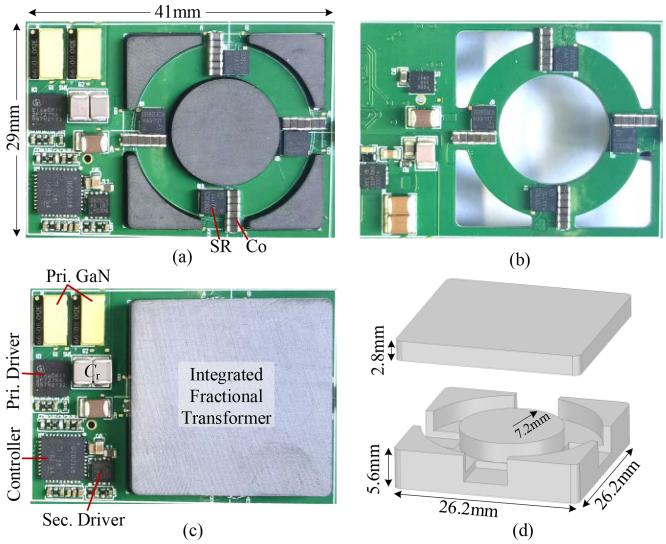


Fig. 21. Experimental prototype. (a) Top view with bottom core. (b) Bottom view without core. (c) Top view of the whole converter. (d) Magnetic core.

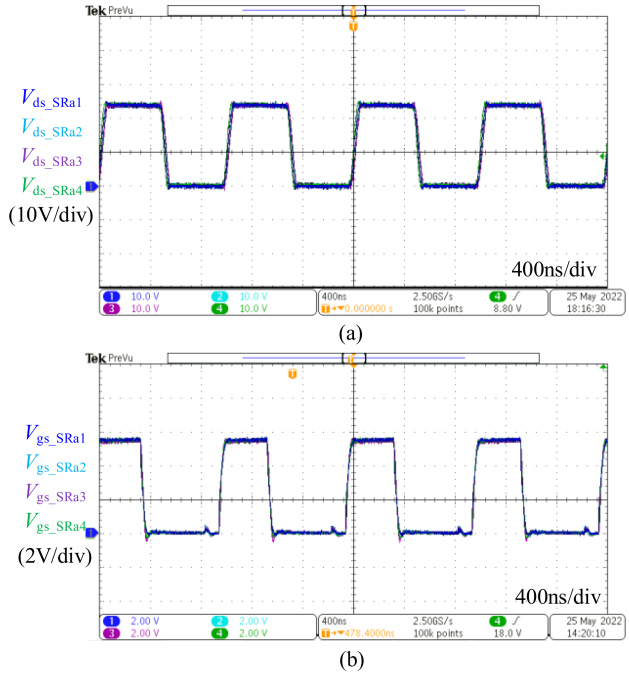


Fig. 22. Measured waveforms of SRs. (a) Drain-source waveforms. (b) Gate-source waveforms.

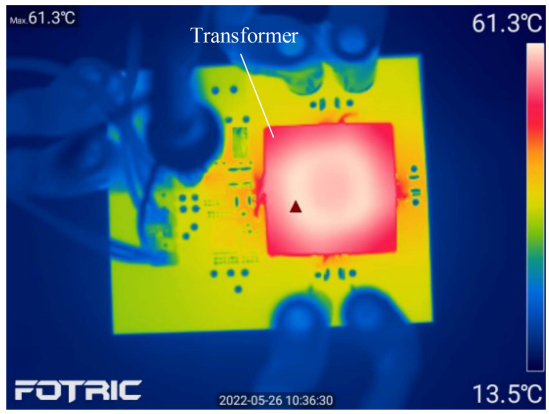


Fig. 23. Measured thermal image under natural convection conditions without fans.

is 99 W/cm^3, including the control and driver circuits. The SRs have a bottom thermal pad, and the heat is mainly dissipated out through the PCB. A thermally conductive material can be filled between the magnetic core and the SRs, and between the magnetic core and the PCB, so that part of the heat can be conducted out through the magnetic core.

Fig. 22 shows V_{gs} and V_{ds} waveforms of the four SRs on the top side. V_{gs} and V_{ds} are measured close to each SR. Both the waveforms V_{gs} and V_{ds} among SRs overlap very well, which shows that the symmetry of the SRs is good. The driving capability of a single driver chip is sufficient as the rising and falling edges of V_{gs} are fast. In addition, there is no overshoot in the gate voltage waveform, which shows that the gate parasitic inductance is acceptable with the optimized layout.

Furthermore, thermal distribution is measured to prove the transformer works well. Fig. 23 gives the thermal distribution under natural convection conditions without fans. All SRs are turned OFF, and the load current is set to 5 A. The main loss of the transformer is the core loss and the diode conduction loss of the SRs. The thermal image was measured at 2 min after loading, and the heat distribution tends to be stable. The thermal distribution of the transformer is very symmetrical, which shows that the symmetry of the transformer is good and the whole circuit works well.

Fig. 24 shows the measured key waveforms at the light and full load. The circuit works well under different loads. The V_{ds} waveforms of both the primary and secondary switches are very clean, and soft switching is fully realized.

Fig. 25 gives the measured efficiency. The output current is up to 85 A, and the output power is up to 1000 W. The peak efficiency is as high as 98.2% at 60% load, and the full-load efficiency reaches 97.8% for the power stage. With the control and driving loss, the peak efficiency is 97.93%, and the full-load efficiency is 97.7%.

Fig. 26 shows the thermal result under full load with forced air cooling. No heat sink was used in the experiment. The wind blows from the upper right corner to the lower left corner, and the wind speed is 3.3 m/s. The thermal image was taken in 2 min,

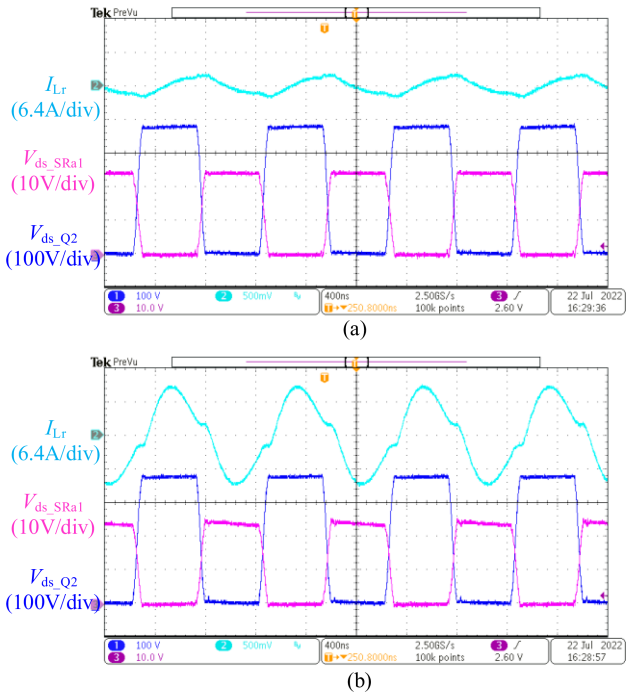


Fig. 24. Measured key waveforms. (a) Light load. (b) Full load.

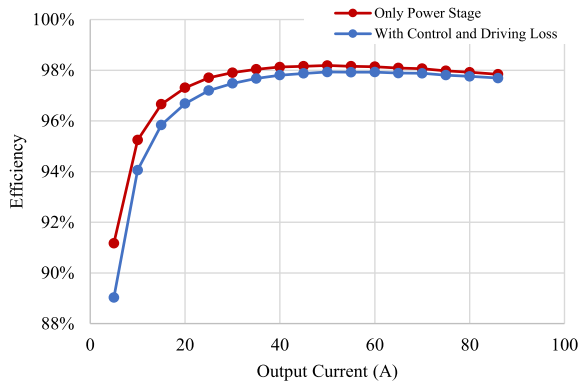


Fig. 25. Measured efficiency.

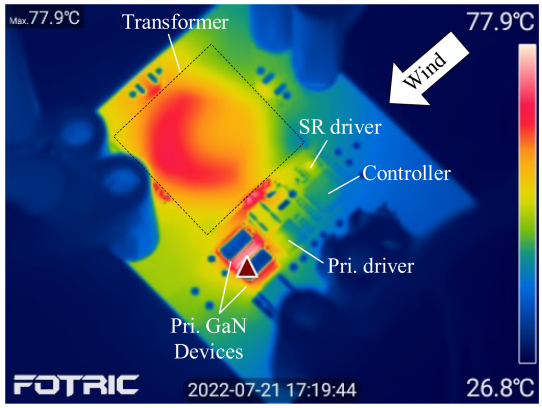


Fig. 26. Measured thermal image under full load with forced air cooling.

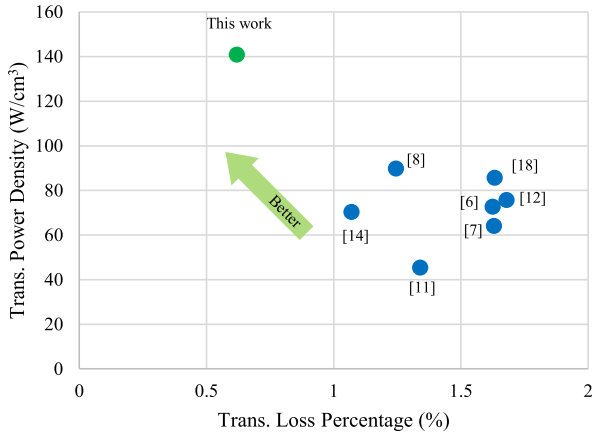


Fig. 27. Comparison of transformer loss and power density.

and the temperature rise of all components tended to be stable. The primary GaN devices' temperature is the highest, reaching 77.9 °C, and the temperature rise is 51.1 °C. If the module is potted and a heat sink is added, the heat dissipation of the devices in the module will be better. The maximum temperature can be further reduced.

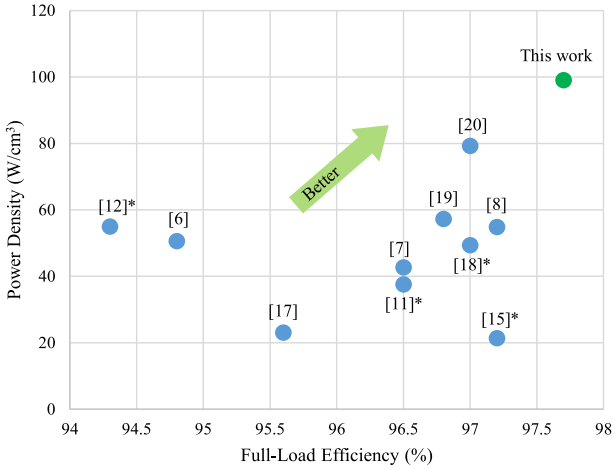
Table III compares various *LLC* DCX with similar specifications where the input voltage of about 380 V and the output voltage of 12 V. The losses and volumes of planar transformers are also compared. The transformer loss percentage is the ratio of the transformer loss to the output power, which can be used to compare the transformers with different power levels. The volumes of some transformers are not directly given and are estimated by referring to the size of the prototype. The SRs and output capacitors are included when estimating the transformer volumes. The transformer power density is the ratio of output power to transformer volume. The loss percentage of the traditional fractional-turn transformers is 1.07%–1.63% [11], [12], [14] while that of the proposed transformer is only 0.62%, which is reduced by 42%–62%. The power density of the traditional fractional-turn transformers is 39.5–72.7 W/cm^3 [11], [12], [14], [15], [17] while that of the proposed transformer is as high as 140.9 W/cm^3, which is increased by 94%–260%. Fig. 27 plots the loss percentage and power density for different transformers. It can be seen that the transformer designed in this article has the smallest loss percentage and the highest power density when compared with other transformer designs.

Fig. 28 compares the power density and efficiency among various 380 V–12 V *LLC* DCX with similar specifications. The *LLC* DCX built with the proposed transformer achieves a power density of 99 W/cm^3 and a full-load efficiency of 97.7%, both of which are currently the highest among the state-of-the-art prototypes. As for the peak efficiency, this work is only 0.1% lower than the best matrix transformer solution [19]. In [18] and [20], the higher peak efficiency is achieved mainly due to the use of lower figure of merit (FOM) switches and stacked-cells topology. Higher peak efficiency could be predicted if the method with low FOM switches and stacked-cells topology is combined with the proposed transformer scheme.

TABLE III
COMPARISON OF 380 V–12 V *LLC* DCX

Reference		[6]	[7]	[8]	[19]	[11]	[12]	[14]	[15]	[17]	[18]	[20]	This work
Key technologies		Matrix transformer				Fractional transformer					Topologies and switches		Fractional transformer
Input voltage V_{in}		390	380	380	400	380	380	380	380	380	380	380	380
Output voltage V_o		12	12	12	12	12	12	12	12	12	12	12	12
Output power (kW)		1	1	0.8	1	1	0.8	1	0.6	0.75	1.8	2	1
Switching frequency (MHz)		1	1	1	0.6	1	1	1	0.75	0.5	1	1	1
Transformer	Copper loss (W)	11.7	11.5	8.6	/	9.8	9.8	9.0	/	/	24.8	/	3.4
	Core loss (W)	5.1	4.8	1.4	/	3.6	3.2	1.7	/	/	4.6	/	2.8
	Total loss (W)	16.8	16.3	10.0	/	13.4	13.0	10.7	/	/	29.4	/	6.2
	Loss percentage (%)	1.68	1.63	1.25	/	1.34	1.63	1.07	/	/	1.63	/	0.62
	Volume (cm^3)	13.2	15.6	8.9	11.1	22.0	11.0	14.2	13.3	19.0	21.0	17.3	7.1
	Power density (W/cm^3)	75.8	64.1	89.9	90.1	45.5	72.7	70.4	45.1	39.5	85.7	115.6	140.9
Power density (W/cm^3)		50.6	42.7	54.9	57.3	37.6	55	/	21.4	23.1	49.4	79.3	99
Peak efficiency (%)		95.4	97	97.6	98.05	97*	96.5*	97.3	98*	97	98.3*	98.4	97.93
Full-load efficiency (%)		94.8	96.5	97.2	96.8	96.5*	94.3*	96.8	97.2*	95.6	97*	97	97.7

*Without control and driving losses.



*Without control and driving losses

Fig. 28. Comparison of 380 V–12 V *LLC* DCX.

VI. CONCLUSION

This article proposes a fractional-turn planar transformer structure with integrated key power devices for MHz and high-current applications. The proposed method can significantly shorten the length of the windings, thus reducing winding losses. Meanwhile, integrating the transformer and key power devices can effectively reduce the overall volume and eliminate terminal losses. The analysis and optimization are carried out in detail. Finally, a 380 V–12 V/1 kW *LLC* DCX was built with the proposed integrated transformer. The circuit works well under different loads. The measured full-load efficiency is 97.7%, and the power density is 99 W/cm^3, which is higher than the state-of-the-art prototypes with similar specifications. The peak efficiency reaches 97.93% with control and driving losses. The proposed method is suitable for high-frequency, high-current, and low-voltage output applications.

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