GaN-Based Isolated Resonant Converter as a Backup Power Supply in Automotive Subnets

Stefano Cabizza, *Student Member, IEEE*, Giorgio Spiazzi, *Member, IEEE*, and Luca Corradini, *Senior Member, IEEE*

***Abstract*—This article presents the analysis, design, and implementation of a 2 MHz, 12 V, 600 mA, GaN-based active-clamped isolated SEPIC converter (ACISC) supporting full zero-voltage switching (ZVS) throughout the 9–18 V automotive range, and intended to provide isolation and power interface between the 12 V battery and the low-power subnet. Designed for resonant discontinuous conduction mode (DCM) operation and leveraging the high switching frequency enabled by Gallium Nitride (GaN) devices, the selected topology leads to a reduction in total magnetic size and footprint, while maintaining a high efficiency profile. Both the theoretical models specifically developed for full ZVS resonant DCM operation, as well as the design and implementation of the transformer, are discussed. The analysis was verified through simulations and experimental measurements taken on a 7.2 W GaN-based prototype employing a planar transformer. Performance comparison with both a 7.2 W GaN-based active-clamped isolated flyback converter (ACIFC) and a commercial flyback converter is also included.**

***Index Terms*—Automotive power distribution, Gallium Nitride (GaN) devices, high-frequency operation, planar magnetics, resonant dc–dc converters, zero-voltage switching (ZVS).**

I. Introduction

IN THE automotive architecture shown in Fig. 1, a variety of low-power electronic loads, such as sensors, microcontrollers, and communication transceivers, are supplied by the 48 V main battery through an intermediate 12 V bus [2]. In case of failure of the latter, the system is sustained by a 12 V backup battery. The isolated converter interfacing the backup battery with the low-power 12 V intermediate bus must operate efficiently over the wide 9–18 V automotive input voltage range, while keeping magnetic size and overall footprint at a minimum. Presently adopted solutions at the industry level are based on the flyback topology with Silicon devices, a poorly efficient solution mostly justified by its low component count and reduced footprint. In this article, a 2 MHz GaN-based active-clamped isolated SEPIC converter (ACISC) [1], [3] is considered a viable substitute for the battery-connected application. In particular, the ACISC topology is here operated in resonant DCM operation to achieve soft rectifier diode turn OFF, i.e., with low di/dt, while ensuring full ZVS of the switches throughout the operating range. While the ACISC topology has been the subject of a number of studies [4], [5], [6], [7], [8], [9], [10], [11], along with similar topologies such as the active-clamped isolated flyback converter (ACIFC) [12], [13], [14], [15], and the asymmetrical half-bridge flyback converter (AHBFC) [16], [17], [18], [19], [20], [21], its design and operation in resonant DCM are still unexplored. For this reason, the contribution of this article is to provide a design methodology to operate the ACISC in resonant DCM while focusing on high-frequency low-power automotive applications. Although here it is considered a battery-connected scenario, the ACISC topology (e.g., operating in resonant DCM operation) can also be used to generate the isolated gate driver power supply for MOSFETs ($V_{out} \sim 15$ V).

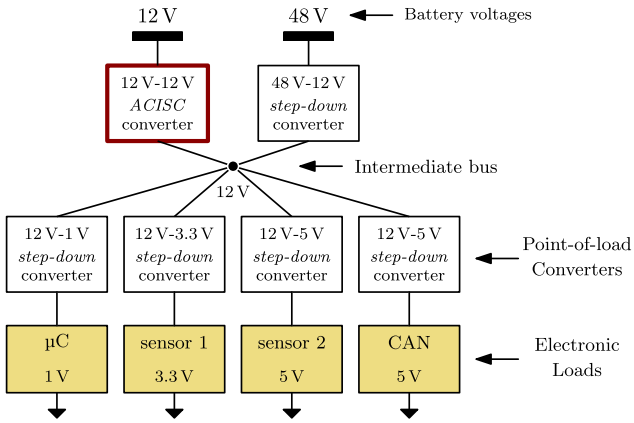


Fig. 1. Example of a dual-battery 48/12 V automotive scenario.

The rest of this article is organized as follows. Section II introduces the topology and its operation in resonant DCM while explaining the advantages of this operating mode. In Section III the analytical expression of the voltage gain M, necessary to develop the theoretical model of the converter, is derived. Section IV addresses the design methodology for the ACISC in order to guarantee full ZVS for both switches over the entire input

Manuscript received 5 August 2022; revised 3 November 2022 and 10 January 2023; accepted 30 January 2023. Date of publication 16 February 2023; date of current version 20 April 2023. The work of Stefano Cabizza was supported by Infineon Technologies Italia S.r.l. (IFX tutors Cristian Garbossa and Andrea Vecchiato) under Ph.D. scholarship. A patent application [1] focusing on the design methodology explained in this paper has been submitted to the U.S. Patent Office. Recommended for publication by Associate Editor Minjie Chen. *(Corresponding author: Stefano Cabizza.)*

Stefano Cabizza and Giorgio Spiazzi are with the Department of Information Engineering, University of Padova, 35131 Padova, Italy (e-mail: stefano.cabizza@phd.unipd.it; giorgio.spiazzi@dei.unipd.it).

Luca Corradini is with the Department of Electrical, Computer and Energy Engineering, University of Colorado Boulder, Boulder, CO 80309 USA (e-mail: luca.corradini@colorado.edu).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2023.3245561.

Digital Object Identifier 10.1109/TPEL.2023.3245561

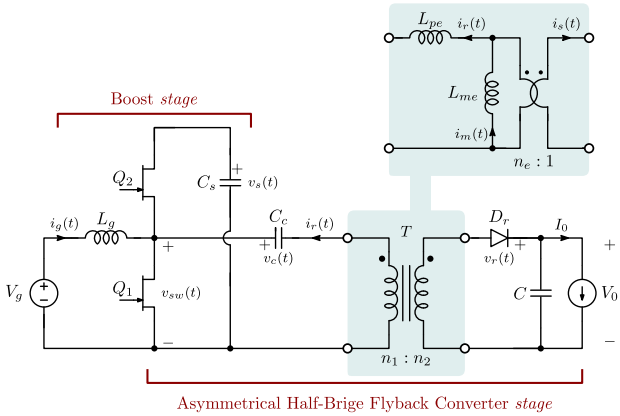


Fig. 2. Schematic of the GaN-based active-clamped isolated SEPIC converter, highlighting the adopted model for the high-frequency transformer T.

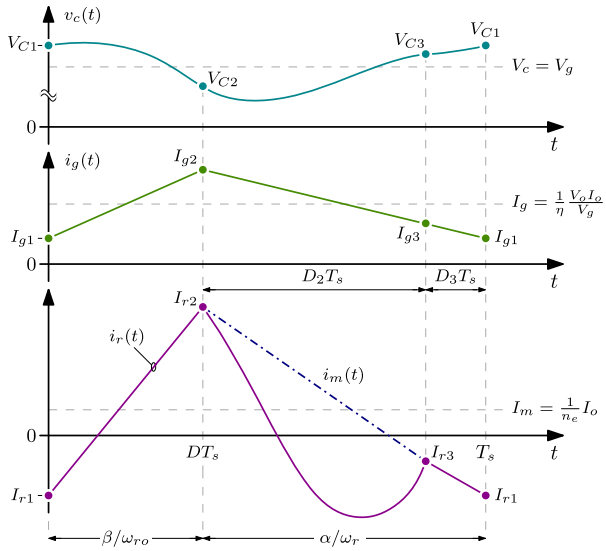


Fig. 3. Example of converter waveforms in resonant DCM operation over a switching period.

voltage variation, along with the design and implementation of the planar transformer. Section V introduces the ACIFC focusing on the differences between the two resonant topologies. Section VI reports the experimental measurements taken on the two 12 V, 600 mA GaN-based prototypes running at 2 MHz and a 400 kHz commercial flyback converter. In this section, both the efficiency profile of the converters and an analytical estimate of the main power losses are provided, together with a comparison in terms of conducted electromagnetic interference (EMI), devices' stresses, physical volume of main components, and thermal analysis as well. Finally, section VII concludes this article.

II. Resonant DCM Operation of the ACISC

The ACISC topology originates from the integration of a boost stage with an asymmetrical half-bridge flyback converter (AHBFC) [16], [17], [18], [19], [20], [21], sharing the same switches. Fig. 2 reports the schematic diagram of the ACISC employing two enhancement-mode GaN devices. Converter magnetics consist of input inductor L_g and a high-frequency transformer T. In the following, the latter will be modeled by an equivalent primary-side leakage inductance L_{pe}, an equivalent primary-side magnetizing inductance L_{me}, and an equivalent turns ratio n_e. Elements C_s, C_c, and C are the clamping capacitor, the resonant capacitor, and the output filter capacitor, respectively. In the following, small-ripple approximation is assumed for both the clamp and output capacitor, but not for the resonant one. The selected topology features galvanic isolation, low input current ripple, reduced voltage stresses, and full ZVS operation for both switches. Combined with the use of GaN technology, the above features make the ACISC an attractive topology for significantly increasing both the efficiency and the switching rate. Assuming steady-state operation and indicating average quantities with uppercase symbols, the following equations can be derived:

$$\underbrace{V_c = V_g,\ V_s = V_g/(1-D)}_{\text{inductors volt-second } balance},\quad \underbrace{I_r = 0,\ I_m = I_o/n_e}_{\text{capacitors charge } balance} \tag{1}$$

where D is the duty cycle of the low-side switch Q_1. Fig. 3 shows the main converter waveforms in one of the possible resonant DCM operations. Here, DCM is defined by the output diode D_r being OFF during a fraction of subinterval $(1-D)T_s$ (see interval D_3T_s in Fig. 3). The ACISC subtopologies which appear during the three different subintervals are shown in Fig. 4. The converter analysis, reported hereafter, makes use of the following parameters:

$$\lambda \triangleq \frac{L_{pe}}{L_{me}},\ Z_r \triangleq \sqrt{\frac{L_{pe}}{C_c}},\ \omega_r \triangleq \frac{1}{\sqrt{L_{pe}C_c}}$$
$$Z_{ro} \triangleq \sqrt{\frac{L_{pe}+L_{me}}{C_c}},\ \omega_{ro} \triangleq \frac{1}{\sqrt{(L_{pe}+L_{me})C_c}}. \tag{2}$$

With these preliminary definitions, operation of the converter in the various subintervals can be summarized as follows.

1) Interval $0 \le t \le DT_s$ [see Fig. 4(a)]
   At $t = 0$, the main switch Q_1 is turned ON, while diode D_r is already OFF. Thus, the two currents $i_r(t)$ and $i_m(t)$ increase, in a resonant manner, under the effect of the total voltage $v_c(t)$ applied to them. As can be seen in Fig. 3, the currents increase almost linearly since the condition $\omega_{ro}T_s \ll 2\pi$ is verified. At the same time, the input current $i_g(t)$ linearly increases with a slope equal to V_g/L_g.
2) Interval $DT_s \le t \le (D+D_2)T_s$ [see Fig. 4(b)].
   After the commutation of the two switches (turn-OFF of Q_1 followed by the turn-ON of Q_2), if the condition

$$\frac{V_s - v_c(DT_s)}{1+\lambda} > n_e V_o \tag{3}$$

   is verified, the output diode D_r is immediately turned ON, starting the energy transfer phase toward the output. The magnetizing current $i_m(t)$ decreases linearly, since the voltage across L_{me} is equal to $-n_eV_o$, while C_c and L_{pe} continue to resonate. In this subinterval, where Q_2

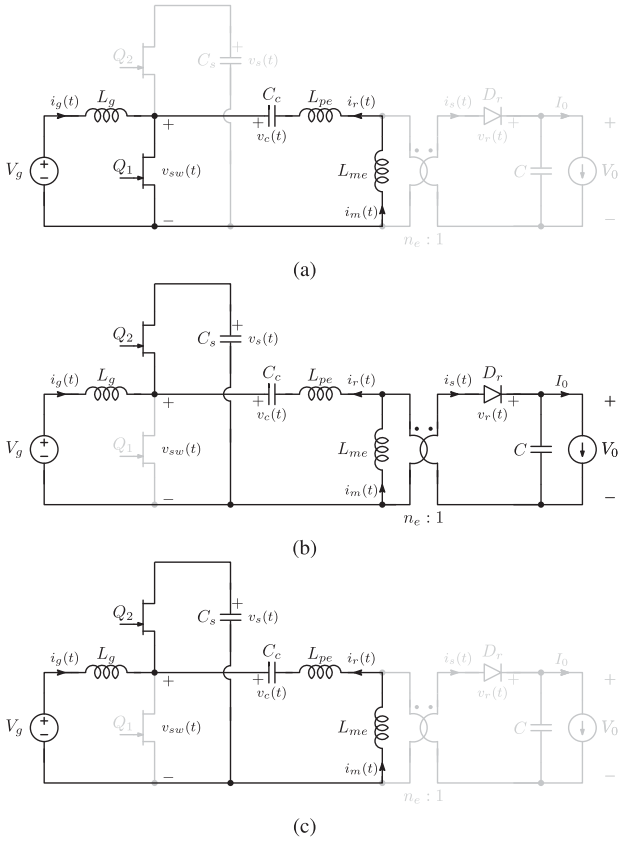


Fig. 4. Subtopologies in a switching period when the converter is operating in resonant DCM operation as depicted in Fig. 3. (a) During subinterval DT_s, (b) during subinterval D_2T_s, and (c) during subinterval D_3T_s.

is conducting, the input current decreases linearly with a slope equal to $(V_g - V_s)/L_g$.

In case (3) *is not* verified, a small subinterval appears, following time instant $t = DT_s$ [refer to Fig. 4(c)], in which voltage $v_c(t)$ would continue to decrease until the turn-ON of the rectifier diode. This situation represents another example of aresonant DCM operation which is likely to occur at light load.

3) Interval $(D + D_2)T_s \leq t \leq T_s$ [see Fig. 4(c)] At $t = (D + D_2)T_s$ the rectifier diode D_r turns-OFF, because the resonant current $i_r(t)$ becomes equal to the magnetizing current $i_m(t)$. This event initiates the last subinterval D_3T_s, during which both currents coincide, and continue to decrease in a resonant manner.

Under the already mentioned small-ripple approximation for the clamp and output capacitors, expressions of the resonant capacitor voltage $v_c(t)$ and of the resonant current $i_r(t)$ are

$$\begin{cases} v_c(t) = -Z_o I_{ri} \sin[\omega_o(t - t_i)] \\ \qquad + (V_{Ci} - V_x)\cos[\omega_o(t - t_i)] + V_x \\ i_r(t) = \dfrac{V_{Ci} - V_x}{Z_o} \sin[\omega_o(t - t_i)] \\ \qquad + I_{ri} \cos[\omega_o(t - t_i)] \end{cases} \tag{4}$$

TABLE I
COEFFICIENTS USED IN (4) FOR VOLTAGE AND CURRENT EQUATIONS IN RESONANT DCM OPERATION

Interval	V_x	Z_o	ω_o	subtopology	D_r
DT_s	0	Z_{ro}	ω_{ro}	Fig. 4a	OFF
D_2T_s	$V_s - n_e V_o$	Z_r	ω_r	Fig. 4b	ON
D_3T_s	V_s	Z_{ro}	ω_{ro}	Fig. 4c	OFF

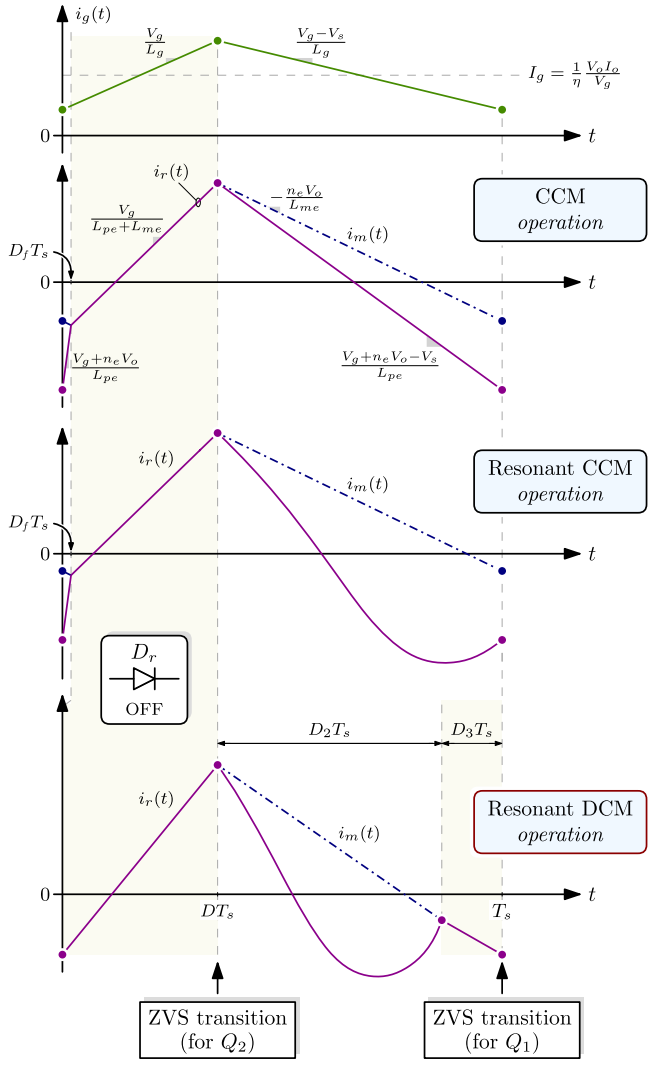


Fig. 5. Converter waveforms over a switching period when the ACISC is operated in CCM, resonant CCM, and resonant DCM operation.

with t_i $(i = 1, 2, 3)$ representing the beginning of each subinterval $(t_1 = 0)$. Expressions of V_x, Z_o, and ω_o, which depend on the considered subinterval, are reported in Table I.

Fig. 5 shows the trend of $i_g(t)$, $i_r(t)$, and $i_m(t)$ with their slopes when the ACISC is operated under three operating modes: continuous conduction mode (CCM), resonant CCM, and resonant DCM (highlighted areas mean that D_r is OFF). Looking at the first two operating modes, output diode D_r is ON either when Q_2 is ON (after $t = DT_s$) and until $i_r(t)$ equals $i_m(t)$ at $t = D_fT_s$. The reasons why the ACISC is here operated in

resonant DCM rather than CCM or resonant CCM operation are mentioned as follows.

1) As shown in Fig. 5, when the ACISC is operated in resonant DCM the output diode D_r is turned-OFF with low di/dt, avoiding steep turn-OFF fronts and, more importantly, additional resonances. The last aspect is crucial in this work because, as it will be proved later, the resonant current waveform $i_r(t)$ is already affected by resonances generated by making use of interleaved planar magnetics operated in the MHz range.
2) No need for a precise transformer leakage inductance value, since the resonant operation can always be ensured by adjusting the value of the resonant capacitor C_c. In other words, for a given value of L_{pe} it is always possible to operate the converter in resonant DCM by changing the value of C_c giving rise to subinterval D_3T_s. This is a big advantage because, in the realization of planar transformers, it is difficult to have a strong control over L_{pe} as it happens with L_{me}.
3) Considering the currents available at the switching node at the switching instant and looking at the ACISC resonant DCM waveforms shown in Fig. 5, the ZVS transition for Q_1 and Q_2 depends on both the input current $i_g(t)$ and the resonant current $i_r(t)$. The latter, which is equal to $i_m(t)$ during both transitions, can be easily estimated analytically at $t = DT_s$ and $t = T_s$ since an approximated triangular waveform can be assumed for $i_m(t)$. On the other hand, CCM and resonant CCM call for a precise estimation of L_{pe} to correctly estimate $i_r(T_s)$ since $i_r(T_s) \neq i_m(T_s)$. In addition, the estimation of $i_r(T_s)$ in resonant CCM is further complicated by its nonlinear behavior.

To achieve the aforementioned benefits given by the DCM operation, the ACISC must be operated in resonant mode. In fact, nonresonant operation forces the converter to always operate in CCM, even for very low output current values [4].

III. Voltage Gain Analysis

In this section, an approximate analysis is presented to relate the voltage gain M and the duty cycle D in resonant DCM operation. When the value of the resonant capacitance C_c is reduced to allow resonant operation, its voltage ripple is significant, and cannot be neglected for a correct analytical study of the converter. An approximated closed loop solution can be found for the particular operating point corresponding at the boundary between CCM and DCM operation, i.e., assuming subinterval $D_3T_s = 0$ (a similar approach was used in [21] for the AHBFC topology). We are going to demonstrate that the derived voltage gain formula yields values close to the simulated ones even when the converter enters DCM. The reason for such result will be explained in the following. Thus, considering the boundary CCM/DCM operating point, the flux balance on the magnetizing inductance L_{me} yields

$$V_{L_{me}} = \frac{1}{T_s}\int_0^{DT_s} \frac{v_c(t)}{1+\lambda}dt - n_eV_o(1-D) = 0. \tag{5}$$

By defining

$$V_y \triangleq \frac{1}{T_s}\int_0^{DT_s} v_c(t)dt. \tag{6}$$

Equation (5) can be rewritten as

$$V_o = \frac{1}{n_e(1+\lambda)}\frac{V_y}{1-D}. \tag{7}$$

The expression of V_y, from the first equation in (4), is given by

$$V_y = \frac{f_s}{\omega_{ro}}\left[V_{C1}\sin\beta - Z_{ro}I_{r1}(1-\cos\beta)\right] \tag{8}$$

with $\beta \triangleq \omega_{ro}DT_s$, as in Fig. 3. In order to evaluate V_y, suitable expressions for the initial conditions V_{C1}, V_{C2}, I_{r1}, I_{r2} (shown in Fig. 3) must be found. To this purpose, by exploiting the continuity property of the voltage $v_c(t)$, it is possible to find the required expressions

$$\begin{cases} V_{C1} = \sin\alpha\left[V_{C2}\cot\alpha - Z_rI_{r2} + (V_s - n_eV_o)\tan\frac{\alpha}{2}\right] \\ V_{C2} = \sin\beta\left[V_{C1}\cot\beta - Z_{ro}I_{r1}\right] \end{cases} \tag{9}$$

with $\alpha \triangleq \omega_r(1-D)T_s$. Then, by assuming an approximated triangular waveform for the magnetizing current $i_m(t)$, it is possible to express I_{r1} and I_{r2} as

$$I_{r2,1} \approx I_m \pm \frac{\Delta i_m}{2} = \frac{I_o}{n_e} \pm \frac{n_eV_o}{2f_sL_{me}}(1-D). \tag{10}$$

Substituting (10) and (9) into (8) yields

$$V_y = k_1\left(\frac{V_g}{1-D} - n_ek_2V_o + k_3\right) \tag{11}$$

where coefficients k_1, k_2, and k_3 are

$$k_1 \triangleq \frac{f_s}{\omega_{ro}}\frac{\sin\alpha\sin\beta}{1-\cos\alpha\cos\beta}\tan\frac{\alpha}{2} \tag{12}$$

$$k_2 \triangleq 1 + Z_r\frac{1-D}{2f_sL_{me}}(1-\gamma)\cot\frac{\alpha}{2} \tag{13}$$

$$k_3 \triangleq Z_r\frac{I_o}{n_e}(1+\gamma)\cot\frac{\alpha}{2} \tag{14}$$

and

$$\gamma \triangleq \sqrt{\frac{1+\lambda}{\lambda}}\cdot\cot\frac{\alpha}{2}\tan\frac{\beta}{2}. \tag{15}$$

Combining (11) with (7) yields the final expression of the voltage gain

$$M \triangleq \frac{V_o}{V_g} = \frac{k_1/[n_e(1-D)]}{(1-D)(1+\lambda) + k_1[k_2 + k_3/(n_eV_o)]}. \tag{16}$$

The above expression, which is the main result of this section, is extensively used in the design procedure described in Section IV. The plot of M as a function of D predicted by (16) is shown in Fig. 6, together with simulated and measured data points, that correspond to the design later disclosed in this article. As we can see, (16) fits reasonably well the resonant DCM behavior of the converter across the operating range of interest because the voltage across the magnetizing inductance L_{me}, during subinterval D_3T_s, is not much lower than the value

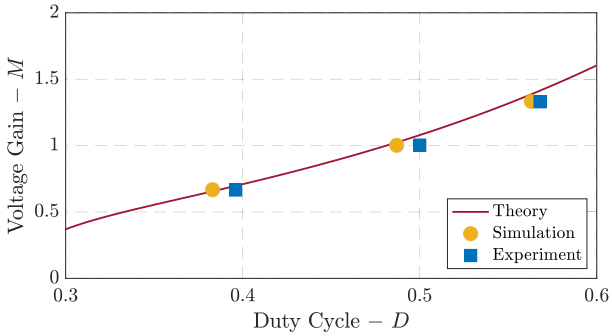


Fig. 6. Voltage gain comparison between theoretical model, simulation, and experimental measurements when $V_o = 12\,\text{V}$ and $I_o = 600\,\text{mA}$. Measured and simulated data points are taken for V_g equal to 9, 12, and 18 V.

TABLE II
CONVERTER SPECIFICATIONS

Parameter	Symbol	Value
Input voltage	V_g	9 V – 18 V
Nominal output voltage	V_o	12 V
Nominal output current	I_o	600 mA
Nominal output power	P_o	7.2 W
Switching frequency	f_s	2 MHz

$n_e V_o$ corresponding to the time interval in which diode D_r is conducting.

IV. Design Methodology for ZVS Resonant DCM Operation

The main specifications dictated by the considered application are reported in Table II. The specified switching frequency was selected to avoid disturbance in the AM band since the low EMI noise is a critical requirement for automotive power supplies. The 100 V, 1.7 A EPC2106 eGaN FET pair [22] is selected to implement the two switches. In this work, we want to turn Q_1 and Q_2 ON with ZVS at $t = T_s$ and $t = DT_s$, respectively, to keep the switching losses under an acceptable level. To guarantee ZVS, the net current

$$i_L(t) \triangleq i_g(t) + i_r(t) \tag{17}$$

injected into the switching node must have the correct polarity and value at each switching transition. As can be seen from Fig. 3, the ZVS turn-ON of Q_2 (at $t = DT_s$) is always guaranteed due to the highest positive value obtained either by $i_g(t)$ and $i_r(t)$, which brings the switching node voltage $v_{sw}(t)$ to the high-level in a few nanoseconds. On the other hand, the critical ZVS transition is the turn-ON of the low-side switch Q_1 at the end of the period, for which $i_L(t)$ must be sufficiently *negative*.

The proposed design procedure is the following. First, determine the amount of current required for the critical ZVS transition. A simple approach is to impose a design constraint on $i_L(t)$—assumed constant and equal to $i_L(T_s)$ during the dead time—in order to guarantee enough negative current for the complete ZVS transition of the switching node during the dead time itself, i.e.,

$$i_L(T_s) < -\frac{C_{eq,Q}}{t_D} V_s \tag{18}$$

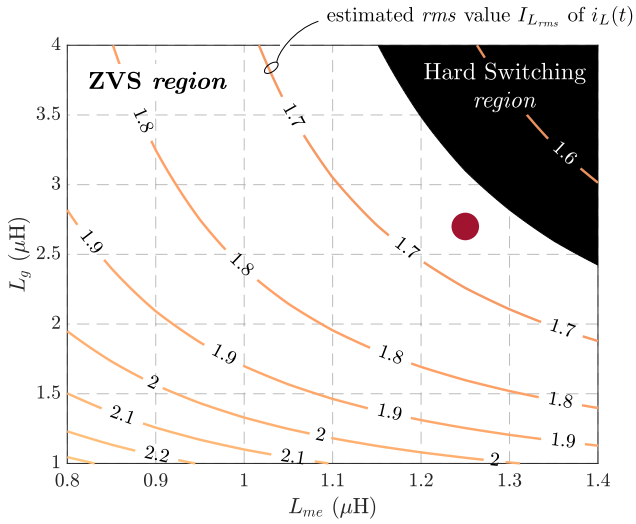


Fig. 7. (L_g, L_{me}) design space relative to the nominal operating point, reporting the ZVS and hard-switching regions, as well as the contour plots of $I_{L_{rms}}$. The final design choice adopted in this work is highlighted with a disk.

where $C_{eq,Q}$ is the charge-equivalent capacitance at the switching node [23], V_s the switching node voltage at the switching instant, and t_D the dead time. Assuming $t_D \approx 15\,\text{ns}$, such current can be estimated from the total output capacitance profile $C_{oss}(v_{ds})$ of the two switches [22].

Next, considering $\lambda = 6\%$ as a reasonable starting value for the transformer leakage-to-magnetizing inductance ratio of a high-frequency interleaved planar transformer, the possible design pairs (L_g, L_{me}) compatible with the ZVS constraint are considered, and reported in Fig. 7. In the plot, which assumes an initial choice $C_c = 48\,\text{nF}$ for the resonant capacitance and refers to the nominal operating point $V_g = 12\,\text{V}$, $I_o = 0.6\,\text{A}$, the ZVS and the hard-switching regions are illustrated. Furthermore, the overlaid contour lines represent the estimated root mean square (rms) value $I_{L_{rms}}$ of $i_L(t)$, a quantity directly related to the total conduction losses of the eGaN pair. Such estimation involves the approximation of $i_r(t)$ with $i_m(t)$, with the consequent almost triangular wave shapes, yielding

$$I_{L_{rms}} \approx (I_g + I_m)\sqrt{1 + \frac{1}{12}\left(\frac{\Delta i_L}{I_g + I_m}\right)^2} \tag{19}$$

where $\Delta i_L = \Delta i_g + \Delta i_m$. The peak-to-peak current ripple Δi_m and the average value of $i_m(t)$ are calculated using (10), while I_g and Δi_g are obtained as

$$I_g = \frac{1}{\eta}\frac{V_o I_o}{V_g}, \quad \Delta i_g = \frac{V_g D}{L_g} T_s. \tag{20}$$

To calculate the average value of the input current an efficiency $\eta = 87\%$ is assumed for the considered operating point. The foregoing equations clearly require the duty cycle value to be recalculated for each design pair (L_g, L_{me}), in order to maintain $V_o = 12\,\text{V}$ throughout the design space. This is accomplished by using the voltage gain model (16) developed in Section III.

Fig. 7 serves as a design tool to explore the tradeoff in the selection of L_g and L_{me}. On one hand, the design point (L_g, L_{me}) should be selected in proximity of the ZVS/hard switching

boundary in order to limit the value of $I_{L_{rms}}$. Within this basic constraint, the ACISC topology offers a degree of freedom in the relative choice of L_g and L_{me}, which translates into different amount of peak-to-peak current ripple on $i_g(t)$ and on $i_m(t)$. The specific design choice here adopted, $L_g \approx 2.7\,\mu\text{H}$ and $L_{me} \approx 1.25\,\mu\text{H}$, is highlighted in the plot with a disk.

Note that choosing a small value for λ—where the latter is a variable in which only L_{me} is controlled by the designer—comes from the initial target of realizing a transformer with a reduced leakage inductance value (interleaving the turns of the windings) to get a higher value for C_c while keeping the ZVS resonant DCM operation in nominal conditions. Increasing the value of the resonant capacitor leads to reducing both its voltage ripple (which is significant in the considered operation mode) and the voltage stress across the output diode D_r. However, this choice does not represent the unique design methodology for such an application. For example, the designer can be interested in minimizing the transformer's interwinding capacitance C_w—which is a critical parasitic capacitance of the converter in the common mode (CM) noise perspective—leading to a higher value of L_{pe} (and, consequently, of λ) since the interleaving between windings no longer represents the correct solution [24], [25]. In any case, one of the main advantages of the resonant operation is to add an additional degree of freedom, since the considered operating mode can always be ensured by adjusting the value of the resonant capacitor C_c.

A. Magnetics Design

To obtain the required magnetizing inductance and to reduce the overall footprint, we decided to use a planar transformer based on two ER9.5 half-cores (material 3F4), with a suitable air gap between the central legs in order to obtain the desired magnetizing inductance value. As a first attempt, the selected number of turns is determined starting from an analytical estimate of the core losses P_{core}. Once the peak flux density value $\hat{B}$ is estimated using the following expression:

$$\hat{B} = \frac{1}{n_1}\frac{n_e V_o}{2 f_s A_e}(1-D) \tag{21}$$

it is possible to calculate P_{core} at a given V_g by consulting the P_v *versus* $\hat{B}$ plot reported in the 3F4's datasheet. The first choice of $n_1 = n_2 = 6$ turns with $380\,\mu\text{m}$ air gap is determined as an adequate compromise between core and winding losses, the latter being estimated based on the calculated dc windings resistance.

Fig. 8 illustrates the planar transformer structure. Each six-turn winding consists of three series-connected layers of two turns each. Each two-turn layer is hosted on a $440\,\mu\text{m}$-thick PCB module, with one turn on the top and the other turn on the bottom. Primary and secondary layers are interleaved in order to minimize the leakage inductance, and separated by $60\,\mu\text{m}$-thick insulator sheets. The footprint area of the resulting structure is approximately $245\,\text{mm}^2$.

As anticipated, in this study the traditional 4-parameters transformer model, accounting for primary-side and secondary-side leakage inductances L_p and L_s, primary-side

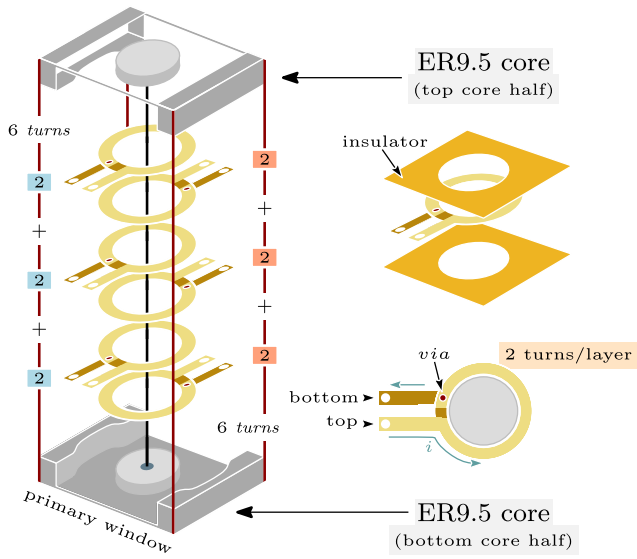


Fig. 8. Exploded view of the planar transformer based on two ER9.5 half-cores and three two-turns layers per winding ($n_1 = n_2 = 6$).

TABLE III
ACISC PARAMETERS

Parameter	Symbol	Value
Input inductance	L_g	2.2 µH
Equivalent primary leakage inductance	L_{pe}	75.2 nH
Equivalent magnetizing inductance	L_{me}	1.2 µH
Equivalent transformer turns ratio	n_e	0.97
Resonant capacitor	C_c	47.8 nF
Clamp capacitor	C_s	1 µF
Output capacitor	C_o	10 µF

magnetizing inductance L_m and turns ratio n, is simplified into the *reduced transformer model* as shown in Fig. 2. Extraction of reduced-model parameters L_{me}, L_{pe}, and n_e is accomplished by first experimentally characterizing the planar transformer by measuring the following three inductances:

1) L_{11}^{SO}: open-circuit primary-side inductance;
2) L_{22}^{PO}: open-circuit secondary-side inductance;
3) L_{11}^{SS} : short-circuit primary-side inductance.

The Agilent 4294 A Precision Impedance Analyzer was used to measure the above inductances at $f_s = 2\,\text{MHz}$. The reduced-order parameters are then simply calculated as

$$L_{pe} = L_{11}^{SS},\ L_{me} = L_{11}^{SO} - L_{11}^{SS},\ n_e = \sqrt{\frac{L_{11}^{SO} - L_{11}^{SS}}{L_{22}^{PO}}}. \tag{22}$$

The obtained values are reported in Table III, from which $\lambda \approx 6.3\%$ is obtained, in good agreement with the design assumption made to obtain the plot shown in Fig. 7.

As far as the required $2.7\,\mu\text{H}$ input inductance is concerned, a six-turn inductor employing ER9.5 cores (same 3F4 material) is realized, measuring the value, at $f_s = 2\,\text{MHz}$, reported in Table III.

TABLE IV
COMPONENTS' VOLTAGE/CURRENT STRESS FOR THE THREE INVESTIGATED TOPOLOGIES

Topology *	[INPUT CURRENT] I_g	[INPUT CURRENT] Δi_g	[MAGNETIZ. CURRENT] I_m	[MAGNETIZ. CURRENT] Δi_m	[VOLTAGE STRESSES] Q_1, Q_2	[VOLTAGE STRESSES] D_r	[OTHER PARAMETERS] I_r	[OTHER PARAMETERS] Δi_r	[OTHER PARAMETERS] M	Missing *parts*
ACISC	$\frac{1}{\eta}\frac{V_o I_o}{V_g}$	$\frac{DV_g}{f_s L_g}$	$\frac{I_o}{n_e}$	$\frac{n_e V_o}{f_s L_{me}}(1-D)$	$\frac{V_g}{1-D}$	$V_o + \frac{v_c(t)}{n_e(1+\lambda)}$	0	Δi_m	(16)	–
ACIFC	//	✗	$I_g + \frac{I_o}{n_e}$	$\frac{DV_g}{f_s L_{me}(1+\lambda)}$	$v_s(t)$	$V_o + \frac{V_g}{n_e(1+\lambda)}$	I_g	//	(23)	L_g, C_c
FLYBACK	//	✗	//	$\frac{n_e V_o}{f_s L_{me}}(1-D)$	$V_g + n_e V_o$	//	//	$I_m + \frac{\Delta i_m}{2}$	(23)	L_g, C_c, C_s, Q_2

* // means that the expression is equal to the one shown immediately above, and ✗ means that there is not an expression for the considered parameter.

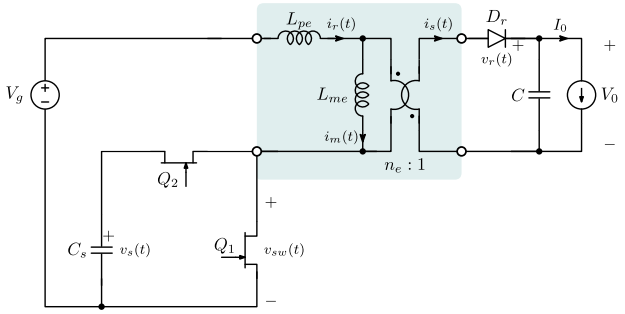


Fig. 9. Schematic of the GaN-based active-clamped isolated flyback converter, highlighting the adopted model for the high-frequency transformer.

V. REVIEW OF THE RESONANT ACTIVE-CLAMPED ISOLATED FLYBACK CONVERTER

An isolated alternative topology to the standard flyback converter and its viable substitute shown throughout this article is the ACIFC [12], [13], [14], [15]. Fig. 9 reports the schematic diagram of the topology which employs two enhancement-mode GaN devices and highlights the adopted model for the high-frequency transformer. Unlike the ACISC topology, this converter exhibits a high-frequency transformer T only as magnetics. Elements C_s and C are the clamping capacitor (in this case it also represents the resonant capacitor) and the output filter capacitor, respectively. Although this topology is capable of achieving ZVS for both switches, it does not employ the input inductor L_g which results in a higher DM conducted noise compared to the ACISC. On the other hand, the advantage of not hosting L_g is that the overall footprint of the ACIFC can be significantly reduced. Another drawback is the higher voltage stress across the switches due to a small value of C_s selected to guarantee a resonant DCM operation. However, one advantage of this topology is the lower voltage stress across the output diode D_r since there is no dependence on the significant voltage ripple across the resonant capacitor. Table IV shows the expressions of the voltages and currents involved both in the two active-clamped topologies operating in resonant DCM and in a standard flyback converter operating in CCM operation. Note that the schematic of the flyback is the same as that shown in Fig. 9 replacing the active clamp (Q_2 and C_s) with a passive one. When the ACIFC is operated in resonant DCM, magnetizing and resonant currents $i_m(t)$ and $i_r(t)$ have a similar trend to that shown in Fig. 3 (when Q_1 is ON now there is no resonance and the currents increase linearly). Expressions of resonant capacitor voltage $v_s(t)$ and of resonant current $i_r(t)$ are similar to the ones shown in (4) (now the coefficients multiplying the sine have opposite sign). Table V reports the new expressions of V_x, which depend on the topology and the considered subinterval, together with the resonant voltage and current equations. Following the procedure shown in Section III, even for the ACIFC topology is possible to find an analytical expression of M when the boundary CCM/DCM operating point is considered. The *volt-second* balance of the magnetizing inductance L_{me} yields

$$M \triangleq \frac{V_o}{V_g} = \frac{D}{1-D}\frac{1}{n_e(1+\lambda)} \tag{23}$$

where D is the duty cycle of the low-side switch Q_1. Note that (23) is equal to (16) once the voltage ripple across the ACISC's resonant capacitor C_c is neglected ($v_c(t) \approx V_c = V_g$).

TABLE V
COEFFICIENTS USED FOR THE RESONANT VOLTAGE AND CURRENT EQUATIONS IN THE ACIFC

Interval *	V_x	Z_o	ω_o	Q_1	Q_2	D_r	reson.
DT_s	–	–	–	ON	OFF	OFF	no
D_2T_s	$V_g + n_e V_o$	Z_r	ω_r	OFF	ON	ON	✓
D_3T_s	V_g	Z_{ro}	ω_{ro}	OFF	ON	OFF	✓

$$v_s(t) = Z_o I_{ri}\sin[\omega_o(t-t_i)] + (V_{Ci} - V_x)\cos[\omega_o(t-t_i)] + V_x$$
$$i_r(t) = \frac{1}{Z_o}(V_x - V_{Ci})\sin[\omega_o(t-t_i)] + I_{ri}\cos[\omega_o(t-t_i)]$$

* Time instant t_i $(i = 1, 2, 3)$ represents the beginning of each subinterval $(t_1 = 0)$.

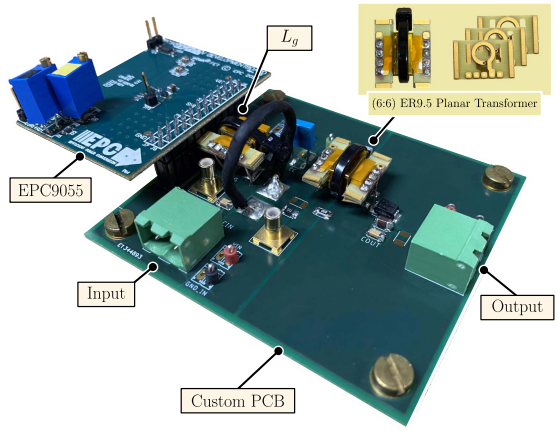


Fig. 10. Picture of the experimental prototype: The GaN-based active-clamped isolated SEPIC converter (ACISC).

VI. EXPERIMENTAL RESULTS

A. ACISC Converter

To validate the design methodology shown in Section IV, a 2 MHz 12 V, 600 mA GaN-based converter is realized. Fig. 10

shows the picture of the experimental prototype with a detail of the 6 : 6 ER9.5 planar transformer. The prototype is built around the EPC9055 development board, which features the selected 100 V, 1.7 A EPC2106 half-bridge pair. The development board, which already hosts a 1 µF clamp capacitor C_s, is connected at the switching node with a custom-designed PCB, where the input inductor, resonant capacitor, planar transformer, and output rectifier stage are located. The experimentally characterized values of the passive components are reported in Table III. A 40 V, 2 A Schottky rectifier is selected for D_r. Because of the large forward voltage drop of the body diode in GaN devices, both driving dead times for the eGaN pair have been adjusted to reduce the body diode conduction time as much as possible throughout the entire input voltage operating range. Such operation was performed manually, once and for all, in nominal condition by adjusting two on-board trimmers (blue boxes in Fig. 10). Fig. 11 reports the converter experimental waveforms for $V_o = 12\,\mathrm{V}$ and $I_o = 600\,\mathrm{mA}$, when the input voltage V_g assumes the minimum, nominal, and maximum values. Despite the high frequency noise, the resonant current $i_r(t)$ exhibits the behavior already shown in Fig. 3, especially for input voltages greater than 9 V where the converter starts operating in DCM operation. Fig. 11 shows that the critical ZVS condition is always satisfied, except for the minimum input voltage, for which the current $i_L(T_s)$ is not sufficiently *negative* to allow $v_{sw}(t)$ to complete the entire transition before the end of the dead time. The fixed dead time for the falling edge of $v_{sw}(t)$ is almost equal to 15 ns and is close to the value chosen to plot Fig. 7.

B. ACIFC Converter

The main specifications dictated by the considered application are reported in Table II. The 100 V, 1.7 A EPC2106 eGaN FET pair [22] is still selected to implement Q_1 and Q_2. As already mentioned in Section IV, the turn-ON of the low-side switch Q_1 represents the critical ZVS transition for which $i_L(T_s)$ must be sufficiently *negative*. Using (18), where V_s is the value of $v_{sw}(t)$ at the end of the period, it is possible to estimate the amount of current required for the critical ZVS transition assuming to have the same dead time set for the ACISC ($t_D \approx 15\,\mathrm{ns}$). As can be seen in Fig. 12 – which shows the experimental screenshot of $v_{sw}(t)$ in nominal condition—the value of the latter at $t = T_s$ is almost 6 V lower then the one obtained for the ACISC [see Fig. 11(b)]. This result represents an advantage for the ACIFC topology since a lower current $|i_L(T_s)|$ is sufficient to turn Q_1 ON with zero-voltage. On the other hand, as shown in Table IV, a big disadvantage of this topology is the higher average magnetizing current value I_m, which calls for a high magnetizing current ripple (*i.e.* a reduced L_{me} value) to provide a sufficiently *negative* value to $i_L(T_s)$. This leads to higher conduction losses of the eGaN pair and, more importantly, higher transformer primary winding losses. A resonant capacitor $C_s = 20\,\mathrm{nF}$ was used as a replacement of the one hosted by the EPC9055 development board to still have the resonant DCM operation.

C. Efficiency Profile

Fig. 13 compares the efficiency of the designed 2 MHz ACISC (curve labeled T_1) with that of the 2 MHz ACIFC (curve labeled T_2) and a 400 kHz commercial flyback converter operating in CCM intended for the same application and having the same input/output voltage and rated current specifications (the measured parameters of the realized transformers T_1 and T_2 are reported in Table VI). The comparison, carried out as a function of both input voltage V_g and output current I_o, reveals a peak efficiency of the designed ACISC of 87.22% at $V_o = 12\,\mathrm{V}$ and $I_o = 600\,\mathrm{mA}$, approximately 7.2% better than the commercial flyback converter despite the fivefold increase in switching frequency. Note that the efficiency profile of the ACIFC is far from that of ACISC mainly due to the low value of

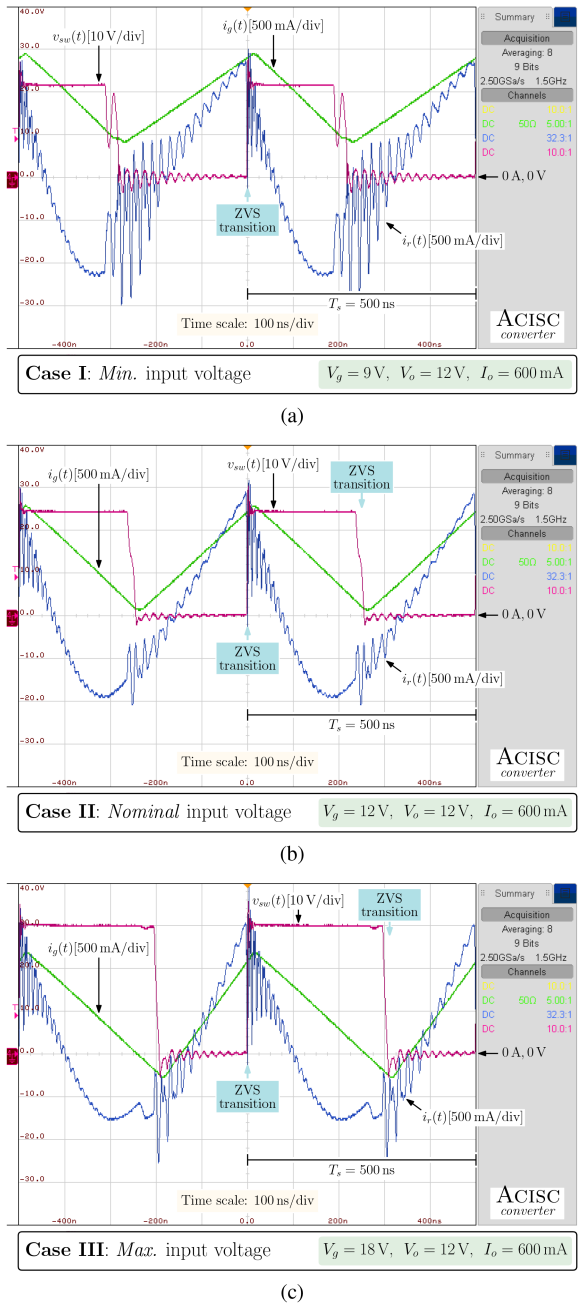


Fig. 11. Experimental screenshot of the input current $i_g(t)$ (500 mA/div), the resonant current $i_r(t)$ (500 mA/div), and the switching node voltage $v_{sw}(t)$ (10 V/div) at $V_o = 12\,\mathrm{V}$ and $I_o = 600\,\mathrm{mA}$, when the input voltage V_g is equal to (a) 9 V, (b) 12 V, and (c) 18 V. Time scale: 100 ns/div.

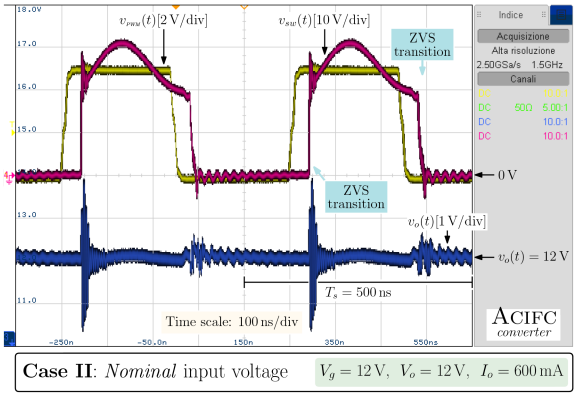


Fig. 12. Experimental screenshot of the output voltage $v_o(t)$ (1 V/div, $v_{offset} = 14$ V), the input PWM $v_{PWM}(t)$ (2 V/div) used to drive the switches, and the switching node voltage $v_{sw}(t)$ (10 V/div) at $V_o = 12$ V and $I_o = 600$ mA, when the input voltage $V_g = 12$ V. Time scale: 100 ns/div.

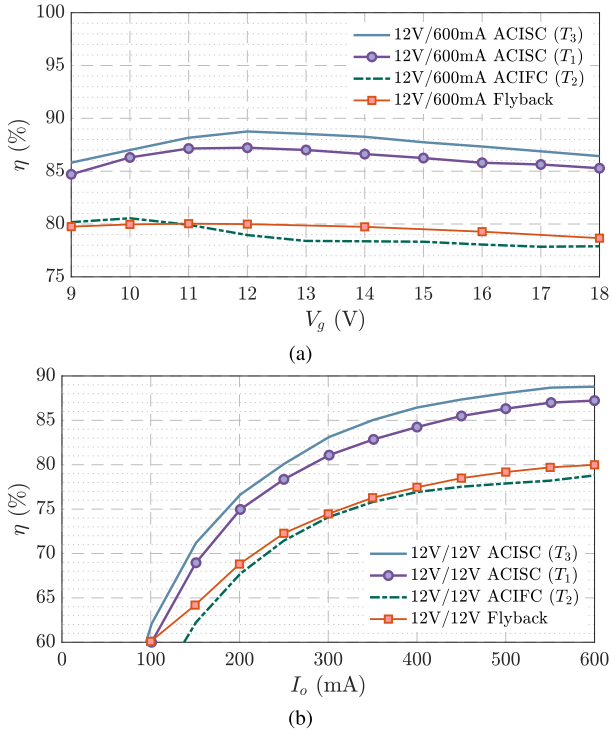


Fig. 13. Efficiency comparison between the designed 2 MHz ACISC, the designed 2 MHz ACIFC, and a 400 kHz commercial flyback converter having the same input/output voltage and current rating specifications, as a function of (a) the input voltage V_g and (b) the output current I_o.

TABLE VI
PLANAR TRANSFORMER PARAMETERS CHARACTERIZED AT $f_s = 2$ MHz

	Turns	Core material	Gap (μm)	L_{me} (μH)	L_{pe} (nH)	$R_{w1,ac}$ (mΩ)	$R_{w2,ac}$ (mΩ)
T_1	6 : 6	3F4	380	1.22	75.2	248	235
T_2	6 : 6	3F4	680	0.62	75.7	197	192
T_3	4 : 4	3F46	88	1.38	43.7	158	136

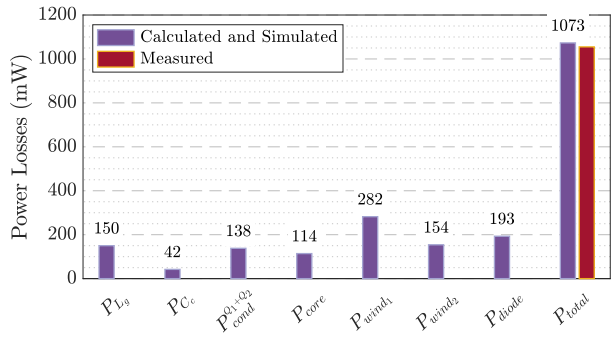


Fig. 14. Power loss breakdown of the designed 2 MHz ACISC topology for $V_g = V_o = 12$ V and $I_o = 600$ mA.

L_{me} required for the ZVS operation which results in a significant increase in transformer primary winding losses P_{wind_1}.

D. Power Loss Breakdown Analysis

At the nominal operating point, the ACISC topology exhibits a total power loss $P_{loss} = V_o I_o(1/\eta - 1) \approx 1055$ mW. A power loss breakdown analysis is described here, for the ACISC operating in nominal conditions, with the purpose of identifying the main loss sources and estimate their relative contributions. All the analytical estimates are carried out considering a temperature equal to 100 °C, except for the GaN's conduction losses where their real temperature is derived using a Laserliner ThermoCamera (see the thermal measurement reported at the end of this section). Thus, from the EPC2106 datasheet, their ON-state resistance was estimated as $R_{ds,(on)}(50\,°\text{C}) \approx 1.18 \cdot R_{ds,(on)}(25\,°\text{C}) = 65$ mΩ. As far as the magnetics are concerned, both core losses P_{core} and winding losses P_{wind} are considered, the latter calculated from the measured ac winding resistances $R_{w1,ac}$ and $R_{w2,ac}$ (for the planar transformer), and $R_{w,ac} = 283$ mΩ (for the input inductor), all taken at 2 MHz (see Table VI, row labeled T_1). The estimation of the output diode conduction losses P_{diode} uses both the threshold voltage $V_{T_0}(T_j)$ and the dynamic resistance $R_D(T_j)$, which are extrapolated from the linear fitting of the i_F-v_F characteristic of the chosen Schottky rectifier. As for the body diode conduction losses of the switches, these are here neglected in light of the preliminary dead time optimization described above. The result of the power loss breakdown analysis for the ACISC topology employing T_1 is shown in Fig. 14, demonstrating a good agreement with the total measured power losses. The largest contribution is associated with the transformer, and in particular with primary winding losses to be attributed to skin and proximity effects in the MHz range. As a matter of fact, the high ac winding resistance is very difficult to predict, being strongly dependent on the leakage flux distribution inside the core window. This, suggested to re-design the planar transformer with a fewer number of turns.

E. Optimization of the Planar Transformer

A new 4 : 4 ER9.5 planar transformer was built for the ACISC to reduce the winding resistance. At the same time, to limit the

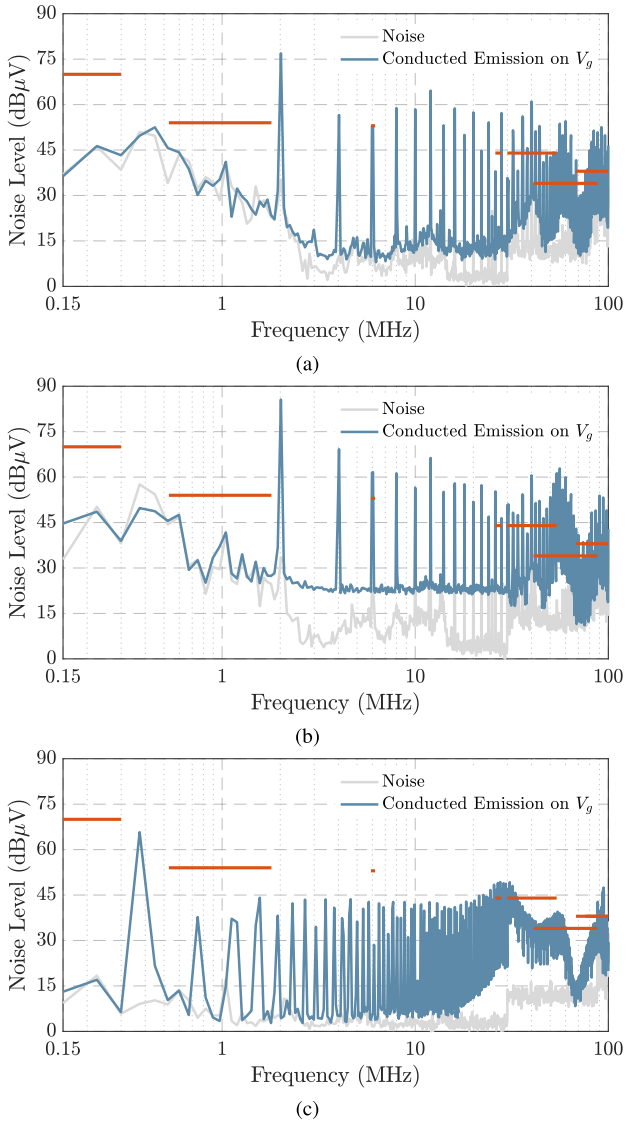


Fig. 15. Conducted emission measured at the input (power supply V_g) using a noise separator and a LISN (nominal conditions). (a) Designed 2 MHz ACISC with transformer T_1. (b) Designed 2 MHz ACIFC with transformer T_2. (c) 400 kHz commercial flyback converter.

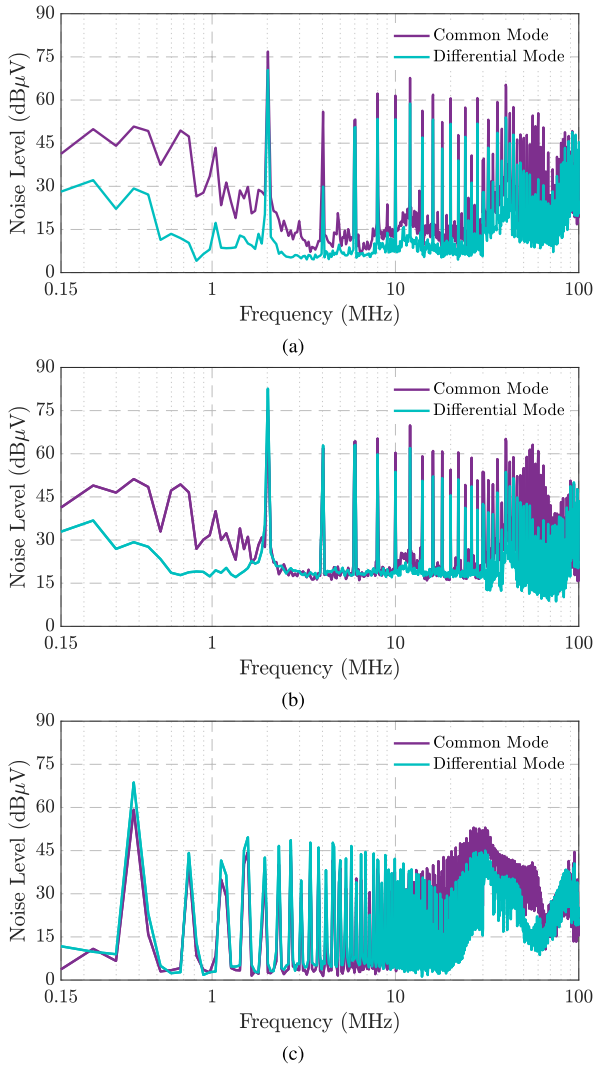


Fig. 16. Input CM and DM conducted noise measured using a noise separator and a LISN (nominal conditions). (a) Designed 2 MHz ACISC with transformer T_1. (b) Designed 2 MHz ACIFC with transformer T_2. (c) 400 kHz commercial flyback converter.

core losses, the new 3F46 high-frequency material was selected, whose power loss density at 2 MHz and $\hat{B} = 40\,\mathrm{mT}$, is about 85% less than the 3F4 material. The air gap was adjusted to obtain almost the same magnetizing inductance L_{me} and the measured parameters are reported in Table VI (transformer T_3). With the new planar transformer the value of the two ac winding resistances is reduced by almost $100\,\mathrm{m\Omega}$. The new measured efficiency is also reported in Fig. 13 (curve labeled T_3), showing a further improvement of roughly 1.5%.

F. EMI Analysis, Temperature Considerations, and Comparison of Physical Dimensions

Here, we want to compare the 2 MHz ACISC with the 2 MHz ACIFC and the 400 kHz commercial flyback converter in terms of EMI noise, temperature in the main components, and physical dimensions. Concerning the EMI measurements, the experimental setup consists of the following: 1) the equipment necessary to supply the converters; 2) a LISN placed between the power supply V_g and the converter's input; and 3) an EMC Analyzer to measure the noise level. The standard CISPR 25—which defines measurement setups and limits of conducted emissions for automotive devices with low-voltage (LV) sources or loads—was adopted, while Class 5 (*Peak* detector) was considered for the conducted disturbances' limits. Fig. 15(a)–(c) provides the conducted emission at the input for ACISC, ACIFC, and the commercial flyback, respectively (both the standard noise level and the limits are shown). Test results are obtained when the three converters are operated in nominal conditions without EMI filters and with roughly the same total input capacitance. On the other hand, Fig. 16 shows the same results depicted in Fig. 15 with the aim of highlighting the input CM and differential mode (DM) conducted noise. The ACISC is better than the ACIFC topology in terms of conducted emission mainly due

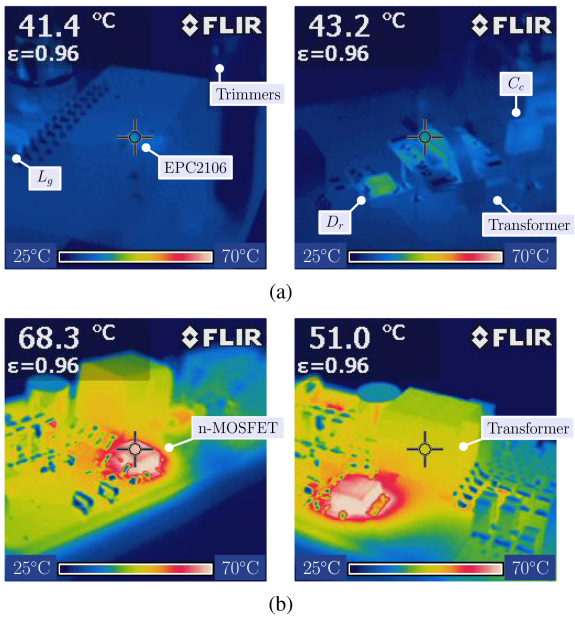


Fig. 17. Measured temperature of transformer and switches in nominal conditions of (a) the designed 2 MHz ACISC with transformer T_1 and (b) the 400 kHz commercial flyback converter.

to the presence of the input inductor L_g which acts as a filter. Comparing Fig. 15(a) with (b), a reduction of almost 10 dBμV can be observed in the ACISC by looking at the first spectral line. The much higher dv/dt of GaN devices, compared with their Si counterparts, increases conducted—and most likely radiated—emissions, especially in terms of CM noise. Indeed, Fig. 16(a) reveals such dominance of the CM noise in the whole considered frequency range. Test results also show that the frequency spectrum of the two GaN-based prototypes exceeds the CISPR 25 limits in the high-frequency range: the use of EMI filters, a better layout, and the optimization of the magnetics in terms of parasitics minimization can help to bring the high-frequency spectral lines under the required limits. *Note* that the increased ground noise level in the low-frequency range highlighted in Fig. 15(a) and (b), compared with Fig. 15(c), was caused by the external waveform generator used to drive the two GaN switches. Finally, the reason why the bottom part of Fig. 15(b) and Fig. 16(b) (ACIFC results) seems to be cut is due to a selected attenuation value in the EMC Analyzer different from 0 dB.

The thermal images shown in Fig. 17, taken after 20 min of nominal operating conditions ($V_g = V_o = 12\,\text{V}$ and $I_o = 600\,\text{mA}$), reveal almost 27 °C less in the eGaN switches and 8 °C less in the transformer comparing the ACISC with the corresponding components in the commercial flyback. Even if it is not shown in the figures, the overall temperature in the main components hosted by the ACISC is almost 15 °C lower then the one observed in the ACIFC topology due to a lower *rms* current flowing in the transformer primary winding and switches.

Table VII summarizes the main experimental results obtained for the three topologies in nominal operating conditions. Looking at the results obtained for the GaN-based topologies, the ACISC is better than the ACIFC in terms of efficiency (+10%), overall temperature in the main components (−15 °C) and EMI. Physical dimensions are also included in Table VII, where it can be seen that the main components employed in the GaN-based topologies are significantly smaller than those used in the commercial flyback converter.

TABLE VII
MAIN RESULTS OBTAINED FOR THE THREE INVESTIGATED TOPOLOGIES

Experimental results *		ACISC	ACIFC	Flyback	
Efficiency η		88.8	79.0	80.0	%
Temperature	[switches]	41.4	57.5	68.3	°C
	[transformer]	43.2	56.0	51.0	°C
Conducted Emission on V_g		76.9	85.6	65.8	dB μV
Physical size switches	↦ WIDTH	1.35	1.35	9.98	mm
	↦ LENGTH	1.35	1.35	6.50	mm
	↦ HEIGHT	0.63	0.63	2.30	mm
Physical size transformer	↦ WIDTH	14.35	14.35	17.75	mm
	↦ LENGTH	17.10	17.10	14.50	mm
	↦ HEIGHT	4.90	4.90	14.00	mm
Type of switches		GaN	GaN	Si	
Operating mode		(RESONANT DCM)		(CCM)	
Switching frequency f_s		2	2	0.4	MHz

* The results are obtained in nominal conditions ($V_g = V_o = 12\,\text{V}$, $I_o = 600\,\text{mA}$), and "Conducted Emission on V_g" is referred to the peak value of the first spectral line.

VII. CONCLUSION

This article addresses the analysis, design, and experimental verification of a 2 MHz, 12 V, 600 mA GaN-based ACISC operating in resonant DCM and intended for low-power automotive applications. The chosen converter operating mode, coupled with the proposed design methodology and high switching rate, guarantees ZVS throughout the intended operating range and leads to reduced magnetic size and overall footprint. A design procedure for the converter is first proposed which enables the designer to tradeoff the input inductance L_g and the magnetizing inductance L_{me} while minimizing the total switch conduction losses. The design details for the high-frequency transformer, realized here as a planar structure, and input inductance, are then outlined. Performance comparison in terms of efficiency, temperature in the main components, EMI, devices' stresses, and physical dimensions is carried out between a 2 MHz GaN-based ACISC topology, a 2 MHz GaN-based ACIFC, and a 400 kHz commercial flyback. Experimental results confirm full ZVS operation in nominal conditions of the GaN-based topologies operated in resonant DCM and a better performance from the ACISC topology. Peak efficiency of the optimized ACISC operating in nominal condition at full load is almost 89%, approximately 9% higher than the efficiency of a commercial 400 kHz flyback converter designed for the same input/output voltages and output current rating.

REFERENCES

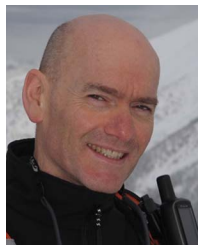
[1] S. Cabizza, G. Spiazzi, and C. Garbossa, "Active-clamped isolated SEPIC converter in the MHz range for low-power subnets," 17/651 137, Feb. 15, 2022.

[2] S. Cabizza, L. Corradini, G. Spiazzi, and C. Garbossa, "Comparative study of 48V-based low-power automotive architectures," in *Proc. 21st IEEE Workshop Control Model. Power Electron.*, 2020, pp. 1–8.

[3] S. Cabizza, L. Corradini, and G. Spiazzi, "Analysis and design of a 2 MHz gan-based active-clamped isolated sepic converter for low-power automotive subnets," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2022, pp. 2127–2134.
[4] P. Athalye, D. Maksimovic, and R. Erickson, "High-performance front-end converter for avionics applications [aircraft power systems]," *IEEE Trans. Aerosp. Electron. Syst.*, vol. 39, no. 2, pp. 462–470, Apr. 2003.
[5] P. Athalye, D. Maksimovic, and R. Erickson, "Improving efficiency of the active-clamped sepic rectifier at high line frequencies," in *Proc. 28th Annu. IEEE Appl. Power Electron. Conf. Expo.*, 2005, vol. 2, pp. 1152–1157.
[6] D. Wu, R. Ayyanar, M. Sondharangalla, and T. Meyers, "High-performance active-clamped isolated SEPIC PFC converter with SiC devices and lossless diode clamp," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 1, pp. 567–577, Mar. 2020.
[7] M. Chen and J. Sun, "Reduced-order averaged modeling of active-clamp converters," *IEEE Trans. Power Electron.*, vol. 21, no. 2, pp. 487–494, Mar. 2006.
[8] G. Spiazzi, L. Rossetto, and P. Mattavelli, "Design optimization of soft-switched insulated DC/DC converters with active voltage clamp," in *Proc. Conf. Rec. IEEE Ind. Appl. Conf. 31st IAS Annu. Meeting*, 1996, vol. 2, pp. 1169–1176.
[9] B.-R. Lin and C.-C. Chen, "Soft switching isolated SEPIC converter with the buck-boost type of active clamp," in *Proc. 2nd IEEE Conf. Ind. Electron. Appl.*, 2007, pp. 1232–1237.
[10] P. Athalye, D. Maksimovic, and R. Erickson, "Averaged switch modeling of active-clamped converters," in *Proc. 27th Annu. Conf. IEEE Ind. Electron. Soc.*, 2001, pp. 1078–1083.
[11] M. A. Al-Saffar, E. H. Ismail, A. J. Sabzali, and A. A. Fardoun, "An improved topology of SEPIC converter with reduced output voltage ripple," *IEEE Trans. Power Electron.*, vol. 23, no. 5, pp. 2377–2386, Sep. 2008.
[12] R. Watson, F. Lee, and G. Hua, "Utilization of an active-clamp circuit to achieve soft switching in flyback converters," *IEEE Trans. Power Electron.*, vol. 11, no. 1, pp. 162–169, Jan. 1996.
[13] X. Huang, J. Feng, W. Du, F. C. Lee, and Q. Li, "Design consideration of MHz active clamp flyback converter with GAN devices for low power adapter application," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2016, pp. 2334–2341.
[14] T. LaBella, B. York, C. Hutchens, and J.-S. Lai, "Dead time optimization through loss analysis of an active-clamp flyback converter utilizing GAN devices," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2012, pp. 3882–3889.
[15] R. Perrin, N. Quentin, B. Allard, C. Martin, and M. Ali, "High-temperature GAN active-clamp flyback converter with resonant operation mode," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 3, pp. 1077–1085, Sep. 2016.
[16] D. H. Seo, O. J. Lee, S. H. Lim, and J. S. Park, "Asymmetrical PWM flyback converter," in *Proc. IEEE 31st Annu. Power Electron. Specialists Conf. Conf.*, 2000, vol. 2, pp. 848–852.
[17] T. Chen and C. Chen, "Analysis and design of asymmetrical half bridge flyback converter," *IEE Proc. - Elect. Power Appl.*, vol. 149, no. 6, pp. 433–440, Nov. 2002.
[18] J. Cho, J. Kwon, and S. Han, "Asymmetrical ZVS PWM flyback converter with synchronous rectification for ink-jet printer," in *Proc. 37th IEEE Power Electron. Specialists Conf.*, 2006, pp. 1–7.
[19] G. Jeong, "High efficiency asymmetrical half-bridge flyback converter using a new voltage-driven synchronous rectifier," *IET Power Electron.*, vol. 3, no. 1, pp. 18–32, Jan. 2010.
[20] H. Kim, J. Jung, J. Baek, and H. Kim, "Analysis and design of a multioutput converter using asymmetrical PWM half-bridge flyback converter employing a parallel-series transformer," *IEEE Trans. Ind. Electron.*, vol. 60, no. 8, pp. 3115–3125, Aug. 2013.
[21] G. Spiazzi and S. Buso, "Extended analysis of the asymmetrical half-bridge flyback converter," *IEEE Trans. Power Electron.*, vol. 36, no. 7, pp. 7956–7964, Jul. 2021.
[22] "Efficient power conversion, EPC2106 enhancement-mode GaN power transistor half-bridge," 2021. [Online]. Available: https://epc-co.com/epc/Portals/0/epc/documents/datasheets/EPC2106_datasheet.pdf
[23] D. Costinett, D. Maksimovic, and R. Zane, "Circuit-oriented treatment of nonlinear capacitances in switched-mode power supplies," *IEEE Trans. Power Electron.*, vol. 30, no. 2, pp. 985–995, Feb. 2015.
[24] Z. Ouyang and M. A. E. Andersen, "Overview of planar magnetic technology–fundamental properties," *IEEE Trans. Power Electron.*, vol. 29, no. 9, pp. 4888–4900, Sep. 2014.
[25] C. Fei, Y. Yang, Q. Li, and F. C. Lee, "Shielding technique for planar matrix transformers to suppress common-mode EMI noise and improve efficiency," *IEEE Trans. Ind. Electron.*, vol. 65, no. 2, pp. 1263–1272, Feb. 2018.

Stefano Cabizza (Student Member, IEEE) received the M.Sc. degree in electronic engineering from the University of Padova, Padova, Italy, in 2019, where he is currently working toward the Ph.D. degree in information engineering with the Department of Information Engineering (DEI), together with the Power Electronics Group.

His research interests include the analysis and design of high-frequency dc–dc converters for automotive applications, soft-switching techniques, and electromagnetic compatibility in power electronics.



Giorgio Spiazzi (Member, IEEE) received the graduation degree *(cum laude)* in electronic engineering and the Ph.D. degree in industrial electronics and informatics from the University of Padova, Padova, Italy, in 1988 and 1993, respectively.

He is currently a Full Professor with the Department of Information Engineering (DEI), University of Padova. His main research interests include dc–dc converters for renewable energy sources, high-power-factor rectifiers, soft-switching techniques, solid-state lamp ballasts, and electromagnetic compatibility in power electronics.

Luca Corradini (Senior Member, IEEE) received the *Laurea* degree in electronic engineering and the Ph.D. degree in industrial electronics from the University of Padova, Italy, in 2004 and 2008 respectively. From 2008 to 2011 he was a Postdoctoral Research Associate at the Colorado Power Electronics Center (CoPEC), University of Colorado at Boulder, USA.

Dr. Corradini has been Assistant Professor with the University of Padova, Italy, from 2011 to 2017. He has been Associate Professor at the Department of Information Engineering of the University of Padova, Italy, since 2017, and at the Department of Electrical, Computer and Energy Engineering of the University of Colorado Boulder, USA, since 2022. He is co-author of the textbook *Digital Control of High-Frequency Switched-Mode Power Converters*. His research interests in power electronics include digital control and modeling of switched-mode power converters, control techniques for dc–dc multi-level converters, modulation and control of bi-directional dc–dc converters, and power management solutions for energy harvesting systems.

Dr. Corradini received the second 2008 Prize Paper Award from the Industrial Power Converter Committee of the IEEE Industry Applications Society. In 2018, he was General Chair of the 19th IEEE Workshop on Control and Modeling for Power Electronics (IEEE COMPEL 2018), held in Padova, Italy. He is currently Associate Editor of the IEEE TRANSACTIONS ON POWER ELECTRONICS, and Chair of the Technical Committee 1 *Control and Modeling of Power Electronics* of the IEEE Power Electronics Society.