Optimum Phase Count in a 5.4-W Multiphase Buck Converter Based on Output Filter Component Energies

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***Abstract*—This article presents an analysis of low-power, multiphase interleaved buck converters to illustrate the extent to which adding more phases is beneficial for reducing the passive components' sizes. The analysis focuses on a typical converter application with a wide operating duty cycle range and requires good load transient. It is shown that by restricting the phase current ripple, the theoretical reduction in total inductor peak energy predicted for increased phase numbers is limited. The article assesses the benefit of inductor coupling and presents guidelines for coupling factor selection to avoid steady-state inductance roll-off over the wide input voltage range. Standard printed circuit board (PCB) manufacturing design rules are shown to place a practical phase count limit considering the reduction in total inductor size. PCB integrated, air-core solenoid and spiral inductors are implemented in both single- and two-phase 5.4 W, 20 MHz buck converter prototypes. When compared with single-phase designs, two-phase spiral inductors are 44% smaller, and the two-phase solenoid has a 54% lower loss. The two-phase prototype converter achieves better overall efficiency and peaks at almost 90% at $V_{IN} = 4.5$ V, $V_{OUT} = 1.8$ V, and $F_{SW} = 20$ MHz.**

***Index Terms*—Air-core inductor, coupled inductor, interleaved converter, multiphase buck, PCB inductor, point-of-load.**

I. Introduction

HIGHER power densities and the longer battery lifetimes desired for computational and battery-powered consumer products increase the motivation for smaller and more efficient devices. High-performance microprocessors, graphical processing units, and other applications are powered by multiphase interleaved buck converters for dc voltage step-down requirements. Generally, the multiphase topology shown in Fig. 1 is a good solution for improving light-load converter efficiency, where phases can be switched OFF as required to reduce per-phase quiescent power loss [1], [2]. Furthermore, multi-MHz switching enables size reduction in the required passive components, particularly important for the inductors, as they are usually the biggest components in converters. Another advantage of interleaving is the partial cancellation of output current ripple and the multiplied output ripple frequency, both of which can contribute to the overall size reduction of the required passive elements for a given output voltage ripple and converter transient response [3], [4]. Separately, individual phase currents need also to be considered to ensure that rms current handling requirements are met.

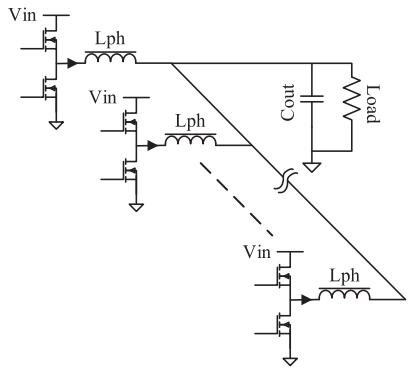

Fig. 1. Schematic of multiphase buck converter.

Determining the number of phases for optimized overall inductor density is essential, especially for size-sensitive applications such as converters employing on-chip and copackaged inductors, as in [5] (1–4 phases), [6] (1–8 phases), [7] (1–4 phases), and [8] (16 phases). The interleaved buck has been widely investigated for various converter specifications and packaging technologies, e.g., [9], [10], [11], [12], [13], [14]. However, to the best of the authors' knowledge, the effect of adding more phases on the overall size of the passive components while considering practical limitations, such as the effect of wide input voltage range and limited current per phase, has not been addressed.

Manuscript received 19 April 2022; revised 17 July 2022 and 8 October 2022; accepted 9 November 2022. Date of publication 5 December 2022; date of current version 14 February 2023. This work was supported by the Science Foundation Ireland under the ADEPT Project 15/IA/3180 "Advanced Integrated Power Magnetics Technology - From Atoms to Systems" for which Prof. Cian O'Mathúna is the Principal Investigator and for which Dr. Maeve Duffy is a Collaborator. Recommended for publication by Associate Editor J. Lam. *(Corresponding author: Youssef Kandeel.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2022.3226708.

Digital Object Identifier 10.1109/TPEL.2022.3226708

Some attempts have been made to determine the optimum number of phases, as in [15], which evaluated the converter efficiency assuming a fixed total inductance divided equally between all phases. For silicon-integrated solenoid inductors, the authors concluded that four phases achieved the best overall efficiency for the three converter specifications considered. However, they did not consider a wide input voltage range; besides, the basis of inductance selection may result in different total output current ripples and is therefore not a like-for-like comparison.

The variation in the optimum number of phases in the previous literature is due to different application requirements and inductor technologies. This article addresses this deficiency by creating a design procedure to determine the optimum number of phases in terms of the overall output filter size.

Another aspect of the interleaved buck topology focuses on the benefits of negative magnetic coupling between phases. Negative coupling partially cancels the dc magnetic field component, alleviating the magnetic core's saturation limit and potentially improving load transient performance. Coupled versus noncoupled inductors have been compared for various applications in [16], [17] at 300, [18] at 600, and [19] at 250 kHz, whereas coupled inductors have been implemented in several multi-MHz converters, e.g., [3], [20], [21], [22], [23], [24]. However, most authors consider a single input voltage value; the optimum choice of coupling factor for a wide input voltage range has not been clearly described. Therefore, this article analyzes the coupling factor that maximizes the effective inductance per phase while also identifying the input voltage range for effective coupling.

To illustrate the findings, PCB air-core inductor designs are considered for a nominal conversion specification of 4.5–1.8 V at 5.4 W. An input voltage range of 2.5–6.6 V is assumed to align with a typical battery-powered converter specification. This incorporates the effect of PCB processes on inductor designs. This article builds on the concepts presented in [25] but covers a broader range of applications through normalized analysis and considers air-core PCB inductors, which were available for fast prototyping.

The rest of this article is organized as follows. Section II presents a normalized analysis of the multiphase interleaved buck converter considering practical circuit specifications and limitations. Section III presents a comparison of passive component specifications for different numbers of phases in a multiphase buck converter for a given converter specification. Section IV presents the inductor modeling and design procedure applied for air-core spiral and solenoid inductors based on given PCB manufacturing design rules. Section V presents a comparison of circuit simulation and measurement results, which confirm the findings on the optimum inductor designs for the fabricated inductors. Finally, Section VI concludes this article.

II. Multiphase Interleaved Buck Analysis

In a multiphase interleaved buck converter, each phase is shifted by $360°/N_{Ph}$ from the next one, where N_{Ph} is the number of phases. This interleaved operation partially cancels the overall current ripple, resulting in smaller output ripple amplitude and multiplied frequency compared with noninterleaved operation. The overall output current ripple ΔI_{Nph} produced by the sum of phase currents is governed by the ripple reduction effect presented in [17], i.e.,

$$\Delta\, I_{Nph\_norm} = \frac{\Delta I_{Nph}}{\Delta I_{Ph}} = \frac{N_{Ph}}{D\,(1-D)}\left(D - \frac{m}{N_{Ph}}\right)\left(\frac{1+m}{N_{Ph}} - D\right) \tag{1}$$

where ΔI_{Nph_norm} is the normalized value of the overall output current ripple relative to the per-phase inductor current ripple ΔI_{Ph}, D is the switching duty cycle, and m is the integer number less than or equal to ($N_{Ph}D$) as explained in [17].

Ideally, the optimum number of phases is at multiples of ($1/D$) where, as shown by (1), the sum of the phase current ripples is theoretically zero. However, considering the practical requirements of individual component specifications (such as the inductors) and operation over a range of D may change the benefits of adding more phases. This work aims to find an optimum number of phases for practical converter specifications from a passive components size perspective.

A. Inductance Selection for Multiphase Buck Converter

As discussed in [25], inductance in a multiphase interleaved buck converter is selected to satisfy a certain total output current ripple requirement ΔI_{Nph}. In this analysis, for comparison purposes, ΔI_{Nph} is set equal to the inductor current ripple in a corresponding single-phase converter ΔI_{1ph}. So, the ripple reduction function in (1) is used to calculate the maximum allowed inductor current ripple per phase ΔI_{Ph} (2)

$$\Delta I_{Ph} = \frac{\Delta I_{Nph}}{\Delta I_{Nph\_norm}} \tag{2}$$

$$\Delta I_{Ph\%} = \frac{\Delta I_{Ph} N_{Ph}}{I_{\mathrm{DC}}} \tag{3}$$

Depending on the level of ripple cancellation, (1)–(2) may predict very high values of ΔI_{Ph}. However, practically, it needs to be limited to avoid excessive current in each phase inductor. For illustration, resulting values of unrestricted and restricted $\Delta I_{Ph\%}$ (3) versus duty cycle are compared in Fig. 2(a) for a three-phase interleaved buck converter at an overall current ripple level, $\Delta I_{Nph\%} = \Delta I_{Nph}/I_{\mathrm{DC}} = 25\%$ at different ripple restriction conditions (100%, 200%, and 300%). Clearly, the unrestricted $\Delta I_{Ph\%}$ becomes very high close to theoretical optimum ripple cancellation conditions, i.e., when N_{Ph} equals multiples of $1/D$.

Then, phase inductance L_{Ph} is calculated as

$$L_{Ph} = \frac{D\,(V_{IN} - V_{OUT})}{\Delta I_{Ph} F_{SW}} \tag{4}$$

where V_{IN}, V_{OUT}, and F_{SW} are the specified input voltage, output voltage, and switching frequency, respectively, and unrestricted ΔI_{Ph} is calculated from (1) and (2) based on N_{Ph} and the specified ripple of the summed phase currents ΔI_{Nph}. This interleaving ripple reduction results in a normalized total

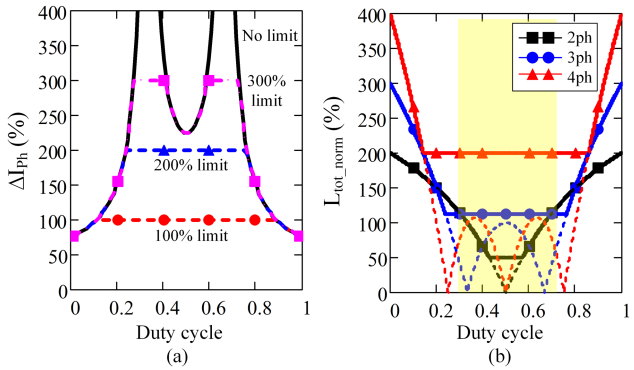


Fig. 2. Inductor analysis at $\Delta I_{Nph} = 25\%$. (a) Three-phase normalized phase current ripple $\Delta I_{Ph\%}$ at different restriction conditions. (b) L_{Tot_norm}, solid and dashed lines are with $\Delta I_{Ph\%}$ restricted at 200% and unrestricted, respectively.

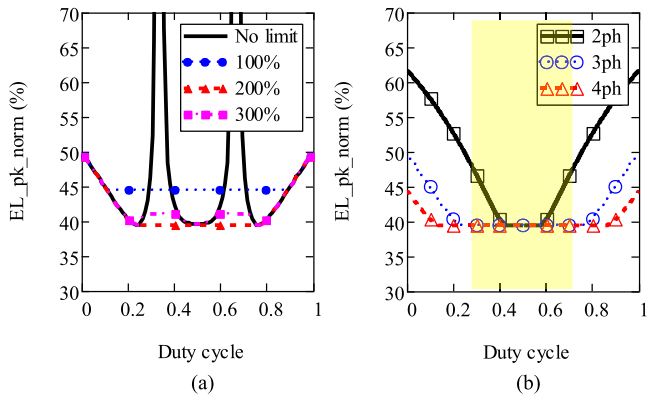


Fig. 3. Inductor analysis at $\Delta I_{Nph} = 25\%$. (a) Three-phase $E_{L\_PK\_norm}$ at different restriction conditions on ΔI_{Ph} showing 200% limit energy at minimum for the broadest duty cycle range. (b) $E_{L\_PK\_norm}$ with $\Delta I_{Ph\%}$ restricted at 200%.

inductance of

$$L_{Tot\_norm} = \frac{N_{Ph} L_{ph}}{L_{1Ph}} = \frac{N_{Ph} \Delta I_{1ph}}{\Delta I_{Ph}} = \frac{N_{Ph}^2 \Delta I_{1ph\%}}{\Delta I_{Ph\%}} \quad (5)$$

relative to a single-phase converter inductance L_{1ph}.

With the previously mentioned assumptions, for illustration L_{Tot_norm} is plotted in Fig. 2(b) for two, three, and four phases; dashed and solid lines are the calculated values with $\Delta I_{Ph\%}$ unrestricted and restricted at 200%, respectively. The effects of different levels of restriction are considered later. As a result of restriction, L_{Tot_norm} is clamped to a certain minimum value for an increasing duty cycle range as the number of phases increases. For example, L_{Tot_norm} for two, three, and four phases are restricted at a minimum of 50%, 112.5%, and 200%, respectively, of an equivalent single-phase buck. For reference, the duty cycle range corresponding to $V_{IN} = 2.5$–6.6 V and $V_{OUT} = 1.8$ V is shaded in Fig. 2(b). This restriction also affects rms and peak phase currents, as considered in Section II-B.

B. Inductor Peak Energy

Peak energy stored in an inductor is an indicator of the inductor size. As the practical inductor in a dc–dc converter is usually required to handle the worst case of operation, i.e., at peak operating current (peak flux density), the total inductor peak energy specification is found as

$$E_{L\_PK} = \frac{1}{2} N_{Ph} L_{Ph} I_{Ph\_PK}^2 \quad (6)$$

where I_{Ph_PK} is the phase current peak value; for a triangular current waveform, it is calculated as

$$I_{Ph\_PK} = \frac{I_{DC}}{N_{Ph}} \left(1 + \frac{\Delta I_{Ph\%}}{2}\right) \quad (7)$$

For normalized analysis, I_{Ph_PK} is normalized to a single-phase converter as

$$I_{Ph\_PK\_norm} = \frac{I_{Ph\_PK}}{I_{1Ph\_PK}} = \frac{2 + \Delta I_{Ph\%}}{N_{Ph}\left(2 + \Delta I_{Nph\%}\right)} \quad (8)$$

Combining L_{Tot_norm} in (5) and $I_{Ph\_PK\_norm}$ in (8), total inductor normalized peak energy is calculated as

$$E_{L\_PK\_norm} = L_{Tot\_norm}\, I_{Ph\_PK\_norm}^2 \quad (9)$$

The effect of restricted ripple current per phase on total inductor peak energy is illustrated in Fig. 3(a), where values of unrestricted and restricted total energy are compared for a three-phase interleaved buck with $\Delta I_{Nph\%} = 25\%$ as before. It is seen that the minimum peak energy is achieved with $I_{Ph\%}$ restricted to 200%, showing an optimum tradeoff between ripple current and inductance. Similar results were found for other values of N_{ph}. Therefore 200% restricted ripple current is considered for the remainder of the article. Graphs in Fig. 3(b) compare $E_{L\_PK\_norm}$ for two, three, and four phases with $\Delta I_{Nph\%} = 25\%$ and 200% restriction. Remembering that inductor peak energy E_{L_PK} is representative of inductor size, this comparison highlights the following few main points.

1) Limiting the maximum ΔI_{Ph} to 200% limits the reduction in E_{L_PK} to a minimum of 40% approximately of an equivalent single-phase design.
2) Depending on the duty cycle range, increasing N_{Ph} is not necessarily beneficial for inductor peak energy reduction and, therefore, inductor size reduction.

C. Output Capacitance Selection for Multiphase Buck Converter

This study assumes an ideal output capacitance to facilitate the derivation of normalized formulas to evaluate the interleaving effect on the output capacitance. A single output capacitance can be chosen to limit the steady-state output voltage ripple, ΔV_{OUT}, to a certain requirement. In the multiphase interleaved buck converter, steady-state output capacitance C_{Out_SS} is given by

$$C_{Out\_SS} = \frac{\Delta I_{Nph}}{8 N_{Ph} F_{Sw} \Delta V_{Out}} \quad (10)$$

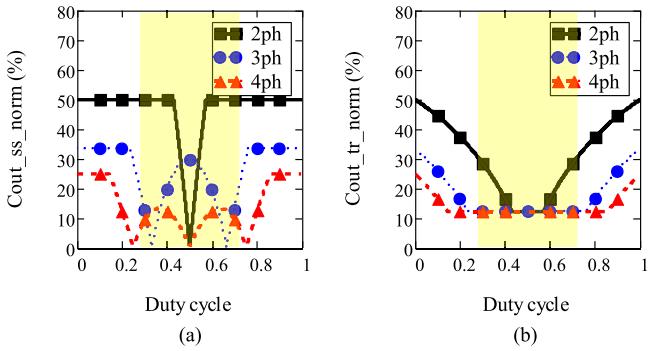


Fig. 4. Output capacitance at $\Delta I_{Nph} = 25\%$. (a) $C_{Out\_SS\_norm}$. (b) $C_{Out\_Tr\_norm}$.

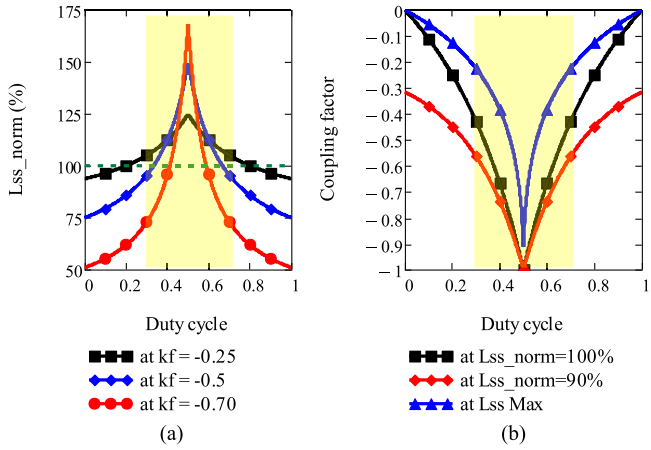


Fig. 5. Two-phase coupled inductor analysis. (a) L_{SS_norm} versus duty cycle at different k_f values. (b) k_f versus duty cycle at different L_{SS_norm} values.

Using (1) and (10), C_{Out_SS} for N_{Ph} is normalized relative to a single-phase converter

$$C_{Out\_SS\_norm} = \frac{C_{Out\_SS\_Nph}}{C_{Out\_SS\_Nph}} = \frac{\Delta I_{Nph}}{N_{Ph}\Delta I_{1ph}} = \frac{\Delta I_{Nph\_norm}\Delta I_{Ph\%}}{N_{Ph}^2\Delta I_{1ph\%}} \tag{11}$$

$C_{Out\_SS\_norm}$ in (11) is plotted in Fig. 4(a) for two, three, and four phases at $\Delta I_{Nph\%} = 25\%$. The graph shows that as long as $\Delta I_{Nph\%} = \Delta I_{1ph\%}$, then $C_{Out\_SS\_norm} = \frac{1}{N_{Ph}}$ as a result of frequency multiplication. However, when $\Delta I_{Ph\%}$ is limited to 200%, ripple cancellation may result in a further reduction in the C_{Out_SS} value as the phase inductance is increased in this region.

Another perspective of output capacitance selection is to fulfill the load transient requirement. For a buck converter with $D < 0.5$, the transition from high current I_{High} to a lower level I_{Low} results in the largest voltage deviation, where the output voltage overshoots by V_{OS}, whereas the inductor discharges (and vice versa for the transition from I_{Low} to I_{High}). So, the output capacitance may be selected to compensate for the change in inductor energy [26]. Note that considering the controller delay to respond to load change may result in $V_{US} > V_{OS}$; however, this is not the scope of this article. In the multiphase buck and assuming an ideal controller, the output capacitance for load transient requirement C_{Out_Tr} is calculated as

$$C_{Out\_Tr} = \frac{L_{Ph}\left(I_{High}^2 - I_{Low}^2\right)}{2N_{Ph}V_{OS}V_{Out}} \tag{12}$$

Then, C_{Out_Tr} is normalized to the capacitance of a single phase as

$$C_{Out\_Tr\_norm} = \frac{C_{Out\_Tr\_Nph}}{C_{Out\_Tr\_1ph}} = \frac{L_{Ph}}{N_{Ph}L_{1ph}} = \frac{L_{Tot\_norm}}{N_{Ph}^2} \tag{13}$$

$C_{Out\_Tr\_norm}$ in (13) is plotted in Fig. 4(b) for two, three, and four phases at $\Delta I_{Nph\%} = 25\%$. Comparison between Fig. 4(a) and (b) shows that limiting $\Delta I_{ph\%}$ affects $C_{Out\_Tr\_norm}$ differently to $C_{Out\_SS\_norm}$. However, understanding of C_{Out_Tr} selection is more important as it is practically much larger than C_{Out_SS}.

In practice, to maintain ΔV_{OUT} or V_{OS} within the specifications, the output capacitance value will be higher to factor for the contribution of the capacitor devices' parasitic resistance and inductance equivalent series inductance (ESL) and equivalent series resistance (ESR). However, this is not considered in this article, as the focus is on analyzing the initial design versus the number of phases.

D. Two-Phase Coupled Inductor Analysis

The basics of coupled inductor analysis are presented in [16] and [27], where negative coupling has been shown to provide potential size reduction for buck converters. Using formulae for equivalent phase inductance L_{SS} for a two-phase interleaved coupled buck converter [16], normalized steady-state equivalent phase inductance L_{SS_norm} is expressed as

$$L_{SS\_norm} = \frac{L_{SS}}{L_{Self}} = \begin{cases} \frac{1-k_f^2}{1+\frac{Dk_f}{1-D}} & D \le 0.5 \\ \frac{1-k_f^2}{1+\frac{(1-D)k_f}{D}} & D > 0.5 \end{cases} \tag{14}$$

where k_f is the coupling factor, and L_{Self} is the noncoupled self-inductance of the inductor per phase, which is considered the baseline for normalization.

Steady-state phase inductance determines the peak-to-peak phase current ripple ΔI_{Ph}. L_{SS_norm} is plotted in Fig. 5(a) at different coupling factor values; it shows areas of L_{SS} enhancement (>100%) and roll-off (<100%). It also indicates the effect of coupling on the duty cycle range for equivalent ripple operation, i.e., where $L_{SS\_norm} = 100\%$. As seen, L_{SS_norm} is impacted depending on the duty cycle and the coupling factor.

An expression for coupling factor can also be solved in terms of L_{SS_norm} using (14), which offers a better way of choosing the k_f value for a typical operating duty cycle range. The derived formula for k_f at a given value for $L_{SS\_norm} = x$ is expressed as

$$k_f\ (x, D) = \begin{cases} \frac{xD+\sqrt{D^2(x^2-4x+4)+8D(x-1)-4x+4}}{2(D-1)} & D \le 0.5 \\ \frac{xD-x-\sqrt{D^2(x^2-4x+4)+2xD-x^2}}{2D} & D > 0.5 \end{cases} \tag{15}$$

Alternatively, the coupling factor may be chosen to maximize the steady-state phase inductance, found by solving $\frac{d}{dk_f} L_{SS\_norm} = 0$. This represents the maximum L_{SS_norm} trajectory and is expressed as

$$k_{f\_Lmax} = \begin{cases} \frac{D-1+\sqrt{1-2D}}{D} & D \leq 0.5 \\ \frac{D-\sqrt{2D-1}}{D-1} & D > 0.5 \end{cases} \quad (16)$$

In Fig. 5(b), coupling factor is plotted at $L_{SS\_norm} = 100\%$ and 90%, and maximum L_{SS_norm} trajectory. Therefore, it provides a tool for selecting a suitable coupling factor for a wide duty cycle range. It shows the maximum coupling factor to maintain L_{SS_norm} at 100%, 90% or that which maximizes the phase inductance if desired. Hence, to maintain $L_{SS\_norm} \geq$ certain value, the minimum $|k_f|$ value over the operating duty cycle range should be selected. For example, for $L_{SS\_norm} \geq 90\%$ over a duty cycle range (0.27–0.72), k_f should be $\leq$ –0.527, whereas for $L_{SS\_norm} \geq 100\%$, k_f should be $\leq$ –0.375. These results ensure effective operation of the multiphase buck converter with a two-phase coupled inductor by clarifying the range of operation over which the advantage of inductance enhancement is achieved. It is acknowledged that phase-shedding for light-load management can only occur for noncoupled phases or sets of coupled phases.

E. Theoretical Analysis Summary and Guidelines

The presented theoretical analysis summarises the following points regarding choosing the number of phases in a multiphase buck converter that operates over a range of duty cycles:

1) While a multiphase buck circuit allows higher current ripple per phase than an equivalent single-phase buck, the ripple current needs to be restricted to prevent excessive rms current levels. A restriction of 200% of the dc phase current provides the lowest inductor peak energy.
2) Accounting for limited per-phase ripple current results in a minimum achievable total inductance and inductor peak energy/inductor size regardless of the number of phases. For an overall output ripple level of 25%, the minimum total inductor peak energy is found to be 40% of an equivalent single-phase inductor.
3) However, the range of duty cycle over which the minimum inductor peak energy is achieved depends on the number of phases, e.g., for $0.4 < D < 0.6$, $N_{Ph} = 2$ provides the minimum peak energy, with $N_{Ph} = 3$ applying for $0.2 < D < 0.4$, etc., as shown in Fig. 3. Note that ideally, a phase count of 4 would be recommended for $D = 0.25$, but not in this case.
4) Similar trends are observed for the output transient capacitance when the inductor ripple current is restricted, i.e., the minimum capacitance is limited to the same value regardless of phase count, and the range of duty cycle at which the minimum is achieved increases with phase count.
5) Coupling factor in a wide duty cycle coupled inductor should not exceed a certain value to avoid degradation of steady state phase inductance, which can result in unexpected phase current increase.

Overall, for minimizing the passives size, the full range of operating duty cycle needs to be considered and the minimum phase count corresponding to the minimum inductor and capacitor peak energies over this range should be chosen. This is illustrated in a demonstrator design in the following.

TABLE I
CONVERTER DESIGN SPECIFICATIONS

Symbol	Quantity	Value	Unit
F_{SW}	Switching frequency	20	MHz
V_{IN}	Input voltage	2.5–6.6	V
V_{OUT}	Output voltage	1.8	V
I_{DC}	Output DC current	3	A
ΔI_{Nph}	Output current ripple	0.75 (25%)	A
ΔV_{OUT}	Output voltage ripple	90 (5%)	mV
V_{OS}	V_{OUT} overshoot	90 (5%)	mV
I_{Low} to I_{High}	Load transient	0–3	A

III. DEMONSTRATOR CONVERTER DESIGN

The considered converter specifications are listed in Table I, which is a typical point-of-load step-down specification for battery-powered applications. For this specification, the duty cycle ranges from 0.27 to 0.72, assuming ideal converter components; this is the same range as indicated by shading in Section II results. This study is a part of a project focused on integrated dc–dc converters with a 10–100 MHz switching frequency range, so the switching frequency is chosen at 20 MHz considering achievable PCB parasitic interconnect inductances.

The normalized analysis of Section II is useful to understand the theoretical impact of interleaving on passive components versus duty cycle while limiting the maximum limit of $\Delta I_{ph\%}$. However, the real converter design accounts for the maximum required values over the operating duty cycle range, which this section considers. The required inductance in a single-phase buck converter is always higher at a lower duty cycle, but this does not necessarily apply to the multiphase converter as the maximum required inductance can be found somewhere in the middle of the duty cycle range. This is considered in the design procedure, i.e., summarized in the flowchart in Fig. 6. The design procedure in Fig. 6 starts by setting the converter specifications, and then ΔI_{Ph} (1)–(3) is calculated over the range of duty cycle at each N_{Ph} value and maintained $\leq 2I_{Ph\_DC}$. Then, other parameters are calculated, mainly L_{Ph}, which is required to calculate I_{Ph_PK}, E_{L_PK}, and C_{Out_Tr}. L_{Ph} and k_f are also calculated for the inductor design in the following section. Then ΔI_{Nph} value is updated to get its maximum value to estimate C_{Out_SS}.

Based on the previously explained design procedure, passives analysis is presented in Fig. 7 for converter specifications in Table I at $\Delta I_{ph} \leq 2I_{Ph\_DC}$ and unrestricted ΔI_{ph}. Results in Fig. 7(a) show that for $N_{ph} > 3$, total inductance continues to increase with increasing phase count due to limiting the maximum ΔI_{ph} to 200%. Inductor peak energy at $\Delta I_{ph} \leq 2I_{Ph\_DC}$ in Fig. 7(b) reduces to a minimum and remains constant for more

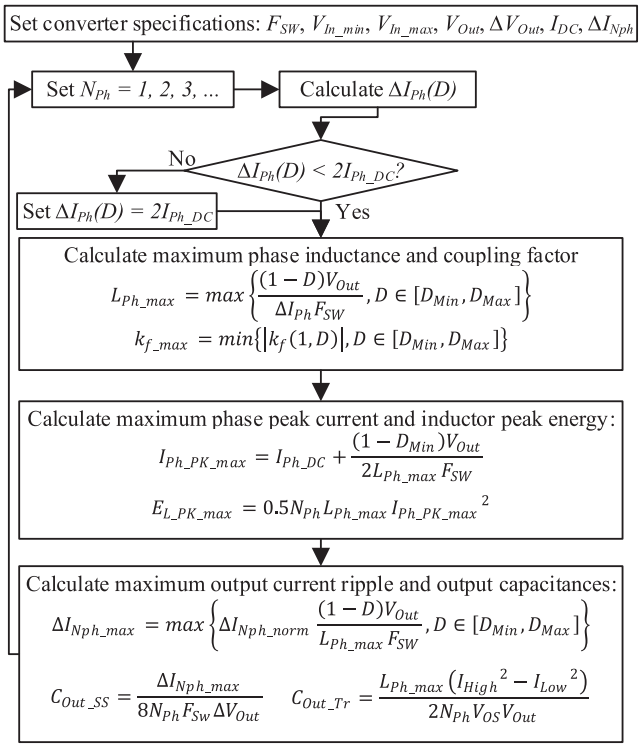


Fig. 6. Design procedure of multiphase buck converter.

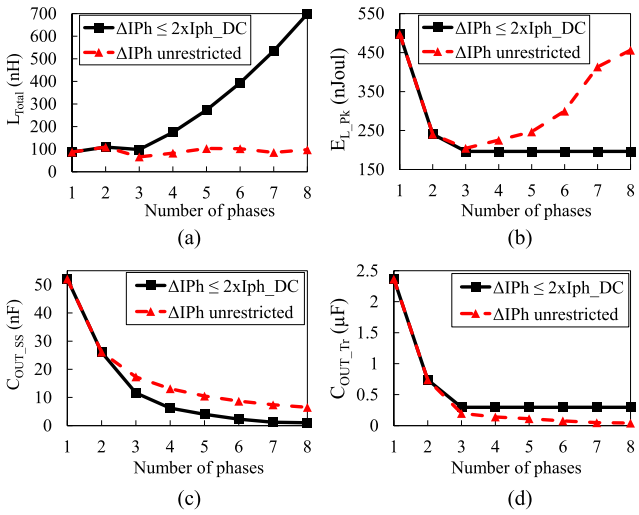


Fig. 7. Passives' analysis versus N_{Ph} for converter specification listed in Table I at $\Delta I_{Ph} < 2\times$ and $100\times$ $2I_{Ph\_DC}$,$100\times$ limit is considered the unrestricted ΔI_{Ph} case: (a) L_{Tot}, (b) E_{L_PK}, (c) C_{Out_SS}, and (d) C_{Out_Tr}.

than three phases. However, the percentage energy reduction relative to a single phase is more significant for two phase (at 48.4%) than three phase (at 39.5%). Results with unrestricted ΔI_{ph} in Fig. 7(a) and (b) show that while L_{Tot} does not increase with N_{Ph} increase, E_{L_PK} increases significantly.

The two-phase option offers a better overall solution considering the additional space and circuit complexity required for extra phases of switches and control, which correlates with the normalized analysis predictions in Fig. 3(b).

Fig. 7(c) and (d) shows the normalized output capacitance for the steady-state ripple requirement $C_{Out\_SS\_norm}$ and load transient requirement $C_{Out\_Tr\_norm}$. As $C_{Out\_Tr\_norm} >> C_{Out\_SS\_norm}$, the reduction in $C_{Out\_Tr\_norm}$ is more important. For two phase, $C_{Out\_Tr\_norm}$ is 0.74 μF (31.25%) and remains at 0.3 μF (12.5%) for three phase and higher, which correlates with the normalized analysis in Fig. 4(b). While a reduction in capacitance is welcomed, the capacitors' size is usually much smaller than inductors. Therefore, the optimum phase count is usually determined by the inductor size.

In terms of two coupled inductors, a suitable coupling factor (k_f) is determined with the aid of Fig. 5(b). For the converter duty cycle range from 0.27 to 0.72, the maximum k_f is –0.37 to prevent steady-state phase inductance from rolling off to below 100%. So, this restriction must be considered in the coupled inductors design. With a coupling factor of –0.37, the application of (14) shows that L_{SS_norm} varies between a minimum of 100% to a maximum of 137% based on the operating duty cycle.

IV. PCB Inductor Design

Fig. 7 explains the impact of increasing the number of phases in terms of passives. However, these relative results may differ from the actual inductor size when manufacturing capabilities and limitations are included, which is discussed in this section. For the prototype design, spiral and solenoid air-core inductors on FR4 double layer PCB are considered. The PCB manufacturing capabilities include a copper thickness of 35 μm, minimum trace and gap width of 0.15 mm, minimum via diameter of 0.2 mm, and PCB height of 1.6 mm. To minimize inductor size, the conductor width for the inductor is calculated according to the Standard IPC-2221A [28] for a temperature rise of 50 °C. However, future work can use the newer standard IPC-2152 [29], [30]. Conductor trace width is practically chosen to meet specific resistance requirements according to the allowable overall inductor power loss.

These assumptions determine the conductor width for a phase inductor, i.e., 0.52 mm in single phase and 0.21 mm in two phase. However, for solenoid inductors, the minimum via-to-via distance (including the surrounding annular ring and solder mask) results in extra space utilized to increase the minimum conductor width to 0.37 mm, which improves the inductor dc resistance. This shows how PCB design rules impose a limiting factor on PCB inductor size reduction.

A. PCB Spiral Inductor Design

The spiral inductor inductance is calculated as in [31]

$$L_S = 0.5\mu_0 N_{Layers} N_T^2 Dia_{Avg}\left(\ln\left(\frac{2.46}{P}\right) + 0.2P^2\right) \quad (17)$$

where μ_0 is the air permeability $\mu_0 = 4\pi 10^{-7}$, N_T is the number of turns, N_{Layers} is the number of the PCB series-connected layers, Dia_{AVG} is the average spiral diameter $Dia_{Avg} = 0.5(Dia_{Out} + Dia_{In})$, and P is the spiral fill factor

$$P = \frac{Dia_{Out} - Dia_{In}}{Dia_{Out} + Dia_{In}} = \frac{1 - Dia_{Ratio}}{1 + Dia_{Ratio}} \quad (18)$$

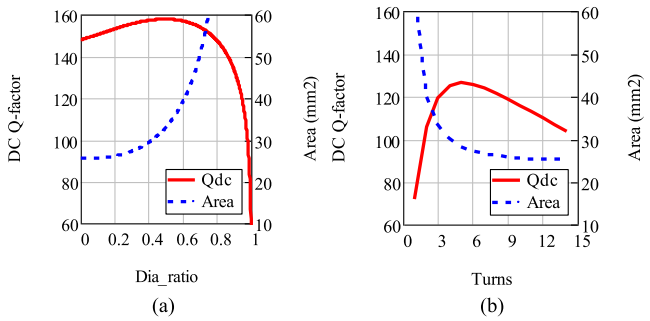


Fig. 8. $Q_{\rm DC}$ and inductor area for single-phase 90 nH double layer inductor designs with $W_C = 0.52$ mm and $S_C = 0.15$ mm. (a) Spiral. (b) Solenoid.

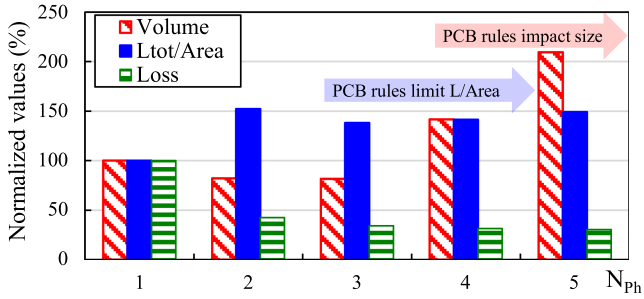


Fig. 9. Multiphase solenoid inductor design in terms of peak energy, volume, and loss normalized to single-phase inductor.

where $Dia_{Ratio} = Dia_{In} / Dia_{Out}$, which is the inner to outer diameter ratio. Then, the spiral inductor inductance is analyzed as a function of Dia_{Ratio}.

DC resistance of the spiral inductor is calculated as

$$R_{\rm DC} = \frac{\rho N_{Layers} \ell_{Spiral}}{W_C T_C} \tag{19}$$

where ρ is the copper conductivity 1.72×10^{-8} Ωm, ℓ_{Spiral} is the spiral inductor length per layer, and W_C and T_C are the conductor width and thickness, respectively, for a rectangular cross-sectional conductor. ℓ_{Spiral} is derived and expressed as

$$\ell_{Spiral} = \int_0^{2\pi N_T} \sqrt{\left(R_{In} + \frac{W_C}{2} + \frac{W_C + S_C}{2\pi}\theta\right)^2 + \left(\frac{W_C + S_C}{2\pi}\right)^2} d\theta \tag{20}$$

where R_{In} is the inner radius and S_C is the conductor spacing.

Then, the inductor dc quality factor is calculated as

$$Q_{\rm DC} = \frac{2\pi F_{SW} L_S}{R_{\rm DC}}. \tag{21}$$

With the aid of the previous formulas, the spiral inductor is analyzed versus Dia_{Ratio}. Fig. 8(a) shows the analysis for a single-phase double-layer 90 nH spiral inductor in terms of $Q_{\rm DC}$ and footprint area as a design example for the single-phase converter in Table II. Dia_{Ratio} was chosen at 0.3155 for this single-phase 90 nH inductor as a balanced point where $Q_{\rm DC}$ (156) is slightly close to the peak value (158), and the inductor area (35.1 mm^2) is close to the minimum value (32.7 mm^2), this balance is reflected on $Q_{\rm DC}$/*Area* value.

B. PCB Solenoid Inductor Design

Based on the solenoid inductance basic equation, the PCB solenoid inductance is calculated approximately as

$$L_S = \frac{\mu_0 N_T^2 \left(W_{Sol} - 2D_{Via}\right)\left(H_{Sol} - 2T_C\right)}{\left(N_T + 1\right) W_C + N_T S_C} \tag{22}$$

where D_{Via} is the PCB via diameter, and W_{Sol} and H_{Sol} are the inductor's overall width and height.

DC resistance of the solenoid inductor is calculated as

$$R_{\rm DC} = \left(N_T + 1\right) R_{DC\_st} + N_T \left(R_{DC\_dia} + 2R_{DC\_via}\right) \tag{23}$$

where R_{DC_st}, R_{DC_dia}, and R_{DC_via} are dc resistances of straight conductors, diagonal conductors, and PCB via, respectively.

Inductor design analysis regarding footprint area and $Q_{\rm DC}$ is presented in Fig. 8(b) versus the number of turns for a single-phase 90 nH solenoid. As shown in Fig. 8(b), at a small number of turns, $Q_{\rm DC}$ is small, and the inductor area is large; so, for this design, the turns count should not be less than 5. For the prototype single-phase 90 nH inductor design of Table II, a six-turns design is suitable. At $N_T = 6$, $W_C = 0.52$ mm and $S_C = 0.15$ mm, a 90 nH solenoid has $Q_{\rm DC} = 126$ and area = 28.6 mm^2 approximately.

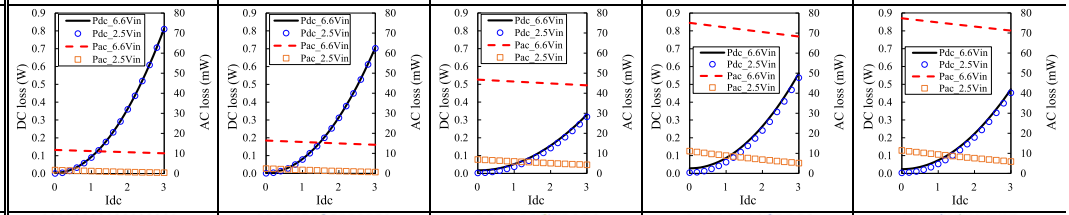
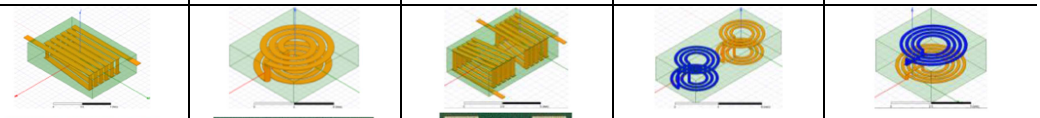
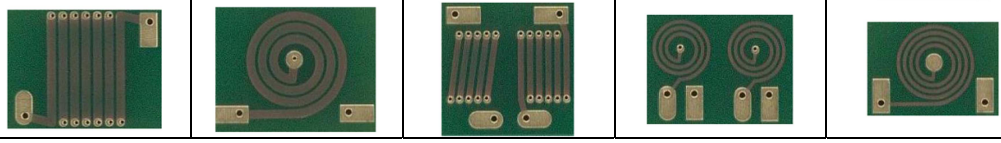
C. PCB Inductor Implementation

Using the procedure described in Section IV-B, a range of solenoid inductors were designed for $N_{Ph} = 1$–5 as presented in Fig. 9. While results of E_{L_Pk} in Fig. 7 suggest that a reduction in inductor size should be achieved, due to the PCB manufacturing limitations, inductor size increases for $N_{Ph} > 3$, and further loss reduction is insignificant. Besides, the maximum inductance density was achieved at two phase with no benefit achieved by adding more phases. Therefore, $N_{Ph} \geq 3$ inductors were discarded from implementation and testing.

Details of the selected inductor designs and finite-element analysis (FEA) simulation results are compared in Table II. FEA simulation was done at a low frequency (1 Hz) to verify L_S, $R_{\rm DC}$, and coupling factor values. These results show good agreement (<10%) with the calculation models presented in Section IV. However, a more accurate analytical model may be required for higher frequencies, as in [32]. Single- and two-phase versions of spiral and solenoid inductors were designed for comparison as described in Section II. One coupled spiral design was considered.

Inductor dc and ac losses were extracted from spice simulation at $V_{IN} = 2.5$ and 6.6 V based on measured $R_{\rm DC}$ and $R_{\rm AC}$ and are presented in Table II. It shows that two-phase compared to single-phase inductors generally have lower dc loss. For two-phase inductors, ac loss is significantly higher at $V_{IN} = 6.6$ V due to higher ripple current, so this predicts a lower light load

TABLE II
SELECTED INDUCTORS' DESIGNS

Design		1Ph_Sol	1Ph_Spi	2Ph_Sol	2Ph_Spi1	2Ph_Spi2
No of phases		1	1	2	2	2
Inductor type		Solenoid	Spiral	Solenoid Axial	Spiral Side by side	Spiral Axial (coupled)
L_{Ph} (nH)		90	90	54.3	54.3	54.3
I_{Ph_DC} (A)		3	3	1.5	1.5	1.5
Calc	R_{DC} (mΩ)	90	72.6	57	106	93
	Area* (mm^2)	28.6	35.1	26	25.6	19.8
	Q_{DC}	126	156	122	64	73
FEA 1 Hz	L_S (nH)	92.7	96.9	55.5	56.9	57.1
	R_S (mΩ)	82	71	63	108	96
	k_f	–	–	–0.024	–0.015	–0.2
	Q at F_{SW}	143	170	110	66	75
Measured R_{DC}, R_{AC} at F_{SW} (mΩ)		90, 266.7	78, 372.1	70, 193.2	119, 310.3	100, 319.5
Inductor loss based on measured R_{DC} and R_{AC} at V_{IN} = 2.5 and 6.6 V						
FEA model						
Manufactured PCB inductors						

*Two-phase inductor geometry considers 1 mm horizontal spacing between inductors; this distance is also considered in overall inductors area.

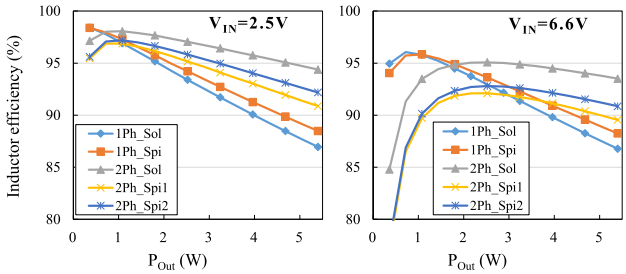


Fig. 10. Calculated inductor efficiency based on measured R_{DC} and R_{AC}.

efficiency at higher V_{IN} values. Accordingly, inductor efficiency versus output power is presented in Fig. 10

$$Ind\,efficiency = \frac{P_{Out}}{P_{Out} + P_{Ind\_Loss}} \tag{24}$$

For single-phase converter designs, the spiral inductor full load efficiency is only 1.53% and 1.47% higher than the solenoid inductor at V_{IN} of 2.5 and 6.6, respectively; however, its area is 21% bigger than the solenoid one. This means a single-phase solenoid inductor utilizes area better than a single-phase spiral inductor on a double layer PCB considering the same manufacturing constraints.

Comparing the two-phase spiral and solenoid designs shows that the solenoid design is more efficient for approximately the same inductor footprint area. Fig. 10 indicates that the two-phase solenoid inductors (2Ph_Sol) have the best overall efficiency over the output power range starting from 0.36 W at 2.5 V_{IN} and from 1.8 W at 6.6 V_{IN}. It achieved a maximum inductor efficiency of 97.2% and 92.8%, and full load inductor efficiency of 92.2% and 90.9% at V_{IN} of 2.5 and 6.6 V, respectively.

Concerning coupling, it was found that the two-phase coupled spiral inductor 2Ph_Spi2 (with $k_f = 0.2$) achieved 1.3% higher inductor efficiency at full load, with 22.7% smaller area (i.e., 19.8 mm^2) compared to the noncoupled spiral (2Ph_Spi1). The 2Ph_Spi2 configuration has an opposing spiral on each layer, which results in partial field cancellation and better electromagnetic interference (EMI) performance than single-phase spiral, known to cause noise radiation [33]. However, detailed EMI performance is not in the scope of this article. The coupling factor of 0.2 was set by the inductor geometry, determined by the PCB manufacturing rules. While this is lower than the recommended value of 0.37, it still results in up to 20% increase in steady-state inductance, resulting in up to 20% reduction in peak-to-peak phase current ripple, and therefore ac losses.

V. CONVERTER MODELING AND MEASUREMENTS

This section investigates the converter's performance with the designed and manufactured single- and two-phase solenoid and spiral inductors presented in Section IV. Converters are based

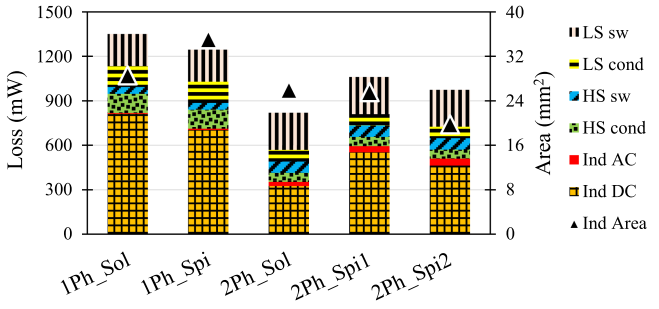


Fig. 11. Calculated full load loss breakdown at $V_{IN} = 4.5$ V and inductor area.

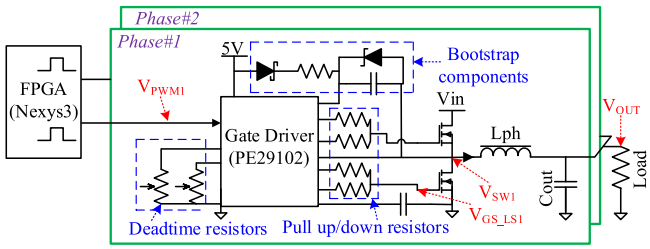


Fig. 12. Circuit schematic of the prototype converter.

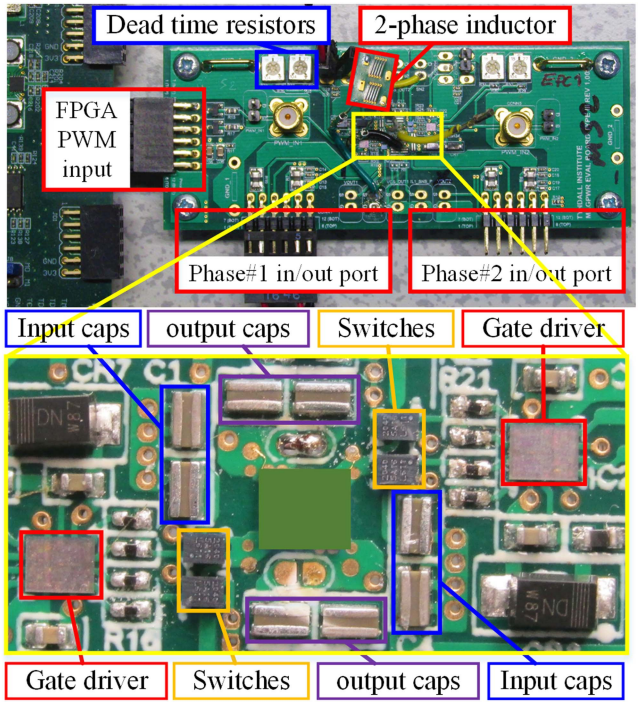


Fig. 13. Picture of the prototype converter.

on EPC2040 GaN FET switches [34] used for each phase's high and low sides. The EPC2040 is rated for 15 V and 3.4 A, and it has a total gate charge of 745 pC, which makes it a good candidate for a 20 MHz switching frequency.

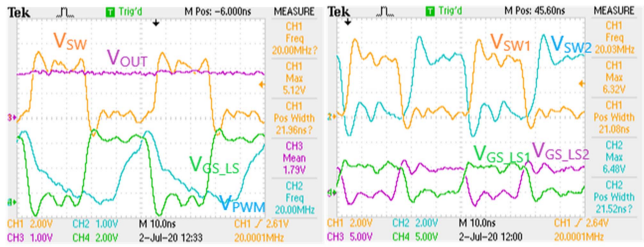
A. Calculated Loss Breakdown

Fig. 11 shows a comparison of the inductors area and the calculated converter loss breakdown at a full load of 5.4 W and nominal V_{IN} of 4.5 V. The converter losses calculations are based on data for EPC2040 switches [34] and formulas guidelines in [35], and inductor loss is calculated as in Table II. In Fig. 11, the single-phase converters' FETs have higher conduction loss and lower switching loss than two-phase converters due to using the same switches for all cases. It may be an unfair comparison, but this is because EPC2040 is the lowest rated and smallest GaN FET so far in the market making it the most suitable FET for 20 MHz operation.

In Fig. 11, 2Ph_Sol achieves the smallest overall loss (0.82 W), mainly due to inductor conduction loss reduction while having nearly the same overall area as other two-phase inductors. The coupled configuration 2Ph_Spi2 design achieves a smaller overall loss (85.3 mW less) with a smaller inductor area (5.8 mm^2 less) against the noncoupled 2Ph_Spi1.

B. Simulation and Measurements

Figs. 12 and 13 present the prototype converter schematic and picture indicating the components. The EPC2040 switches are driven by a Peregrine PE29102 gate driver, capable of 40 MHz [36]. The pulsewidth modulation (PWM) input signal is generated using a DIGILENT Nexys3 field-programmable gate array (FPGA) development board, i.e., Xilinx Spartan-6



(a) (b)

Fig. 14. Testing waveforms at 20 MHz, $V_{IN} = 4.5$ V, $V_{OUT} = 1.8$ V. (a) Single-phase FPGA PWM signal to the gate driver (V_{PWM}), low side FET V_{GS}, V_{SW}, V_{OUT}. (b) Two-phase low side FETs V_{GS}, V_{SW}.

LX16 FPGA chip. The FPGA was programmed to generate a 20 MHz signal with the duty cycle adjusted externally. The deadtimes during rising and falling are adjusted manually using external variable resistors, as shown in Fig. 12, to minimize the overshoot/undershoot in the switching voltage V_{SW} signal. The load is an electronic resistive load, so the output current is reflected in the V_{Out} signal.

Measured waveforms for single- and two-phase operations are shown in Fig. 14. Although the PCB parasitic effects on the FPGA signal (V_{PWM}) in Fig. 14(a), it does not affect the gate driver operation as seen in V_{GS_LS} signal. Fig. 14(a) and (b) also shows reasonable V_{SW} overshoot/undershoot values. Induced interference voltages were created in the ground loop of the voltage probes. However, for efficiency measurements, no voltage probes were attached to reduce the effect of the oscilloscope's added capacitances and ground loops to the circuit.

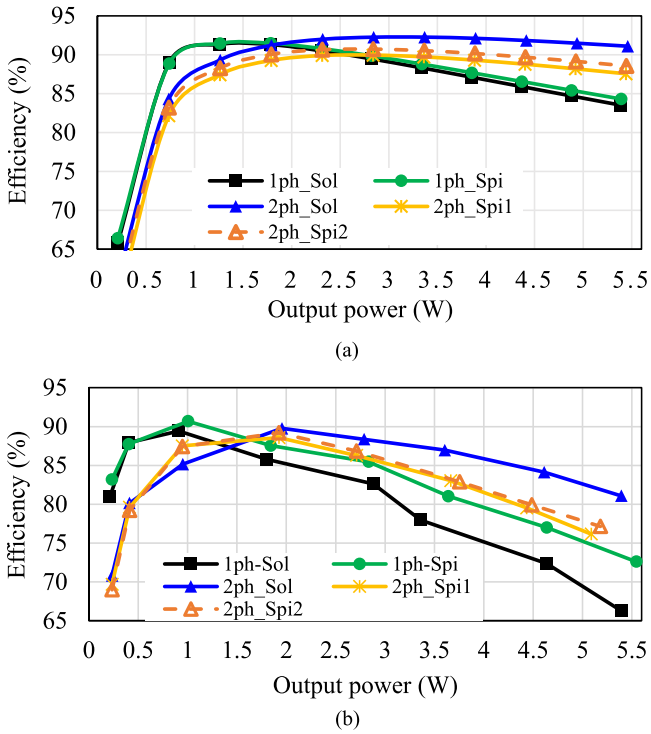


Fig. 15. Converter efficiency at $V_{IN} = 4.5$ V. (a) Simulation. (b) Measured.

Efficiency was measured in terms of dc voltage and current at the converter input and output.

Simulation and measured converter efficiencies are shown in Fig. 15(a) and (b), respectively, at the nominal $V_{IN} = 4.5$ V, $V_{OUT} = 1.8$ V, and $F_{SW} = 20$ MHz. Converter simulation was performed with LTspice software, including EPC2040 spice models. Deadtimes between high and low side gate driver signals were tuned in the simulation to reduce overall switching loss. Measured efficiency was adjusted to account for the dc losses in the inductor interconnecting wires (20 mΩ / phase approximately).

Fig. 15 shows a good match between the simulation and measured converter efficiency at light loads and the trend in relative efficiency for different inductors; however, there is a mismatch that increases with the load increase. There are possible reasons for this, e.g., PCB parasitic effects, the near field radiated losses from the air-core inductors, the impact of the high switching frequency or temperature on the GaN FETs dynamic resistance, as described in [37] and [38] (but not yet characterized for EPC2040), or the common source inductance in the gate driver loop [35], which will be investigated further in future work. Nonetheless, the two-phase converter with the noncoupled solenoid inductors (2Ph_Sol) has a better efficiency curve than other configurations, correlating with the results trend in Fig. 10, whereas there is a slight improvement provided by coupled versus noncoupled two-phase spiral inductors.

Table III presents that the implemented inductors achieved high inductance density and high L_{Ph}/R_{DC} compared with other converters that employed air-core inductors in buck topology. This results from the proposed design procedure to optimize the number of phases selection and the inductor design procedure to choose the optimum design point to maximize Q_{DC} while minimizing the inductor area.

TABLE III
COMPARISON WITH CONVERTERS THAT EMPLOYED AIR-CORE INDUCTORS IN BUCK TOPOLOGY

Reference	[39] Single turn	[3] Spiral	[2] Solenoid	This work	
				2Ph_Sol	2Ph_Spi2
Inductor technology	Co-packaged	On-chip 65nm	Co-packaged	PCB Two layers	
N_{Ph}	1	2	4	2	
V_{IN} (V)	1.7	2–2.2	1.6	2.5–6.6	
V_{OUT} (V)	1	0.7–1.2	1.1	1.8	
I_{DC} (A)	0.8	0.7	4.4	3	
F_{SW} (MHz)	200	500	150	20	
$L_{Total}/Area$ (nH/mm^2)	0.68	8.6	1.97, 0.93	4.18	5.48
L_{Ph}/R_{DC} (nH/mΩ)	0.656	0.0053	0.14, 0.1	0.88	0.6

VI. CONCLUSION

A detailed normalized analysis of passives in multiphase interleaved buck converter is presented in terms of total inductance and output capacitance for steady-state and load transient requirements considering wide input voltage converter specifications and phase current ripple limitations. The analysis shows that for a wide input voltage range specification and maintaining positive phase currents, the passive components' peak energies will be reduced by increasing phase count to a certain number, beyond which there are diminishing returns.

Increasing the number of phases above this number is not necessarily going to reduce the size of the passive components, where the total peak inductor energy achieves a minimum value due to the restriction on per phase current ripple. Unrestricted phase current ripple would cause both increasing total inductor peak energy and increasing rms losses with phase count. A straight-forward analytical procedure is proposed to analyze the passives in a multiphase buck converter for wide input voltage, which helps determine the optimum number of phases.

This article builds on the previous coupled inductor literature by presenting a coupling factor selection guideline to either maintain or maximize the phase inductance over noncoupled inductors, which is applicable to the case of wide operating duty cycle range.

For experimental validation, air-core PCB inductors were employed to exclude the complexity of nonlinear core losses. The inductors were designed considering standard PCB manufacturing capabilities and a target temperature rise. The study shows that different inductor geometries affect the inductor efficiency and footprint area. For both solenoid and spiral, the implemented 20 MHz converter confirms the predicted trends of two-phase inductors offering lower area and higher efficiency compared to equivalent single-phase inductors.

Comparison against other literature is difficult because of different converter electrical specifications, switching frequency, and packaging technologies. However, this work indicates that the combination of the optimum choice of the number of phases

and the PCB inductor design in our prototype resulted in an impressive combination of inductance densities and dc resistances for air-cored PCB-based inductors.

ACKNOWLEDGMENT

The authors would like to acknowledge Dermot Dobbyn at Tyndall National Institute for his effort in the layout of the prototype converter board.

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