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RESEARCH ARTICLE

Frequency-Dependent Characteristics and Parametric Modeling of the Silicon Substrate in TSV-Based 3-D ICs

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ABSTRACT This paper presents an in-depth investigation of the silicon substrate characteristics based on frequency-dependent parameters in the through-silicon via (TSV)-based 3-D ICs. It is the first time to define the frequency bands accurately on the ground of a quantitative standard of calibration to represent different characteristics of the silicon substrate. Moreover, by converting the conventional model of a TSV pair into an *RC* parallel circuit, a simplified model is established which makes the analysis of the silicon substrate concise associated with the frequency variation. To further reveal the influence of silicon substrate on the signal transmission between adjacent TSVs, relevant impedance parameters of the silicon substrate are converted into the impedance (Z) matrix for parametric modeling, which is validated by 3D full-wave simulations. This work contributes a systematic examination of the silicon substrate characteristics with the variation of frequency, and provides significant guidance for parametric analysis and modeling in TSV-based 3-D ICs.

INDEX TERMS Silicon substrate, frequency-dependent parameters, through-silicon via, frequency bands, parametric modeling, 3-D ICs.

I. INTRODUCTION

Owing to growing concerns about traditional planar integrated circuits (ICs) suffering from a bottleneck of integrating the every-increasing transistors with a single package, the 3-D system integration with chiplets has emerged as a promising solution to embody the intrinsic value of ''More-than-Moore'' by dividing a monolithic system-on-chip (SoC) into several functional blocks and then interconnecting them, thus achieving highly heterogeneous integrations [1], [2]. An important strategy greatly contributing to the promotion of 3-D system integration with chiplets is the through-silicon via (TSV), which vertically interconnects the stacked dies, and naturally paves a path to the next-generation heterogeneity [3], [4]. With such features, the TSV-based 3-D ICs have been further developed with shorter chip-chip interconnect lengths, reduced power consumptions, and maximized I/O numbers with a small area overhead [5].

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As the vertical interconnections provided by TSVs pass through the silicon substrate, the performance of the 3-D ICs suffers from serious signal losses especially at higher frequency, including the crosstalk, the simultaneous switch nose, and the electromagnetic interference [6]. Due to the highly vertical integration density, these losses are generally induced by the parasitic effects of TSV as well as the inherent loss of silicon substrate [7], [8]. To deal with these issues, various TSV configurations including the ground-signal (GS) and the ground-signal-ground (GSG) have been extensively studied based on lumped circuit models [9], [10], [11], [12], [13], trying to analyze the TSV electrical parasitics in detail such as their resistance, inductance, capacitance, and conductance (*RLCG*). Moreover, the slow-wave, skin-effect, and dielectric quasi-TEM modes have been taken into account to examine the TSV and signal transmission characteristic at high frequency [14], and the distributed circuit model utilizing the multi-segment *RLC* networks has also been presented to investigate the frequency-dependent properties of TSVs [15]. Additionally, it is known that the use of

differential signal is an effective way to guarantee the signal integrity [16], [17], [18], and one of the most commonly used differential TSV configurations is the ground-signal-signal-ground (GSSG)-type TSV, which has been established, validated and manufactured [19]. Another effective solution for vertical signal transmission is to use the coaxial TSV for interconnections, which can suppress the noise decoupling significantly. While this coaxial structure requires special manufacturing process for the out metal ring, which is justified only for demanding applications [20].

Up to now, no prior studies have been reported to provide a comprehensive understanding of the core physics of the silicon substrate considering the frequency variation in TSV-based 3-D ICs. The purpose of this paper is to fill the blank of dividing the frequency bands of the silicon substrate based on a definite standard according to its frequency-dependent characteristics, and present a methodology for accurate parametric modeling of the silicon substrate in the preliminary design stage. The rest of this paper is organized as follows. Section II proposes two important frequency-dependent parameters, including the transition frequency f_T and the standard of calibration $Z_{C_{Si}}/Z_{R_{Si}}$. By virtue of these two proposed parameters, the frequency bands which capture the silicon substrate characteristics can be defined quantitatively. Section III describes a parametric modeling approach with fewer parameters required to reveal the influence of silicon substrate on the signal transmission in TSV-Based 3-D ICs, and the established model is validated by comparing with simulated results over a wide frequency range. Finally, the conclusion is drawn in Section IV.

II. FREQUENCY-DEPENDENT PARAMETERS

A. TRANSITION FREQUENCY f_T: A TURNING POINT WHERE THE SILICON SUBSTRATE CHARACTERISTIC CHANGES

As the TSV embedded in the silicon substrate plays the role of electrical interconnection between vertically-stacked dies, it is helpful to apply the Maxwell's Equation to investigate the electrical characteristics of the silicon substrate, in which the current density $\vec{J}_{Si}$ can be derived as

$$\nabla^2\vec{J}_{Si} = j\omega\mu\sigma_{e,\,Si}\vec{J}_{Si}, \tag{1}$$

where ω stands for the angular frequency, μ the vacuum permeability. $\sigma_{e,Si}$ in (1) is the effective conductivity of silicon, given as

$$\sigma_{e,\,Si} = \sigma_{Si} + j\omega\varepsilon_{Si}\varepsilon_0, \tag{2}$$

where σ_{Si}, ε_{Si}, ε_0 are the conductivity, relative permittivity of silicon substrate, and the absolute dielectric permittivity, respectively. According to Ampere's law [21], (2) can be expressed as the numerator of the loss tangent of silicon substrate as

$$\tan\delta_{Si} = \frac{\sigma_{Si} + \omega\varepsilon''}{\omega\varepsilon'}, \tag{3}$$

where $\varepsilon' = \varepsilon_{Si}\varepsilon_0$, which is the permittivity of silicon substrate, and ε'' is the imaginary part of ε'. It is also seen from (2) that $\sigma_{e,Si}$ can be divided into two parts, the real (σ_{Si}) part and the imaginary ($\omega\varepsilon_{Si}\varepsilon_0$) part, shown as

$$\sigma_{Si} = \text{real}\left(\sigma_{e,\,Si}\right), \tag{4}$$

$$\omega\varepsilon_{Si}\varepsilon_0 = \text{imag}\left(\sigma_{e,\,Si}\right). \tag{5}$$

When the real part (4) is equal to the imaginary part (5), a transition frequency f_T is derived, which is defined as a turning point where the characteristic of the silicon substrate changes, and f_T is the first frequency-dependent parameter we propose in this paper, shown as

$$f_T = \frac{\sigma_{Si}}{2\pi\varepsilon_{Si}\varepsilon_0}. \tag{6}$$

Here, it should be pointed out that f_T is similar with the cutoff frequency in an RC circuit given as $f = 1/(2\pi RC)$, which is a special frequency used to describe the frequency characteristics of the RC circuit [22]. To describe f_T in a way the same as the cutoff frequency, we can easily get the expression below

$$R_{Si}C_{Si} = \frac{\varepsilon_{Si}\varepsilon_0}{\sigma_{Si}}. \tag{7}$$

It is evidently seen that the σ_{Si} and $\varepsilon_{Si}\varepsilon_0$ discussed above are correlated with the resistance and capacitance in the silicon substrate, which indicates that the nature of the silicon substrate will be influenced by the ratio of $\varepsilon_{Si}\varepsilon_0$ to σ_{Si} under the condition of frequency change. When $\omega\varepsilon_{Si}\varepsilon_0$ is considerably smaller than σ_{Si}, the silicon substrate exhibits more like a resistive medium. On the other hand, the silicon substrate will behave as a dielectric medium than a lossy resistance when $\omega\varepsilon_{Si}\varepsilon_0$ is far greater than σ_{Si}.

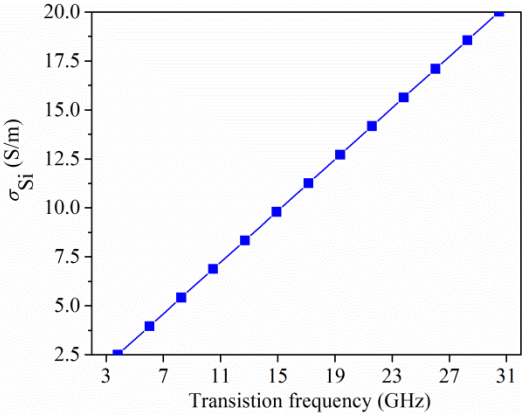

FIGURE 1. Conductivity of silicon substrate as a function of transition frequency f_T.

To further clarify the definition of the proposed f_T, the conductivity of silicon substrate σ_{Si} as a function of transition frequency f_T is calculated based on (6), as shown in Fig. 1. In the calculation, the permittivity of silicon substrate $\varepsilon_{Si}\varepsilon_0$ is set to be $11.8 \times 8.85 \times 10^{-12}$ F/m, and σ_{Si} is considered to be obtained in a range from 2.5 S/m to 20 S/m in order to cover the range of conductivities for commercial silicon substrates. As can be seen, σ_{Si} gets larger linearly with increasing f_T. It is worth to mention that f_T depicted in Fig. 1 is actually

not the operating frequency of the 3-D IC, and f_T just stands for a turning point that distinguishes between the resistive and the dielectric nature of the silicon substrate [22]. For example, σ_{Si} is increased to 15 S/m with f_T of 22.86 GHz compared to 10 S/m with f_T of 15.24 GHz, which indicates the larger σ_{Si} chosen, the higher the frequency up to which the silicon substrate will behave like a resistive medium. This proves that changing of σ_{Si} can determine the frequency bands with different characteristics of the silicon substrate, and this provides great convenience for the substrate design, as different values of σ_{si} can be obtained easily by varying the doping concentration of the substrate. However, exact frequency bands representing different characteristics of the silicon substrate are unable to be achieved for lacking of accurate quantitative analysis. Therefore, a quantitative standard of calibration with respect to the ratio of $\varepsilon_{Si}\varepsilon_0$ to σ_{Si} as well as the frequency variation should be established, which will be discussed in the following part.

B. IMPEDANCE RATIO OF C_{Si} TO R_{Si}: A QUANTITATIVE STANDARD OF CALIBRATION

Herein, based on (7), the ratio of $\varepsilon_{Si}\varepsilon_0$ to σ_{Si} can be equivalently converted into the impedance ratio of C_{Si} to R_{Si} ($Z_{C_{Si}}/Z_{R_{Si}}$), and thus we can have the following

$$\frac{Z_{C_{Si}}}{Z_{R_{Si}}} = \frac{1}{\omega} \cdot \frac{\sigma_{Si}}{\varepsilon_{Si}\varepsilon_0}. \tag{8}$$

As can be seen, $Z_{C_{Si}}/Z_{R_{Si}}$ shows to be related to the frequency, and it is the second frequency-dependent parameter we propose in this paper. By comparing (6) and (8), it is shown that f_T can also be considered as a specific value obtained when $Z_{C_{Si}}/Z_{R_{Si}} = 1$. To demonstrate the impact of impedance ratio of C_{Si} to R_{Si} on the silicon substrate, the coupling current between two adjacent TSVs are analyzed in three different frequency bands according to $Z_{C_{Si}}/Z_{R_{Si}}$ variations. Fig. 2 (a) shows the equivalent circuit model of two adjacent TSVs embedded in the silicon substrate, and it is worth to note that the depletion capacitance is not included for the analysis owing to that the silicon substrate is considered to be unbiased in our work [23]. As seen in Fig. 2, the outer ring marked as blue color stands for the SiO_2, and the inner circle marked as orange color represents the copper. Herein, it should be noted that the equivalent circuit model of a TSV pair and their coupling path analysis have been presented in prior works. For instance, the TSV to TSV coupling based on a lumped circuit model and the coupling path in the low frequency region (< 1 GHz), the middle frequency region (1 GHz to 8 GHz) and the high frequency region (> 8 GHz) wereanalyzed [24]. Moreover, a lumped crosstalk noise model was proposed, and the TSV to TSV coupling was investigated in three frequency regions including the low frequency region (< 1 GHz), the middle frequency region (1 GHz to 10 GHz) and the high frequency region (> 10 GHz) [25]. These two works studied the coupling between TSVs with a systematic examination, which are of great significance for the development of design guidelines for 3-D ICs. However, the frequency regions categorized in these two works were lack of accuracy divisions, especially when the conductivity of silicon substrate is adjusted. Different from prior works, we categorize the frequency bands of silicon substrate based on a definite standard of calibration shown in (8), and different frequency bands will be classified quantitatively according to the nature of the silicon substrate shown in Fig. 2 (b)–(d).

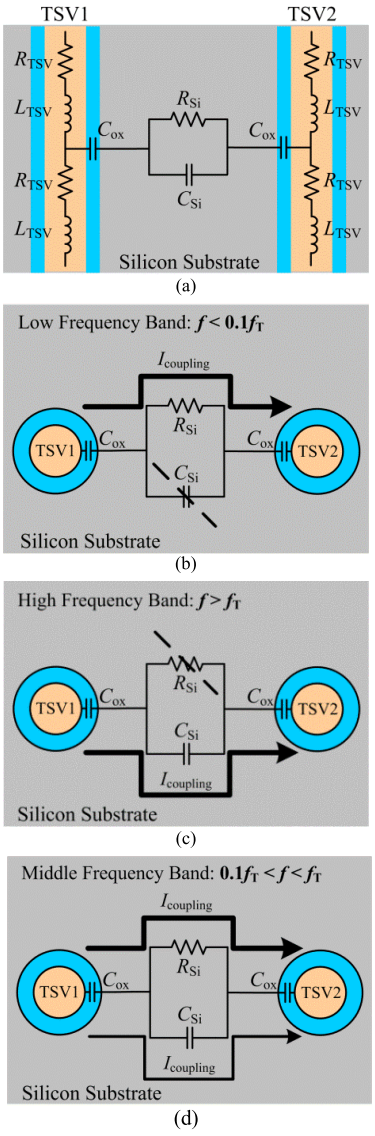

FIGURE 2. Equivalent circuit model of (a) two TSVs in the silicon substrate, and analysis of their coupling current (b) in the low frequency band ($f < 0.1f_T$) where $Z_{C_{Si}}/Z_{R_{Si}} > 10$, (c) in the high frequency band ($f > f_T$) where $Z_{C_{Si}}/Z_{R_{Si}} < 1$, and (d) in the middle frequency band ($0.1f_T < f < f_T$) where $1 < Z_{C_{Si}}/Z_{R_{Si}} < 10$.

If $Z_{C_{Si}}/Z_{R_{Si}}$ is considerably high, it is seen in (8) that the frequency calculated will be correspondingly low. Here, the tenfold ratio is set as a criterion for classifying boundaries between different frequency bands. When $Z_{C_{Si}}$ is at least one-order magnitude greater than $Z_{R_{Si}}$ (i.e., in a frequency band lower than 0.1 f_T), $Z_{C_{Si}}$ simply makes it an open circuit where almost no coupling current flows as shown in Fig. 2 (b). In other words, the silicon substrate can be seen

as a resistive medium when the frequency is sufficiently low. Fig. 2 (c) shows the case that, when $Z_{C_{Si}}/Z_{R_{Si}} < 1$, smaller $Z_{C_{Si}}$ paves an easier path for the coupling current to transmit, which happens in a frequency band higher than f_T. Fig. 2 (d) illustrates another occasion when $1 < Z_{C_{Si}}/Z_{R_{Si}} < 10$, the coupling current will flow through C_{Si} and R_{Si} between TSVs simultaneously. In terms of frequency band classification, this happens in a middle frequency band ranging between $0.1f_T$ and f_T. Moreover, it is worth to mention that the coupling current flowing through C_{Si} is weaker than R_{Si} owing to the different values of their impedances. In short, the above-mentioned analysis reveals that the path of coupling current between two adjacent TSVs in the silicon substrate differs associated with the change of $Z_{C_{Si}}/Z_{R_{Si}}$.

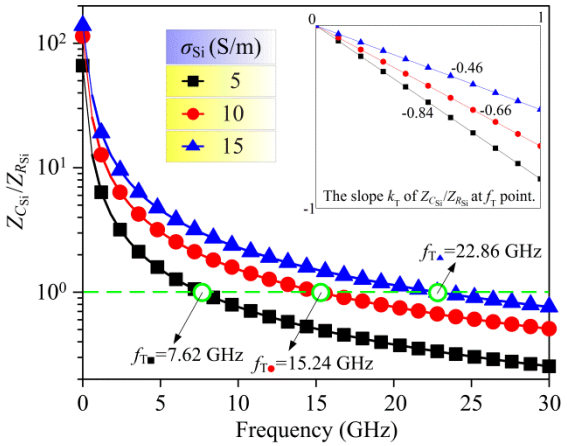

FIGURE 3. Comparisons of frequency band boundaries determined by the value of $Z_{C_{Si}}/Z_{R_{Si}}$ with different silicon substrate conductivities of 5 S/m, 10 S/m, and 15 S/m.

To further investigate how $Z_{C_{Si}}/Z_{R_{Si}}$ influences silicon substrate characteristics in detail, σ_{si} with three different values of 5 S/m, 10 S/m and 15 S/m are set in simulations to observe the phenomenon of frequency band boundaries changing shown in Fig. 3. It is displayed that the low frequency bandwidth ($f < 0.1f_T$, where $Z_{C_{Si}}/Z_{R_{Si}} > 10$) broadens by increasing σ_{si}, and that is to say the area where the silicon substrate exhibits resistive characteristic becomes widened. In addition, the slope k_T of the $Z_{C_{Si}}/Z_{R_{Si}}$ curve at the f_T point turns out to be flattened from -0.84 to -0.46 with increasing σ_{si} from 5 S/m to 15 S/m correspondingly, indicating that the larger σ_{Si} used, the higher the starting point (f_T) of a high frequency band shown in Fig. 2 (c) becomes. In other words, the frequency band where the silicon substrate behaving like a capacitive medium can be adjusted to start from a higher frequency, when we select a silicon substrate with larger conductivity. Thus, it is more appropriate to classify the frequency bands using the quantitative standard of calibration, which is highly adaptive for different silicon substrates with various conductivities.

In order to grasp the frequency-dependent characteristics between adjacent TSVs in the silicon substrate, the equivalent circuit model of a TSV pair can be equivalently converted into an *RC* parallel circuit model as shown in Fig. 4. This

TABLE 1. Relevant parameters used in this work.

Symbol	Parameter	Value
l_{TSV}	TSV height	60 μm
p	TSV pitch	30 μm
d_{TSV}	TSV diameter	10 μm
t_{ox}	insulator thickness	0.5 μm
σ_{Si}	conductivity of silicon	10 S/m
ε_{ox}	relative permittivity of insulator	4
ε_{Si}	relative permittivity of silicon	11.8
ε_0	absolute dielectric permittivity	8.85×10^{-12} F/m

conversion is based on the fact that these two circuit models have the same overall impedance. It is seen that the simplified *RC* parallel model on the right side is condensed to a large extent, and the SiO_2 surrounding the TSV can be removed for analysis. The only two parameters between a TSV pair are R_{eq} and C_{eq}, both of which are related to frequency, expressed as [26]

$$R_{eq}(\omega) = \frac{4+\omega^2 R_{Si}^2 (2C_{Si}+C_{ox})^2}{\omega^2 R_{Si} C_{ox}^2}, \quad (9)$$

$$C_{eq}(\omega) = \frac{2C_{ox}+\omega^2 R_{Si}^2 C_{Si} C_{ox} (2C_{Si}+C_{ox})}{4+\omega^2 R_{Si}^2 (2C_{Si}+C_{ox})^2}, \quad (10)$$

where the analytical formulas of R_{Si} and C_{Si} are $[(\pi\sigma_{si} l_{TSV})/\cosh^{-1}(p/d_{TSV})]^{-1}$ and $\pi\varepsilon_{si}\varepsilon_o l_{TSV}/\cosh^{-1}(p/d_{TSV})$, respectively, and C_{ox} is $2\pi\varepsilon_{ox}\varepsilon_o l_{TSV}/\ln[(d_{TSV}+2t_{ox})/d_{TSV}]$ [14]. Herein, l_{TSV}, p, d_{TSV}, and t_{ox} in the above formulas represent the TSV height, the TSV pitch, the TSV diameter, and the SiO_2 thickness, respectively.

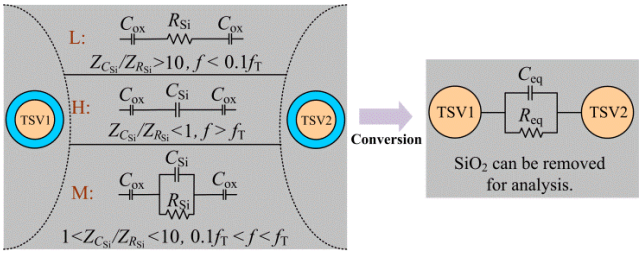

FIGURE 4. Electrical models of a TSV pair in the low (L), high (H) and middle (M) frequency bands affected by $Z_{C_{Si}}/Z_{R_{Si}}$ (on the left side), and the simplified *RC* parallel model only comprised of two frequency-dependent parameters (on the right side). Through this conversion, C_{ox} wrapping around the copper is no longer considered, which has been combined into the $R_{eq}C_{eq}$ product.

In addition, values obtained by different methods, including the formula calculation and analytical approximation, are compared with the simulated result, in order to display the implication of the equivalent values extracted in our simplified model. The simulation is performed by the quasi-static solver ANSYS Q3D, and the relevant parameters for simulations are shown in Table 1. Note that resistance is unable to simulate in Q3D with frequency changing, and thus the R_{eq} will be calculated at several frequencies based on (9) and compared with the approximation value using the analytical formula. The calculation shows that R_{eq} will decrease slightly

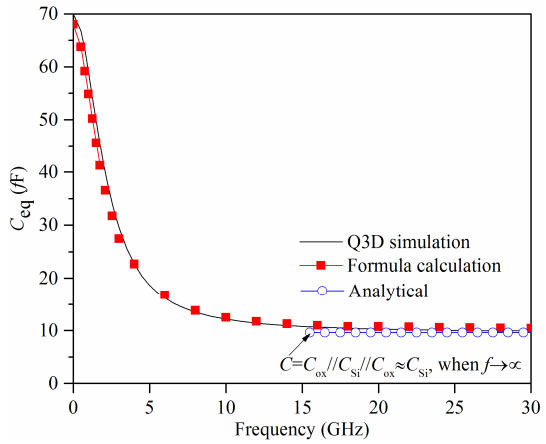

FIGURE 5. The calculated values versus the analytical approximation and the quasi-static simulated results for the equivalent capacitance between a TSV pair.

with the increasing the frequency. For instance, the value of R_{eq} will decrease to 1063 Ω at 30 GHz, compared to 1071 Ω at 20 GHz. The R_{si} obtained using the analytical formula is 935 Ω, and it can be predicted that R_{si} will even more approach R_{eq} with a higher frequency. For the comparison of capacitance values, Fig. 5 shows that the calculated C_{eq} is in good agreement with the simulation result. It is also seen that the higher frequency is, the more precisely the value of C_{eq} will approach the analytical C_{si}. For instance, the value of C_{eq} will decrease to 9.92 fF at 30 GHz, compared to 10.29 fF at 20 GHz, which is more close to the analytical C_{si} of 9.63 fF. This is due to the fact that the capacitance between a TSV pair is formed as C_{ox} // C_{si} // C_{ox}, and its equivalent parallel capacitance will be C_{si} approximately since the TSV diameter is usually sufficiently larger than the insulator thickness ($C_{ox} \gg C_{Si}$). Moreover, when the frequency is an infinite value, R_{eq} and C_{eq} shown in (9) and (10) reduce to $R_{Si}(2C_{Si}+C_{ox})^2/C_{ox}^2$ and $C_{Si}C_{ox}/(2C_{Si}+C_{ox})$, respectively, both of which become constants. Considering $C_{ox} \gg C_{Si}$, R_{eq} and C_{eq} can be further reduced, which are approximately equal to R_{Si} and C_{Si}, respectively. Thus, under the condition of sufficiently high frequency, we can get the expression as

$$R_{eq}C_{eq} \approx R_{Si}C_{Si}, \tag{11}$$

showing that the $R_{eq}C_{eq}$ product in our simplified model is also dependent to $\varepsilon_{Si}\varepsilon_0$ and σ_{Si} (see (7)) with a fairly high frequency.

III. MODELING AND DISCUSSION

To reveal the influence of silicon substrate on the signal transmission in TSV-Based 3-D ICs, we propose a frequency-dependent model to examine the coupling coefficient (S_{21}) between adjacent TSVs by converting the relevant impedance parameters into the impedance (Z) matrix to derive the expression of the S_{21}. Different from traditional ways of obtaining considerable impedance parameters, the parameters required are merely comprised of R_{eq} and C_{eq} from our simplified RC parallel model as shown in Fig. 4. As can be seen, the total impedance Z_{Total} between two TSVs is $Z_{R_{eq}}//Z_{C_{eq}}$, given as

$$Z_{Total} = \frac{R_{eq}}{1+\omega\cdot R_{eq}C_{eq}}. \tag{12}$$

The structures of two adjacent signal (S) TSVs and their reference ground (G) TSVs for simulations are depicted in Fig. 6 (a), which form one of the most commonly used configurations, the GSSG-type TSVs. It should be noted that the layout of ground TSV tends to be an important factor, as its position determines how large the impedance existed between adjacent TSVs on account of the silicon substrate impedance is finite. Technically, the ground TSVs can be inserted anywhere around signal TSVs with the pitch larger than the minimum distance requirement. In this paper, the placement of two ground TSVs are inserted vertically below the two signal TSVs and each two TSVs have the same pitch to demonstrate the most popular case. Due to the symmetry of the GSSG configuration, three impedance parameters Z_1, Z_2 and Z_3 existed between two adjacent TSVs are the equivalent impedance with the same value of Z_{Total} expressed in (12).

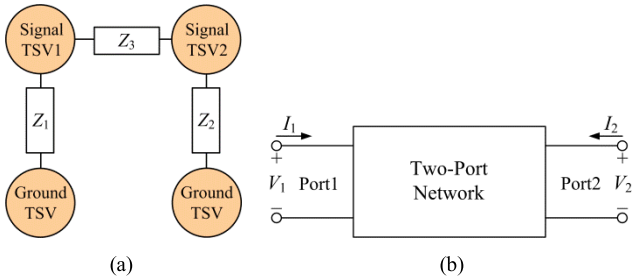

FIGURE 6. (a) Impedance parameters established for the GSSG configuration, and (b) a general two-port network with voltages and currents defined.

Herein, a general two-port network shown in Fig. 6 (b) is utilized to represent the electrical model of the GSSG configuration, and the port voltages and currents can be defined by the impedance parameters in a simply way. For the general port-two network, we can have the followings below

$$V_1 = Z_{11}I_1 + Z_{12}I_2, \tag{13}$$
$$V_2 = Z_{21}I_1 + Z_{22}I_2, \tag{14}$$

where V and I are the port voltage and current. Based on the model shown in Fig. 6, we can obtain Z_{11} which is the input impedance of port 1 when port 2 is open

$$Z_{11} = \left.\frac{V_1}{I_1}\right|_{I_2=0} = \frac{Z_1(Z_2+Z_3)}{Z_1+Z_2+Z_3}. \tag{15}$$

Then, Z_{12} can be derived by measuring the open-circuit voltage V_1 on port 1 when the current I_2 is applied to port 2

$$Z_{12} = \left.\frac{V_1}{I_2}\right|_{I_1=0} = \frac{Z_1Z_2}{Z_1+Z_2+Z_3}. \tag{16}$$

Similar to the method of deriving the relevant impedances above, Z_{21} is given as

$$Z_{21} = \left.\frac{V_2}{I_1}\right|_{I_2=0} = \frac{Z_1Z_2}{Z_1+Z_2+Z_3}, \tag{17}$$

and Z_{22} has the following

$$Z_{22} = \left.\frac{V_2}{I_2}\right|_{I_1=0} = \frac{Z_2\,(Z_1+Z_3)}{Z_1+Z_2+Z_3}. \tag{18}$$

It is noted that the two-port network is reciprocal and thus $Z_{12} = Z_{21}$. Therefore, the Z matrix is expressed as

$$\begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} = \begin{bmatrix} \dfrac{Z_1\,(Z_2+Z_3)}{Z_1+Z_2+Z_3} & \dfrac{Z_1Z_2}{Z_1+Z_2+Z_3} \\ \dfrac{Z_1Z_2}{Z_1+Z_2+Z_3} & \dfrac{Z_2\,(Z_1+Z_3)}{Z_1+Z_2+Z_3} \end{bmatrix}. \tag{19}$$

Based on the definition of the coupling coefficient (S_{21}) for the two-port network, the S_{21} can be obtained from the Z matrix as

$$S_{21} = \frac{2Z_{21}Z_0}{(Z_{11}+Z_0)\,(Z_{22}+Z_0) - Z_{21}Z_{12}}. \tag{20}$$

Finally, the 3-D full-wave field solver HFSS is utilized for the model verification. The conductivities of silicon substrate σ_{Si} are varied with the values of 5 S/m, 10 S/m, and 15 S/m for simulations. It is seen in Fig. 7 (a) that the coupling level gets reduced by decreasing σ_{Si}, which is owing to that smaller σ_{Si} makes the total impedance and R_{Si} larger, thus resulting in the coupling coefficient decreased. The discrepancy of comparisons for the coupling level indicates that our model slightly underestimates the value in the low frequency region, and overestimates the value in the high frequency region, compared to the 3-D field solver HFSS. While the trend of the coupling level variations suggests that our model has well captured the coupling coefficient changing associated with the frequency and the design parameter. Furthermore, the TSV pitches ranging from 30 um to 90 um are chosen for simulations. As can be seen, the coupling level increases by decreasing the pitch. That is due to the fact that the long distance between two TSVs makes the parasitic effects weakened, and consequently improves the insertion loss. On the other hand, it should be noted that the increased pitch makes the R_{si} larger and C_{si} smaller, thus enlarging the impedance between two adjacent TSVs and leading to the decreased coupling coefficient shown in Fig. 7 (b). Besides, the TSV heights and diameters are set from 20 um to 100 um, and 6 um to 14 um, respectively, for simulations. As seen in Fig. 7 (c), our model captures the coupling coefficient variations well with the simulation results, and it shows that the coupling coefficient gets reduced by decreasing the TSV height. This results from the fact that the values of TSV parasitic increase in proportion to the TSV height, and the same goes for the relations between the coupling coefficient and the TSV diameter seen in Fig. 7 (d), which shows that the coupling coefficient decreases by reducing the TSV diameter. In general, the results compared from our model and the 3-D field solver HFSS are well correlated with frequency changing, and the errors for comparisons are less than 5% for the variations of different physical parameters.

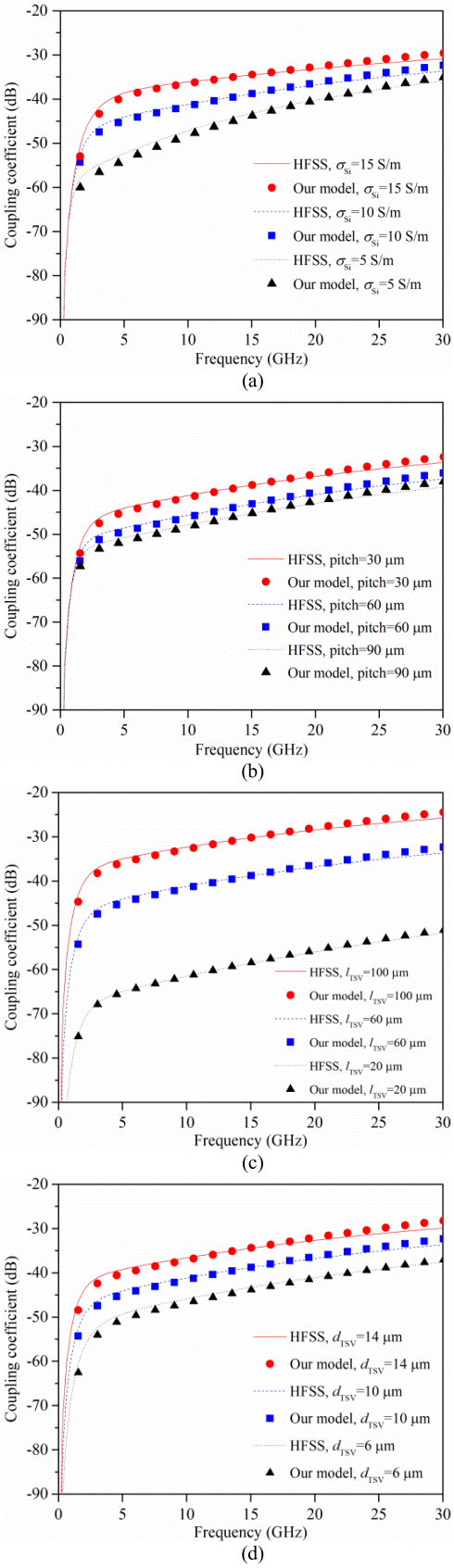

FIGURE 7. Comparisons of coupling coefficient with variations of (a) the silicon substrate conductivity, (b) the TSV pitch, (c) the TSV height, and (d) the TSV diameter, for the verification of our model.

IV. CONCLUSION

The characterization of silicon substrate with respect to the frequency variation was investigated in this paper. To the best of our knowledge, the accurate frequency bands representing different characteristics of the silicon substrate were first defined and obtained with a quantitative standard of calibration in our paper. Moreover, we converted the traditional circuit of a TSV pair into a simplified *RC* parallel model, which makes the analysis concise to a large extent for the silicon substrate associated with the frequency variation. Then, relevant parameters of the silicon substrate were converted into the impedance (Z) matrix for modeling in order to analyze the signal transmission in the silicon substrate. Different from traditional ways of establishing the model, the parameters required were only comprised of R_{eq} and C_{eq} both from our simplified *RC* parallel model. The coupling coefficient (S_{21}) for a general two-port network was then derived and validated in comparison with 3D full-wave electromagnetic simulations. Finally, influences of design parameter variations on the coupling level were studied, discussing helpful details for parametric modeling of the silicon substrate in TSV-based 3-D ICs.

REFERENCES

[1] T. Fukushima, "Chiplet-based advanced packaging technology from 3D/TSV to FOWLP/FHE," in *Proc. Symp. VLSI Circuits*, Jun. 2021, pp. 1–2.

[2] C. Zhi, G. Dong, Y. Wang, Z. Zhu, and Y. Yang, "Trade-off-oriented impedance optimization of chiplet-based 2.5-D integrated circuits with a hybrid MDP algorithm for noise elimination," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 69, no. 12, pp. 5247–5258, Dec. 2022.

[3] R. Kuttappa, B. Taskin, S. Lerner, and V. Pano, "Resonant clock synchronization with active silicon interposer for multi-die systems," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 68, no. 4, pp. 1636–1645, Apr. 2021.

[4] J. Kim, G. Murali, H. Park, E. Qin, H. Kwon, V. Chaitanya, K. Chekuri, N. Dasari, A. Singh, M. Lee, H. M. Torun, K. Roy, M. Swaminathan, S. Mukhopadhyay, T. Krishna, and S. K. Lim, "Architecture, chip, and package co-design flow for 2.5D IC design enabling heterogeneous IP reuse," in *Proc. 56th Annu. Design Autom. Conf.*, Jun. 2019, pp. 1–6.

[5] L. England and I. Arsovski, "Advanced packaging saves the day!—How TSV technology will enable continued scaling," in *IEDM Tech. Dig.*, Dec. 2017, pp. 3.5.1–3.5.4.

[6] W. Li, Z. Liu, W. Qian, Z. Wang, W. Wang, Y. Zhao, and X. Zhang, "Modeling of the RF coaxial TSV configuration inside the silicon interposer with embedded cooling cavity," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 12, no. 1, pp. 3–10, Jan. 2022.

[7] J.-M. Yook, Y.-G. Kim, W. Kim, S. Kim, and J. C. Kim, "Ultrawideband signal transition using quasi-coaxial through-silicon-via (TSV) for mm-wave IC packaging," *IEEE Microw. Wireless Compon. Lett.*, vol. 30, no. 2, pp. 167–169, Feb. 2020.

[8] W.-S. Zhao, Q.-H. Hu, K. Fu, Y.-Y. Zhang, D.-W. Wang, J. Wang, Y. Hu, and G. Wang, "Modeling of carbon nanotube-based differential through-silicon vias in 3-D ICs," *IEEE Trans. Nanotechnol.*, vol. 19, pp. 492–499, 2020.

[9] J. Kim, "High-frequency scalable electrical model and analysis of a through silicon via (TSV)," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 1, no. 2, pp. 181–195, Feb. 2011.

[10] V. Kumar, H. Oh, X. Zhang, L. Zheng, M. S. Bakir, and A. Naeemi, "Impact of on-chip interconnect on the performance of 3-D integrated circuits with through silicon vias: Part I," *IEEE Trans. Electron Devices*, vol. 63, no. 6, pp. 2503–2509, Jun. 2016.

[11] K. J. Han, M. Swaminathan, and T. Bandyopadhyay, "Electromagnetic modeling of through-silicon via (TSV) interconnections using cylindrical modal basis functions," *IEEE Trans. Adv. Packag.*, vol. 33, no. 4, pp. 804–817, Nov. 2010.

[12] I. Ndip, "Analytical, numerical-, and measurement-based methods for extracting the electrical parameters of through silicon vias (TSVs)," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 4, no. 3, pp. 504–515, Mar. 2014.

[13] Q. Lu, Z. Zhu, G. Shan, Y. Liu, X. Liu, and X. Yin, "3-D compact 3-dB branch-line directional couplers based on through-silicon via technology for millimeter-wave applications," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 9, no. 9, pp. 1855–1862, Sep. 2019.

[14] I. Ndip, "High-frequency modeling of TSVs for 3-D chip integration and silicon interposers considering skin-effect, dielectric quasi-TEM and slow-wave modes," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 1, no. 10, pp. 1627–1641, Oct. 2011.

[15] R. Gordin, "Design and modeling methodology of vertical interconnects for 3DI applications," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 1, no. 2, pp. 163–167, Feb. 2011.

[16] Q. Lu, Z. Zhu, Y. Yang, and R. Ding, "Electrical modeling and characterization of shield differential through-silicon vias," *IEEE Trans. Electron Devices*, vol. 62, no. 5, pp. 1544–1552, May 2015.

[17] C. Qu, R. Ding, and Z. Zhu, "High-frequency electrical modeling and characterization of differential TSVs for 3-D integration applications," *IEEE Microw. Wireless Compon. Lett.*, vol. 27, no. 8, pp. 721–723, Aug. 2017.

[18] K. Cho, "Signal integrity design and analysis of differential high-speed serial links in silicon interposer with through-silicon via," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 9, no. 1, pp. 107–121, Apr. 2019.

[19] J. Kim, "High-frequency scalable modeling and analysis of a differential signal through-silicon via," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 4, no. 4, pp. 697–707, Apr. 2014.

[20] C. Hwang, B. Achkir, and J. Fan, "Capacitance-enhanced through-silicon via for power distribution networks in 3D ICs," *IEEE Electron Device Lett.*, vol. 37, no. 4, pp. 478–481, Apr. 2016.

[21] D. M. Pozar, *Microwave Engineering*, 3rd ed. New York, NY, USA: Wiley, 2005.

[22] M. Pfost, H. M. Rein, and T. Holzwarth, "Modeling substrate effects in the design of high-speed Si-bipolar ICs," *IEEE J. Solid-State Circuits*, vol. 31, no. 10, pp. 1493–1501, Oct. 1996.

[23] R. Weerasekera, G. Katti, R. Dutta, S. Zhang, K. Chang, J. Zhou, and S. Bhattacharya, "An analytical capacitance model for through-silicon vias in floating silicon substrate," *IEEE Trans. Electron Devices*, vol. 63, no. 3, pp. 1182–1188, Mar. 2016.

[24] T. Song, C. Liu, D. H. Kim, S. K. Lim, J. Cho, J. Kim, J. S. Pak, S. Ahn, J. Kim, and K. Yoon, "Analysis of TSV-to-TSV coupling with high-impedance termination in 3D ICs," in *Proc. 12th Int. Symp. Quality Electron. Design*, Mar. 2011, pp. 14–16.

[25] L. Qian, Y. Xia, and G. Liang, "Study on crosstalk characteristic of carbon nanotube through silicon vias for three dimensional integration," *Microelectron. J.*, vol. 46, no. 7, pp. 572–580, Jul. 2015.

[26] Z. Xu and J.-Q. Lu, "Through-strata-via (TSV) parasitics and wideband modeling for three-dimensional integration/packaging," *IEEE Electron Device Lett.*, vol. 32, no. 9, pp. 1278–1280, Sep. 2011.

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