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RESEARCH ARTICLE

EMI and Voltage Ripple Co-Optimization of a Spread-Spectrum Controller in Buck Converters

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ABSTRACT The buck converters can use spread-spectrum technique to ensure the reduction of electromagnetic emissions by distributing the energy around the switching frequency and reducing its amplitude. The switching frequency change causes the output voltage to change which manifests in an unwanted voltage ripple. This paper considers a spread-spectrum controller which uses a Phase Locked Loop (PLL) with a programmable divider to generate the changing switching frequency. The programmable divider uses a divider generator to generate the random sequence of dividers and the paper analyses generators based on Linear Feedback Shift Registers (LFRS) and memories. The Electromagnetic Interference (EMI) caused by the buck converter and the output voltage ripple are numerically modelled and then used to optimize divider generators. The results show that the memory-based generator designs have larger influence on EMI levels and duty cycle ripple which makes it more suitable for the co-optimization procedure. The co-optimization procedure results in memory-based designs which offer better performance in terms of EMI and duty cycle ripple compared to the LFSR-based designs. Implementation of the divider generators in field-programmable gate array (FPGA) shows that the memory-based generators have a larger programmable logic footprint. The measurements of the generator designs in a buck converter confirm the estimated relations of the modelled Figures-of-Merit.

INDEX TERMS DC-DC converter, digital design, spread-spectrum, phase-locked loop, duty cycle ripple, EMI.

I. INTRODUCTION

Recently the switching frequency of switch-mode power direct current (DC-DC) converters has shifted into MHz range which led to the availability of the first fully integrated converters. Fully-integrated switch-mode power DC-DC converters have a number of advantages when compared to the converters which use discrete components. These advantages include simpler utilization, reduced cost and improved reliability [1]. The most important characteristic of power converters is its efficiency. Using resonant soft-switching techniques reduces the switching losses and preserves a high efficiency even in the case of the switching frequencies in the range of tens of MHz [2], [3], [4].

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The increase in the switching frequency of switch-mode power DC-DC converters also increases the generated electromagnetic interferences (EMI) which makes it one of the foremost challenges in the design of high-frequency DC-DC converters. The maximum levels of the generated electromagnetic interferences have to be below the defined limits specified by the electromagnetic compatibility (EMC) standards [5]. Even a low-power devices (< 0.5 W) switching at the frequency of more than 160 MHz can fail the electromagnetic compatibility (EMC) conformity tests as reported in [6] and [7].

Furthermore, advanced management techniques can be also used practically at no cost other than the silicon area, e.g. a spread-spectrum modulator. The spread-spectrum technique reduces the emitted electromagnetic interferences (EMI) by distributing the energy of the interfering signal

to the frequency band around it. This modulation scheme doesn't change the total energy of the interfering signal and consequently the amplitudes of the spread-spectrum frequency components are reduced relative to the amplitude of the original interfering signal.

Spread-spectrum technique is an efficient technique for reduction of electromagnetic interferences emitted by switching converters and lately it is gaining in popularity [8]. The spread-spectrum technique is applied in many different switching devices, e.g. SATA controllers [9], audio amplifiers [10], [11] and power converters [8], [12]. Spread-spectrum technique is often used in commercial products, but it was shown in [13] that often the parameters of the spread-spectrum technique in the given application are not optimized.

Applying spread-spectrum technique is commonly a trade-off – while it improves the EMC, it worsens other performance characteristics of the converter, e.g. the efficiency. Commercially available converters usually use a fixed spread-spectrum modulation, i.e. its parameters cannot be configured by the end user. A configurable spread-spectrum modulator can be used to analyse these trade-offs and to optimize the reduction of the generated electromagnetic (EM) emission without sacrificing the performance of the device (e.g. the efficiency). Another important trade-off is the presence of a ripple in the output voltage of the converter which is caused by changing the switching frequency while the on-time of the pulse-width modulation (PWM) controller remains constant as shown in [14] and [15].

The standards CISPR 25 and IEC 61967 describe EMC measurements in the frequency range of interest (from 150 kHz to 30 MHz) [16]. The profile of frequency change can be deterministic (e.g. sinusoidal, cubic, triangular...), but the random frequency change results in the flattest spectra as shown in [8], [17], and [18]. The random frequencies are often generated using Linear Feedback Shift Registers (LFSR) as shown in [19], [20], and [11]. While the random frequency change results in flattest EMI spectra, i.e. best EMC performance, it is expected that the random frequency change also produces the greatest output voltage ripple due to great variance of the duty cycle. These two performance characteristics of the DC-DC converter are in a trade-off relationship.

This paper compares the LFSR- and the memory-based spread-spectrum controllers of a buck converter which are designed using a co-optimization procedure. The presented co-optmization procedure minimizes Figures-of-Merit which model the electromagnetic interference and the output voltage ripple induced by the spread-spectrum-based buck converter.

The application of the spread-spectrum technique in controlling a buck converter is introduced in Section II. The spread-spectrum technique application is based on the Phase Locked Loop (PLL) with a programable divider which is described in Subsection II-A. Subsections II-B and II-C present the LFSR- and memory-based methods of generating an array of PLL dividers used in the spread-spectrum technique. Next, Section III develops numerical models of the effects in the buck converter caused by the application of the spread-spectrum technique. Subsection III-A models the electromagnetic interference generated by the buck converter, while Subsection III-B models the output voltage ripple of the buck converter caused by the spread-spectrum technique. Furthermore, Section IV uses the derived numerical models of the EMI and the voltage ripple induced by the spread-spectrum technique and cooptimizes the PLL divider generation. Subsection IV-A shows the co-optimization results in the case of the LFSR-based divider generation and Subsection IV-B in the case of the memory-based divider generation. Section V presents a physical verification of the co-optimization results on an example buck converter. Subsection V-B describes the measurement set-up and Subsection V-C shows the measurement results. Subsection V-D compares the measurement and the co-optimization results. Finally, Section VI presents the conclusions of the paper.

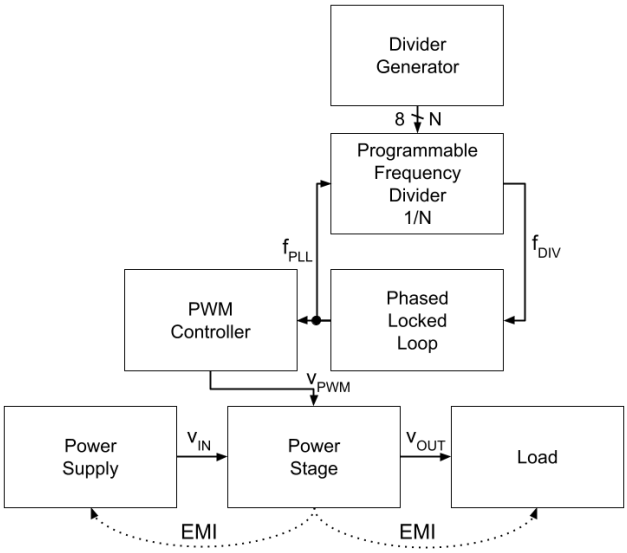

FIGURE 1. The buck converter based on a programmable PLL.

II. APPLICATION OF SPREAD-SPECTRUM TECHNIQUE IN BUCK CONVERTERS

A. PROGRAMMABLE PLL-BASED BUCK CONVERTER CONTROLLER

Fig. 1 shows a buck converter which features a controller with a programmable switching frequency generator. The programmable frequency generator generates the switching frequency f_{PLL} of the buck converter used to apply the spread-spectrum technique to the buck converter and thus reduce the overall electromagnetic interference caused by the buck converter. The programmable frequency generator is based on a Phase Locked Loop which consists of a PLL core-circuit and a programmable divider. The programmable divider divides the PLL output frequency by N where N is an 8-bit word in the presented case. The output of the

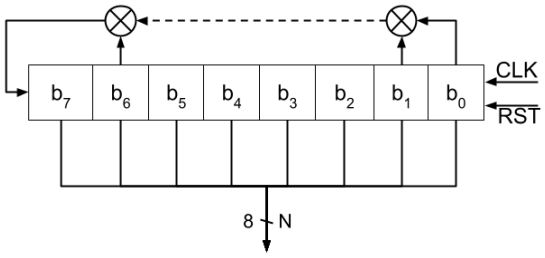

FIGURE 2. The PLL divider generator based on a linear feedback shift register (LFSR).

programmable divider is a signal having the frequency f_{DIV} which is fed back to the PLL core-circuit [21].

The PLL output frequency f_{PLL} is used as the switching frequency of the buck converter and it is fed to the PWM (pulse-width modulation) controller. The PWM controller generates an output pulse signal with a given on-time and this signal is used to control the power stage of the buck converter. The power stage steps down the input voltage v_{IN} supplied by the power supply and outputs the output voltage v_{OUT} to the load. The switching action of the power stage results in generation of heavy electromagnetic interferences (EMI) caused by steep slew rates of the voltages and currents in the circuit.

The spread-spectrum technique is used to spread the generated EMI from a narrow band around the switching frequency into a wider bandwidth thus reducing the maximum peaks of EMI. However, if the on-time of the PWM signal is kept constant, the applied spread-spectrum technique results in the modulation of the output voltage or output voltage ripple.

B. LFSR-BASED PLL DIVIDER GENERATION

Fig. 2 shows the PLL divider generator based on a linear feedback shift register (LFSR). The linear feedback shift register consists of an array of flip-flops which form the shift register and a feedback combinatorial network which determines the next bit shifted in. The feedback network consists of a number XOR gates which use select bits in the shift register to determine the feedback bit. The select bits or taps form the polynomial of the LFSR. The state of the LFSR constitutes the divider value N, an 8-bit word which is used to determine the PLL divider value. The LFSR uses the system clock *CLK* and reset *RST* signals.

C. MEMORY-BASED PLL DIVIDER GENERATION

Fig. 3 shows the PLL divider generator based on a memory. This divider generator uses a predetermined sequence of random numbers to generate the PLL dividers. The sequence of random numbers is stored in a memory with a 64-word capacity and an 8-bit width. The sequence stored in the memory is addressed by the address counter which generates a 6-bit address for the divider sequence memory. The address counter counts from the lowest to the highest address and then wraps around to the lowest address.

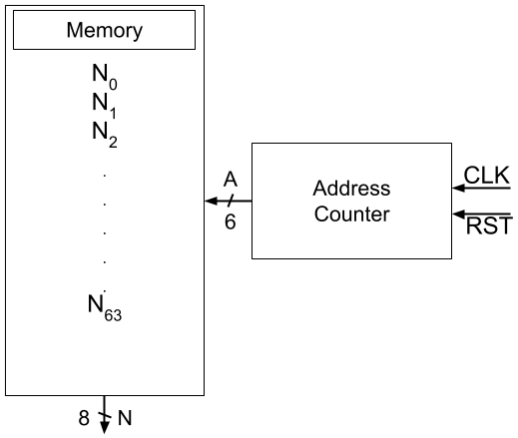

FIGURE 3. The PLL divider generator based on a memory.

III. NUMERICAL MODELLING OF SPREAD-SPECTRUM EFFECTS

A. SPREAD SPECTRUM EMI MODELING

The Phase Locked Loop circuit controls a Voltage Controlled Oscillator (VCO) based on a signal with the reference frequency f_{REF} and a feedback signal which represents the VCO frequency divided by the given factor N. The PLL settles when the reference frequency signal and the feedback signal are in phase and have the same frequency which is defined as

$$f_{REF} = \frac{f_{PLL}}{N} \tag{1}$$

where f_{PLL} is the PLL output frequency, i.e. the frequency of the VCO. This relation explains how the PLL output frequency can be changed by using a programmable divider in its feedback loop and in this case the PLL output frequency changes in time as determined by

$$f_{PLL}(t) = N(t) \cdot f_{REF} \tag{2}$$

while the reference frequency f_{REF} is kept constant. The PLL output frequency is used as the switching frequency in the buck converter $f_{SW} = f_{PLL}$ and it determines the output voltage and current waveforms of the buck converter, but also the electromagnetic interferences caused by the converter. These interferences can be conducted and radiated, but in both cases these interferences are proportional to the output voltage and current of the buck converter. E.g. the measured conducted electromagnetic interference are represented by the EMI detector voltage v_{EMI} which can be defined as

$$v_{EMI}(f) = k(f) \cdot i_{out}(f) \tag{3}$$

where $k(f)$ is a proportionality constant which describes the measurement system and the EMI coupling [22].

A critical component of the detector used in EMI measurements is its intermediate-frequency (IF) filter. The IF filter has a finite bandwidth which defines the resolution of the measurement. The amplitude frequency characteristic of the

IF filter is modelled as

$$A_{RBF}(f) = \frac{1}{1+\frac{(f-f_C)^2}{(f_{BW}/2)^2}} \tag{4}$$

where f_C is the central frequency, i.e. the measurement frequency and f_{BW} is the resolution bandwidth (RBW).

The sequence of dividers generated by the PLL divider generator, either based on an LFSR or memory approach, is designated as N and N_i is the i-th divider in the sequence. The estimated EMI spectrum $v_{EMI}(f)$ consists of all of the dividers, i.e. switching frequency contributions and it is defined as

$$v_{EMI}(f) = \sum_{i=0}^{M} A_{RBF}(f)\,|_{f_C=N_i \cdot f_{REF}} \tag{5}$$

where M is the number of considered dividers, i.e. memory size in the case of the memory-based generator. This leads to

$$v_{EMI}(f) = \sum_{i=0}^{M} \frac{1}{1+\frac{(f-N_i \cdot f_{REF})^2}{(f_{BW}/2)^2}} \tag{6}$$

by including the definition of the IF filter frequency characteristic (4). This summing operation across all of the divider instances constitutes an average type EMI detector.

The EMC standards define maximum limits for the electromagnetic emissions of the Device-under-Test in given frequency ranges and measurement methodologies and consequently the Figure-of-Merit with respect to the electromagnetic interference is defined as the maximum value of the estimated spectrum, i.e.

$$v_{EMI,max} = \max_f v_{EMI}(f). \tag{7}$$

B. OUTPUT VOLTAGE RIPPLE MODELING

The output voltage of a buck converter is determined by the duty cycle D of the PWM signal controlling the output stage of the buck converter and it is defined as

$$V_{OUT} = D \cdot V_{IN}. \tag{8}$$

The duty cycle of the PWM signal is controlled by the on-time T_{ON} of the PWM controller and it is determined as

$$D = \frac{T_{ON}}{T_{SW}} = T_{ON} \cdot f_{SW} \tag{9}$$

where the T_{SW} is the period of the switching frequency, f_{SW}.

Furthermore, by taking into account the variable switching frequency in the case of the spread-spectrum technique, the time-dependant duty cycle is defined as

$$D(t) = T_{ON} \cdot f_{REF} \cdot N(t). \tag{10}$$

The relations (8) and (10) are combined and the time-varying output voltage is defined as

$$v_{OUT}(t) = D(t) \cdot V_{IN} = V_{IN} \cdot T_{ON} \cdot f_{REF} \cdot N(t) \tag{11}$$

where the on-time T_{ON}, the reference frequency f_{REF} and the input voltage V_{IN} are assumed constant. Consequently, the Figure-of-Merit with respect to the output voltage ripple is simplified by calculating the deviation of the duty cycle

$$\sigma_D = \sqrt{\frac{1}{M}\sum_{i=1}^{M}\left(N_i - \bar{N}\right)^2} \cdot T_{ON} \cdot f_{REF} \tag{12}$$

where $\bar{N}$ is the mean value of the PLL divider. The defined duty cycle deviation σ_D represents the Root-Mean-Square (RMS), i.e. the effective value of the duty cycle ripple which is proportionally present in the output voltage of the buck converter.

IV. EMI AND VOLTAGE RIPPLE CO-OPTIMIZATION

The co-optimization procedure in this paper considers a buck converter design with the reference frequency $f_{REF} = 1$ kHz and the mean divider value $\bar{N} = 1000$. The divider values are determined using the generated 8-bit divider value in the range [873, 1128] in 256 steps. This results in the switching freqeuncy range $f_{SW} = [0.873, 1.128]$ MHz. The considered PWM controller uses the on-time $T_{ON} = 500$ ns.

The defined Figures-of-Merit are evaluated for a number of different LFSR- and memory-based PLL divider generator designs. An LFSR-based generator design consists of the feedback polynomial which is then used to generate the divider sequence, while a memory-based generator design is defined by the exact divider sequence.

The co-optimization procedure simultaneously minimizes the EMI spectrum peak $v_{EMI,max}$ as defined in (7) and the duty cycle deviation σ_D as defined in (12). The result of the procedure is a set of Pareto-optimal divider generator designs.

The design space of the LFSR-based generator designs is relatively small ($2^8 = 256$ designs) and all of the designs are evaluated. The design space of the memory-based generator designs is incomparably larger, 2^{64}, and it is explored using a Random Optimization (RO) technique [23]. The RO technique is based on randomly modifying dividers in the divider sequence and then keeping the divider modification if it resulted in a better combination of the Figures-of-Merit.

Fig. 4 shows the front of Pareto-optimal designs in Figure-of-Merit space. It is observed that the Pareto fronts of both the LFSR- and memory-based designs cover a similar range of spectrogram peak values, i.e. both types of designs can be similarly engineered with respect to the EMC characteristics. More importantly, the Pareto front of the memory-based designs also covers much smaller values of the duty cycle ripple when compared to the Pareto front of the LFSR-based generators.

Three different design examples are selected for both the LFSR- and the memory-based generator designs. One of the designs represents the low emissions design which features the comparably best EMC performance. Another design represent the low ripple design which yields the comparably lowest duty cycle ripple and consequently output voltage ripple. Also, a Pareto optimal design was selected which lies in between the two previous designs with respect to the EMC and output voltage ripple performance.

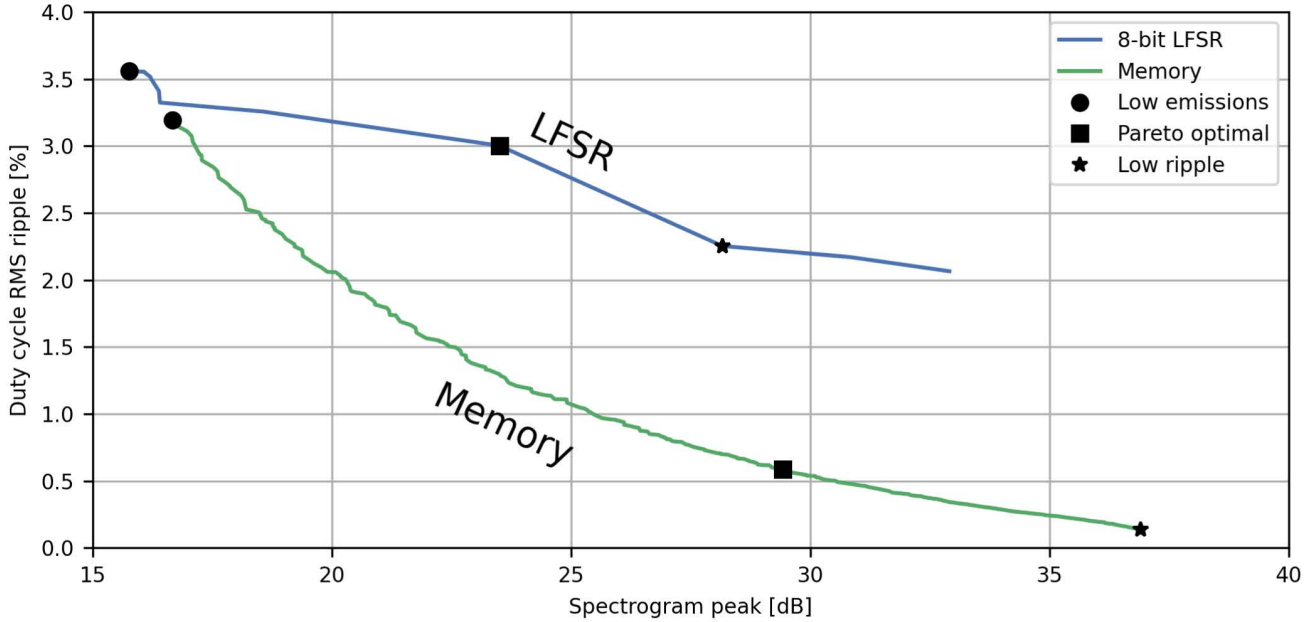

FIGURE 4. The front of Pareto-optimal designs in Figure-of-Merit space.

TABLE 1. The characteristics of the example LFSR designs.

LFSR-based design	Polynomial	Spectrogram peak [dB]	Duty cycle RMS ripple [%]
Low emissions	[7, 6, 2, 1]	15.76	3.558
Pareto optimal	[3, 1]	23.50	3.002
Low ripple	[4, 3, 2, 1]	28.16	2.252

TABLE 2. The characteristics of the example memory-based designs.

Memory-based design	Spectrogram peak [dB]	Duty cycle RMS ripple [%]
Low emissions	16.67	3.192
Pareto optimal	29.43	0.5858
Low ripple	36.90	0.1372

A. CO-OPTIMIZATION OF LFSR-BASED DIVIDER GENERATION

Table 1 shows the characteristics of the example LFSR designs. Table shows the feedback polynomial taps, the spectrogram peak and the duty cycle RMS ripple for the three example LFSR designs. The low emissions LFSR design produces an estimated spectrogram peak which is half the value of the spectrogram peak produced by the low ripple LFSR design. The low emissions LFSR design also has an approx. 50% greater duty cycle ripple than the low ripple LFSR design.

Fig. 5 shows the histogram of the dividers generated by the example LFSR designs. The histogram shows that the low emissions LFSR design has an approx. uniform distribution of generated dividers, while the low ripple LFSR design generates dividers which are distributed unevenly in the design space of available divider values.

Fig. 6 shows the frequency spectra of the modelled EM emissions for the example LFSR designs. The histogram observations are directly reflected in the estimated spectrograms with the low emissions LFSR design having the flattest and the overall lowest spectra. This kind of a flat spectrum is the aim of the spread-spectrum technique application.

Fig. 7 shows the waveforms of the duty cycle for the example LFSR designs. The waveforms show that indeed the low ripple design has the smallest duty cycle ripple of the three selected designs. It also shows that the low ripple design has a sequence of random number with the shortest period.

B. CO-OPTIMIZATION OF MEMORY-BASED DIVIDER GENERATION

Table 2 shows the characteristics of the example memory-based designs. Table shows the spectrogram peak and the duty cycle RMS ripple for the three example memory-based designs. The low emissions design produces an estimated spectrogram peak which is approx. 45% of the value of the spectrogram peak produced by the low ripple LFSR design. The low emissions LFSR design also has an approx. 25 times greater duty cycle ripple than the low ripple LFSR design. It is important to note that the majority of memory-based designs have considerably better performance than the LFSR-based designs. The exception are the LFSR-based designs with the lowest EMI levels which have similar EMI levels and values of duty cycle RMS ripple compared to the memory-based designs.

Fig. 8 shows the histogram of the dividers generated by the example memory-based designs. The histogram shows that the low emissions memory-based design has an approx. uniform distribution of generated dividers, while the low

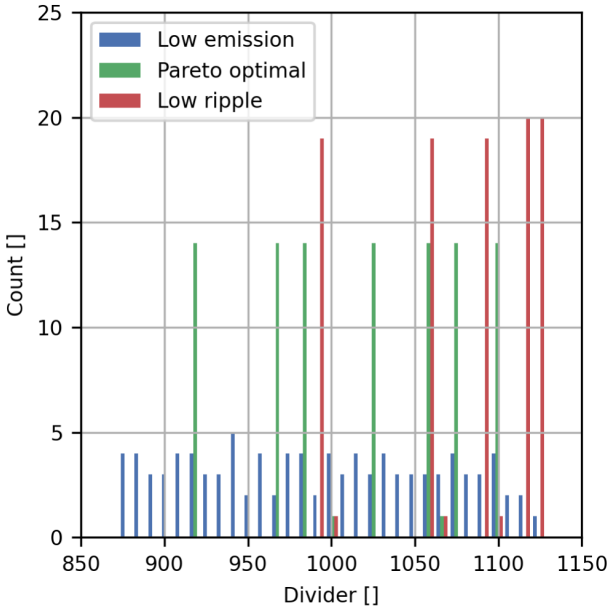

FIGURE 5. The histogram of the dividers generated by the example LFSR designs.

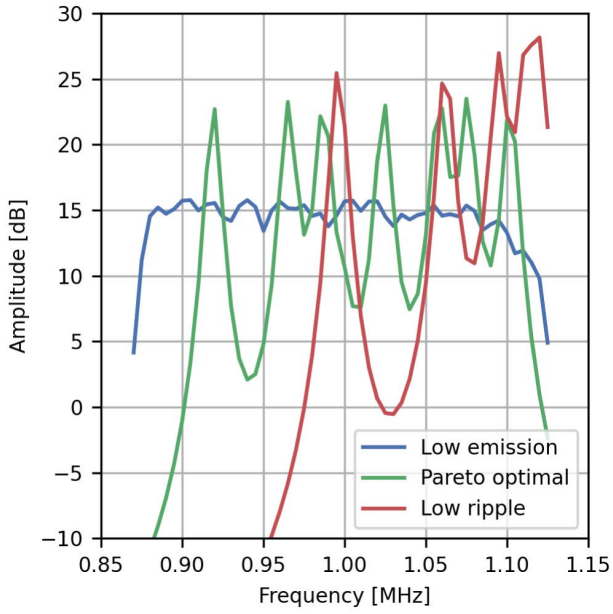

FIGURE 6. The frequency spectra of the modelled EM emissions for the example LFSR designs.

ripple memory-based design generates dividers which are distributed extremely unevenly and concentrated around $N = 1000$ as could have been expected.

Fig. 9 shows the frequency spectra of the modelled EM emissions for the example memory-based designs. The histogram observations are again directly reflected in the estimated spectrograms with the low emissions memory-based design having the flattest and the overall lowest spectra.

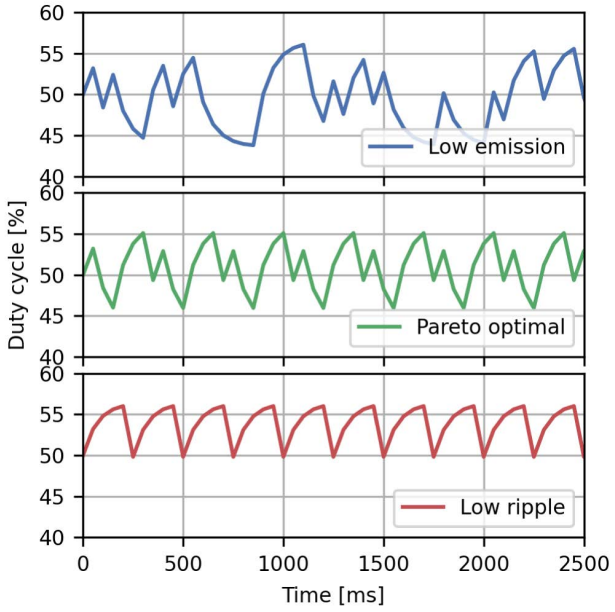

FIGURE 7. The waveform of the duty cycle for the example LFSR designs.

Fig. 10 shows the waveform of the duty cycle for the example memory-based designs. The waveforms show that indeed the low ripple design has the smallest duty cycle ripple of the three selected designs and the difference between the low emissions and the low ripple designs is much greater than it was the case for the LFSR-based designs.

V. EXAMPLE CASE STUDY

A. FPGA IMPLEMENTATION OF DIVIDER GENERATOR

Table 3 shows the area utilization of the divider generator implemented in an FPGA. The area utilization is shown for the LFSR- and memory-based divider generators and their accompanying designs. The area utilization on the FPGA shows the utilization of the Look-Up Tables (LUT) and Flip-Flops (FF) in the programmable fabric. The Look-Up Tables are used to implement combinatorial digital functions, while the Flip-Flops are used to implement the sequential digital functions. These area utilization results are based on the reports given by the used Xilinx Vivado digital synthesizer [24]. The targeted FPGA development system is the Nexys A7 board [25] based on the Xilinx Artix-7 series of FPGAs which use 6-input Look-Up Tables.

All of the LFSR-based divider generator designs utilize the same amount of Look-Up Tables and Flip-Flops. The Look-Up Tables in this case implement the linear feedback of the LFSR which is a combinatorial function consisting of a number of XOR operations. The utilized Flip-Flops in this case implement the shift-register and represent the state of the LFSR. The number of the utilized Flip-Flops is the same as all of the LFSR have a shift register of an equal width $W = 8$.

The number of Look-Up-Tables vary between the different memory-based divider generator designs. The Look-Up

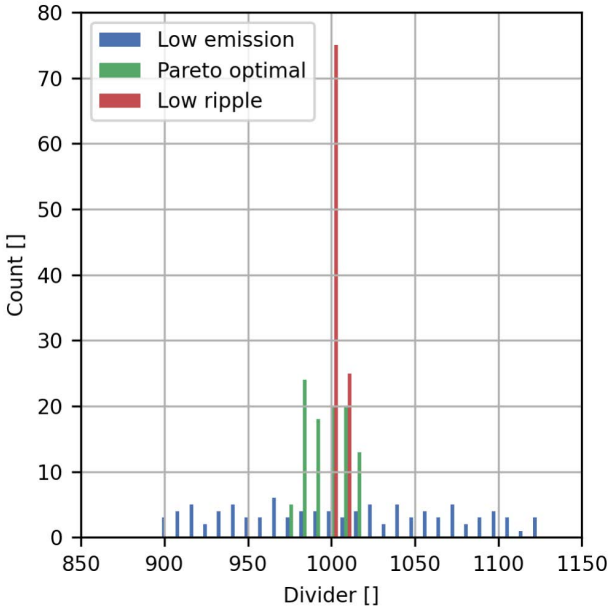

FIGURE 8. The histogram of the dividers generated by the example memory-based designs.

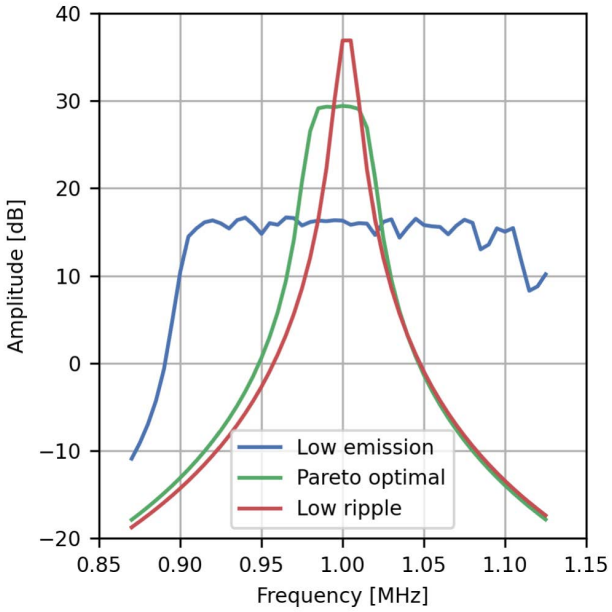

FIGURE 9. The frequency spectra of the modelled EM emissions for the example memory-based designs.

TABLE 3. The area utilization of the divider generator implemented in an FPGA.

Generator type	Design	LUT []	FF []
LFSR	Low emissions	2	8
	Pareto optimal	2	8
	Low ripple	2	8
Memory	Low emissions	15	6
	Pareto optimal	13	6
	Low ripple	12	6

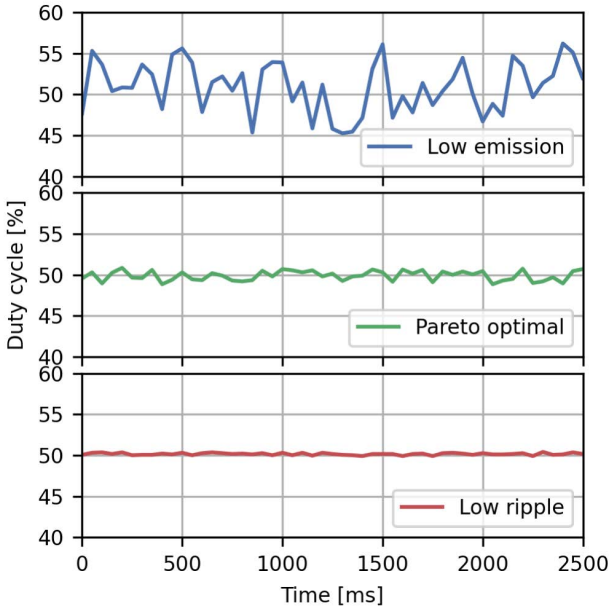

FIGURE 10. The waveform of the duty cycle for the example memory-based designs.

Tables in this case are used to implement the Read-Only Memory which contains the divider sequence and the memory address decoder. As the divider sequence is fixed the memory is implement as a combinatorial digital functions which decodes the given address to a divider value. The differences in the number of Look-Up Tables can be attributed to the distributions of the divider designs. The narrowest divider distribution is in the case of the low emissions design which features the lowest number of Look-Up Tables, while the low emissions design has the widest divider distribution and consequently the highest number of Look-Up Tables. All of the memory-based divider generator designs utilize the same amount of Flip-Flops. These Flip-Flops are used in the address counter module of the memory-based divider generator and they are equal to the width of the counter which is used to address the divider memory $U = 6$.

B. MEASUREMENT SET-UP

Fig. 11 shows the measurement set-up used to test the PLL divider generator designs. The measurement set-up reflects the system shown in Fig. 1 and implements a complete buck converter. The EMI generated by the buck converter are measured using an EMI receiver and a Coupling-Decoupling Network (CDN) positioned on the power supply lines. The output voltage and its ripple is measured using an oscilloscope.

The buck converter consists of an integrated output stage Vishay SiC651 [26] and a custom built controller. The different divider generator designs are implemented in the FPGA as shown in Subsection V-A, while the programmable frequency divider and the PLL circuit are implemented in an ASIC

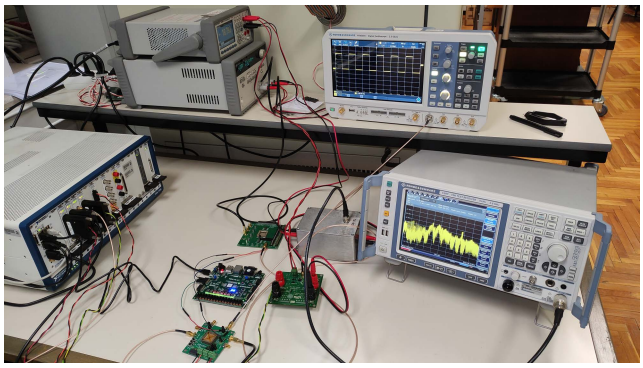

FIGURE 11. The measurement set-up used to test the PLL divider generator designs.

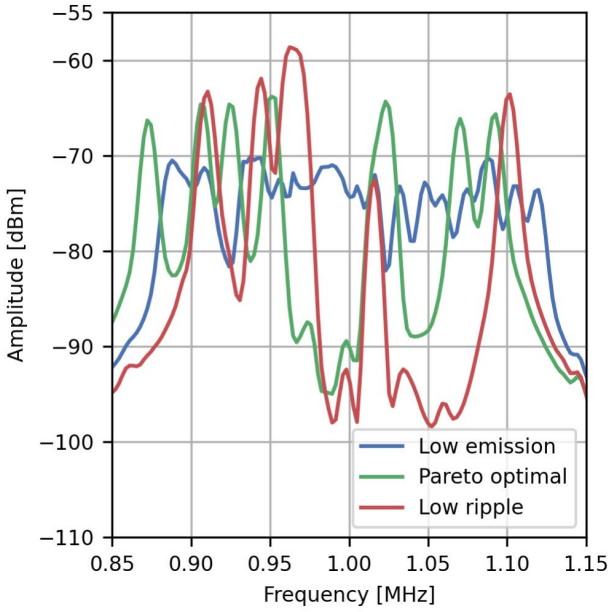

FIGURE 12. The measured EMI frequency spectra of the buck converter for the LFSR-based controller designs.

which is described in more detail in [27]. The programmable divider has an SPI communication port which is used to set the divider values generated by the divider generator.

The used EMI receiver is Rohde & Schwarz ESRP which is set to measure in the CISPR frequency bands A and B, i.e. from 150 kHz to 30 MHz with a resolution bandwidth of a 9 kHz. The average detector is used with measuring time of 1 s. The Coupling-Decoupling Network decouples the EMI generated by the buck converter from the power supply and redirects it towards the EMI receiver and it is used to measured the common-mode conducted EMI [28].

The buck converter is supplied by the power supply Keysight E3646A which supplies the input voltage $V_{IN} = 5$ V. The output of the buck converter is connected to an electronic load which consists of the NI PXIe-4139 Source Measure Unit (SMU). The output voltage is measured using the Rohde & Schwarz RTB2004 oscilloscope. The duty cycle of the

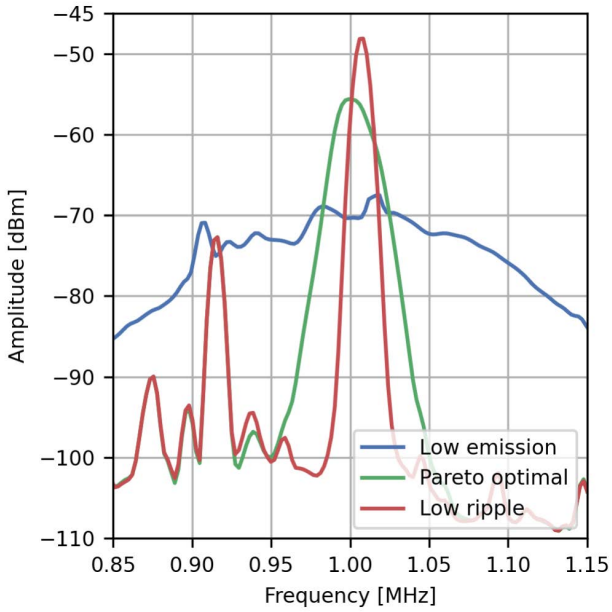

FIGURE 13. The measured EMI frequency spectra of the buck converter for the memory-based controller designs.

output voltage is calculated by dividing the measured output voltage by the set input voltage as defined in relation (8).

C. MEASUREMENT RESULTS

Fig. 12 shows the measured EMI frequency spectra of the buck converter for the LFSR-based controller designs in the frequency range of interest. The measured EMI spectrum in the case of the low emissions design is flattest and has an overall lowest amplitude, while the low ripple design has the highest, narrowest measured EMI spectrum. The Pareto-optimal LFSR-based design has the EMI spectrum which is qualitatively in between the previous two designs. These measurement observations agree with the model-based expectations shown in Fig. 6.

Fig. 13 shows the measured EMI frequency spectra of the buck converter for the memory-based controller designs in the frequency range of interest. The measured EMI spectrum in the case of the memory-based designs clearly showcases the aim of the co-optimization procedure. The EMI of the low emissions design has a flat, wide spectrum which is typical when applying the spread-spectrum technique. The low ripple design spectrum shows the opposite case where all of the EMI is concentrated in a single peak. Again, the Pareto-optimal design exhibits an intermediate EMI spectrum. These measurement observations agree with the model predictions shown in Fig. 9.

Fig. 14 shows the measured output voltage ripple of the buck converter for the LFSR-based controller designs. All of the measured waveforms have a visible periodic nature with the low ripple design having the shortest period. The low ripple design waveform has indeed the lowest duty cycle ripple of approx. 5% peak-to-peak, while the low emission design

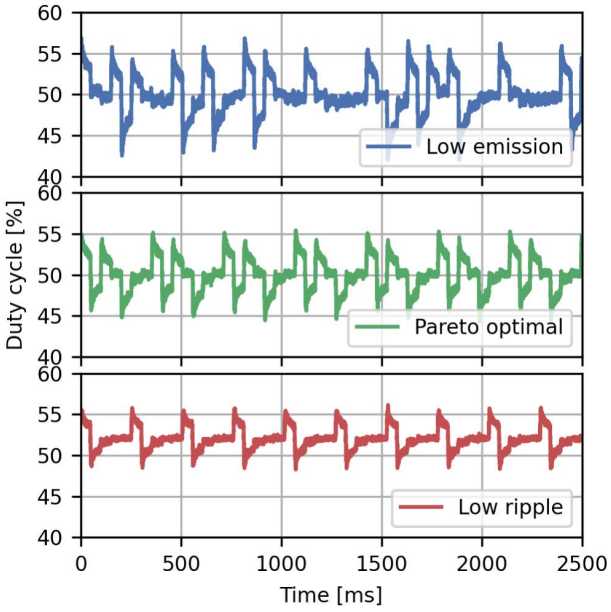

FIGURE 14. The measured output voltage ripple of the buck converter for the LFSR-based controller designs.

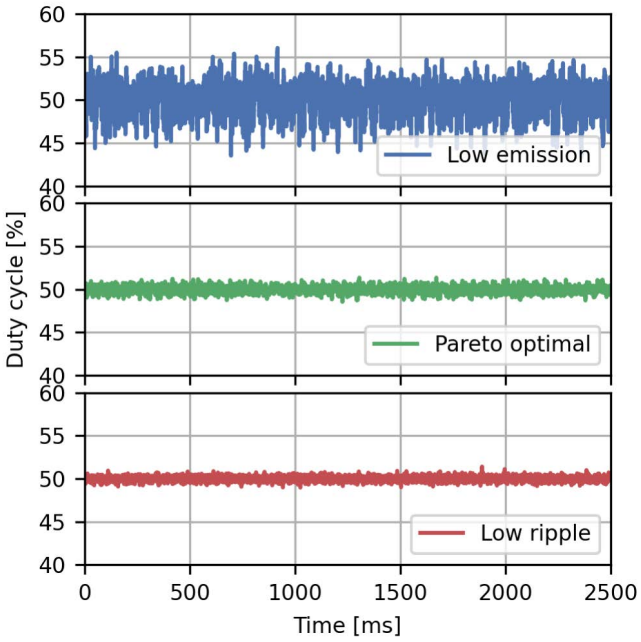

FIGURE 15. The measured output voltage ripple of the buck converter for the memory-based controller designs.

has approx. double the duty cycle ripple. These observations are in line with the numerical model estimations shown in Fig. 7.

Fig. 15 shows the measured output voltage ripple of the buck converter for the memory-based controller designs. Both the low ripple and the Pareto-optimal designs have a very low duty cycle ripple, while the low emissions design has a much higher duty cycle ripple. The duty cycle ripple measurements show a typical random, i.e. noisy waveforms. These observations agree with the modelling results shown in Fig. 10.

D. CO-OPTIMIZATION AND MEASUREMENT RESULTS COMPARISON

The co-optimization and the measurement results for both the LFSR- and memory-based designs are compared in a tabular form. The comparison is based on calculating the results difference between the different designs with Pareto-optimal design being the reference design (signified by the zero difference value in the tables).

Table 4 shows the EMI results comparison of the spread-spectrum controller designs. The LFSR-based designs have approx. −8/+5 dB estimated EMI levels with respect to the reference, Pareto-optimal design and similarly the measurements show −6/+5 dB EMI levels with respect to the reference design. The memory-based designs have approx. -13/+7 dB estimated EMI levels with respect to the reference and similarly the measurements show −12/+8 dB EMI levels with respect to the reference design. The measurements also show that the memory-based designs span a greater range of EMI levels than the LFSR-based design (approx. 20 vs. 11 dB).

The low emission designs for both the LFSR- and the memory-based generators produce a similar levels of EMI which makes them both suitable in spread-spectrum technique for purely EMC-optimal applications.

Table 5 shows the duty cycle ripple results comparison of the spread-spectrum controller designs. The LFSR-based designs have approx. 1.2/0.75 times the duty cycle ripple with respect to the reference, Pareto-optimal design and similarly the measurements show approx. 1.2/0.63 times the duty cycle ripple with respect to the reference design. The memory-based designs have approx. 5.4/0.23 times the duty cycle ripple with respect to the reference and similarly the measurements show 6/0.32 times the duty cycle ripple with respect to the reference design. The measurements also show that the memory-based designs span a much greater range of the duty cycle ripple than the LFSR-based design (approx. 2 vs. 20 times).

The low emission designs for both the LFSR- and the memory-based generators have a similar level of duty cycle ripple. The low ripple design for the case of the memory-based generator has more than order of magnitude smaller duty cycle ripple.

Both Figures-of-Merit span greater ranges in the case of the memory-based designs which makes those designs more suitable for the co-optimization procedure. Furthermore, the memory-based designs feature a large range of duty cycle ripple values which allows for fine tuning the designs with respect to the duty cycle ripple Figure-of-Merit.

The presented comparison shows that the developed models can be used to effectively model the EMI and the duty cycle ripple for the purpose of co-optimizing these values

TABLE 4. The EMI results comparison of the spread-spectrum controller designs.

	LFSR-based				Memory-based			
	Co-optimization		Measurements		Co-optimization		Measurements	
Design	Spectrogram peak [dB]	Diff. [dB]	Spectrogram peak [dBm]	Diff. [dB]	Spectrogram peak [dB]	Diff. [dB]	Spectrogram peak [dBm]	Diff. [dB]
Low Emissions	15.76	-7.74	-70.12	-6.29	16.67	-12.76	-67.57	-11.95
Pareto Optimal	23.50	0	-63.83	0	29.43	0	-55.62	0
Low Ripple	28.16	+4.66	-58.66	+5.17	36.90	+7.47	-48.12	+7.50

TABLE 5. The duty cycle ripple results comparison of the spread-spectrum controller designs.

	LFSR-based				Memory-based			
	Co-optimization		Measurements		Co-optimization		Measurements	
Design	Duty cycle RMS ripple [%]	Diff. [%]	Duty cycle RMS ripple [%]	Diff. [%]	Duty cycle RMS ripple [%]	Diff. [%]	Duty cycle RMS ripple [%]	Diff. [%]
Low Emissions	3.558	1.185x	3.654	1.209x	3.192	5.448x	2.951	6.016x
Pareto Optimal	3.002	0	3.021	0	0.5858	0	0.4905	0
Low Ripple	2.252	0.7501x	1.896	0.6276x	0.1372	0.2342x	0.1549	0.3158x

and designing a PLL divider generator with desired qualities. While the numerical models do not estimate exact values of the Figures-of-Merit, they accurately model the relative ratios of the Figures-of-Merit of considered divider generator designs. This enables a purposeful co-optimization of the Figures-of-Merit and designs a Pareto-optimal PLL divider generator.

The estimated and the measured values of the duty cycle ripple are in a better agreement than the estimated and the measured EMI levels. This can be attributed to the fact that the the duty cycle ripple Figure-of-Merit is represented by Root-Mean-Square value which features an integrating quality over all estimated or measured values, while the EMI Figure-of-Merit is represented by a single, maximum value which is more prone to the noise influence.

VI. CONCLUSION

The spread-spectrum technique is used to improve the EMC performance of a buck converter by spreading the electromagnetic interference caused by switching. This technique is based on changing the switching frequency in time which also changes the duty cycle of the buck converter and causes a ripple in the output voltage. The main design factor in the spread-spectrum technique is the way the switching frequency is modulated. This paper analyses a spread-spectrum controller which uses a Phase Locked Loop with a programmable divider to generate the changing switching frequency. The LFSR- and memory-based divider generators are considered and they are optimized with respect to the developed numerical EMI and duty cycle ripple Figures-of-Merit. The results show that the memory-based generator is more suitable for the co-optimization procedure and it yields designs which show better performance in terms of EMI and duty cycle ripple compared to the LFSR-based designs, while having a larger programmable logic footprint. The designs are physically verified in a buck converter and the measurements of generated EMI and output voltage ripple confirmed the estimated ratios of the modelled Figures-of-Merit.

REFERENCES

[1] B. Chen, "Fully integrated isolated DC–DC converter using micro-transformers," in *Proc. 23rd Annu. IEEE Appl. Power Electron. Conf. Exposit.*, Feb. 2008, pp. 335–338.
[2] R. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*. New York, NY, USA: Springer, 2001.
[3] M. K. Kazimierczuk and D. Czarkowski, *Resonant Power Converters*. Hoboken, NJ, USA: Wiley, 2011.
[4] N. Bertoni, G. Frattini, R. G. Massolini, F. Pareschi, R. Rovatti, and G. Setti, "An analytical approach for the design of class-E resonant DC–DC converters," *IEEE Trans. Power Electron.*, vol. 31, no. 11, pp. 7701–7713, Nov. 2016.
[5] C. Paul, *Introduction to Electromagnetic Compatibility*. Hoboken, NJ, USA: Wiley, 2006.
[6] Z. Tianting, Z. Yue, and C. Baoxing, "An isolated DC–DC converter with fully integrated magnetic core transformer," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, Austin, TX, USA, Apr. 2017, pp. 1–4.
[7] M. Cantrell, "Recommendations for control of radiated emissions with *iso*power devices," Analog Devices, Norwood, MA, USA, Application note AN-0971, 2014.
[8] F. Pareschi, R. Rovatti, and G. Setti, "EMI reduction via spread spectrum in DC/DC converters: State of the art, optimization, and tradeoffs," *IEEE Access*, vol. 3, pp. 2857–2874, 2015.
[9] F. Pareschi, G. Setti, and R. Rovatti, "A 3-GHz serial ATA spread-spectrum clock generator employing a chaotic PAM modulation," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 57, no. 10, pp. 2577–2587, Oct. 2010.
[10] B. Deutschmann, G. Winkler, and T. Karaca, "Emission reduction in class D audio amplifiers by optimizing spread spectrum modulation," in *Proc. 10th Int. Workshop Electromagn. Compat. Integr. Circuits (EMC Compo)*, Edinburgh, Nov. 2015, pp. 1–6.
[11] X. Ming, Z. Chen, Z.-K. Zhou, and B. Zhang, "An advanced spread spectrum architecture using pseudorandom modulation to improve EMI in class D amplifier," *IEEE Trans. Power Electron.*, vol. 26, no. 2, pp. 638–646, Feb. 2011.
[12] V. Subotskaya, K. Cherniak, K. Hoermaier, and B. Deutschmann, "Emission reduction with spread spectrum clocking for switched capacitor buck converter," in *Proc. IEEE Int. Symp. Electromagn. Compat. IEEE Asia–Pacific Symp. Electromagn. Compat. (EMC/APEMC)*, Singapore, May 2018, pp. 297–302.
[13] F. Pareschi, G. Setti, R. Rovatti, and G. Frattini, "Practical optimization of EMI reduction in spread spectrum clock generators with application to switching DC/DC converters," *IEEE Trans. Power Electron.*, vol. 29, no. 9, pp. 4646–4657, Sep. 2014.

[14] H.-P. Park, M. Kim, and J.-H. Jung, "Spread spectrum technique to reduce EMI emission for an LLC resonant converter using a hybrid modulation method," *IEEE Trans. Power Electron.*, vol. 33, no. 5, pp. 3717–3721, May 2018, doi: 10.1109/TPEL.2017.2766284.
[15] R. Wang, Z. Lin, J. Du, J. Wu, and X. He, "Direct sequence spread spectrum-based PWM strategy for harmonic reduction and communication," *IEEE Trans. Power Electron.*, vol. 32, no. 6, pp. 4455–4465, Jun. 2017, doi: 10.1109/TPEL.2016.2597005.
[16] S. Kennedy, M. R. Yuce, and J.-M. Redoute, "Evaluation of conducted emission test methods for charge pump DC/DC converters," *IEEE Trans. Rel.*, vol. 66, no. 1, pp. 170–177, Mar. 2017, doi: 10.1109/TR.2016.2633532.
[17] M. Faisal, J. Yousaf, and W. Nah, "Effect of random modulation switching schemes on harmonics and CE levels of a buck converter," in *Proc. Int. SoC Design Conf. (ISOCC)*, Oct. 2019, pp. 208–209, doi: 10.1109/ISOCC47750.2019.9027744.
[18] C.-H. Moon, C.-J. Chen, and S.-W. Lee, "A random modulation spread-spectrum digital PWM for a low system clock digital buck converter," *IEEE Access*, vol. 9, pp. 156663–156671, 2021, doi: 10.1109/ACCESS.2021.3126556.
[19] R. Gamoudi, D. Elhak Chariag, and L. Sbita, "A review of spread-spectrum-based PWM techniques—A novel fast digital implementation," *IEEE Trans. Power Electron.*, vol. 33, no. 12, pp. 10292–10307, Dec. 2018, doi: 10.1109/TPEL.2018.2808038.
[20] G. M. Dousoky, M. Shoyama, and T. Ninomiya, "FPGA-based spread-spectrum schemes for conducted-noise mitigation in DC–DC power converters: Design, implementation, and experimental investigation," *IEEE Trans. Ind. Electron.*, vol. 58, no. 2, pp. 429–435, Feb. 2011, doi: 10.1109/TIE.2010.2049708.
[21] B. Razavi, *Design of CMOS Phase-Locked Loops: From Circuit Level to Architecture Level*. Cambridge, U.K.: Cambridge Univ. Press, 2020.
[22] D. K. Cheng, *Field and Wave Electromagnetics*. India: Pearson Education, 1989.
[23] A. Sigrún, "A review of random search methods," in *Handbook of Simulation Optimization*. New York, NY, USA: Springer, 2015, pp. 277–292.
[24] Xilinx. *Vivado Design Suite User Guide: Synthesis*. Accessed: Nov. 25, 2022. [Online]. Available: https://www.xilinx.com/content/dam/xilinx/support/documents/sw-manuals/xilinx2021-2/ug901-vivado-synthesis.pdf
[25] Digilent. *Nexys A7 Reference Manual*. Accessed: Nov. 25, 2022. [Online]. Available: https://digilent.com/reference/programmable-logic/nexys-a7/reference-manual
[26] Vishay. *Datasheet 50 A VRPower® Integrated Power Stage SiC651*. Accessed: Nov. 25, 2022. [Online]. Available: https://www.vishay.com/docs/77108/sic651.pdf
[27] J. Kundrata, I. Skeledzija, and A. Baric, "Voltage regulation in an integrated controller of a spread-spectrum-clocked buck converter," in *Proc. 45th Jubilee Int. Conv. Inf., Commun. Electron. Technol. (MIPRO)*, 2022, pp. 185–190, doi: 10.23919/MIPRO55190.2022.9803464.
[28] *Electromagnetic Compatibility (EMC)—Part 4–6: Testing and Measurement Techniques—Immunity to Conducted Disturbances, Induced by Radio-Frequency Fields*, document IEC 61000-4-6:2013, Accessed: Nov. 25, 2022. [Online]. Available: https://webstore.iec.ch/publication/4224

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