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RESEARCH ARTICLE

Robust Control and Stable Performance of a Grid-Tied Dumbbell-Type Multilevel Converter Interfaced DG Unit Using Differential Flatness Theory

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ABSTRACT This paper proposes a robust control technique based on Differential Flatness Theory (DFT) for a grid-tied Distributed Generation (DG) to mitigate several uncertainties while controlling the DG for its main functions. A recently introduced structure named Dumbbell Type (D-type) Switched-Capacitor Multilevel Converter (SC-MLC) with a single DC source, utilizing only ten switches with no further series diodes, is employed as an interfacing converter. The DFT enriched by the Lyapunov criterion is developed for the SC-MLC to guarantee both the stable performance of the proposed DG-based supply system and the robustness feature against any unwanted uncertainties. The control inputs of the D-type converter are initially shaped using the reactive and active power-based flat outputs without the observance of stability issues. To attain the proposed robust control inputs, a Lyapunov function is properly defined and engaged in providing the global asymptotic stability for the grid-tied multilevel converter by means of the proportional and integral errors of the flat outputs under the model uncertainties and parameter change. Lyapunov coefficients are subsequently assessed through their related active and reactive power errors. Both simulation and experimental results are employed to verify the ability of the proposed generation system in robust performance against parameter alternations, transient stability during contingency events at the grid side, and dynamic and steady state stability under different scenarios of power sharing with direct active and reactive power flows control.

INDEX TERMS Multilevel converter, grid-tied distributed generation (DG), D-type switched capacitor multilevel converter (SC-MLC), differential flatness theory (DFT), Lyapunov stability, robust controller.

I. INTRODUCTION

By increasing the use of renewable energy sources (RESs), the penetration of distributed generation (DG) units based on power electronic converters (PECs) in electrical grids is accelerating rapidly. On the other hand, designers face

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challenges in determining how to combine the best of circuit topology and control in their proposed DG units due to the wide variety of power converter topologies and available control methods. A control system must be accurately designed and matched with the converter in such a way that it could follow all predefined functions in a stable manner while being robust against unwanted uncertainties and having the best dynamic and steady-state responses.

One of the most essential features required to be supported by the interfacing converter in a DG system is the capability of boosting the voltage, especially when the DC side is supplied by low voltage renewable energy sources (RES) such as photovoltaic system (PV). It means that the output voltage amplitude will be higher than the supply voltage source. This important feature which has not been incorporated even in more recent structures such as Packed E-Cell (PEC) [1] and U-Cell (PUC) [2], eliminates the need for bulky transformers or inductors. Another concern about the interfacing converter is hiring a voltage balancing strategy of DC capacitors that should be performed accurately in neutral point clamped (NPC) [3] and flying capacitor (FC) [4] converters that suffer from limited switching states. This concern severely exists in cascaded H-Bridges (CHB) [5], especially when numerous DC sources are required that result in increased cost and size of the converter as well. So, the ability of self-balancing is assumed as an effective feature that should be considered in the converter employed in the DG systems.

Switched Capacitor Multilevel Converters (SC-MLCs) are considered significant progress in this context [6]. Unlike conventional CHB, FC and NPC, SC-MLCs can be structured to benefit from both voltage boosting and self-voltage balancing abilities without the need to use bulky transformers or auxiliary circuits for capacitors voltage balancing. To reach this end, they employ several capacitors in series or parallel and use fewer DC power supplies than other concepts to synthesize multilevel output voltage.

Recently, a modified SC-MLC named Dumbbell Type (D-type) has been introduced in [7] to diminish the drawbacks of the original one regarding less peak inverse voltage (PIV), total standing voltage (TSV), total harmonic distortion (THD), and overall cost. This converter can be a great option to be employed as an interfaced grid-tied single-phase DGs due to important features such as the boosting capability and the ability of capacitors' voltage self-balancing without the need for auxiliary circuits, which simplifies the controller design.

Although D-type SC-MLC provides several advantages, it needs more considerations to be qualified as an applicable interfacing converter in a DG system including its control mechanism, transient and dynamic stability, and robustness feature. While both standalone and grid-connected operations of a converter can be conducted by similar modulations, the latter needs further considerations for synchronization, voltage regulation, and power sharing criteria. Therefore, the control strategy incorporated in grid-tied DG systems interfaced by D-type SC-based MLC should also satisfy critical requirements such as stability, less computational burden, robustness against parameter changes, and the excellent dynamic and steady-state performance.

In the literature, several control strategies have been introduced to control PECs in DG applications. While each strategy offered some functionalities and advantages, the following shortcomings have been identified. A classic controller has not shown satisfactory performance in both

dynamic and steady-state operation [8]. Linear resonance and feedback feedforward controllers exhibit unsatisfactory transient behavior due to their linear feature [9]. Model Predictive Control (MPC) based strategy is highly dependent on the accuracy of the system model [10], [11]. In control schemes based on fuzzy logic, working out proper rules and comprehensiveness as well as persistency of rules, tuning several parameters including fuzzification, defuzzification and inference are assumed as the main limitations [12]. Artificial Neural Network (ANN)-based strategies need comprehensive training and usually do not perform well in situations for which they were not trained [13]. Adaptive control needs an accurate model of the system [14], [15]. A control system based on sliding mode suffers from chattering and is limited to discontinuous control law [16]. Back-stepping control strategy is sensitive to parameter alternation and may need non-linear observers [17].

Among different control strategies, the approach based on differential flatness theory (DFT) is preferred for nonlinear control of parallel DC/AC converters [18]. This method was established in the nineties [19] and became a promising technique for providing stable responses for nonlinear systems in various applications [18], [20]. The flatness theory has been able to characterize the flat system behavior and its stability margin, leading to a more precise control design [21]. This strategy was employed for a multiphase interleaved DC-DC converter to solve the stabilization problems [22]. Moreover, authors in [23] presented a differential flatness-based full-order nonlinear control for a modular multilevel converter (MMC) to attain a very high dynamic performance when both noisy measurements and parametric disturbances existed. As one of the exclusive merits of the DFT-based approach, both active and reactive power flows are forced to track their desired values with a fast dynamic execution [20]. This method of control not only guarantees the robustness of the DG unit against uncertainties but also has better transient behavior in comparison with conventional control techniques such as PI controller [20], [24]. So, it can be considered an effective control method for PEC control in grid-connected DG applications.

The strategy based on the Lyapunov theory is a reliable tool to assess the stability margin in power converters. Paper [25] proposes a control system based on the Lyapunov stability criteria for modular multilevel converter (MMC)-based STATCOM to achieve fast dynamic and accurate tracking response. The transient stability domain of a grid-forming inverter is calculated in [26] using the Lyapunov stability theory. Paper [27] uses the adaptive finite-set model predictive control (AMPC) stabilized through Lyapunov stability criteria to overcome the problem of finite-set model predictive control (FSMPC) which fails to assure system stability. A grid current synchronization in a grid-connected packed-E cell (PEC) inverter is achieved in [28] by using a phase locked loop (PLL) based on Lyapunov filter.

In this paper, a DFT-based control system is designed for a D-type SC-MLC to develop a new grid-connected

DG system. The proposed power generation unit is robust against several uncertainties, such as unwanted changes in PCC voltage or the values of passive components. In this system, the DFT theory is enriched by the Lyapunov stability criterion in such a way that the converter follows critical functions such as accurate power-sharing as well as power quality and guarantees the dynamic and steady-state stability as well as the robustness of the proposed DG system.

The proposed DFT based D-type SC-MLC has the distinctive attributes described as follows:

- Since the voltages of the capacitors are self-balanced, this term is neglected in dynamic state-space equation, leading to more effective and more simple flat outputs for the proposed DFT based controller.
- An effective design of the control process is executed in which unnecessary complication is avoided and as such the external control loop is not essential.
- The controller only takes the output current dynamics into account for forming the DFT flat outputs.
- A Lyapunov function based on the integral and proportional errors of flat outputs guarantees the stability of the converter against disturbances, errors, and uncertainties.
- The proposed method provides advantages such as robustness, accurate power sharing ability, and direct control of active and reactive power as the state variables.

In the proposed control system, the instantaneous active and reactive power of the D-type SC-MLC are defined as the flat outputs. The switching functions with and without stability considerations are achieved by employing the Lyapunov criterion. Further, mathematical assesment is also accomplished to obtain the relations between the flat outputs and their errors for evaluating the variation trend of Lyapunov coefficients.

The rest of the paper is organized as follows. The structure of the topology is investigated in section II. Then, the proposed DFT control strategy is described in section III. This section consists of two sub-sections that explain the original DFT and Lyapunov-based DFT models, respectively. In section IV, the assessment of the controller coefficients is discussed. Afterward, the performance evaluation of proposed converter and its control mechanism via both simulations and laboratory experiments are accomplished in sections V and VI, respectively. Finally, the conclusion is provided in section VII.

II. INTRODUCING THE GRID-CONNECTED TOPOLOGY

A topological structure of the proposed grid-connected DG including D-type MLC and DFT-based control system is presented in Fig.1 (a). From the circuit diagram depicted in Fig.1(b) and (c), the SC-MLC utilizes two capacitors and only ten switches including eight unidirectional and one bidirectional to shape the output voltage waveform. The peak voltage stress of this topology is twice the input voltage (the PIV is $2 \times V_{dc}$) [7]. Both capacitors are directly charged by a DC power supply. Capacitors C_1 and C_2 have the same

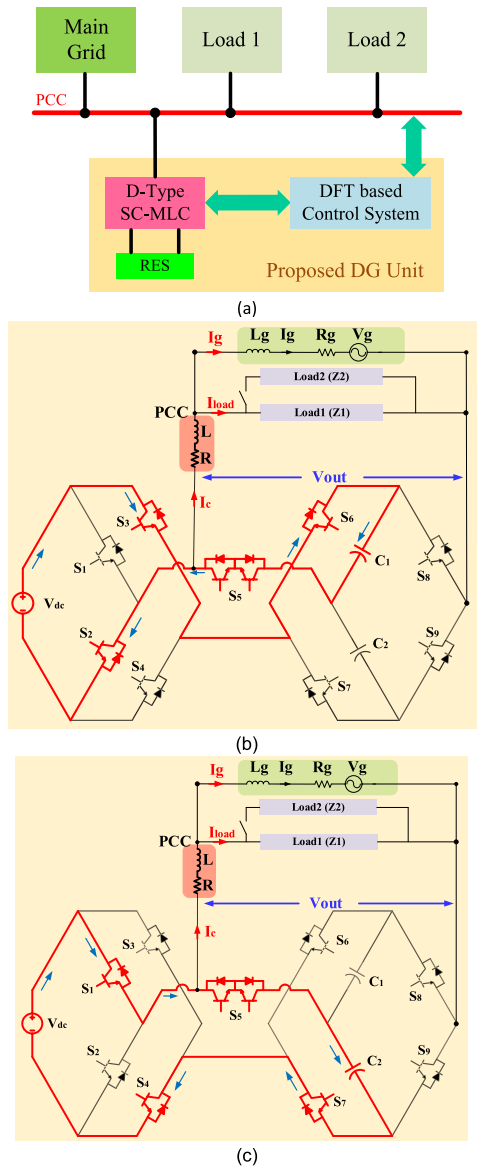


FIGURE 1. A topological overview of: (a) proposed grid-tied SC-MLC based DG, (b) charging path for C_1 and (c) charging path for C_2 .

capacitance values. The equivalent capacitance of the circuit (C_{eq}) while supplying the load can be determined by $C_{eq} \geq \Delta Q_c / kV_{dc}$; where, k is the maximum acceptable voltage ripple, as represented in [7]. The appropriate charging path for C_1 and C_2 are depicted in Fig.1(b) and (c) respectively. The output voltage of the converter (V_{out}) is formed by using predefined current flow paths during specific time intervals. To reach this goal, each state is shaped by the help of several switches and capacitors. In fact, by arranging various current paths for supplying the load, using a series combination of two capacitors besides the input power supply during the peak voltage period, a voltage three times V_{dc} is generated. The output voltage levels of the proposed converter consist of $(0, \pm 1, \pm 2, \pm 3) \times V_{dc}$ levels. To reach this goal, the corresponding arrangement as described in Table 1 is defined. For enforcing the multilevel converter to operate commensurate

with the mentioned points, the Phase Disposition Pulse Width Modulation (PD-PWM) technique is applied. More details about the D-type SC-MLC circuit analysis and its operation are provided in the previously published paper [7].

TABLE 1. Active switches for generating each voltage level.

Output Voltage	Correspond Switches
$+3 \times V_{dc}$	S_1, S_4, S_6, S_9
$+2 \times V_{dc}$	S_1, S_3, S_6, S_9
$+1 \times V_{dc}$	S_1, S_4, S_5, S_7, S_9
$0 \times V_{dc}$	S_1, S_3, S_6, S_8
$-1 \times V_{dc}$	S_2, S_3, S_5, S_6, S_8
$-2 \times V_{dc}$	S_2, S_4, S_7, S_8
$-3 \times V_{dc}$	S_2, S_3, S_7, S_8

III. DFT-BASED CONTROL STRATEGY

This section explains the design of the control system based on DFT for the D-type SC-MLC. In the first sub-section, the general design of the controller is performed without considering any stability condition. In the next sub-section, the Lyapunov criterion is employed for specifying the controller inputs as well as guaranteeing the stability condition.

A. DFT MODEL

Based on Fig.1 (b) and (c), dynamic model of the converter which describes the relationship between the input DC voltage, output voltage and output current is defined as (1).

$$L \frac{di_c}{dt} + Ri_c - uv_{dc} + v_{PCC} = 0 \quad (1)$$

where i_c and v_{PCC} represent the converter current and PCC voltage, respectively. R and L are equivalent resistance and inductance of the converter filter and $uv_{dc} = v_{out}$ is the converter output voltage. Using the matrix transformation given by (2) and the orthogonal components ($x^{\alpha, \beta}$), the d - q reference frame dynamic model of the converter is obtained as (3) and (4).

$$\begin{bmatrix} x^d \\ x^q \end{bmatrix} = \begin{bmatrix} \sin(\omega t) & -\cos(\omega t) \\ \cos(\omega t) & \sin(\omega t) \end{bmatrix} \begin{bmatrix} x^\alpha \\ x^\beta \end{bmatrix} \quad (2)$$

$$L \frac{di_c^d}{dt} + Ri_c^d - \omega Li_c^q - u^d v_{dc} + v_{PCC}^d = 0 \quad (3)$$

$$L \frac{di_c^q}{dt} + Ri_c^q + \omega Li_c^d - u^q v_{dc} + v_{PCC}^q = 0 \quad (4)$$

These dynamic equations are utilized to develop the DFT-based control strategy and assess the variations in the controller inputs and their impacts on the flat outputs. According to the DFT principle, the output variables of the flat systems can be defined as a function of the input and state variables along with a finite number of their time derivatives as defined in (5) [18], [19], [20].

$$y = g(x, u^{(1)}, u^{(2)}, u^{(3)}, \dots, u^{(\lambda)}) \quad (5)$$

A prominent feature of DFT is that the input and state variables can be represented directly in terms of the flat

outputs and a finite number of their time derivatives as given in (6).

$$\mathbf{U} = \Psi(y^{(1)}, y^{(2)}, y^{(3)}, \dots, y^{(\kappa)}) \quad (6)$$

Based on these definitions and by considering the dynamic equations defined by (3) and (4), a DFT-based control strategy will be designed. The DFT variables including the control input vector (\mathbf{U}) and state variables (\mathbf{X}) as well as the flat outputs (\mathbf{Y}) are defined as,

$$\mathbf{X} = \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} = \begin{bmatrix} i_c^d \\ i_c^q \end{bmatrix}, \quad \mathbf{U} = \begin{bmatrix} u_1 \\ u_2 \end{bmatrix} = \begin{bmatrix} u_d \\ u_q \end{bmatrix}, \quad (7)$$

$$\mathbf{Y} = \begin{bmatrix} y_1 \\ y_2 \end{bmatrix} = \begin{bmatrix} P \\ Q \end{bmatrix}$$

According to (8), the state variables are expressed as a function of the instantaneous active and reactive power of the converter that are assumed as the flat outputs.

$$\mathbf{X} = \Psi(\mathbf{Y}) = [\Psi(y_1) \quad \Psi(y_2)]^T = \left[\frac{y_1}{v_{PCC}^d} \quad \frac{-y_2}{v_{PCC}^d} \right]^T \quad (8)$$

It is deduced from (8) that the d and q components of the converter currents ($i_c^{d,q}$) are adequate to be considered as the state variables to describe the flat outputs. In addition, since the voltages of the capacitors are self-balanced, it is not necessary to consider them as state variables and their dynamics can be neglected in overall model of the converter. So, the proposed second-order model of the converter can sufficiently represent its dynamic characteristics to be incorporated in the DFT based control scheme. The proposed converter model is considered to be flat if all state variables and flat outputs can be found from the dynamic equations. In this model, the differential term of the flat output is expressed by the state and input variables with no integration part. By considering (3), (4), and (8) and variables defined by (7), the control inputs (u_1 and u_2) are achieved in terms of dynamic flat outputs as represented by (9) and (10).

$$u_1 = \frac{L}{v_{PCC}^d v_{dc}} \dot{y}_1 + \frac{1}{v_{PCC}^d v_{dc}} (R - L \frac{\dot{v}_{PCC}^d}{v_{PCC}^d}) y_1 + \frac{L\omega}{v_{PCC}^d v_{dc}} y_2 + \frac{v_{PCC}^d}{v_{dc}} \quad (9)$$

$$u_2 = \frac{-L}{v_{PCC}^d v_{dc}} \dot{y}_2 + \frac{1}{v_{PCC}^d v_{dc}} (L \frac{\dot{v}_{PCC}^d}{v_{PCC}^d} - R) y_2 + \frac{L\omega}{v_{PCC}^d v_{dc}} y_1 + \frac{v_{PCC}^q}{v_{dc}} \quad (10)$$

These input variables are the switching functions generated by the proposed DFT-based strategy. The input variables will control the operation of the SC-MLC without guaranteeing the stability. The next sub-section will concentrate on this issue.

B. LYAPUNOV-BASED DFT MODEL

In order to guarantee the stability of the proposed control strategy especially when the uncertainty such as variation in

the converter impedance occurs, the Lyapunov criterion is utilized in this sub-section. The flat output errors are defined as the proportional error (e_{1j}) and integral error (e_{2j}) represented by (11).

$$\begin{cases} e_{1j} = y_j^* - y_j \\ e_{2j} = \int (y_j^*(t) - y_j(t))dt \end{cases}, \quad j = 1, 2 \quad (11)$$

The Lyapunov function is defined in (12) to make the control commands such that they force the aforementioned flat output errors to decrease towards zero.

$$V(e_{1j}, e_{2j}) = \frac{1}{2} \sum_{i=1,2} \sum_{j=1,2} e_{ij}^2 \quad (12)$$

It should be ensured that the flat output errors are highly inclined to zero. To this end, supposing $e_{2j} = e_{1j}$ achieved from (11), the time derivative of (12) can meet.

$$\dot{V}(e_{1j}, e_{2j}) = \sum_{j=1,2} (e_{1j}\dot{e}_{1j} + e_{2j}\dot{e}_{1j}) \quad (13)$$

Although there is no concern regarding the capacitors' voltage in the steady state as they are able to be balanced with no need for auxiliary circuits, but they may be affected by some disturbance at ac side, and therefore, it should be considered in the controller design. In order to address this issue, the DC link voltage (v_{dc}) is set to $\frac{v_{C1}+v_{C2}}{2}$ in the Lyapunov function and the variation of the capacitors' voltage are defined by considering the voltage changes (Δv_{C1} and Δv_{C2}) as $v'_{C1} = v_{C1} + \Delta v_{C1}$, $v'_{C2} = v_{C2} + \Delta v_{C2}$. By assuming ΔR and ΔL as an alteration in the impedance of the converter output filter and considering $R + \Delta R \triangleq R'$ and $L + \Delta L \triangleq L'$, after substituting \dot{y}_j from (9) and (10) into the derivation of (11), (13) can be rewritten according to (14).

$$\dot{V} = \begin{pmatrix} e_{11} \begin{pmatrix} \dot{y}_1^* - \frac{\dot{v}_{PCC}^d}{v_{PCC}^d} y_1 + \frac{R'}{L'} y_1 + \omega y_2 \\ -\frac{1}{L'} v_{PCC}^d (\frac{v'_{C1} + v'_{C2}}{2}) u_1 \\ + \frac{1}{L'} (v_{PCC}^d)^2 + e_{21} \end{pmatrix} \\ + e_{12} \begin{pmatrix} \dot{y}_2^* - \frac{\dot{v}_{PCC}^d}{v_{PCC}^d} y_2 + \frac{R'}{L'} y_2 - \omega y_1 \\ + \frac{1}{L'} v_{PCC}^d (\frac{v'_{C1} + v'_{C2}}{2}) u_2 \\ - \frac{1}{L'} v_{PCC}^d v_{PCC}^q + e_{22} \end{pmatrix} \end{pmatrix} \quad (14)$$

According to the Lyapunov criterion, (14) should have a negative value so that the stability condition of the SC-MLC will be guaranteed. Eq. (15) represents a condition through which (14) reaches negative value or equalizes to zero.

$$\dot{V} = - \sum_{j=1,2} k_j e_{1j}^2, \quad k_j > 0 \quad (15)$$

When the stability condition is applied by equalizing (14) and (15), the first and the second terms in the brackets are

equalised to $k_1 e_{11}$ and $k_2 e_{12}$, respectively. The proposed control inputs are obtained according to (16) and (17).

$$u_1 = \frac{2L'}{v_{PCC}^d (v'_{C1} + v'_{C2})} (\dot{y}_1^* - \frac{\dot{v}_{PCC}^d}{v_{PCC}^d} y_1 + \frac{R'}{L'} y_1 + \omega y_2 + \frac{1}{L'} (v_{PCC}^d)^2 + e_{21} + k_1 e_{11}) \quad (16)$$

$$u_2 = \frac{2L'}{v_{PCC}^d (v'_{C1} + v'_{C2})} (-\dot{y}_2^* + \frac{\dot{v}_{PCC}^d}{v_{PCC}^d} y_2 - \frac{R'}{L'} y_2 + \omega y_1 + \frac{1}{L'} v_{PCC}^d v_{PCC}^q - e_{22} - k_2 e_{12}) \quad (17)$$

The proposed control inputs lead to the global asymptotic stability of the flat outputs and make the converter operation stable. Fig. 2 presents the block-diagram of the proposed DFT-based control strategy wherein (18) is used as the general format of (16) and (17). According to this diagram, only the measurements at the load side are needed and the load model is not required to be incorporated in the equations of the control strategy. It should be noted that since y_j^* has been considered as a constant value, its derivative was equalized to zero. Also, since proposed converter is tied to the grid, it is supposed that the d-component of PCC voltage has approximately no fluctuations leading to a derivative controller without noises in its output (or approximately zero value in the output). Otherwise, to deal with the noises made by the derivative part, a low pass filter (LPF) along with a limiter can be employed in the derivation unit.

When the values of parameters and variables such as R, L , or $V_{C1,2}$ changed to R', L' , and $V'_{C1,2}$, respectively, the controller keeps the flat output errors (active and reactive power of the converter) including the proportional error (e_{11}, e_{12}) and integral error (e_{21}, e_{22}) represented by (11) around zero. This is achieved by selecting the coefficients k_1 and k_2 in stable area and it depends on the operating point of the converter as elaborated in the next section.

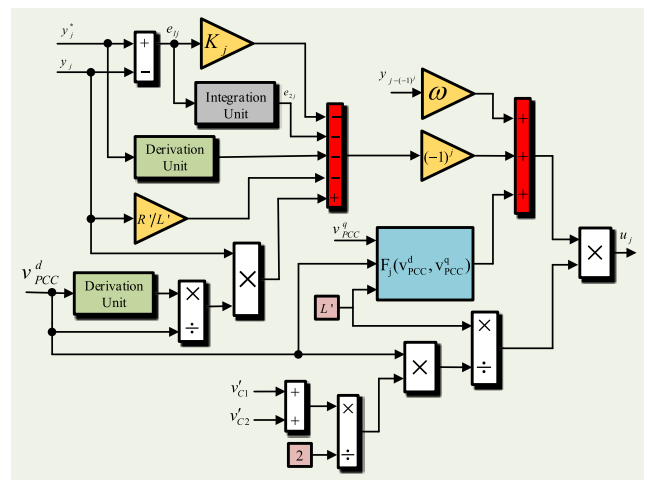


FIGURE 2. Block-diagram of the proposed DFT-based control strategy.

It is worth noticing that the PD-PWM strategy is applied as the switching process of the converter.

$$u_j = \frac{2L'}{v_{PCC}^d(v'_{C1} + v'_{C2})} \times \begin{pmatrix} (-1)^j(-\dot{y}_j^* + \frac{\dot{v}_{PCC}^d}{v_{PCC}^d}y_j - \frac{R'}{L'}y_j - e_{2j} - k_j e_{1j}) \\ +\omega y_{j-(-1)^j} + F_j(v_{PCC}^d, v_{PCC}^q) \end{pmatrix} \quad (18)$$

where $F_j(v_{PCC}^d, v_{PCC}^q)$ is given in (19).

$$F_j(v_{PCC}^d, v_{PCC}^q) = \begin{cases} \frac{1}{L}(v_{PCC}^d)^2, & j = 1 \\ \frac{1}{L}v_{PCC}^d v_{PCC}^q, & j = 2 \end{cases} \quad (19)$$

IV. ASSESSMENT OF THE PROPOSED CONTROLLER COEFFICIENTS

The controller coefficient k_j used in (18) is the Lyapunov variable that should keep the converter operation in stable area. According to the stability condition represented by (15), the proposed controller provides the stable operating conditions for the converter, if the coefficients have positive values. The coefficient values must be evaluated to acquire zero values for all proportional and integral errors. To this end, the controller coefficients k_1 and k_2 from (16) and (17) are defined as the functions of the converter active power (P) and reactive power (Q) (y_1 and y_2 , respectively) as well as the errors of e_{1j} and e_{2j} , as given in (20) and (21).

$$k_1 = \frac{\begin{pmatrix} (\frac{v'_{C1}+v'_{C2}}{2})(v_{PCC}^d)^2 u_1 - L'v_{PCC}^d \dot{P}^* \\ +(L'v_{PCC}^d - R'v_{PCC}^d)P \\ -L'\omega v_{PCC}^q Q - (v_{PCC}^d)^3 - L'v_{PCC}^d e_{21} \end{pmatrix}}{L'v_{PCC}^d e_{11}} \quad (20)$$

$$k_2 = \frac{\begin{pmatrix} -(\frac{v'_{C1}+v'_{C2}}{2})(v_{PCC}^d)^2 u_2 - L'v_{PCC}^d \dot{Q}^* \\ +(L'v_{PCC}^d - R'v_{PCC}^d)Q \\ +L'v_{PCC}^d \omega P + (v_{PCC}^d)^2 v_{PCC}^q - L'v_{PCC}^d e_{22} \end{pmatrix}}{L'v_{PCC}^d e_{12}} \quad (21)$$

Fig. 3 depicts the 3-dimension curves of the coefficient k_1 as a function of errors e_{11} and e_{21} for five different operating points of the converter. It can be realized from Fig. 3 that the coefficient k_1 is very sensitive to the proportional error of the converter active power (e_{11}) especially when it is close to zero. According to the figure, the coefficient k_1 takes bigger values while the proportional error of the active power (e_{11}) is approaching zero. It should be noticed that the positive values are acceptable as a stability condition represented by (15). It can be easily inferred from the figure that the surfaces move away from each other as the errors are approaching to zero. The higher active and reactive power delivered by the converter needs the bigger values of k_1 to keep the errors around zero. On the other hand, when the errors get far from zero, the surfaces are close to each other and the coefficient k_1

moves toward zero as well. It means that the controller cannot decrease the errors to any active and reactive power level without taking the Lyapunov coefficient into account.

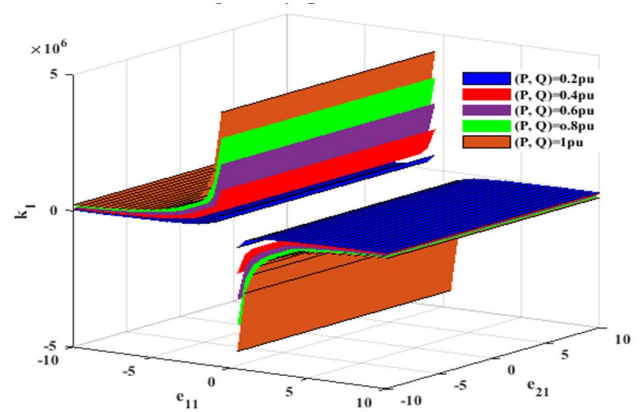


FIGURE 3. The 3-dimension curves of the coefficient k_1 as a function of errors e_{11} and e_{21} for five different operation points of the converter.

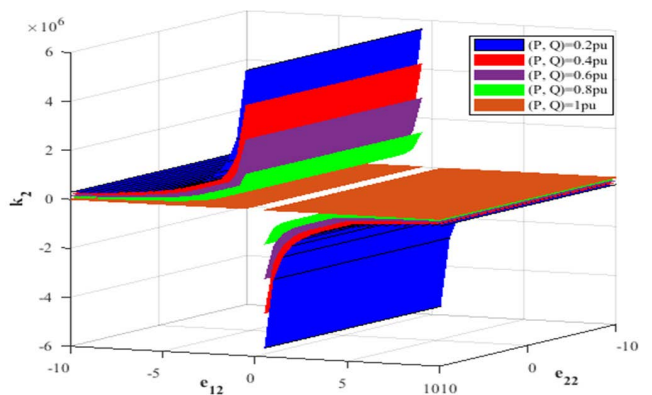


FIGURE 4. The 3-dimension curves of the coefficient k_2 as a function of errors e_{12} and e_{22} for five different operation points of the converter.

Fig. 4 shows the 3-Dimension curves of the coefficient k_2 for five different converter active and reactive power while the proportional and integral errors of the reactive power (e_{12} and e_{22} , respectively) are changed. According to Fig. 4, the coefficient k_2 is very sensitive to the proportional error of the reactive power while it declines to zero. Similar to the curves of the coefficient k_1 , the coefficient k_2 takes big values to keep proportional error at around zero. By comparing Fig. 3, and Fig. 4, it demonstrates a different trend here and the bigger values of the converter active and reactive power will be achieved through the smaller values of the coefficient k_2 . The impact of k_2 on the accuracy of the controller can be inferred using Fig. 4 as well. Based on this figure, the errors will be increased at any operating point of the converter when this coefficient is getting close to zero. The assessment reveals that high positive Lyapunov coefficients are essential to guarantee the stability of the converter and enable accurate operation of the controller with small active and reactive power errors.

Also, the coefficients k_1 and k_2 take bigger values when the active and reactive power of the converter increase or decrease, respectively. On the other hand, k_1 and k_2 take smaller values while the converter power decrease or increase, respectively. By using (16) and (17), the proportional and integral errors ($e_{ij,i,j=1,2}$) can be rewritten in terms of active power (P) and reactive power (Q) (y_1 and y_2 , respectively), the reference values, the switching functions and other converter parameters as represented by matrix format in (22).

$$\begin{bmatrix} k_1 & 0 \\ 0 & k_2 \end{bmatrix} [e_{11} \ e_{12}] + \mathbf{I}_2 [e_{21} \ e_{22}] = \begin{bmatrix} \left(\frac{v'_{C1} + v'_{C2}}{2L'} (v_{PCC}^d) u_1 - \dot{P}^* + \left(\frac{\dot{v}_{PCC}^d}{v_{PCC}^d} - \frac{R'}{L'} \right) P \right) \\ -\omega Q - \frac{1}{L'} (v_{PCC}^d)^2 \\ \left(-\frac{v'_{C1} + v'_{C2}}{2L'} (v_{PCC}^d) u_2 - \dot{Q}^* + \left(\frac{\dot{v}_{PCC}^d}{v_{PCC}^d} - \frac{R'}{L'} \right) Q \right) \\ +\omega P + \frac{1}{L'} v_{PCC}^d v_{PCC}^q \end{bmatrix} \quad (22)$$

where \mathbf{I}_2 is the second-order identity matrix. In the case that all errors tend to zero ($e_{ij} \rightarrow 0$), (23) is achieved.

$$\begin{bmatrix} \frac{\dot{v}_{PCC}^d}{v_{PCC}^d} - \frac{R'}{L'} & -\omega \\ \omega & \frac{\dot{v}_{PCC}^d}{v_{PCC}^d} - \frac{R'}{L'} \end{bmatrix} \begin{bmatrix} P \\ Q \end{bmatrix} = \begin{bmatrix} -\frac{v'_{C1} + v'_{C2}}{2L'} (v_{PCC}^d) u_1 + \dot{P}^* + \frac{1}{L'} (v_{PCC}^d)^2 \\ -\frac{v_{dc}}{L'} (v_{PCC}^d) u_2 - \dot{Q}^* - \frac{1}{L'} v_{PCC}^d v_{PCC}^q \end{bmatrix} \quad (23)$$

By solving this equation, the active and reactive power of the converter are written as (24) and (25). Equations (24) and (25) represent the converter active and reactive power range while their proportional and intergral errors are around zero. These power quantities are stated as a function of their desired values, input variables, DC link voltage, d and q components of the grid voltage as well as passive element values.

$$P = \frac{\begin{pmatrix} \left(-\frac{v'_{C1} + v'_{C2}}{2L'} (v_{PCC}^d) u_1 + \dot{P}^* \right) \\ + \frac{1}{L'} (v_{PCC}^d)^2 \left(\frac{\dot{v}_{PCC}^d}{v_{PCC}^d} - \frac{R'}{L'} \right) \\ -\omega \left(\frac{v'_{C1} + v'_{C2}}{2L'} (v_{PCC}^d) u_2 \right) \\ + \dot{Q}^* \frac{1}{L'} v_{PCC}^d v_{PCC}^q \end{pmatrix}}{\left(\frac{\dot{v}_{PCC}^d}{v_{PCC}^d} - \frac{R'}{L'} \right)^2 + \omega^2} \quad (24)$$

$$Q = \frac{\begin{pmatrix} \left(-\frac{v'_{C1} + v'_{C2}}{2L'} (v_{PCC}^d) u_2 \right) \\ - \dot{Q}^* \frac{1}{L'} v_{PCC}^d v_{PCC}^q \left(\frac{\dot{v}_{PCC}^d}{v_{PCC}^d} - \frac{R'}{L'} \right) \\ -\omega \left(-\frac{v'_{C1} + v'_{C2}}{2L'} (v_{PCC}^d) u_1 + \dot{P}^* \right) \\ + \frac{1}{L'} (v_{PCC}^d)^2 \end{pmatrix}}{\left(\frac{\dot{v}_{PCC}^d}{v_{PCC}^d} - \frac{R'}{L'} \right)^2 + \omega^2} \quad (25)$$

V. VALIDATION OF DESIGN THROUGH SIMULATION

To validate the performance of the proposed DFT based SC-MLC, a system depicted in Fig. 1(a) is simulated in MATLAB/Simulink environment. The simulation parameters are given in Table 2. In this study, the second load is added to the system at $t=1$ sec and the performance is evaluated during two different operating points. Fig. 5 exhibits the active power of the converter, grid and load, simultaneously. The reference values of active power for DG are set at 0.5kW and 1kW during the first and second operating points, respectively. The figure shows that the converter could accurately follow the references and deliver a quarter of the load demand in both operating points. The reactive power of the converter, grid and load are displayed simultaneously in Fig. 6.

TABLE 2. The simulation parameters.

Symbol	Quantity	Value
V_{dc}	dc link voltage	110V
V_g	Grid voltage	350V
f_{base}	Nominal frequency	50Hz
C_1, C_2	Converter capacitors	2200 μ F
L_g	Grid equivalent inductance	2mH
R_g	Grid equivalent resistance	0.1ohm
K_1	Proposed controller coefficient	5e5
K_2	Proposed controller coefficient	1.5e5
K_{pd}, K_{pq}	PI controller proportional coefficient	6e3
K_{id}, K_{iq}	PI controller integral coefficient	3e3

The reference values for reactive power of DG are equal to the reactive power absorbed by the loads during both operating points. It is easily understood from the figure that the converter could follow its reference and respond to the reactive power demand of the load during two operating conditions. It can be deduced from the results that thanks to

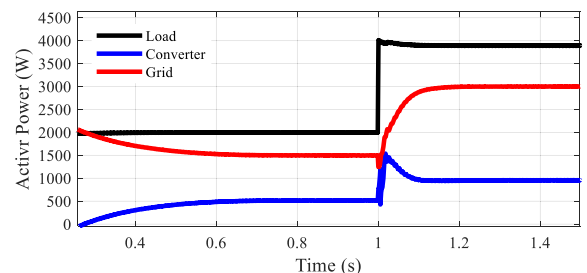


FIGURE 5. Active power of the converter, grid and load simultaneously.

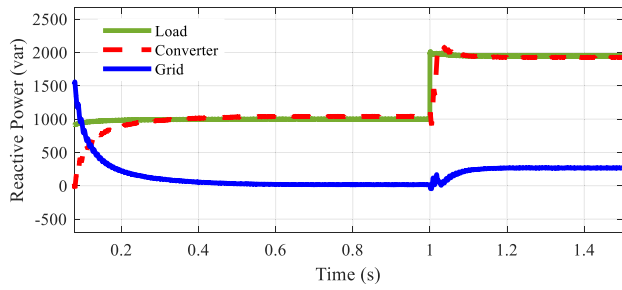


FIGURE 6. Reactive power of the converter, grid and load simultaneously.

the assignment of e_{ij} and k_j for values in the ranges achieved in section IV, the proposed controller is able to guarantee the reference tracking with no steady state error. Moreover, it is demonstrated that the converter could change the operating point with no disturbances during transient intervals.

Fig. 7 depicts the grid current (i_g) and small-scale grid voltage (v_g) at the same time. According to this figure, the phase difference between grid voltage and current is zero (unity power factor) and 0.245 Rad (power factor=0.97 Lag) during the first and second operating points, respectively, and there is no disturbance at the transient instant. Also, according to the FFT analysis provided by Fig. 8, the THD of the grid current is 2.15% that meets IEEE-Std. 519-2014 standard.

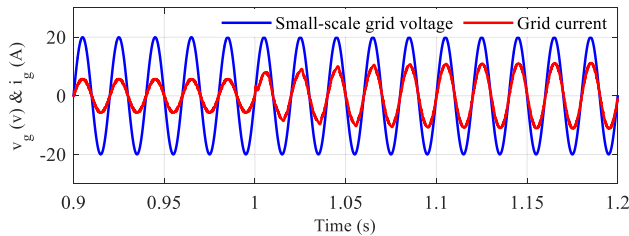


FIGURE 7. The grid current and small-scale grid voltage.

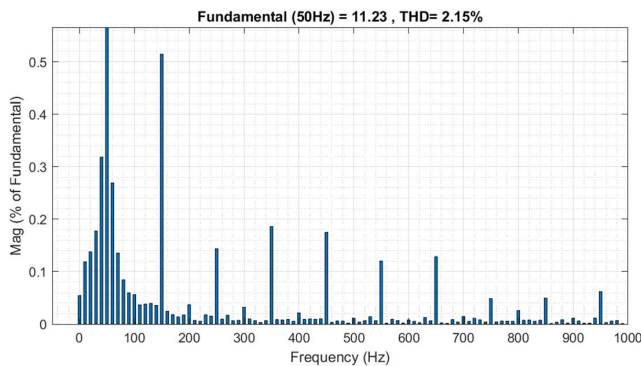


FIGURE 8. The grid current and small-scale grid voltage.

To validate the superiority of the proposed DG system over conventional one in terms of robustness feature of the controller under disturbances, another scenario is taken into account. In this test, the value of the converter inductance (L) is reduced to half at $t=0.8$ s. Fig. 9 (a) and (b) illustrate

the active and reactive power of the converter simultaneously before and after impedance change while the DFT based and traditional PI controllers are employed, respectively. According to Fig. 9 (a), when the proposed DFT based converter has been used, both active and reactive power of the converter are remained constant after impedance change.

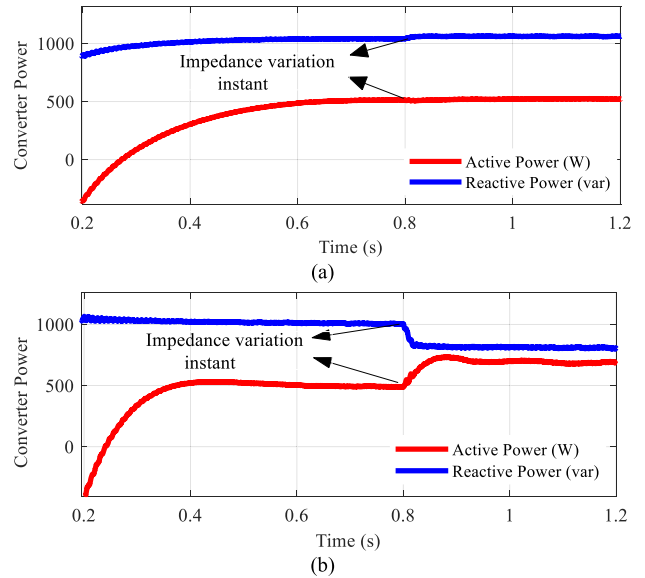


FIGURE 9. Active and reactive power of the converter after the parameter variation when (a) DFT based and (b) PI-controller are employed.

However, it can easily be inferred from Fig. 9 (b) that the active and reactive power of the converter experience deviations of around 40% and 20%, respectively. It means that the converter controlled by the conventional PI controller is adversely affected by the uncertainties and the injected power change considerably. It should be noted here that the trial-and-error method has been carried out to obtain the best coefficients of the PI controller so that the fair comparison is made. This test demonstrates that the proposed DFT based DG system is robust sufficiently against the parameter alternation and the converter is not suffered from unwanted uncertainties. Furthermore, in order to verify the ability of the proposed DG unit in the case of disturbance at the grid side in the form of a voltage sag (v_g), a single-phase earth fault has been simulated at $t=1$ s and removed at $t=1.084$ s as depicted in Fig. 10. According to the figure, the voltage has been dropped to 0.5p.u. for five cycles which satisfies the voltage sag definition according to the IEEE standards such as IEEE Std 1668-2017.

Fig. 11 and Fig. 12, which illustrate the delivered active power (P_{con}) and injected reactive power by the D-type converter (Q_{con}), confirm that the DG is able to be recovered during the voltage sag and follow the pre-fault reference values for active and reactive power with no steady state deviation during and after the fault. The capacitor's voltages ($V_{C1,2}$) are shown in Fig. 13. The figure clearly shows that the DC level has remained constant during the fault and there is only 1.8%

overshoot and no steady state error in the waveform. This test verifies the ability of the proposed control strategy in robust performance of the converter when the grid side experiences the fault, and the voltage sag is occurred.

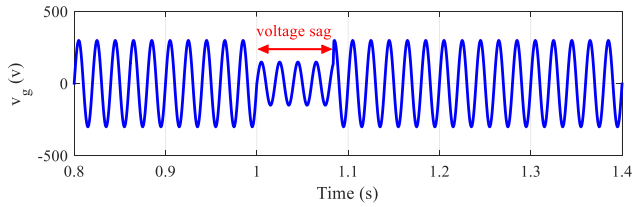


FIGURE 10. The grid voltage during fault.

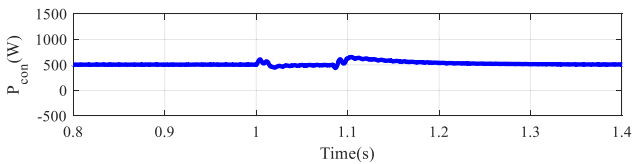


FIGURE 11. The active power delivered by the converter during fault.

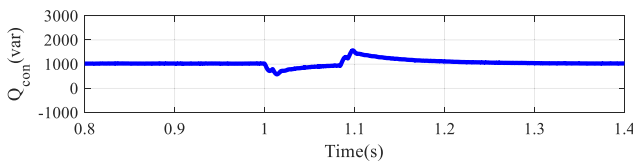


FIGURE 12. The reactive power injected by the converter during fault.

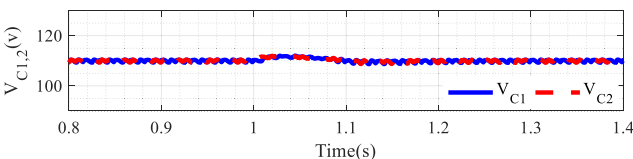


FIGURE 13. The capacitors voltages during the fault.

VI. EXPERIMENTAL RESULTS

In order to further validate the proposed DFT-based control applied to SC-MLC, several experimental results are acquired from the setup shown in Fig. 14, including Digital Signal Processing (DSP) unit TMS320F28335 with the sampling time of $10\mu s$, IRFP460 MOSFET as main switches with the switching frequency of 5kHz, opto-coupler driver HCPL3120, with the following specified values $V_{dc} = 50V$, $V_g = 100V$, $f_{base} = 50Hz$, and $C_1 = C_2 = 2200\mu F$. To limit the inrush current of the empty circuit capacitors at the start of the experiment, the input voltage of the power supply is gradually increased addressing the voltage spikes of the empty capacitors.

The grid voltage, grid current and the converter voltage are simultaneously depicted in Fig. 15. It indicates that the

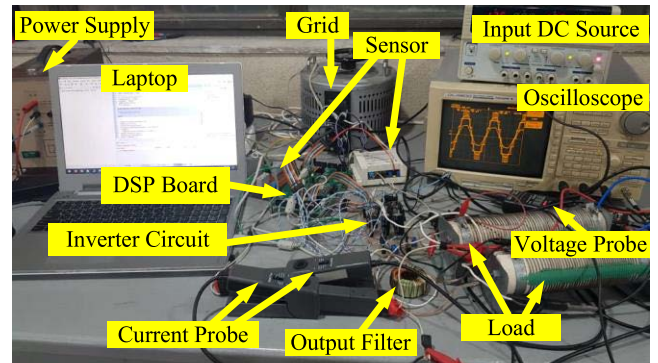


FIGURE 14. The experimental setup including DSP TMS320F28335 for grid-connected SC-MLC controlled by the DFT technique.

converter voltage has been accurately synchronized with the grid voltage with no phase difference between them and all seven levels have been made correctly. Also, the grid current is in the same phase with the grid voltage so that the grid power factor is unity. In addition, the grid current waveform is almost sinusoidal with a THD measured at 3.98% which satisfies IEEE-Std. 519-2014 standard.

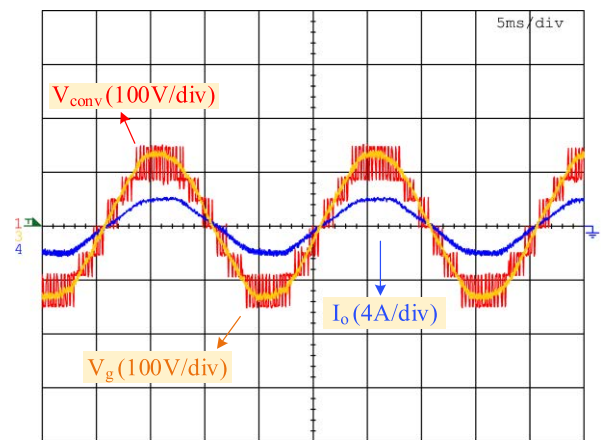


FIGURE 15. The grid voltage, grid current and the converter voltage around the transient instant.

Fig. 16 provides the experimental results of the converter and the capacitors voltages when the operating point of the converter is fixed and only the converter impedance is decreased to 50% of its initial value. By comparing the waveforms before and after variation, it is inferred that the impedance variation has no impact on the normal operation of the converter. This test demonstrates the robust converter as the proposed control technique responds against such uncertainties and can successfully keep the capacitors voltage unchanged after variation in the impedance with no steady state and dynamic disturbances.

To evaluate the operation of the converter under different conditions, further experimental tests have been conducted based on three scenarios. In the first scenario, the proposed distribution network depicted in Fig. 1(a) is initially supplying the first local load (Z_1) and after a while, the

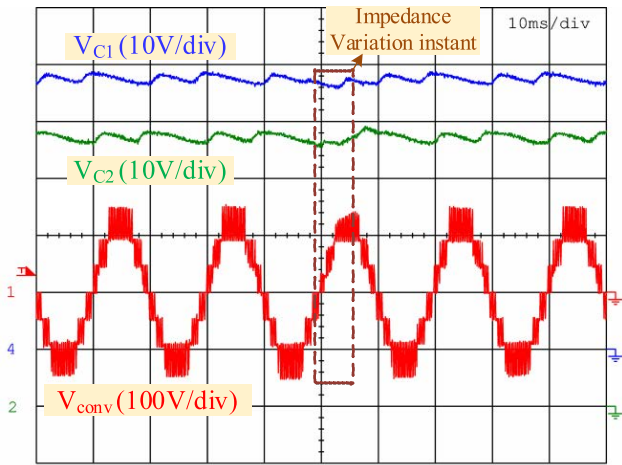


FIGURE 16. The capacitors voltage and the converter output voltage after variation in the impedance of the converter.

second load (Z_2) with the same configuration is added to the system. According to the Fig. 17, since the reference current of the converter is kept at constant value (1A) during both conditions of the load demand, after connecting the second load (Z_2), the injecting current of the converter stays intact and further demand of the local loads is supplied by the grid. It can be realized from that there is no perturbation during the transient interval and the converter could support all voltage levels accurately. Thus, the proposed DG system could effectively respond to the load variations with excellent dynamic behaviour.

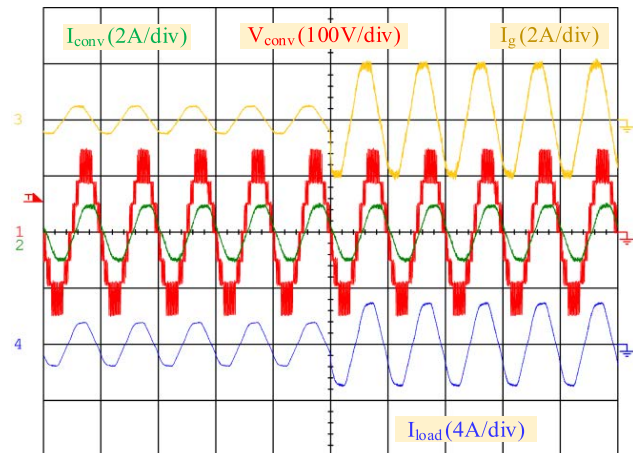


FIGURE 17. The power sharing commensurate with scenario 1.

In the second scenario, the converter responds to the new added load and supplies all further power demanded by Z_2 . According to Fig. 18, the grid current remains constant during both operating points and the reference power of the converter increases accordingly. The figure clearly shows that the converter could keep the nominated voltage accurately and could react to the variation with acceptable dynamic response without any transient problem.

In the last scenario, there is no extra load demand but the operation point of the converter is changed by increasing the reference power of the converter. As Fig. 19 displays, the fixed load demand is supplied by incorporating two different strategies of power sharing in the proposed DG system. During the first part of the test, the converter and grid supply around 30% and 70% of the load demand, respectively. In the second part, the converter supplies twice the previous value and the power delivered by the grid is reduced to 40% of the load demand. It is verified from the figure that the converter can change its operating point with no dynamic disturbance and does not impose any transient distortion in either the DG or the network. This test demonstrates that the proposed DFT based DG system can flexibly perform any contribution in power sharing strategies with no steady-state error and transient distortion. The results confirm that the controller is compatible with the Dumbbell type switched capacitor multilevel converter to perform the main functions of the DG system.

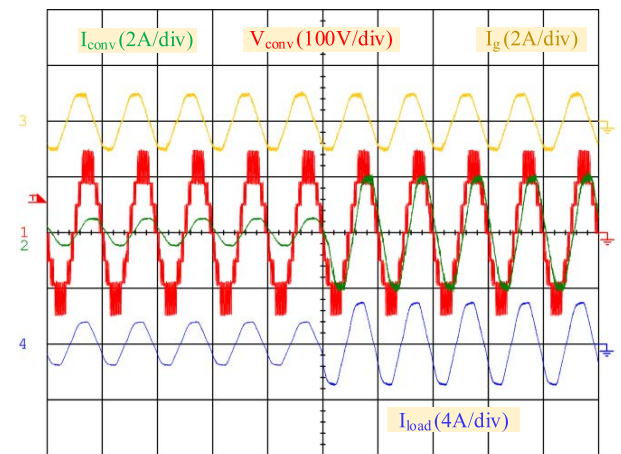


FIGURE 18. The power sharing in the proposed grid-connected system considering scenario 2.

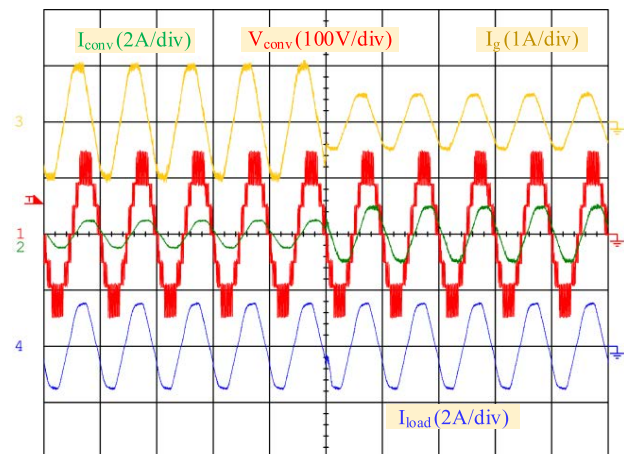


FIGURE 19. The power sharing in the proposed grid-connected system considering scenario 3.

VII. CONCLUSION

A control system based on differential flatness theory (DFT) has been designed and incorporated for developing a robust grid-connected DG interfaced through the recently introduced multilevel converter named D-type switched capacitor multilevel converter (SC-MLC). The initial control inputs of the multilevel converter have been made through the current dynamic model as well as the active and reactive power-based flat outputs. In order to achieve the ultimate control inputs along with taking the global asymptotic stability into account, the direct Lyapunov method has been applied based on both proportional and integral errors of the flat outputs. Mathematical analysis has also been accomplished to obtain the relations between the flat outputs and their errors for evaluating the variation trend of Lyapunov coefficients. To validate the stable and transient performance as well as robust treatment of the considered multilevel converter-based grid-tied system under the proposed controller operation, both simulation and experimental results have been presented. This study has focused on low voltage applications in distribution networks. Therefore, all considerations in the control system are limited to the requirements recommended by standards in low voltage levels. The authors future work will be employing an (intelligent) optimized strategy for tuning the controller coefficients k_1 and k_2 when the operating points change and/or uncertainties occur.

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