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RESEARCH ARTICLE

A 32 kW Power-Dense Six-Phase Dual-Interleaved DC–DC Buck-Boost Converter With Three Interphase Transformer

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ABSTRACT This article presents a power-dense, six-phase dual-interleaved DC-DC Buck-Boost converter for electric/hybrid vehicle applications. This converter uses six hard-switched arms at 75 kHz, three dual-interleaved interphase transformers together with three common inductors and two filter capacitors at the input and output. The steady-state current ripple frequency of the common inductors is twice the switching frequency due to the dual interleaving in the interphase transformers. The resultant ripple current frequency of the input and output filters is six times the switching frequency; size and weight reduction of the passive components are obtained due to this frequency increase. The design and construction details of a 32 kW, 315-385 V supply, SiC-based prototype are presented along with experimental investigation. The prototype converter was successfully operated up to full load with a 350 V output, being the phase currents relatively balanced in the continuous conduction mode without a closed-loop control system. The prototype efficiency is 98 % at full load, being the gravimetric power density 7.56 kW/kg.

INDEX TERMS Buck-boost converter, dual-interleaved, high-power density, interphase transformer.

I. INTRODUCTION

The trend of using more electric technology in mobility applications has increased the power rating of electronic energy platforms, impairing the weight and size of the power converters aboard vehicles and affecting their autonomy [1], [2]. These problems constitute nowadays a technological bottleneck.

High-power-density DC-DC converters have opened a field of development and research that currently aid reducing size and weight in medium power applications [3], [4], [5], either with or without bidirectional capability. This technology strategy incorporates interleaved switching arms together with integrated magnetics such that the power handling capacity is divided into two or more cells [6], [7], [8]; however, the complexity of these circuits could increase due to the high number of switching devices. For example, [9] presented a DC-DC converter that uses this trend for a 20 kW application, whose density is improved significantly increasing the number of switching variables.

One way to improve gravimetric power density is through wide bandgap semiconductors devices, allowing the switching frequency to be increased with high current and medium voltage levels in combination with interleaving techniques. Examples of this methodology are described in [10], [11], and [12] that show attractive improvements in gravimetric power density and efficiency. Reference [13] reported a 15.7 kW/kg power density of an 80 kW SiC converter with a

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97% efficiency utilizing integrated split-core magnetic inductors combined with two interleaved switching arms. Variants of this sort of circuit arrangement are presented in [14], [15], and [16] which exploited inherent frequency multiplication in the common node connection of an interleaved arrangement without increasing the operating frequency, resulting in the reduction of passive filters size and energy storage components.

Alternative strategies of power density improvement are described in [17] and [18] that use nanocrystalline magnetic core materials, which reduce the core size and weight of inductors and transformers. This technology has become available from several manufacturers allowing high operating frequencies with magnetic flux densities around 1 T. References [19] and [20] described the development of DC-DC converters that used magnetic materials such as Finemet and Kool Mu, respectively, obtaining attractive results in weight distribution and power losses while the magnetic components slightly figured as bulky components. The use of planar coils potentially offers a fashion of reducing the size and weight of magnetics devices without impairing power losses. References [21] and [22] described an interesting strategy of achieving uniform flux density distribution in high-frequency power inductors of DC-DC converters, which aids enclosing the copper winding and benefiting magnetic flux density distribution along the core. This technique could further improve the power density in future electronic converters.

This paper presents a 32 kW, Six-Phase Dual-Interleaved Buck-Boost Converter (SPDIBBC) prototype, implemented with SiC devices and nanocrystalline magnetics, intended to regulate the energy drawn from a fuel cell in an electric vehicle (EV). The major contribution of this work is to achieve high power density levels by utilizing six switching arms, hard-switched at 75 kHz, in a multiphase DC-DC converter, which uses three interphase transformers (IPTs) together with three common inductors and input and output filter capacitors. A brief description of the SPDIBBC under steady-state operation is firstly presented, detailing an analysis of the appropriate number of cells that may suit the converter to achieve improved power density; secondly, the design and selection of components for a 32 kW SiC-based prototype are described bearing in mind the operation limits of continuous current mode described in the steady state analysis of the converter. Experimental and simulation results are compared to validate the principle of operation described in the first section, verifying the converter performance with an open-loop duty cycle driving scheme. Finally, the paper concludes showing the most relevant achievements together with possible future research.

II. STEADY-STATE ANALYSIS OF THE CIRCUIT

A. DESCRIPTION OF THE SIX-PHASE DUAL-INTERLEAVED BUCK-BOOST CONVERTER

Fig. 1 presents the circuit diagram of the SPDIBBC. Six unidirectional, Buck-Boost switching arms are connected in parallel to a single DC input voltage, V_{in}, through the drain

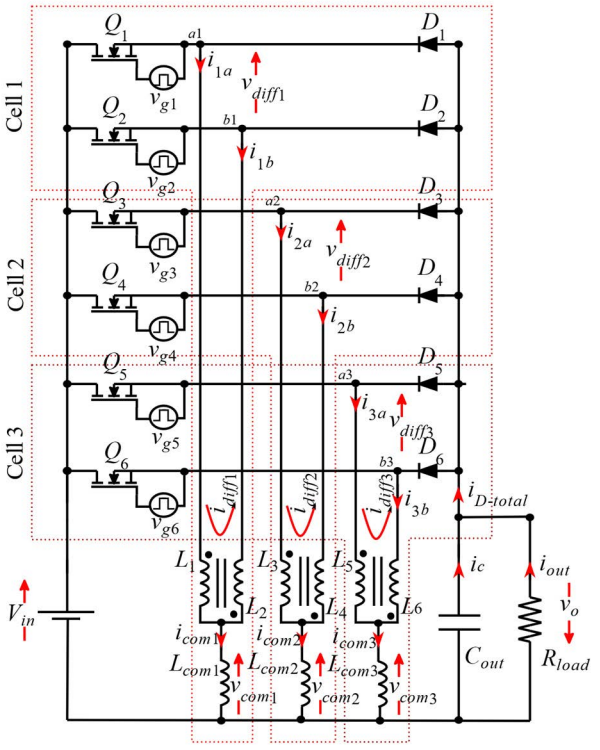

FIGURE 1. Six-Phase Dual-Interleaved DC-DC Buck-Boost converter.

terminal of six MOSFETs transistors, Q_1 to Q_6, and by means of the cathode terminal of six cascade diodes, D_1 to D_6. An output filter capacitor, C_{out}, smooths the total diode current to feed the load R_{load}. Three IPTs are connected in the midpoint nodes of each switching arm, such that coupled inductors pairs, L_1-L_2, L_3-L_4 and L_5-L_6, are formed. Three common inductors, L_{com1} to L_{com3}, of identical inductance are connected in the central tap node of the IPTs, as shown in Fig. 1, to add the DC current drawn of the IPTs inductors and smooth the produced ripple current, having twice the switching frequency as a consequence of the IPT common voltage connection. The states of Q_1 to Q_6 are driven by six Pulse-Width Modulated (PWM) control signals, v_{g1} to v_{g6}, ideally operated in an interleaved fashion with a 60° phase shift and equal duty ratios, $D = D_{1-6}$.

The operation of the circuit in Fig. 1 may be described assuming three identical cells of Dual-Interleaved Buck-Boost Converters (DIBBCs), [14], connected in parallel and sharing the same input and output ports. Each DIBBC cell is assumed to be operating with a 120° phase shift between cells and in the Continuous Current Mode (CCM), being the individual IPT inductor currents, i_{1a}-i_{1b}, i_{2a}-i_{2b}, and i_{3a}-i_{3b}, ideally coupled through equalized self inductances, $L_1 = L_2$, $L_3 = L_4$ and $L_5 = L_6$. The IPT magnetizing currents are three differential currents, $i_{diff\,1}$ to $i_{diff\,3}$, that flow in the mid nodes of the switching arms throughout the magnetizing inductances $L_{diff\,1}$, $L_{diff\,2}$ and $L_{diff\,3}$, which are respectively equal to $4L_1$, $4L_3$ and $4L_5$ since the IPTs have a 1:1 turn ratio. The components are assumed to be lossless with negligible input and output voltage ripples.

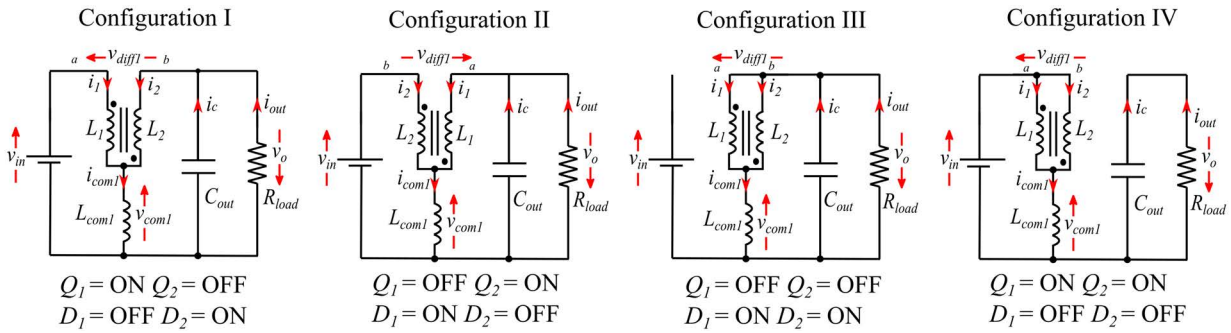

FIGURE 2. The four circuit configurations of the Dual-Interleaved DC-DC Buck-Boost cell.

B. FUNDAMENTAL OF OPERATION OF THE SPDIBBC

Four per cell circuit configurations are produced by the transistor switching, which are shown in Fig. 2 as Configurations I to IV. The SPDIBBC principle of operation in CCM may be described using the idealized waveforms in Fig. 3 and the equivalent circuits in Fig. 2, both for the step-down and step-up operating modes. These idealized waveforms are the same as those used to describe the principle of operation of the dual interleaved converter of [14], however, the current waveforms of Fig. 3 are assumed to be a third part amplitude of those described in [14]. The symmetrical phase shift between cells significantly minimizes the current ripples, the size and weight of the inductors and capacitors is thereby reduced.

The idealized steady state waveforms of the SPDIBBC are displayed in Fig. 3 organized by cells considering the step-down and step-up operation modes at the left and right sides of the same figure. v_{g1} to v_{g6} are shown in pairs at the top of Fig. 3 with a 180° phase shift to obtain switching symmetry. The next waveforms depict the differential voltages across the midpoint nodes of each cell, $v_{diff\,1}$ to $v_{diff\,3}$, together with the common inductor voltages, v_{com1} to v_{com3}. These impressed differential and common voltages produce the differential and common currents, $i_{diff\,1}$ to $i_{diff\,3}$ and i_{com1} to i_{com3}, respectively, which are presented below in Fig. 3. i_{1a}-i_{1b}, i_{2a}-i_{2b}, and i_{3a}-i_{3b} are the last group of waveforms plotted in Fig. 3 which are the resulting combination of the differential and common current given by:

$$i_{xa} = \frac{i_{comx}}{2} + i_{diffx} \tag{1}$$

$$i_{xb} = \frac{i_{comx}}{2} - i_{diffx} \tag{2}$$

where $x = 1$, 2 or 3. The sum of the diode currents, $i_{D-total}$, is the last waveform shown in the same figure, which has a ripple frequency of six times the switching frequency due to the cells interleaved connection.

The configuration sequence per cell is listed at the bottom of Fig. 3, just below the ideal waveforms. As a result, a whole combination of switching states is produced, giving the idea of the existence of alternative switching patterns to operate the circuit; however, for the presented analysis the basic switching pattern shown in Fig. 3 is assumed.

A summary of the DC levels, I_{com1-3} and I_{1-6}, and ripple amplitude expressions, ΔI_{com1-3}, ΔI_{1-6}, and $\Delta I_{diff\,1-3}$, of the ideal common inductor and IPT current waveforms of Fig. 3 are listed in Table 1. Moreover, the RMS value of the output filter capacitor, I_{oRMS}, is also listed at the bottom of the same table.

C. COMPARATIVE STEADY STATE ANALYSIS OF THE SPDIBBC

The voltage conversion ratio of the SPDIBBC, listed in Table 1, is obtained from a L_{com} Volts-seconds balance, which is identical to the DIBBC and the conventional Buck-Boost converter; nevertheless, the RMS and average values are considerably reduced in the SPDIBBC in contrast to the DIBBC as detailed below.

The use of multiple cells, or phases, may significantly reduce the current ripple amplitudes, the dimensions of the filter capacitors and magnetic components in DC-DC converters and, therefore, increase the converter power density since the main common inductor current is split into the number of cells.

A normalized plot of the DC level of the common current inductor, I_{com1-3}, is shown in Fig. 4(a) against the duty ratio for cells ranging from 1 to 6. The number of cells that produce a minimal deviation of I_{com} can be determined using this plot, whilst the number of cells increases. In Fig. 4(a), I_{com} reduces its deviation when D is close to 0.5 and the number of cells is 3, ensuring that the split current slightly decreases for more than 3 cells. The latter is verified using the plot of Fig. 4(b), where the common inductor, RMS split current level, has been calculated ranging the duty ratio again from 0 to 1, together with the number of cells from 1 to 6. Once more, a slight deviation around the neighbourhood of $D = 0.5$ occurs for the RMS current. In this fashion, the extension of DIBBC cells in the SPDIBBC begins to have the same effect when 3 DIBBC cells are used and, thereby, in this work, it was judged that 3 cells were suitable to increase the power density of the interleaved DC-DC converter, ensuring low complexity due to the high number of switching devices and control issues.

The output capacitor RMS current, I_{oRMS}, of the DIBBC and SPDIBBC was calculated as a function of D, as listed in Table 1, by using the ideal waveforms of $i_{D-total}$ of

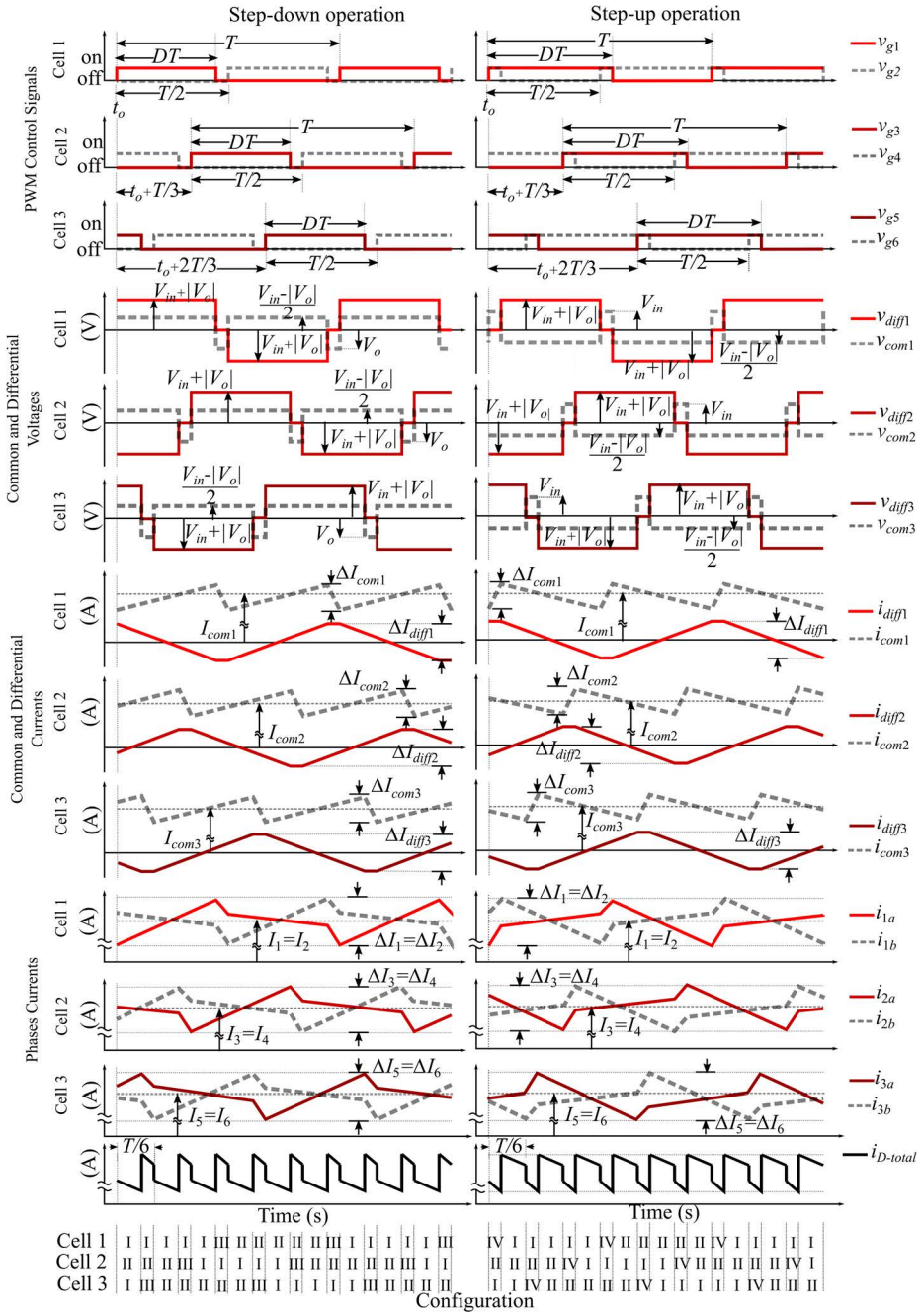

FIGURE 3. Idealized waveforms of the Six-Phase Dual-Interleaved DC-DC Buck-Boost converter with D < 0.5 (Step-down operation) and D > 0.5 (Step-up operation).

Fig. 3 without DC offset. The results are compared in the normalized plot of Fig. 5, where I_{oRMS} is substantially minimized for the SPDIBBC in contrast to that of DIBBC, since the current ripple has six times the switching frequency. A reduced-size, filter capacitor with a lower RMS rating can be selected using this characteristic. Furthermore, I_{oRMS} becomes virtually minimal for the SPDIBBC, around 2 % in contrast to 18 % for the DIBBC, when $D = 0.5$, which is the commonplace range of this sort of DC-DC converters.

D. BOUNDARIES BETWEEN CONTINUOUS AND DISCONTINUOUS CURRENT MODE

The discontinuous current mode (DCM) occurs when any of the phase currents, i_{1a}-i_{1b}, i_{2a}-i_{2b}, or i_{3a}-i_{3b} in the IPT windings of each DIBBC cell satisfies the following condition:

$$\frac{I_{comx}}{2} < \frac{\Delta I_{xa}}{2} \tag{3}$$

The above condition typically happens at light load or low IPT magnetizing inductance. The boundary between the

TABLE 1. Dimensions of current levels in the six-phase dual-interleaved DC-DC buck-boost converter.

	$D < 0.5$ (Step-down)	$D > 0.5$ (Step-up)
$\frac{V_o}{V_{in}}$	$\frac{D}{1-D}$	
$I_{com1\text{-}3}$	$\frac{V_{in}}{3R_{load}}\left[\frac{D}{(1-D)^2}\right]$	
$I_{1\text{-}6}$	$\frac{V_{in}}{6R_{load}}\left[\frac{D}{(1-D)^2}\right]$	
$\Delta I_{com1\text{-}3}$	$\frac{V_{in}DT}{2L_{com1-3}}\left[\frac{1-2D}{1-D}\right]$	$\frac{V_{in}T}{2L_{com1-3}}(2D-1)$
$\Delta I_{1\text{-}6}$	$\frac{V_{in}DT}{2(1-D)}\left[\frac{1-2D}{2L_{com1-3}}+\frac{1}{4L_{1-6}}\right]$	$\frac{V_{in}T}{2}\left[\frac{(2D-1)}{2L_{com1-3}}+\frac{1}{2L_{1-6}}\right]$
$\Delta I_{diff1\text{-}3}$	$\frac{V_{in}T}{L_{diff1-3}}\left(\frac{D}{1-D}\right)$	$\frac{V_{in}T}{L_{diff1-3}}$
I_{oRMS}	$\sqrt{6\left[\frac{j}{6}-D\right]\left[I_{xa}{}^2+\frac{\Delta I_{xa}{}^2}{12}\right]+6\left[D-\frac{j-1}{6}\right]}$	
j	3	4

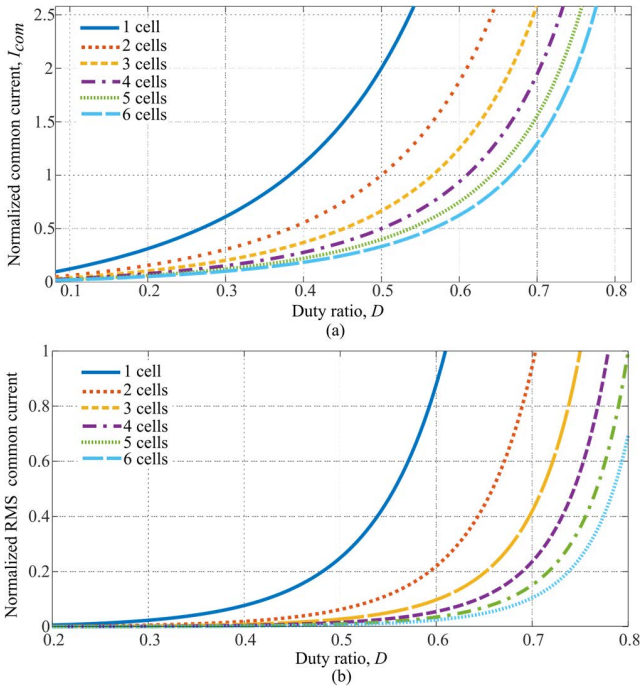

FIGURE 4. Analysis of the (a) average and (b) RMS common inductor current for different number of DIBBC cells against the duty ratio, D.

CCM and DCM may be determined assuming that the valley of one phase current becomes zero, as depicted in Fig. 6, for the step-down and step-up operating modes, [23]. This boundary can be analysed substituting I_{comx} and ΔI_{xa} from Table 1 in (3) for the step-down and step-up operating modes,

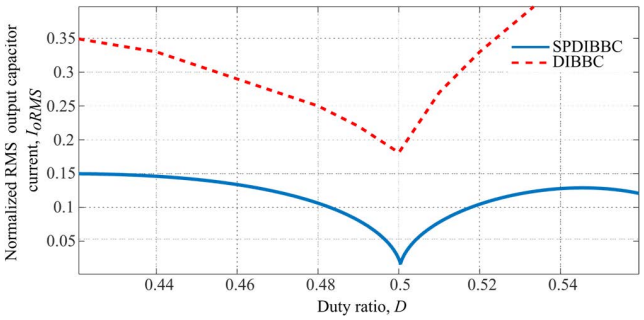

FIGURE 5. Comparison of the RMS current of the output capacitor in the DIBBC and SPDIBBC against the duty ratio, D.

such that the standard form of $k > k_{critical}(D, L_r)$ is, thereby, obtained and expressed as:

$$k > k_{critical}(D, L_r) = \begin{cases} 3(1-D)\left(\frac{1}{2}-D+\frac{2}{L_r}\right) \text{ for } D < 0.5 \\ \frac{3(1-D)^2}{D}\left(D-\frac{1}{2}+\frac{2}{L_r}\right) \text{ for} D > 0.5 \end{cases} \tag{4}$$

where L_r is the inductance ratio, $L_r = L_{diff}/L_{com}$, and k given as follows:

$$k = \frac{2L_{com}}{R_{load}T} \tag{5}$$

Eq. (4) is plotted in Fig. 7 for $L_r = 25$, 35, 50 and 100, and D ranging from 0 to 1. The converter operates in the CCM when k is above the $k_{critical}$ SPDIBBC traces shown in Fig. 7, shortening the D range in this mode; on the contrary, the converter operates in the DCM for almost the full range of D for $k < 0.262$ when $L_r = 25$. This constraint valley is reduced incrementing the L_r inductance ratio, as shown in the same figure. Fig. 7 also depicts $k > k_{critical}(D, L_r)$ for the DIBBC converter described in [14], which is a third part of (3), implying that the DIBBC has a larger CCM region than the SPDIBBC, since the IPT ripple current amplitude is directly determined by the input and output voltages while the common current is equally divided by the three cells. The latter suggests that the SPDIBBC should be designed using either a larger common inductor or inductance ratio, in such a way that CCM operating regions become similar to that of the DIBBC.

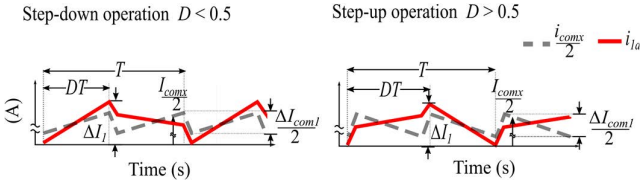

FIGURE 6. Idealized steady-state waveforms of i_{1a} and $i_{com1}/2$ in the cell 1 of the SPDIBBC at the continuous current boundary for step-down and step-up operation.

III. DESIGN AND CONSTRUCTION OF A 32 kW PROTOTYPE

The design and construction of a 32 kW SPDIBBC prototype based on SiC devices are described below. The design

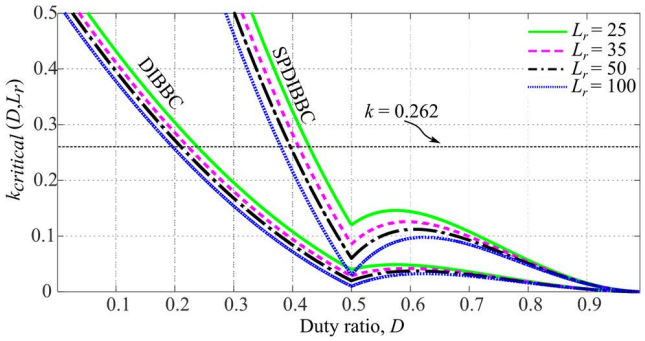

FIGURE 7. $k_{critical}$ for DIBBC and SPDIBBC against the duty ratio, D. L_{com} = 7 μH, R_{load} = 4 Ω and T = 13.33 μs, Data was obtained from [14].

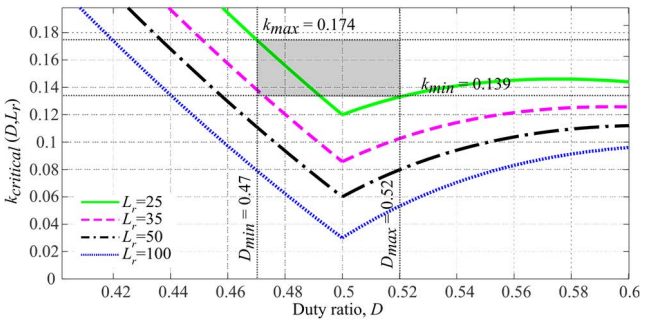

FIGURE 8. $k_{critical}$ for SPDIBBC against the duty ratio, D, considering the design critical cases.

TABLE 2. Design Parameters of the 32 kW Prototype.

Symbol	Name	Value
P_{out}	Output power	32 kW
f_{sw}	Switching frequency	75 kHz
V_{in}	Input voltage	350 V ±10%
V_o	Output voltage	350 V
D	Duty ratio range	0.47 to 0.52
T_r	Temperature rise	100 °C
$\Delta I_{com1\text{-}3}$	Common inductor current ripple	20 % of $I_{com1\text{-}3}$
$\Delta I_{1\text{-}6}$	Phase inductor current ripple	20 % of $I_{1\text{-}6}$
R_{load}	Nominal resistive load	4 Ω

parameters, selected materials and construction details were determined for a prototype intended to regulate a 350 V ± 10%, unidirectional DC supply to feed a traction motor system of an EV. The switching frequency, f_{sw} = 75 kHz and the output power, P_{out} = 32 kW, were selected as those used in the DIBBC prototype reported in [14], to obtain an accurate comparison between both realizations. Table 2 lists the design parameters selected for the 32 kW rig. In addition, a 75 kHz switching frequency was found to be suitable to obtain an adequate compromise between power density and power losses.

The duty ratio range for the SPDIBBC design, D_{min}, and D_{max}, was calculated using the voltage conversion ratio listed in Table 1, and using the input voltage V_{in}±10 %, and output voltage V_o, from Table 2. The determination of $k_{critical}$ was carried out using the duty ratio range, being this identified inside the plot of Fig. 7. This inset region is presented as the plot shown in Fig. 8, where the determined $k_{critical}$ is shown as a pair of continuous dashed lines, respectively for the minimum and maximum supply voltages, together with the duty ratio range. The $k_{critical}$ traces, previously shown in Fig. 7, are presented again in Fig. 8, with L_r ranging from 25 to 100. The grey box shown in Fig. 8 suggests an inductance ratio of L_r = 25 under this ratio, since the converter operates in the CCM for most of the duty ratio and supply voltage range.

A. DESIGN OF MAGNETIC COMPONENTS

L_{com1} to L_{com3} support the large DC flux due to the input current on each DIBBC cell. The calculation of L_{com} was carried out using the ΔI_{com1-3} equation listed in Table 1, which was solved for L_{com}, such that:

$$L_{com} = \frac{3R_{load}}{2\gamma f_{sw}} \left[\frac{(1 - D_{max})^2}{D_{max}} \right] (2D_{max} - 1) \tag{6}$$

where γ is equivalent to 20 % of I_{com1-3}. L_{com1-3} was determined using (6) and the listed values of Table 2, such that, L_{com1-3} = 18 μH.

A Kool Mu, E-shape core from Magnetics, [24], was chosen to build three 18 μH common inductors. The parameters and construction guidelines to build these inductors are summarized at the top of Table 3, which were obtained from a Magnetics spreadsheet based on the LI^2 Watts-seconds balance capability. The temperature rise and weight were important factors to obtain a lightweight design with a controlled steady-state temperature.

The IPTs design was performed assuming a differential inductance of L_{diff} = 450 μH, since $L_{diff} = L_r L_{com}$. The differential current was utilized as the main source that produces the magnetic flux density, and the phase currents rating as the principal factor to choose the wire gauge to obtain a 5 A/mm^2 current density without impairing the winding copper temperature beyond 100 °C, [25]. Each IPT was assembled using a customized C geometry core from MK-Magnetics, [26], being the FT-3, M1 nanocrystalline material suitable for the design, in contrast to other nanocrystalline materials, such as Metglas or Finemet, due to their low power losses and wide frequency response. The individual IPT number of turns, N, was determined using the gapped-inductor, energy balance methodology described in [27] that is shown in (7):

$$N = \sqrt{\frac{l_g L_{diff}}{0.4\pi A_c F(10^{-8})}} \tag{7}$$

where F is the fringing factor, l_g is a small airgap, chosen in this work as l_g = 0.15 mm, and A_c is the core cross-sectional area. Moreover, the Finement maximum flux density, B_{max} = 1.2 T, was used at 50 % in this work together with the v_{diff} waveform at the critical operating condition of D = 0.5 in each IPT core, such that the expression in (8):

$$NA_c = \frac{(V_{in} + V_o)DT}{B_{max}} \tag{8}$$

TABLE 3. Design guidelines of common inductors.

Symbol	Name	Value per component
$L_{com1\text{-}3}$	Common inductor value	18 µH
$f_{sw\text{-}com}$	Switching frequency of current ripple	150 kHz
$I_{com1\text{-}3}$	Common inductors current average value	55.6 A to 61.5 A
$\Delta I_{com1\text{-}3}$	Common inductors current ripple value	0 A to 11.54 A
T_r	Temperature rise	35.9 °C
	Core part number	0K7228E026
N	Number of turns	15
	Number of strands	3 of 10 AWG
	Individual total weight	0.4 kg

TABLE 4. Design guidelines of the IPTs.

Symbol	Name	Value per component
$L_{diff1\text{-}3}$	Differential inductance value	450 µH
$L_{1\text{-}6}$	Self and mutual inductance values	112.5 µH
f_{sw}	Switching frequency of current ripple	75 kHz
$I_{1\text{-}6}$	Phase inductors current average value	27.8 A to 30.7 A
$\Delta I_{1\text{-}6}$	Phase inductors current ripple value	9.7 A to 10.5 A
T_r	Temperature rise	164 °C
	Core Part Number	Customized based on SC2045M1. 25 mm strip width, 8.8 mm leg build-up
N	Number of turns	20
	Number of strands	1 of 10 AWG
	Individual total weight	0.3 kg

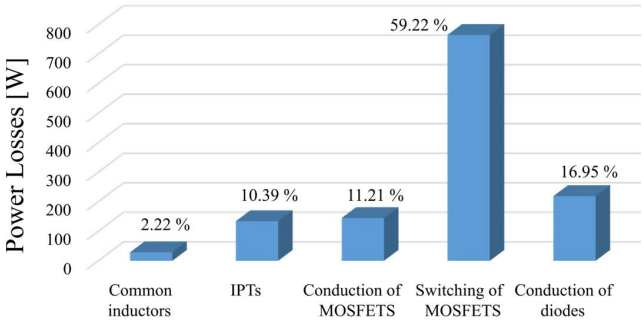

FIGURE 9. SPDIBBC power losses breakdown at 32 kW. The total power losses are around 1291 W.

defines a NA_C constant. The C core size was selected using the M1, MK-Magnetics C core range, ensuring that the offered core window area suits the required winding volume whilst the strip width and core leg build-up were customized to satisfy (8). A customized SC2045M1 C core was carefully chosen for the IPT design, and their design parameters are listed in Table 4.

B. SEMICONDUCTOR DEVICES SELECTION

The selection of the Q_{1-6} switching devices was carried out bearing in mind the high-frequency switching and the blocking voltage, V_{BK}, that should be slightly greater than $V_{in}+V_o$, such that the critical condition occurs when $V_{in} = 385$ V and $V_o = 350$ V, leading $V_{BKmax} > 735$ V. The maximum drain current of Q_{1-6} may be determined estimating the RMS value of the current phase:

$$I_{1-6-RMS} = \begin{cases} \frac{V_{in}D}{2(1-D)}\left\{\frac{1}{R_{load}(1-D)} + \frac{T}{2}\left[\frac{(1-2D)}{2L_{com1-3}} + \frac{2}{L_{diff\,1-3}}\right]\right\} \\ \text{for } D< 0.5 \\ \frac{V_{in}}{2}\left\{\frac{1}{R_{load}}\left(\frac{D}{(1-D)^2}\right) + \frac{T}{2}\left[\frac{(2D-1)}{2L_{com1-3}} + \frac{2}{L_{diff\,1-3}}\right]\right\} \\ \text{for } D> 0.5 \end{cases} \quad (9)$$

yielding $I_{1-6-RMS} = 36.4$ A with a minimum supply voltage. Two 1.2 kV, 50 A CCS050M12CM2 modules from CREE, [28], were thereby selected to exploit its high-frequency, three-phase SiC MOSFETs bridge capability contained in a single module, being the latter suitable for this application to reduce weight and connections between components. In addition, two CGD15FB45P1 gate drivers manufactured by CREE, [29], were used together with the SiC modules, whose external turn-on and the turn-off gate resistors, R_{GON} and R_{GOFF}, respectively, were set to $R_{GON} = 6.6\ \Omega$ and $R_{GOFF} = 4.7\ \Omega$ to enhance appropriate switching speed of each MOSFET.

C. POWER LOSSS ESTIMATION AND THERMAL MANAGEMENT

The estimated power loss breakdown of the SPDIBBC prototype at 32 kW is illustrated in Fig. 9, being 1291 W and 95 % of the total power losses and efficiency. The copper winding and core power losses of the common inductors were estimated using the Magnetics spreadsheet design tool [24], while the corresponding power losses of the IPTs were calculated using the W/kg ratio and the conductor resistance at 100 °C. The conduction power losses of the MOSFETs and diodes were calculated assuming the on-state resistance, $R_{DS(on)} = 35$ mΩ at 100 °C, with $V_{GS} = 20$ V, and the forward voltage drop, $V_F = 2.3$ V, respectively; whilst the MOSFETs switching losses were estimated using the turn on and off periods with $V_{in} + V_o$ at their respective valley and peak of the phase currents. The capacitors power losses were neglected in Fig. 9 since these are smaller than those produced by the magnetic and switching components.

A 416601U00000G, Aavid liquid cold plate [30], was utilized to remove the heat generated by the semiconductors and IPTs power losses. The semiconductor modules were mounted on the top face of the cold plate together with the IPTs, which were encapsulated in a customized aluminium pot, filled up with a 50-3150FR, thermal conductive resin of Epoxies, [31]. This resin was found to be suitable for this work due to its high thermal conductivity, 2.16 W/mK, and wide range of operation temperatures, from −60 °C to 200 °C.

D. CONSTRUCTION DETAILS

Fig. 10 displays a picture of the 32 kW SPDIBBC prototype. The power devices were connected using planar copper bars, through connections as short as possible to minimize parasitic

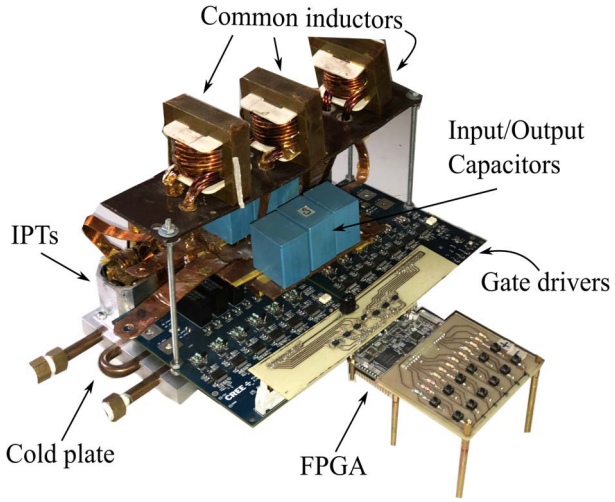

FIGURE 10. Picture of the 32 kW SPDIBBC prototype assembled in the laboratory.

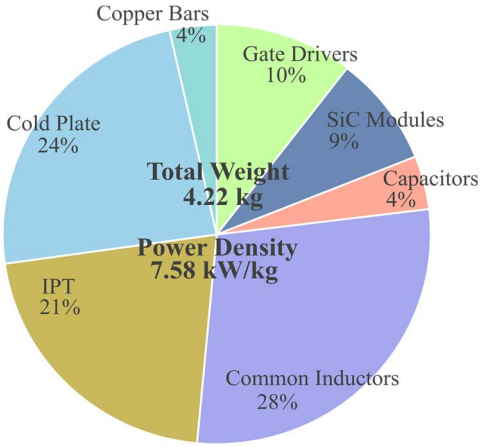

FIGURE 11. Distribution of weight in the 32 kW SPIDBBC prototype.

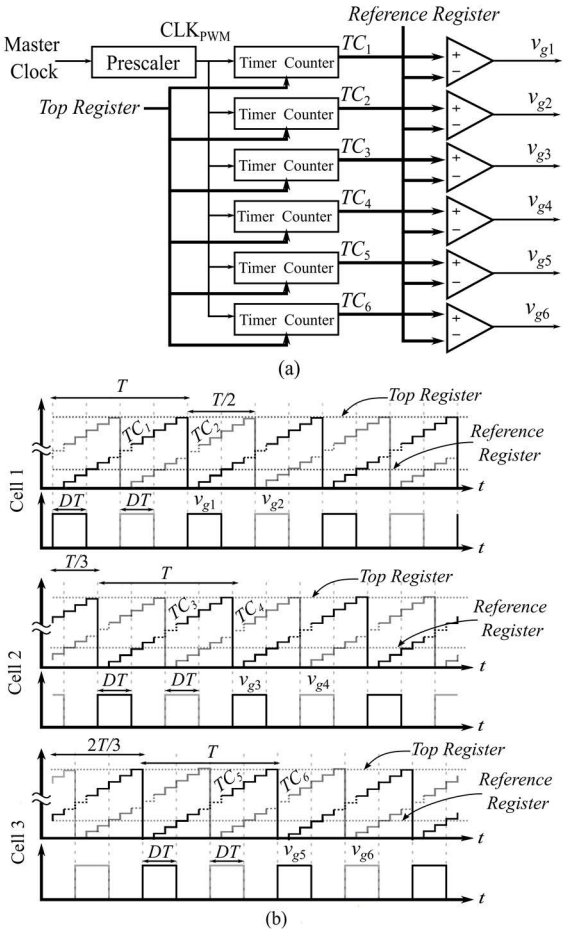

FIGURE 12. Digital PWM scheme for the control signals in the SPDIBBC prototype: (a) block diagram of the control system, (b) signals generated by the control system.

inductances at the high *di*/*dt* junctions and adjusted to the dimensional physical barrier of the component. In addition, two parallel arrangements of three 10 μF, 840 V polypropylene film capacitors, B32776P8106K000, were straight soldered over the copper bars to operate as input and output filters. Fig. 11 shows a component weight breakdown, being the converter total weight 4.22 kg. It is evident that most of the weight can be attributed to the magnetic devices and the cold plate. A 7.58 kW/kg gravimetric power density is achieved, assuming the maximum power capacity and total weight.

The v_{g1} to v_{g6} switching states were performed using a typical high-frequency digital PWM scheme, in count up mode operation, implemented in an Altera DE0 Nano FPGA, [32], as depicted in Fig. 12. The 50 MHz FPGA Master clock was prescaled to drive six 12-bit timer counters, TC_1-TC_6, limited and compared by the Top and Reference Registers, respectively, to produce six 75 kHz, PWM control signals, such that a duty cycle resolution of 0.5 %/switching cycle was obtained. The initial conditions of TC_1-TC_6 were set to produce the appropriate phase shifts. The duty cycle is modified when the Reference Register is updated through two buttons in the FPGA and TC_1-TC_6 are rebooted when the fixed Top Register is attained. The FPGA switching states terminals were connected to the gate drivers through a customized buffer circuitry. The lower gating signals were set to 0 to produce the operation of the anti-parallel Schottky diodes of the three-phase SiC modules and, thereby, cause the circuit diagram of Fig. 1.

IV. EXPERIMENTAL VERIFICATION

The SPDIBBC prototype was tested using a 32 kW, Regatron DC power supply, [33], together with a 32 kW resistive bank. Steady-state electrical and thermal performances of the SPDIBBC prototype were evaluated in the step-down and step-up operating modes of the converter.

Fig. 13 shows the experimental IPT current phases, i_{1a}-i_{1b}, i_{2a}-i_{2b}, and i_{3a}-i_{3b}, measured at 32 kW using two V_{in} supply voltage cases, 385 V and 315 V, such that $D = 0.48$ and $D = 0.52$, which are straightforward displayed at the left and right hand sides of the same figure, Figs. 13(a) and 13(b) respectively. A slight DC current imbalance is evident

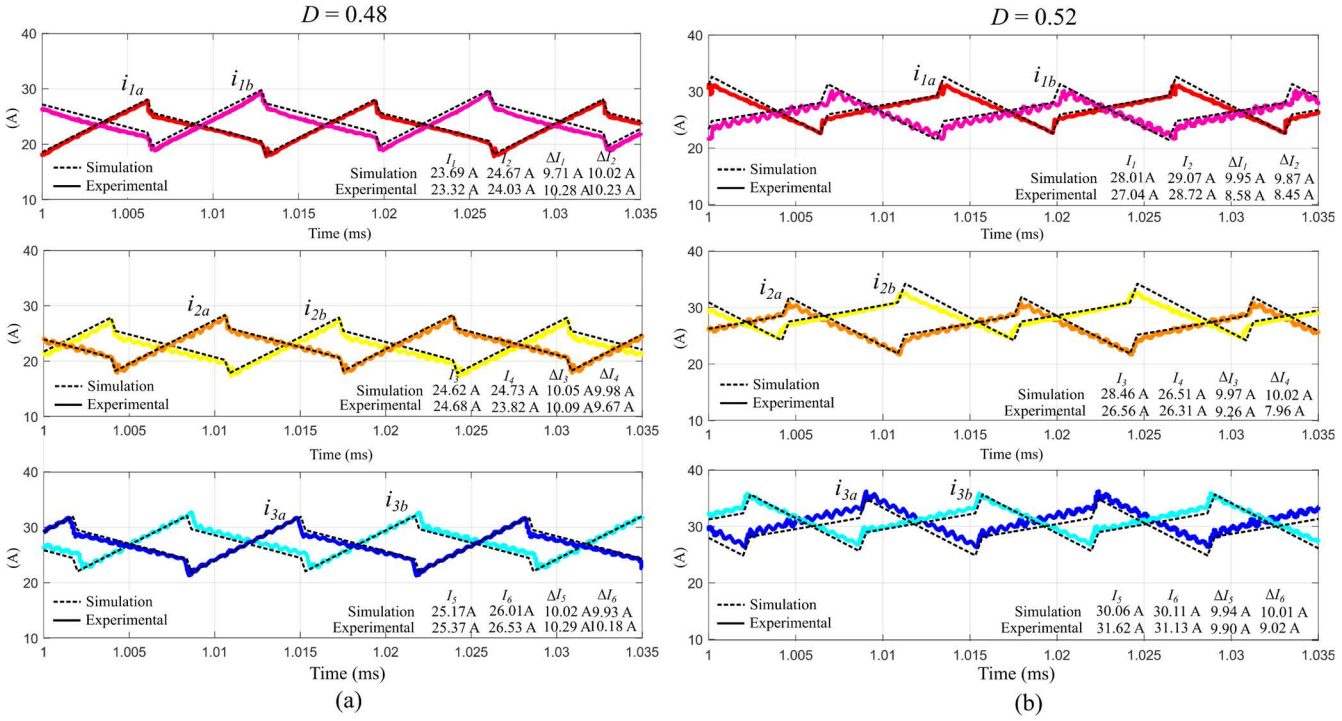

FIGURE 13. Experimental and simulation results of i_{1a}-i_{1b}, i_{2a}-i_{2b}, and i_{3a}-i_{3b} at 32 kW, $V_O = 350$ V when the converter is operating with (a) $D = 0.48$, $V_{in} = 385$ V and (b) $D = 0.52$ $V_{in} = 315$ V.

between each pair of current phases, which was thought to be caused by slight duty cycle mismatches and copper and core losses. The latter was confirmed using a Microcap simulation, shown in the same figure, including the estimated core and copper losses together with the supply and load conditions used in both experiments. A 1.16 A DC imbalance occurs between i_{3a} and i_{3b}, being the critical imbalance among the other phases when $D = 0.48$; however, the imbalance becomes 1.6 A when $D = 0.52$, since the phase currents offsets are greater than the current drawn by the core losses. A high-frequency ripple is noticed in the IPT current waveforms of both modes of operation in Fig. 13, which were thought to be caused by the parasitic interwinding capacitances in the IPT that allow current injection derived from the high-frequency voltage overshoots present at the IPT main connections. The experimental and simulated current ripples ΔI_{1-6} match each other with minimal deviations, which confirms the design inductances of the magnetic components.

Figs. 14(a) and 14(b) present the i_{com1} to i_{com3} measured common inductor currents, respectively for the step-down and step-up operating modes of the prototype at 32 kW and the previously described conditions of V_{in} and D. The experimental waveforms were again compared against the Microcap simulation. A 7.5 A offset deviation is evident between I_{com1} and I_{com3} in the experimental waveforms of Fig. 14(a); meanwhile, an 8 A critical offset imbalance is present between I_{com1} and I_{com3} in Fig. 14(b). These offset imbalances were thought to be caused by slight duty cycle mismatches between switching phases and copper losses, which are comprised of a three-strand copper winding. A small high-frequency ripple is, similarly, evident in the i_{com1} to i_{com3} measured results of Fig. 14 as occurs in the IPT current phases. This characteristic was also attributed to the IPT interwinding capacitances; nevertheless, this ripple became smaller than that of the i_{1a}-i_{1b}, i_{2a}-i_{2b}, and i_{3a}-i_{3b} results of Fig. 13 due to the inherent cancelation ripple originated by each pair of phases. In addition, a 2.3 A maximum deviation is evident in Fig. 14(b) between the simulation and measurement of ΔI_{com2}, which is produced by the output voltage and current increase of the numerical step-up mode result that uses lossless switching devices.

Fig. 15 presents a screenshot of a high-performance oscilloscope used to verify the SPDIBBC prototype operation at 3 kW with $V_{in} = 100$ V and $D = 0.35$. Measurements of $v_{diff\,1}$ to $v_{diff\,3}$ are shown at the top of this figure, whilst v_{com2} and i_{com2} are displayed at the bottom of Fig. 15. These measurement results verify that the SPDIBBC prototype still preserves the ideal steady-state behaviour of Fig. 3, even out of the designed duty cycle range of operation; nevertheless, high-frequency voltage overshoots are visible at the $v_{diff\,1}$ to $v_{diff\,3}$ rising and falling edges due to the typical hard switching phenomena and the parasitic inductances that intrinsically surround the power transistors.

Since the power converter is open-loop controlled and the common current sharing may become slightly unequal, the SPDIBBC prototype was dynamically tested to a 200-to-150 V supply step, and the i_{com1}, i_{com2}, i_{com3}, and v_o responses are shown in Fig. 16, which were captured with the

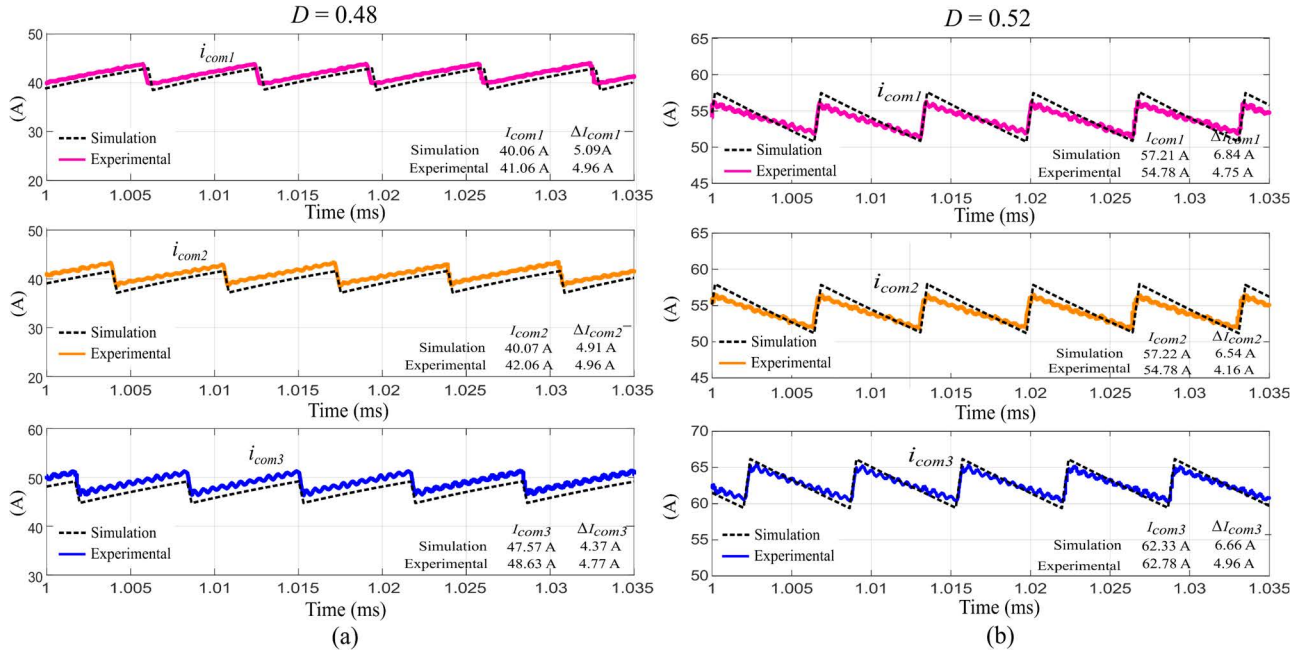

FIGURE 14. Experimental and simulation results of i_{com1}, i_{com2} and i_{com3} at 32 kW, $V_O = 350$ V when the converter is operating with (a) $D = 0.48$, $V_{in} = 385$ V and (b) $D = 0.52$ $V_{in} = 315$ V.

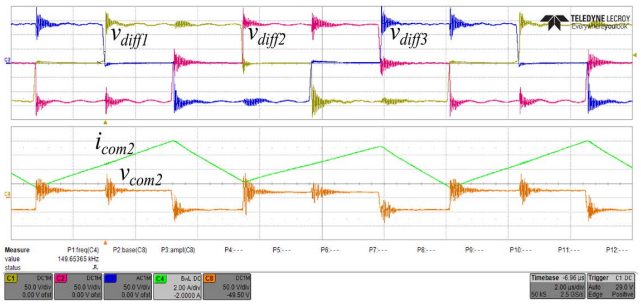

FIGURE 15. $v_{diff\,1}$, $v_{diff\,2}$, and $v_{diff\,3}$ experimental results obtained from the scope together with v_{com2} and i_{com2}. $V_{in} = 100$ V, $D = 0.35$, $P_O = 3$ kW.

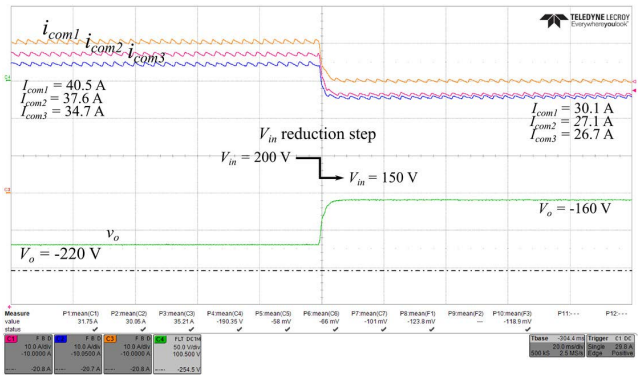

FIGURE 16. Experimental results of i_{com1}, i_{com2}, i_{com3} and v_o with $P_{in} = 25$ kW when a 200-to-150V V_{in} step is applied to the converter being $D = 0.52$.

high-performance oscilloscope when the prototype rig was operating at 25 kW with $D = 0.52$. The latter was performed to analyse the prototype behaviour while emulating a full-cell hard discharge. A current offset imbalance is evident before the step; however, two common currents become almost balanced after the step event, being noticeable a 3.4 A maximum imbalance between I_{com1} and I_{com3} in Fig. 16. Close current sharing imbalance was again observed when the prototype was tested with other supply steps, which was judged to be naturally caused due to the open-loop operation of the multiphase converter and, also, small transistor switching time deviations between phases.

A simplified steady-state thermal model was obtained using the thermal resistances and the estimated power losses of each component of the SPDIBBC prototype, which is presented in the block diagram of Fig. 17(a), assuming the critical operation condition at 32 kW with $D = 0.52$. The IR photographic temperature measurements shown in Figs. 17(b) and 17(c) depict the thermal behaviour of the prototype in the step-down and step-up modes, respectively, at a thermal steady state, which complies with the predicted temperatures of Fig. 17(a). A 113 °C hottest spot was revealed at the IPT cores in the thermal picture of Fig. 17(c), which is acceptable since it is well below the core maximum allowable temperature of 155 °C, [32].

The overall efficiency of the SPDIBBC was measured, ranging the load from 5 kW to 32 kW, while a thermal steady-state was reached. Fig. 18 plots this measured experimental efficiency supplying the rig with the two supply voltage cases of 385 V and 315 V, and a 350 V output. Maximum efficiency of 98 % is obtained at full load at maximum supply voltage,

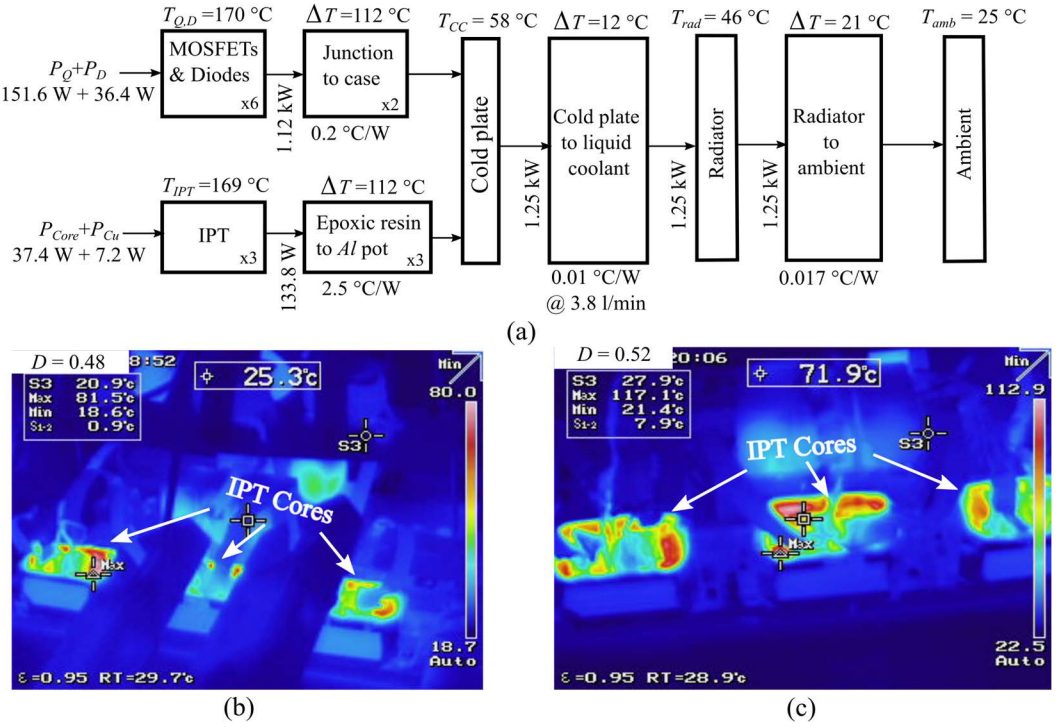

FIGURE 17. Thermal management of the SPDIBBC. (a) Simplified thermal model of the SPDIBBC operating at 32 kW. Screenshot of the thermal IR camera at 32 kW when the SPDIBBC is operating as step-down, (b), and step-up, (c), DC-DC converter.

TABLE 5. Comparison of multiphase dc-dc converters.

	SPDIBBC	DIBBC [14]	Dual-Interleaved Boost converter [13]	Multiphase dc-dc converter [34]
Power flow	Unidirectional	Unidirectional	Bidirectional	Bidirectional
Power capacity	32 kW	32 kW	80 kW	56 kW
Transistors	6	2	4	20
V_{BK}	$V_{in} + V_o$	$V_{in} + V_o$	V_o	V_o
Magnetic components	6	2	2	18
Phases	6	2	2	4
Weight	4.22 kg	4.35 kg	5.09 kg	5 kg
Efficiency	98 %	97 %	97%	96 %
Gravimetric power density	7.58 kW/kg	7 kW/kg	15.7 kW/kg	11.2 kW/kg
V_{in}	315 – 385 V	315 – 385 V	300 – 380 V	200 V

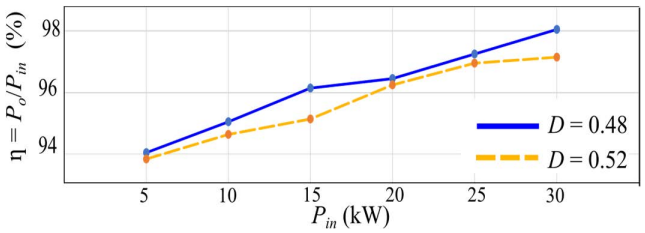

FIGURE 18. SPDIBBC Prototype measured efficiency ranging the load from 5 to 32 kW.

whereas the efficiency becomes 94 % when the load draws 5 kW. The prototype is more efficient when the supply is at its maximum rather than operating with a minimum supply voltage, which is evident in Fig. 18 since the device currents are slightly reduced.

Table 5 lists and summarizes the main features accomplished in the SPDIBBC prototype compared to other converters reported in the literature. As shown in Table 5, high power capacities are used while the number of switching devices is increased; nevertheless, V_{in} is around 350 V in most converters listed because current EV power trains require this voltage level in their DC link.

Due to the number of controlled switching devices of the proposed topology, concerns about control complexity and power scalability may arise. It is known that model-based control using conventional average modelling may lead to high-order controllers as the number of dynamic

elements increases. However, since power electronics tend to split power to reduce dimensions, alternative control techniques should be considered.

In particular, a type of hybrid controller was introduced in [37] and [38] that, based on the controllability issues of approximated integrating switched systems, derives very simple controllers, regardless of the number of switching devices [37], [38]. Such proposals can also lead to simple controllers based on discrete models, as in [36]. Contrary to conventional controllers, those in [37] and [38] can address multi-objective problems such as current tracking, phase and ripple control from the first switching event. The use of such a control strategy is foreseen as promising in the control of high-density converters.

V. CONCLUSION

Using multiple DIBBC cells sharing the same input and output filters allowed improvement of the gravimetric power density while producing almost balanced current sharing between phases in open loop conditions. The latter encourages the study of other realizations of interleaved strategies with magnetic coupling for being developed in multiple cells, offering compact medium-power DC-DC converters for electromobility applications. However, the technique is open for other applications where high-power density is critical. An analysis of the principle of operation of the SPDIBBC, together with a brief comparison respective to the DIBBC, was presented, showing numerical verification of the steady-state idealized waveforms in contrast to experimental measurements obtained from a 32 kW prototype. The achieved gravimetric power density is 7.58 kW/kg, and the measured efficiency is 98 % at full load, being the temperature slightly below 110 °C at full load. Moreover, the individual IPTs of the SPDIBBC were built using single wire windings, which is easier to implement and construct than the copper foil utilized for the DIBBC IPT in [14].

The SPDIBBC was operated with a 350 V $\pm$ 10 % supply voltage, and a 75 kHz switching frequency and robust steady-state experimental results were obtained. The load ranged from 5 to 32 kW, and the efficiency was analysed, 4 % efficiency reduction was obtained when the converter operated at light conditions and increased with the supply voltage. The optimal operation of the SPDIBBC occurred in the buck converter mode, with $D < 0.5$, having high efficiency and lower temperature compared to the boost operation. Dynamic load experiments revealed a small current imbalance between the IPTs phases and common currents. We hypothesize that this could be caused by slight duty ratio and/or inductance deviations that may be improved using a current control scheme. Hybrid control schemes such as those in [37] and [38] could be implemented to ensure well-balanced phase currents on the 32 kW SPDIBBC prototype without introducing complexity in the controller.

Further investigation is needed to improve the gravimetric power density of the common inductors and magnetic integration of the IPTs, which would be especially significant in electromobility. Also, the implementation of bidirectional power capability could be examined to regenerate energy into an energy bank.

Finally, considering the unavoidable extension of the power level in electric transportation, this sort of Buck-Boost converter should be able to block high voltage levels. Nowadays, with the maturation of SiC semiconductors, there are high-voltage, SiC, MOSFET modules capable of operating with 1.7, 2.5, and 3.3 kV, [3]. The SPDIBBC prototype may be scaled through the use of these modules, adjusting the thermal management and gate drivers.

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REFERENCES

[1] B. Sarlioglu, "Automotive power electronics: Current status and future trends," in *Proc. Int. Aegean Conf. Electr. Mach. Power Electron. (ACEMP) Int. Conf. Optim. Electr. Electron. Equip. (OPTIM)*, Aug. 2019, pp. 1–2, doi: 10.1109/ACEMP-OPTIM44294.2019.9007120.

[2] P. Shibata, J. Ramoul, R. Rodriguez, A. D. Callegaro, P. Suntharalingam, J. S. Cotton, and A. Emadi, "Weight reduction considerations for thermal management of aerospace power electronics," in *Proc. IEEE Transp. Electrific. Conf. Expo (ITEC)*, Jun. 2021, pp. 502–506, doi: 10.1109/ITEC51675.2021.9490150.

[3] D. Dong, X. Lin, L. Ravi, N. Yan, and R. Burgos, "Advancement of SiC high-frequency power conversion systems for medium-voltage high-power applications," in *Proc. IEEE 9th Int. Power Electron. Motion Control Conf. (IPEMC-ECCE Asia)*, Nov. 2020, pp. 717–724, doi: 10.1109/IPEMC-ECCEAsia48364.2020.9367948.

[4] Z. S. Du, P. Channegowda, P. Kshirsagar, and S. Dwari, "High density high power DC-DC converter architectures for future electric transportation applications," in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE)*, Sep. 2019, pp. 5862–5869, doi: 10.1109/ECCE.2019.8913313.

[5] L. Zhang, Y. Li, Y. Zhang, X. Yuan, Z. Wang, and Z. Li, "A 100 kW forced-air-cooled SiC MOSFET converter achieving a power density of 1.657 kW/L and an efficiency over 98.5%," in *Proc. IEEE 9th Int. Power Electron. Motion Control Conf. (IPEMC-ECCE Asia)*, Nov. 2020, pp. 3443–3448, doi: 10.1109/IPEMC-ECCEAsia48364.2020.9368191.

[6] S. Kimura, K. Nanamori, and M. Yamamoto, "Modeling and design of interleaved multi-phase DC-DC converter with 2-phase coupled inductor cell for high power density," in *Proc. IEEE 6th Int. Conf. Renew. Energy Res. Appl. (ICRERA)*, Nov. 2017, pp. 416–422, doi: 10.1109/ICRERA.2017.8191096.

[7] J. Scoltock, G. Calderon-Lopez, and A. J. Forsyth, "Topology and magnetics optimisation for a 100-kW bi-directional DC-DC converter," in *Proc. IEEE Vehicle Power Propuls. Conf. (VPPC)*, Dec. 2017, pp. 1–6, doi: 10.1109/VPPC.2017.8330900.

[8] S. Lu, M. Mu, Y. Jiao, F. C. Lee, and Z. Zhao, "Coupled inductors in interleaved multiphase three-level DC–DC converter for high-power applications," *IEEE Trans. Power Electron.*, vol. 31, no. 1, pp. 120–134, Jan. 2016, doi: 10.1109/TPEL.2015.2398572.

[9] D. De, C. Klumpner, C. Patel, K. Ponggorn, M. Rashed, and G. Asher, "Modelling and control of a multi-stage interleaved DC–DC converter with coupled inductors for super-capacitor energy storage system," *IET Power Electron.*, vol. 6, no. 7, pp. 1360–1375, 2013.

[10] S. S. Alharbi and M. Matin, "Experimental evaluation of medium-voltage cascode gallium nitride (GaN) devices for bidirectional DC-DC converters," *CES Trans. Electr. Mach. Syst.*, vol. 5, no. 3, pp. 232–248, Sep. 2021, doi: 10.30941/CESTEMS.2021.000227.

[11] G. Calderon-Lopez, A. J. Forsyth, D. L. Gordon, and J. R. McIntosh, "Evaluation of SiC BJTs for high-power DC–DC converters," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2474–2481, May 2014, doi: 10.1109/TPEL.2013.2273293.

[12] R. Bosshard and J. W. Kolar, "All-SiC 9.5 kW/dm^3 on-board power electronics for 50 kW/85 kHz automotive IPT system," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 5, no. 1, pp. 419–431, Mar. 2017, doi: 10.1109/JESTPE.2016.2624285.

[13] G. Calderon-Lopez, J. Scoltock, Y. Wang, I. Laird, X. Yuan, and A. J. Forsyth, "Power-dense bi-directional DC–DC converters with high-performance inductors," *IEEE Trans. Veh. Technol.*, vol. 68, no. 12, pp. 11439–11448, Dec. 2019, doi: 10.1109/TVT.2019.2943124.

[14] T.-R. Granados-Luna, I. Araujo-Vargas, A. J. Forsyth, K. Cano-Pulido, P.-E. Velazquez-Elizondo, I. Cervantes, F. Gomez-Olguin, and A. Villarruel-Parra, "Two-phase, dual interleaved buck–boost DC–DC converter for automotive applications," *IEEE Trans. Ind. Appl.*, vol. 56, no. 1, pp. 390–402, Jan. 2020, doi: 10.1109/TIA.2019.2942026.

[15] A. Villarruel-Parra and A. J. Forsyth, "Modeling phase interactions in the dual-interleaved buck converter using sampler decomposition," *IEEE Trans. Ind. Electron.*, vol. 66, no. 5, pp. 3316–3322, May 2019, doi: 10.1109/TIE.2018.2854585.

[16] G. Traiki, H. Ouajji, A. Bifadene, and O. Bouattane, "Comparative study of boost, interleaved and double dual boost converter topologies," in *Proc. Int. Conf. Electron., Control, Optim. Comput. Sci. (ICECOCS)*, Dec. 2018, pp. 1–6, doi: 10.1109/ICECOCS.2018.8610575.

[17] G. Calderon-Lopez, Y. Wang, and A. J. Forsyth, "Mitigation of gap losses in nanocrystalline tape-wound cores," *IEEE Trans. Power Electron.*, vol. 34, no. 5, pp. 4656–4664, May 2019, doi: 10.1109/TPEL.2018.2863665.

[18] J. Scoltock, Y. Wang, G. Calderon-Lopez, and A. J. Forsyth, "Rapid thermal analysis of nanocrystalline inductors for converter optimization," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 3, pp. 2276–2284, Sep. 2020, doi: 10.1109/JESTPE.2019.2947223.

[19] K. Warnakulasuriya, F. Nabhani, and V. Askari, "Development of a 100 kW, 20 kHz nanocrystalline core transformer for DC/DC converter applications," in *Proc. Int. Exhib. Conf. Power Electron., Intell. Motion, Renew. Energy Energy Manag. (PCIM Europe)*, vol. 2016, pp. 1–8.

[20] G. R. C. Mouli, J. H. Schijffelen, P. Bauer, and M. Zeman, "Design and comparison of a 10-kW interleaved boost converter for PV application using SI and SiC devices," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 5, no. 2, pp. 610–623, Jun. 2017, doi: 10.1109/JESTPE.2016.2601165.

[21] H. Cui, K. D. T. Ngo, J. Moss, M. H. F. Lim, and E. Rey, "Inductor geometry with improved energy density," *IEEE Trans. Power Electron.*, vol. 29, no. 10, pp. 5446–5453, Oct. 2014, doi: 10.1109/TPEL.2013.2289926.

[22] H. Cui, K. D. T. Ngo, J. Moss, M. Lim, and E. Rey, "Design and evaluation of the constant-flux inductor with enclosed-winding," in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE)*, Sep. 2014, pp. 5229–5236, doi: 10.1109/ECCE.2014.6954118.

[23] R. W. Erickson and D. Maksimović, *Fundamentals of Power Electronics*, 2nd ed. New York, NY, USA: Springer, 2004, ch. 7, pp. 235–241.

[24] Magnetics Inc. *Magnetics Powder Core Catalog*. Accessed: 2020. [Online]. Available: https://www.mag-inc.com

[25] W. Flanagan, *Handbook of Transformer Design and Applications*. New York, NY, USA: McGraw-Hill, 1993.

[26] *MK-Magnetics*. Accessed: 2022. [Online]. Available: https://www.mkmagnetics.com

[27] C. W. T. McLyman, *Transformer and Inductor Design Handbook*. Boca Raton, FL, USA: CRC Press, 2004.

[28] *CCS050M12CM2 Datasheet of Wolfspeed*. Accessed: 2021. [Online]. Available: https://www.wolfspeed.com

[29] *CGD15FB45P1 Datasheet of Wolfspeed*. Accessed: 2021. [Online]. Available: https://www.wolfspeed.com

[30] *AAVID Thermal Division of BOYD Corp*. Accessed: 2022. [Online]. Available: https://www.boydcorp.com/aavid.html

[31] *Epoxies Technical Bulletin*. Accessed: 2014. [Online]. Available: https://epoxies.com/

[32] *DE0-Nano Development and Education Board*. Accessed: 2022. [Online]. Available: https://www.terasic.com.tw/cgi-bin/page/archive.pl?No=593

[33] Regatron Inc. *Regatron*. Accessed: 2022. [Online]. Available: https://www.regatron.com/programmable-power-supplies/en/

[34] M. Pavlovsky, G. Guidi, and A. Kawamura, "Assessment of coupled and independent phase designs of interleaved multiphase buck/boost DC–DC converter for EV power train," *IEEE Trans. Power Electron.*, vol. 29, no. 6, pp. 2693–2704, Jun. 2014, doi: 10.1109/TPEL.2013.2273976.

[35] A. Villarruel-Parra and A. J. Forsyth, "Enhanced average-value modeling of interleaved DC–DC converters using sampler decomposition," *IEEE Trans. Power Electron.*, vol. 32, no. 3, pp. 2290–2299, Mar. 2017, doi: 10.1109/TPEL.2016.2559449.

[36] K. Cano-Pulido, I. Araujo-Vargas, I. Cervantes, T.-R. Granados-Luna, and P.-E. Velázquez-Elizondo, "Sampled-data model of a two-phase, dual interleaved buck–boost converter with PCM," *IEEE Trans. Power Electron.*, vol. 37, no. 6, pp. 6349–6358, Jun. 2022, doi: 10.1109/TPEL.2021.3125968.

[37] A. Mendoza-Torres, N. Visairo, C. Nuñez, J. Armenta, E. Rodríguez, and I. Cervantes, "Switching rule for a bidirectional DC/DC converter in an electric vehicle," *Control Eng. Pract.*, vol. 82, pp. 108–117, Jan. 2019.

[38] O. F. Ruiz, A. Mendoza-Torres, I. A. Diaz-Diaz, I. V. N. Cervantes, C. Nunez, and E. Barcenas, "Controllability of rectifiers and three point hysteresis line current control," *Control Eng. Pract.*, vol. 55, pp. 212–225, Oct. 2016, doi: 10.1016/j.conengprac.2016.06.012.

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