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RESEARCH ARTICLE

Cryogenically-Cooled Power Electronics for Long-Distance Aircraft

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ABSTRACT New aerodynamic aircraft concepts enable the storage of volumetric liquid hydrogen (LH_2). Additionally, the low temperatures of LH_2 allow technologies such as the superconductivity of electrical components. An increased power density of the onboard wiring harness and the electrical machine can be expected. Nevertheless, the power electronic drive inverter has to deliver high power and high switching frequencies (f_{PWM}s) under challenging conditions. Therefore, knowledge of the electric behaviour of different semiconductor materials under cryogenic temperatures is essential to answer the question: "Are modern power electronics a technology enabler or a system bottleneck?" This publication shows a comprehensive novelty study for cryogenic power electronics based on experimental-driven semiconductor investigations, mission profile-based considerations, requirement analyses of superconducting electrical machines, and studies of the cooling concepts. All aspects are discussed within one interdisciplinary publication. A cryogenic system cannot be considered without a feasible cooling concept. Different semiconductor structures based on various materials (silicon (Si), silicon carbide (SiC) and gallium nitride (GaN)) are evaluated for their suitability. The collected data and the literature review draw a technology feasibility studies supported by detailed cooling system analyses and superconducting electrical machine requirements. The power demand and high f_{PWM} lead to a SiC non-cryogenic inverter approach. Due to the detailed cooling system assessment, a loss reduction is achieved by optimising the junction temperature (T_J) under various load cases (LCs) out of the mission profile.

INDEX TERMS Long-distance aircraft, fuel cell, liquid hydrogen, cryogenic cooler design, high temperature superconductivity, cryogenic electrical power supply system, cryogenic power electronics, experimental semiconductor comparison, cryogenic inverter design.

ACRONYMS

2DEG	two-dimensional electron gas
AC	alternating current
AlGaAs	aluminium gallium arsenide
AlSiC	aluminium matrix with SiC particles
ANPC	active neutral point clamped
BLI	body layer ingestion
BWB	blended wing body
CAL	controlled axial lifetime
CFD	computational fluid dynamics
CO_2	carbon dioxide
D-HEMT	depletion-mode HEMT
DC	direct current
DCB	direct bonded copper
DPT	double pulse test
DUT	device under test
E-HEMT	enhancement-mode HEMT
EMC	electromagnetic compatibility
FEM	finite element method

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FPGA	field-programmable gate array
GaAs	gallium arsenide
GaN	gallium nitride
H_2	hydrogen
He	helium
HEMT	high-electron-mobility transistor
HTS	high-temperature superconductors
HV	high voltage
IGBT	insulated gate bipolar transistor
IMAB	Institute for Electrical Machines, Traction and Drives
LC	load case
LH_2	liquid hydrogen
LHe	liquid helium
LHV	lower heating value
LN_2	liquid nitrogen
MF	manufacturer
MOSFET	metal-oxide-semiconductor field-effect transistor
N	nitrogen
NASA	National Aeronautics and Space Administration
NO_x	nitrogen oxide
PCB	printed circuit board
PEM	proton-exchange membrane
Pt	platinum
RBCC	reverse brayton cycle cryocoolers
ReBCO	rare-earth barium copper oxide
RMS	root mean square
SE^2A	Sustainable and Energy-Efficient Aviation
Si	silicon
SiC	silicon carbide
THD	total harmonic distortion
TO	transistor outline
WBG	wide-bandgap

LIST OF SYMBOLS

A_{Ch}	cross-section of the cooling channel
A_{r}	effective heat transfer surface
A_{T}	real heat transfer area
b_{C}	cooler width
b_{Ch}	channel width
B_{ext}	outer magnetic field
b_{r}	raster of the cooling channels
b_{s}	side wall
C_{Ch}	circumference of the channel
$\cos\varphi$	power factor
$c_{\mathrm{p,H2}}$	thermal capacity of H_2
d	thickness of the superconductor
D_{C}	hydr. diameter of cooling channel
D_{h}	hydr. diameter
d_{z}	wall thickness laser-welded sheets
E_{off}	turn-off energy loss per pulse
E_{on}	turn-on energy loss per pulse
E_{rec}	reverse recovery energy loss
f	frequency
f_{PWM}	switching frequency
f_{s}	stator frequency
F_{svm}	fourier decomposed factor
h	flight altitude
H_0	amplitude of the oscillating external magnetic field
h_{C}	cooler height
h_{Ch}	channel height
h_{o}	upper cover
h_{spr}	minimum height of base plate
h_{z}	height laser-welded heat exchanger
I_{c}	critical current
i_{C}	collector current
I_{Device}	nominal device current (at $T_{\mathrm{J}} = 298.15\,\mathrm{k}$)
I_{dss}	drain-to-source leakage current
$I_{\nu,\mathrm{s}}$	nth RMS harmonic of the phase current
$\hat{i}_{\mathrm{s}}$	phase peak current
I_{ref}	reference current
I_{s}	RMS phase current
I_{t}	transport current
$J_{\perp}$	current density distribution
L_{C}	cooler length
L_{Ch}	cooler channel length
L_{y}	vertical distance between the tapes
L_{z}	length laser-welded heat exchanger
M	modulation level
m	phase number
m_{Cp}	mass of the cooling plate
m_{Ex}	weight of heat exchanger without connecting flanges
$\dot{m}_{\mathrm{Ch}}$	mass flow per channel
$\dot{m}_{\mathrm{cp}}$	mass flow through the cooler plate
$\dot{m}_{\mathrm{H2}}$	H_2 mass flow
$\dot{m}_{\mathrm{He}}$	H_e mass flow
m_{Switch}	mass of a single-switch module
n_{Chip}	number of parallel-switched chips per module
n_{Ch}	number of cooling channels
N_{u}	nusselt number
$N_{\mathrm{u,m}}$	medium value of nusselt number
n_{zm}	number of channels for each medium
P_{C}	compressor power
P_{in}	added electrical power
P_{L}	power losses
$P_{\mathrm{L,Amb}}$	boiling losses
$P_{\mathrm{L,Bb}}$	power losses backbone
$P_{\mathrm{L,C}}$	conductive-dependent power losses
$P_{\mathrm{L,Ch}}$	power losses per channel
$P_{\mathrm{L,Chip}}$	power losses per chip
$P_{\mathrm{L,Con}}$	power losses DC/DC converter
$P_{\mathrm{L,EM}}$	power losses per electrical machine
P_{LH2}	H_2 power
$P_{\mathrm{L,HB}}$	power losses per half-bridge
$P_{\mathrm{L,Inv}}$	power losses per inverter
$P_{\mathrm{L,S}}$	frequency-dependent power losses
$P_{\mathrm{L,Switch}}$	power losses per switch

P_{mag}	magnetisation losses
P_{Shaft}	mechanical shaft power
P_{T}	turbine power
P_{trans}	transport losses
Q	hysteresis loss per cycle
Q_{oss}	output charge
Q_{rr}	reverse recovery charge
r	corner radius of the cooler
R_{CE}	collector-to-emitter resistance
$R_{\mathrm{DS,on}}$	drain-to-source resistance ($R_{\mathrm{DS,on}}$)
$R_{\mathrm{DS,on,dyn}}$	dynamic drain-to-source resistance
R_{e}	reynolds number
$R_{\mathrm{e,m}}$	medium value of reynolds number
R_{F}	forward resistance (R_{F})
R_{on}	on-resistance
$R_{\mathrm{th,C-H2}}$	thermal resistance from case to H_2
$R_{\mathrm{th,J-C}}$	thermal resistance from junction to case
$\sum R_{\mathrm{th,J-C}}$	cumulated thermal resistance from junction to case
S	entropy
s	position
T	temperature
t	time
T_{C}	critical temperature
t_{fall}	fall time
T_{Hi}	H_2 input temperature heat exchanger
T_{Ho}	H_2 output temperature heat exchanger
T_{J}	junction temperature
T_{m}	average working temperature
T_{NBP}	temperature at normal boiling point
t_{rise}	rise time
V_{Break}	breakdown voltage
v_{CE}	collector-emitter voltage
V_{CE0}	zero collector-to-emitter voltage
V_{DC}	DC voltage
v_{DS}	drain-source voltage
V_{F0}	zero forward voltage drop
$\dot{V}$	volume flow
v_{GE}	gate-emitter voltage
v_{GS}	gate-source voltage
V_{Th}	threshold voltage
V_{ref}	reference voltage
w	width of the superconductive tape
w_{z}	width laser-welded heat exchanger
α_{m}	average coefficient of heat transfer
Δh	enthalpy change
ΔT	temperature difference
$\Delta T_{\mathrm{m,Ex}}$	medium temperature drop in the heat exchange
$\eta_{\mathrm{LH2-Shaft}}$	full efficiency chain from tank to shaft
λ	failure in time
λ_{AlSiC}	thermal conductivity of AlSiC
λ_{H2}	thermal conductivity of H_2
λ_{m}	medium thermal conductivity
ϱ_{H2}	density of H_2

I. INTRODUCTION

The worldwide transportation sector produced over 16.2 % of greenhouse gases in 2016. Before 2020, civil aviation accounted for around 1.9 % of global traffic, although only 10 % of the world's population has access to air travel. A further traffic increase is expected after the pandemic, mainly due to further economic development in Asia [1, Pages: 84189-84190].

However, the harmful carbon dioxide (CO_2) emissions caused by humans must be reduced to limit climate change. The provision of sustainable energy generation and the efficiency from energy production to consumption are crucial.

Several technical solutions meet the specified goals with high and low technology readiness levels to overcome our transportation challenge. Technical solutions have been discussed that promise to meet the stated goals. However, the degree of technology maturity varies greatly, so more detailed investigations are necessary.

Technologies for long-range rail and air transport compete under climate constraints. Within a continent, an improved train infrastructure can achieve higher efficiencies under high infrastructure costs, high material investments, and increased travel time as air traffic ($t \leq 2.5$ h) [2].

Principally, high-speed intercontinental traffic could be possible with evacuated magnetic levitation trains. Nevertheless, this technology has substantial infrastructure costs and high material investment of up to 64 million dollars per kilometre, depending on the location [3, Page: 23]. Separately, new aerodynamics and drive train concepts could improve short- to long-range aircraft to an acceptable efficiency level to combine customer needs and environmentally friendly transportation [1]. The infrastructure requirements for air traffic are low and aviation has lower material investments than evacuated magnetic levitation [3, Page: 24]. Moreover, multiple power source opportunities exist to improve the sustainability of long-range aircraft, leading to different power trains.

A. COMPARISON OF SUSTAINABLE PROPULSION CONCEPTS FOR LONG-DISTANCE AIRCRAFT

Fig. 1 compares two possible power train configurations and shows essential global social aspects to gain the research on cryogenic operating electrical components, such as the inverter.

Synthetic fuel is a ''climate neutral'' energy source option generated from renewably-produced hydrogen (H_2) and CO_2 by Fischer-Tropsch-Synthesis or methanol pathway. A turbine generates thrust conventionally [4]. Synthetic fuels offer good gravimetric and volumetric energy densities, e.g., 19.9 MJ $\cdot$ kg^{-1} and 15.9 MJ $\cdot$ L^{-1} for Methanol [4], which is only half the size of jet fuel A1 with 43.2 MJ $\cdot$ kg^{-1} and 34.9 MJ $\cdot$ L^{-1}. A mixture of H_2 and Ammonia promises a further increase [4, Page: 18]. The upper path in Fig. 1 illustrates the production-to-thrust efficiency potentials of e-fuel

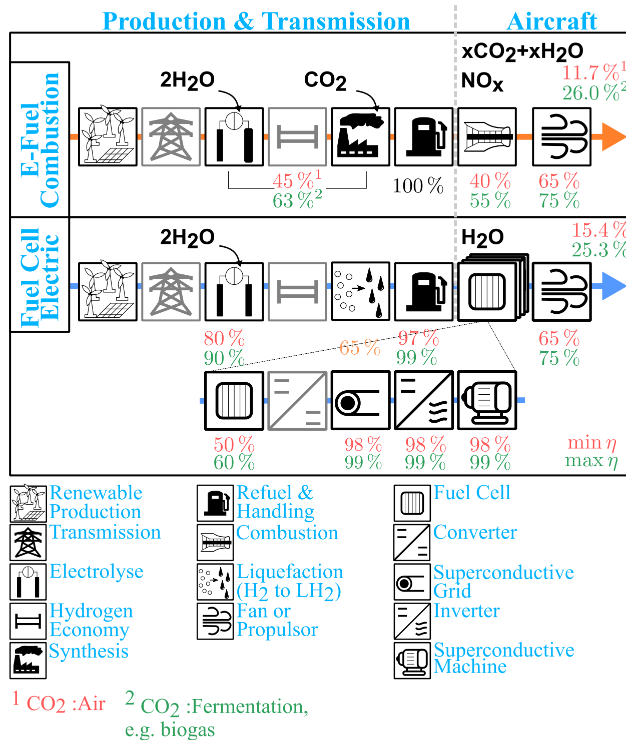

FIGURE 1. Comparison of E-Fuel combustion and fuel cell superconductive electric approach.

combustion with a worst case of 12 % up to the best value of 26 %. The power-to-liquid efficiency with high-temperature electrolysis is given by 45 % (source: air) and up to 63 % (source: biogas) [5, Page: 17]. Today's gas turbines reach up to 40 % overall efficiency (a combination of propulsive and thermodynamic efficiency) [6, Page: 37]. Thereby, the propulsive efficiency of the turbine is over 75 %, and the thermodynamic efficiency is about 55 %. Further developments predict a yearly thermodynamic efficiency increase of 0.4 % [6, Page: 37].

Another energy source opportunity is to use H_2 as energy source. Compressed H_2 gaseous (700 bar) has excellent gravimetric of $120\,\mathrm{MJ} \cdot \mathrm{kg}^{-1}$ (lower heating value (LHV)) but lower volumetric energy densities $5.6\,\mathrm{MJ} \cdot \mathrm{L}^{-1}$ [7, Page: 1]. Nevertheless, liquefaction can nearly double the volumetric energy density of $10.1\,\mathrm{MJ} \cdot \mathrm{L}^{-1}$ [8].

It is also possible to burn H_2 in a turbine conventionally or use it in a fuel cell system [8]. Thus, the National Aeronautics and Space Administration (NASA) works on the turboelectric hybrid blended wing body (BWB) concept N3-X. This approach uses two superconducting turbo-generators at the wingtips to produce electricity. After-fans with superconducting electrical machines fed by power electronics generate the thrust [9].

In this suggested approach, a fuel cell reduces the impact of burned H_2 at high flight altitude (h). There are statements that the H_2O out of a fuel cell has less climate impact because of its short life at high altitudes [10, Page: 12]. Moreover, the lower pathway in Fig. 1 illustrates the fuel cell approach's production-to-thrust efficiency potentials, which could improve the overall average efficiency chain. Moreover, this approach reduces noise and nitrogen oxide (NO_x) during taking off and landing. Production efficiencies of H_2 from 80 % up to 90 % in high-temperature electrolysis are reached, but 35 % of the stored energy has to be used to liquefy to cryogenic temperatures to reach acceptable volumetric densities [8]. The proton-exchange membrane (PEM) fuel cell systems allow efficiencies from 50 % to 60 % [8, Page: 13]. Additionally, cryogenic temperatures enable using superconducting components in the drive train.

This suggested fuel cell cryogenic drive train approach has a lot of technical challenges and requires fundamental research on:

- H_2 transport and renewable production
- Lightweight storage of LH_2 and integration
- The increasing power density of the fuel cell (Currently: up to $4\,\mathrm{kW} \cdot \mathrm{kg}^{-1}$, [8, Page: 15], future (approx. 10 to 20 years): $10\,\mathrm{kW} \cdot \mathrm{kg}^{-1}$ [11, Page: 5])
- Increasing the efficiency of the fuel cell system and cooling efforts of the fuel cell system
- Advanced cooling system and the use of combined system synergies
- Avoiding leakage of the H_2 system
- High voltages (HVs) in cryogenic media to face high electrical power demands
- Design of current limiters in case of failure
- **Investigation of a superconducting electrical machine fed by power electronics**
- **Understanding the electrical behaviour of power electronic devices in cryogenic media**
- **Cooling of superconducting and non-superconducting components**

The drive inverter is one crucial electrical component. It must deliver high power and f_{PWM} under challenging conditions. Are the power electronics a bottleneck of this fuel-cell driven cryogenic drive train for a long-distance aircraft or not? It is essential to answer this question by considering system aspects, semiconductor material behaviours and the inverter's heat sink design. A few excellent studies focus on cryogenic drive train analyses, semiconductor material investigations under cryogenic media, or inverter design with nitrogen (N) cooling considerations.

B. SCIENTIFIC CONTRIBUTION

A holistic system approach for a turboelectric short-range passenger aircraft is discussed in [12]. This publication analyses turboelectric propulsion's electromagnetics, thermic and mechanics system interactions. The cryogenic cooling system of a superconducting aircraft propulsion system is modelled in [13]. On the power electronic component level, there are two suggestions for a turboelectric inverter design with cooling considerations. A scaled cryogenic 44 kW Si-active neutral point clamped (ANPC) inverter design with liquid and gaseous N is presented in [14]. Otherwise, the non-cryogenic

inverter approach is based on the SiC-ANPC inverter. A MW non-cryogenic SiC inverter design with liquid and gaseous N cooling considerations is outlined in [15]. Moreover, the first cooling evaluation results based on gaseous and liquid nitrogen (LN_2) are presented in [16]. Other cryogenic power electronic inverter designs in the literature have lower power ratings without cooling considerations. On the semiconductor level, a few studies on the measurement of semiconductor materials in the cryogenic working environment exist. These studies usually focus on one semiconductor material and analyse the physical mechanisms.

This contribution is based on requirement-oriented comprehensive analyses for cryogenic-cooled power electronics for long-distance aircraft, from system analyses to semiconductor experimental investigations to final cryogenic inverter design with cooling considerations. The design of high-power cryogenic electrical components strongly depends on the cooling system. Therefore, a cryogenic analysis of a power-dense drive inverter for a fuel-cell-driven aircraft without cooling analyses on component and system levels is not feasible. The mission profile from a fuel-cell-driven long-distance aircraft shows the challenges posed by the widely differing LCs. Recently, H_2 direct cooling and helium (He) indirect cooling have been discussed. Due to the different LCs and associated fuel cell mass flows, challenging cooling capabilities are available to the superconducting components. Moreover, the superconducting tape inside the electrical machine requires a current with minor total harmonic distortion (THD), leading to high f_{PWM}. These mentioned top-level requirements are challenging for the inverter design. A possible configuration is discussed out of semiconductor loss experiments considering all semiconductor materials. With the help of a scalable semiconductor model, initial predictions can be made because wide-bandgap (WBG) semiconductors are not yet available in this power range. The cooling of the half-bridge uses the cold H_2 mass flow ($\dot{m}_{\mathrm{H2}}$) as heat sink and is evaluated for both cooling configurations. Besides the comprehensive study of power electronic elements under low temperatures, this paper presents an interdisciplinary and comprehensive feasibility analysis of the power electronics for a cryogenic power train of a long-distance aircraft.

C. PAPER's STRUCTURE

The paper starts with a description of the system level to define component boundaries, followed by an experimental investigation of the semiconductor device level to investigate the material's cryogenic behaviour and ends with the power electronic component design with detailed cooling considerations. Moreover, section II presents the opportunity to reduce hysteresis loss per cycle (Q) of superconducting electrical machines by increasing the inverter f_{PWM}. All these challenges and requirements are taken into account in section III. Section II explains the electrical and cooling system, which influences the design of a cryogenic power electronic drive train inverter. Significantly, the analyses consider two cooling concepts based on a direct and indirect cryogenic cooling approach. Section III contains a comprehensive literature review of semiconductor investigations under cryogenic temperatures, the methodology of experimental investigation, a self-developed cryogenic double pulse testbench, an evaluation of experimental results and a comparison of semiconductor materials' suitability for cryogenic aircraft drive trains. Based on section III, the suitability of semiconductor materials, a cryogenic power inverter design with detailed cooling considerations is discussed in section IV. The optimal T_{J} can increase the inverter efficiency. Therefore, a detailed heat sink design and experimental investigations allow evaluating the influence of different LCs. Finally, section V concludes all gained insights and suggests preferred perspectives.

II. CRYOGENIC DRIVE TRAIN SYSTEM ANALYSES

This section discusses the boundary conditions for the electro-thermal design of a power electronic inverter for a long-distance aircraft driven by a cryogenic drive train. Aircraft design influences the power ranges of electrical components and the available cooling $\dot{m}_{\mathrm{H2}}$ from the fuel cell system. Two cooling system concepts are analysed in detail to prove their suitability for a cryogenic drive inverter. The design of the superconducting electrical machine is challenging and possesses some inverter requirements. In particular, the loss mechanism in superconducting materials requires high f_{PWM}s. A finite element method (FEM)-based evaluation indicates loss reduction opportunities introduced by Q. These analysed system-level requirements affect the choice of power electronic topologies and semiconductor material.

A. AIRCRAFT DESIGN SPECIFICATIONS

Fig. 2 shows the calculated mission profile of Sustainable and Energy-Efficient Aviation (SE^{2}A) long-distance aircraft.

In the future, emission-free long-distance commercial aircraft will have to use the synergies between distributed electric drives and aerodynamic improvements fully utilised to

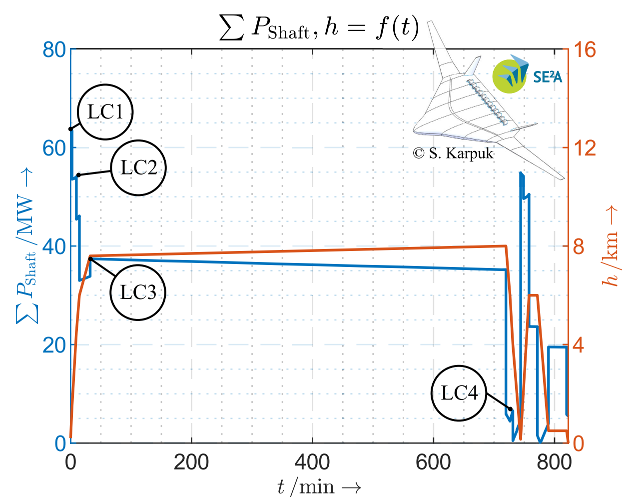

FIGURE 2. Mission profile of a long-distance aircraft based on data from SE^{2}A.

save energy, as proposed in [17]. The study [18] illustrates the multi-fidelity design optimisation of the long-range BWB in the SE^{2}A consortium. Aerodynamics improvements could reach higher fuel efficiencies. Some new air-frame technologies are used, for example, active flow control, active load alleviation, body layer ingestion (BLI), new materials, and structure concepts. Superconducting concepts yield novel weight-saving ideas and could allow the usage of a fuel cell system with an increased power density. Aircraft design offers space for volumetric cryotanks because of LH_2 poor volumetric energy density, as mentioned in the introduction. A mission profile is calculated using the optimisation methodology like [18]. Four LCs with their mechanical shaft power (P_{Shaft}) specifications are sufficient to study the system's feasibility.

B. ELECTRICAL SYSTEM

Tab. 1 summarises the mission profile in four LCs to define specifications for the design of the drive inverter. Twelve superconducting electrical drives powered by a highly efficient fuel cell supplied with H_2 from cryotanks will be used for propulsion.

TABLE 1. LCs based on the mission profile analysis.

Load Case		Total Shaft Power $\sum P_{Shaft}$ MW	Shaft Power per Propulsor's P_{Shaft} MW
LC1	Peak Rating	64.8	5.4
LC2	Climb	54	4.5
LC3	Cruise	37.4	3.12
LC4	Landing	6.24	0.52

The critical LC will be the peak power (LC1) because of its losses. The time of the climb phase is too long to operate the power train in an overload strategy, as used in the automotive industry to increase the power density of electrical components [19]. A further challenging LC is the cruise (LC3) because this has the longest operation time of more than 700 min. Therefore, the electrical power train has to deal with peak power and shows good efficiencies at partial loads, such as cruise. These power requirements could be fulfilled with high currents and HVs.

1) CRYOGENIC MEDIA's BREAKTHROUGH BEHAVIOUR

Cryogenic media's breakthrough behaviour determines the voltage level choice influenced by the insulation coordination. Reliable statements on the breakdown behaviour of cryogenic media require knowledge about the physical state, temperature behaviour, field formation and the kind of electrical field (alternating current (AC), direct current (DC), pulsed, fast-changing).

The Paschen law can describe gaseous media, but the physical phase change can be challenging. The breakdown behaviour of LN_2 is investigated in [20]. The publication [21] presents an investigation of He in liquid and gaseous states. The boiling point and different electrode formations are discussed in detail — the breakdown voltage capability increases at lower temperatures. Gaseous He possesses a worse electrical breakdown than gaseous H_2 [22, Page: 576]. liquid helium (LHe) also has a worse breakdown behaviour than LH_2 [22, Page: 579]. Therefore, the cooling system also impacts the insulation coordination of the electrical system and the power electronic design.

The inverter leg current level is defined by the switched DC voltage (V_{DC}), P_{Shaft} and the electrical machine's phase number (m).

2) MULTI-PHASE SUPERCONDUCTING ELECTRICAL MACHINE

The design of the electrical machine possesses advantages in increasing the fault tolerance and lowering the RMS phase current (I_s) by using a multi-phase electrical machine.

A multi-phase machine can increase fault tolerance with a field-oriented control algorithm [23, Page: 31]. In a case of a single fault (for example, a single semiconductor failure) in one three-phase system of the 3×3 machine (I), the single drive train can still deliver 2/3 of its nominal power. The other eleven drives give their full nominal power and are not affected by the fault in the superconducting machine (I).

Reducing the I_s by increasing the m also reduces the leg current of the inverter. Another essential parameter is the desired inverter f_{PWM}, which strongly impacts the frequency-dependent power losses ($P_{L,S}$) of the inverter and the cooling design. A detailed look at the loss mechanism of the superconducting machine, which the f_{PWM} can influence, is essential.

3) REDUCING SUPERCONDUCTING MACHINE LOSS MECHANISM BY INCREASING THE SWITCHING FREQUENCY

Superconducting electrical machines require a rotating magnetic field. It is essential to understand the loss mechanisms in superconductors to operate them with a required AC current. The most challenging in the design process of superconducting electrical machines is preventing losses because a huge power density is needed. Additionally, high magnetic fields exist, insulation coordination has to avoid arcing, mechanical wire construction faces forces, and cooling design must guarantee low temperatures.

The loss mechanism in superconductors is very complex and depends on several parameters, and analytical approaches are not accurate. The publication [24] discusses the analytical formulae for AC loss calculation and suggests a calorimetric loss evaluation with FEM-based analyses. Moreover, the publication [24, Page: 23-28] presents some strategies to avoid AC losses, for example, filamentation of high-temperature superconductors (HTS), roebel arrangements, flux diverters and windings techniques.

Own FEM-based analysis shows the influence of f_{PWM} on the power losses (P_L) of the superconducting electrical machine. The superconductors of machine stators are investigated. These are fed with AC currents at stator frequency (f_s) of up to 266 Hz. The calculations use a $\delta = 3$ mm wide rare-earth barium copper oxide (ReBCO)-tape with a critical

current (I_c) of 130 A at 77 K. These tapes are stacked inside the air gap. When operating the superconductor at the fundamental frequency and exposing the tape to a perpendicular outer magnetic field (B_{ext}) of 0.3 T, the current distribution in the tape depends on time (t) and f_s. A current density distribution ($J_\perp$) over the width of the superconductive tape (w) and the t is shown in Fig. 3. The $J_\perp$ increases at the edge of the tape, which is a transient occurrence.

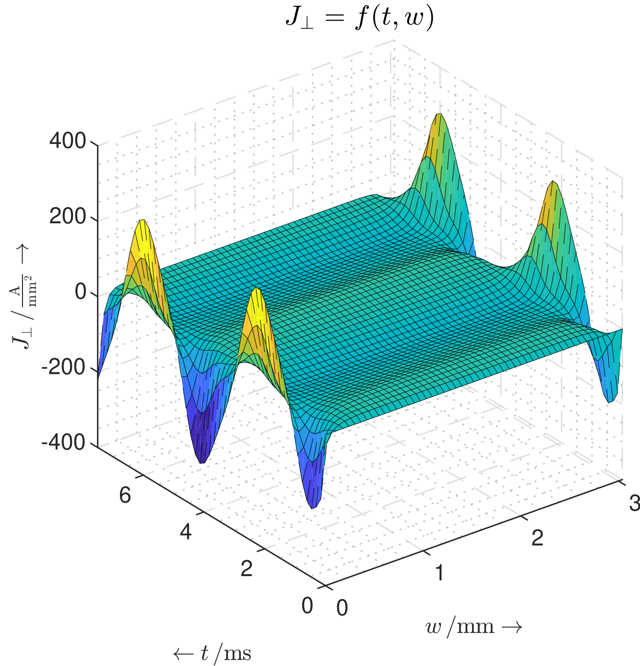

FIGURE 3. $J_\perp$ **transient occurrence at the edge of the tape.**

An ideal loss-minimised situation for the superconductor would be a sinusoidal current. As a real-world superconducting aviation drive will be inverter-supplied, current ripples are superimposed on the transport current. The following diagrams in Fig. 4 show dominant ripple spectrums of a 5.4 MW HTS-drive for inverter f_{PWM} of 10 kHz, resp. 20 kHz. Fig. 4 illustrates the investigated nth RMS harmonic of the phase current ($I_{\nu,s}$) for superconductive material transport and loss evaluation.

The results originate from a circuit simulation with a partial machine (one three-system of nine-phase) without a winding coupling. There is not yet a complete model of the electric machine.

For a given oscillating transport current (I_t), Q (in $J \cdot m^{-1}$) can be determined with a formula for an infinite tape stack, initially formulated by Mawatari [25]:

$$\frac{Q}{Q_c} = i_0^2 \cdot \int_0^1 (1 - 2 \cdot s) \cdot \ln\left[\frac{\cosh^2(\pi \cdot w/L_y)}{\cosh^2(\pi \cdot i_0 \cdot w \cdot s/L_y)} - 1\right] ds \quad (1)$$

With $Q_c = \mu_0 \cdot I_c^2/\pi$ and $i_0 = I_t/I_c$. i_0 is the ratio of the I_t to I_c. L_y is the vertical distance between the tapes, and position (s) is half the w.

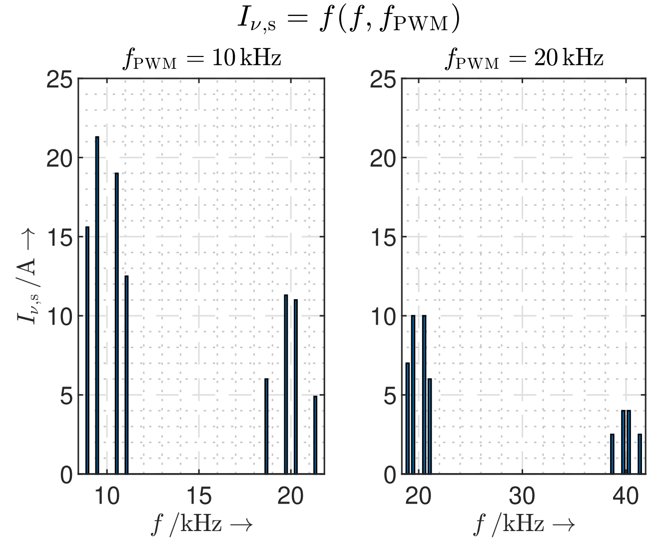

FIGURE 4. Simulation results of current harmonic originate from a circuit simulation with a partial machine without winding coupling (until 2nd order of f_{PWM}).

The Q of an external oscillating magnetic field without a I_t is being considered by a different formula [25]:

$$\frac{Q}{Q_c} = \left(\frac{L_y}{\pi \cdot w}\right)^2 \cdot h_0^2 \int_0^1 (1 - 2 \cdot s) \cdot \ln\left[1 + \frac{\sinh^2(\pi \cdot w/L_y)}{\cosh^2(h_0 \cdot s)}\right] ds \quad (2)$$

With $h_0 = \pi \cdot H_0/(J_c \cdot d)$, d is the thickness of the superconductor, H_0 is the amplitude of the oscillating external magnetic field.

The amplitudes of the spectrum in Fig. 4 generate the following losses (Fig. 5 and 6) using Eqns. 1 and 2.

A comparison of the P_{trans} in Fig. 5 indicates a reduction in loss amplitudes. This reduction of P_{trans} also relates to the

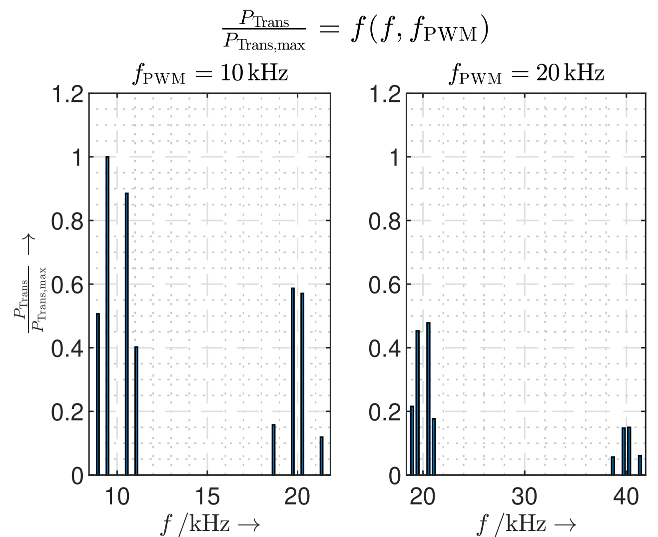

FIGURE 5. Normalised P_{trans} due to current harmonics, f_{PWM} of 10 kHz and 20 kHz.

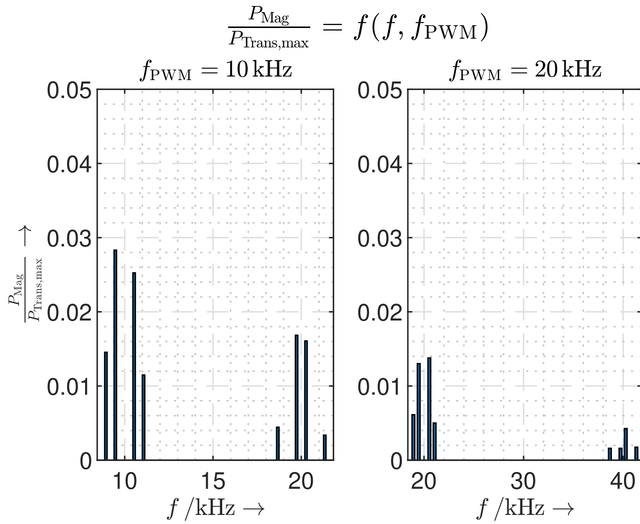

FIGURE 6. Normalised P_{mag} due to current harmonics, f_{PWM} of 10 kHz and 20 kHz.

P_{mag} in Fig. 6. Therefore, the total losses in this example are significantly reduced to 10 % of the 10 kHz values when applying the 20 kHz inverter f_{PWM}. An increase in f_{PWM} significantly reduces the losses of superconducting drives.

Therefore, the superconductor needs a current with low THD. Additionally, superconducting machines tend to have a small inductance; a high f_{PWM} is necessary to avoid undesired current harmonics. The fundamental f_s must be minor, and the f_{PWM} must be high to reduce the THD. The following Eqn. 3 expresses the THD.

$$THD_I = \sqrt{\sum_{h_2}^{h_{max}} \left(\frac{I_{\nu,s}}{I_s}\right)^2} \cdot 100\,\% \qquad (3)$$

A small THD is also reachable with massive filter efforts, but this technical opportunity increases the inverter's mass.

Pursuing only a high-current approach with a DC onboard voltage below 1 kV would lead to high inverter leg currents. The active semiconductor chip area increases with higher inverter currents; this leads to increased parasitic semiconductor output capacities. Those increased output capacities limit the inverter f_{PWM}s. Nevertheless, the cryogenic behaviour could positively affect semiconductor's conductivity and switching behaviour.

It should be noticed that high f_{PWM}s and high power demands lead to challenging inverter cooling requirements.

A further increase in power density can be achieved by optimising the electrical system level.

4) ELECTRICAL SYSTEM LEVEL OPTIMISATION

From the previous discussions of the electrical system level and the load, many possibilities for optimising the electrical system level open up. Many contradictory design parameters of the fuel cell, power electronics, the DC onboard superconducting wiring harness, and the superconducting electrical machine must be considered. Additionally, aircraft specifications, for example, the system fault tolerance or the electromagnetic compatibility, influence the system design further. A holistic multi-parameter system-level optimisation is required to find the best parameter set, as suggested by [12] for a short-range aircraft's cryogenic power train. First system-level optimisations have been made in the SE^{2}A consortium based on a non-cryogenic short-range commuter [26].

In future design steps, an optimum has to be found by multi-parameter system analysis considering all electrical components for SE^{2}A long-distance aircraft. System-level requirements affect the choice of power electronic topologies and semiconductor material. Some essential parameters are discussed and assumed for a non-optimised electrical design starting point. This study uses a DC onboard voltage of 3 kV. A 5.4 MW drive with nine phases, and three independent star points 3 × 3 requires a phase peak current ($\hat{i}_s$) of 870 A by $V_{DC} = 3\,kV$. The f_{PWM} should be higher than 10 kHz.

C. COOLING SYSTEM ANALYSES

The cooling system defines essential inverter design input parameters — two cryogenic cooling concepts are presented. The available cryogenic $\dot{m}_{H2}$ dependent on the power demand of the fuel cell system influences the power electronic's heat sink design and the operating T_J. Four challenging LCs impact the cooling design.

The total power dissipation of the electrical drive components and a part of the fuel cell losses are used to bring the H_2 to the appropriate operating temperature of the fuel cell. Nevertheless, the aircraft design also requires an additional efficient cooling system of the fuel cell because the cooling capability of the $\dot{m}_{H2}$ is not enough. Moreover, increasing the $\dot{m}_{H2}$ to cool the fuel cell system leads to a volumetric tank. The temperature level of the fuel cell system and the efficiency has to increase.

These suggested cooling concepts for the superconducting components should also be considered in the holistic multi-parameter optimisation to identify the most promising weight-saving system topology.

1) DIRECT COOLING SYSTEM

As proposed in [12], the most straightforward cooling system uses the cold gas H_2 flow for the fuel cell supply to remove all the losses in the DC backbone, the superconducting machines, and the power electronics. Fig. 7 shows the direct cooling approach with the smallest number of components but preventing leakages is more challenging.

The direct $\dot{m}_{H2}$ and the state of matter are essential parameters for the power electronic heat sink design.

2) INDIRECT COOLING SYSTEM

A spacious long-distance aircraft requires a comprehensive piping system with many flanges and seals, which implies the risk of inflammable H_2 gas leakage. A direct and short connection between the tank and fuel cell is proposed to minimise the risk of leakage [13]. An indirect cooling system

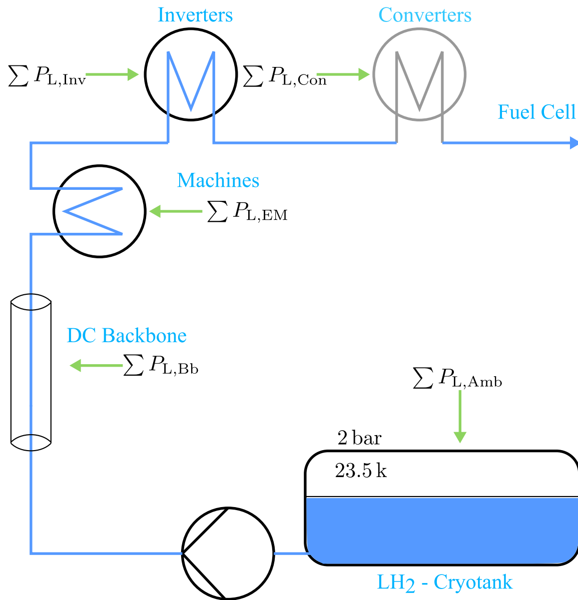

FIGURE 7. Systematical view: direct cooling with LH_2 (the need for converters depends on the possible output voltage of the fuel cell).

offers these needs. As shown in Fig 8, the superconducting components are coupled to the $\dot{m}_{H2}$ by using reverse brayton cycle cryocoolers (RBCC).

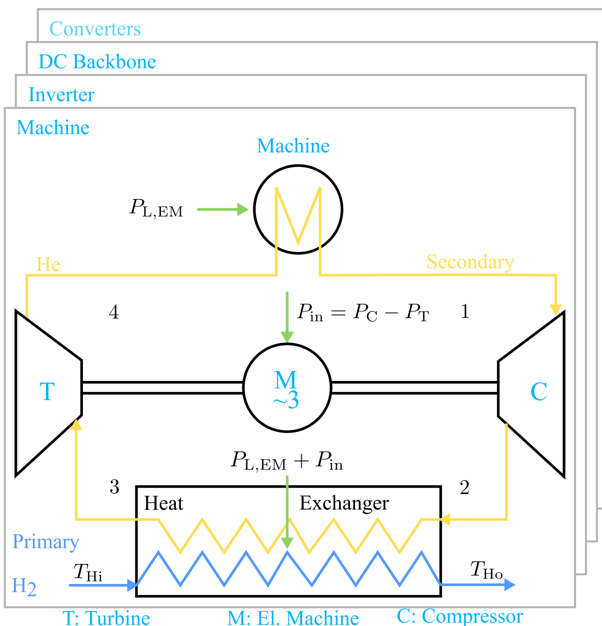

FIGURE 8. Systematical view: indirect cooling with He via RBCC (the need for converters depends on the possible output voltage of the fuel cell).

In this alternative concept, He is used as an inert cooling fluid in the cryocoolers. The RBCC technology, as presented in [13], is the most promising approach in the discussed temperature and power range. All electric drive components are coupled in parallel to the H_2 flow by heat exchangers and serve heat flow for warming up the H_2 for the fuel cell. The disadvantage of using cryocoolers and heat exchangers is an increase in the weight of the drive system, which has to be assessed in a complete system analysis.

The choice of semiconductors and their properties in low-temperature ranges determines whether to use a RBCC or not. For example, semiconductors with advantages in cryogenic temperature ranges probably require a RBCC.

3) CRYOGENIC MASS FLOW ESTIMATION

Evaluation the $\dot{m}_{H2}$ inserts essential cryogenic heat sink design parameters and clarifies the technical feasibility of using the cryogenic drive concept. The H_2 power input and the $\dot{m}_{H2}$ are calculated with assumed efficiencies, which also cover the partial load conditions of the electrical machine, inverter and wiring harness:

- Electricity generation by a fuel cell with approximately 55 % efficiency (range 50 % to 60 %, as mentioned in the introduction I)
- Superconducting backbone efficiency of above 99 %
- Superconducting motor efficiency of above 99 %
- Targeted inverter efficiency of above 99 %
- Estimated auxiliary consumption of around 0.5 MW (for example, air conditioning [1])

The total $\dot{m}_{H2}$ can be calculated using the Eqn. 4 with the gravimetric energy density (LHV) of H_2 of $120\,\mathrm{MJ \cdot kg^{-1}}$ [7, Page: 1] and considering the $\eta_{LH2-Shaft}$ to calculate the H_2 power demand P_{LH2}.

$$\dot{m}_{max} = \frac{P_{LH2,max}}{LHV_{LH2}} \tag{4}$$

Additionally, the $\dot{m}_{H2}$ of each propulsor is spread in parallel to the nine half-bridges of the inverter. Tab. 2 represents the required $\dot{m}_{H2}$.

These considerable low values in Tab. 2 are due to H_2's high gravimetric energy density. The cruising and landing phase needs particular attention because of the long cruising time and the low $\dot{m}_{H2}$ during landing. Moreover, the $\dot{m}_{H2}$ is only available if the plane is operating in flight mode. At the airport, a small separate supply of cooling gas is necessary to maintain the superconducting state of all cryogenic devices.

TABLE 2. Estimated required $\dot{m}_{H2}$.

Load Case	Total power (incl. Subs.) MW	$\dot{m}_{H2}$ Total $\mathrm{g \cdot s^{-1}}$	per engine $\mathrm{g \cdot s^{-1}}$	per half-bridge $\mathrm{g \cdot s^{-1}}$
LC1	122	1,016	84.7	9.41
LC2	102	847	70.6	7.84
LC3	70.7	588	49	5.4
LC4	12.2	102	8.5	0.94

The flight profile in Fig. 2 gives an energy consumption of the fuel cell of 3.24 TJ. This estimation yields a m_{LH2} of 27 t of LH_2 with the gravimetric energy density of H_2. This m_{LH2} could be stored in one or several tanks with advanced super insulation as already used in industry and some automotive projects [19], [27] or as proposed in [28].

These tanks have a low weight but allow a typical maximum pressure of 4 to 5 bar before the boil-off valve opens. Moreover, the operating pressure is estimated to be two to three bars in flight. Valves and accessories technology are industry standards and can easily be upgraded for aircraft technology requirements. The gross volume of the LH_2 to be stored is approximately 380 m^3 (cubic tank; out line of 7.2 m).

The system analysis clarifies the challenges for the design of power electronics. A suitable semiconductor material will be selected based on comprehensive literature research and experimental investigation to fulfil the challenging system requirements. In particular, a loss-reducing operating T_J recommendation can be drawn out from the experimental studies. The identified $\dot{m}_{H2}$ defines essential input data for the inverter heat sink design.

III. CRYOGENIC SEMICONDUCTOR BEHAVIOUR

Section discusses the state of the art, fundamentals of semiconductors under deep temperature, investigation methodology, cryogenic testbed design, the experimental procedure, and comparison of semiconductor's behaviour.

Power electronics can be a bottleneck of an electrified aircraft's comprehensive superconducting drive train design because of the switching semiconductor devices. The knowledge of the behaviour of semiconductors under cryogenic temperatures shows the feasibility of each material. This paper will discuss requirement-oriented designs with the understanding of several semiconductor devices. The superconducting drive train system needs high f_{PWM} above 10 kHz, HV of 3 kV and high power ratings of 5.4 MW per drive, as mentioned in the previous section II. Therefore, it needs to be assessed which semiconductor device has advantages and disadvantages under cryogenic temperatures, and which semiconductor requirements must be taken into account to achieve an overall high performing concept.

A. STATE OF THE ART OF CRYOGENIC SEMICONDUCTOR RESEARCH AND FUNDAMENTALS

This subsection illustrates the state of the art in capturing the power semiconductor behaviour under cryogenic temperatures, but there are also some interesting overall discussions on cryogenic power electronics. Two papers give a general overview of the topic [29], [30]. A further publication [31] describes the design of a cryogenic power electronic fed DC motor and the paper [32] illustrates a loss evaluation of a cryogenic DC/DC-converter. Also, strategies to improve the performance of cryogenic power electronics are given in article [33]. Publication [34] describes the semiconductor physics for Si-based devices (switches and diodes) under cryogenic conditions mathematically, presents an excellent overview and illustrates some optimisations in the design of semiconductor devices for cryogenic applications.

1) LITERATURE REVIEW ON DEVICE LEVEL

Tab. 3 below is separated into different materials, technologies, voltage ratings and publications. Unfortunately, the T_J (also the test temperature) could not be included in the table because the temperature ranges varied greatly in the individual experiments.

TABLE 3. State of the Art: Cryogenic semiconductor investigations.

Material	Structure	Voltage	Publication
Si	Diode	various	[31][34][36]
SiC	Diode	various	[31][34][36]
Si	MOSFET	$\leq$650 V	[37][36][38][39][40]
Si	IGBT	$\leq$650 V	[34][41][42][43]
Si	IGBT	$\geq$1200 V	[34][43][44][45]
SiC	MOSFET	1200 V	[44][46][47][48][49]
GaN	HEMT & Cascode	$\leq$650 V	[50][49][51][52][53][54] [55][56][57]

There are a lot of semiconductor materials, such as Si, SiC and GaN. Especially, WBGs offer the potential to reach high-required power densities under normal conditions. Also, semiconductor architectures and structures provide different advantages and disadvantages. For example, insulated gate bipolar transistors (IGBTs) have advantages in short current capabilities compared to SiC Metal-oxide-semiconductor field-effect transistors (MOSFETs) under normal conditions [35]. As superjunction and trench gate, these arrangements decrease the on-resistance (R_{on}) at high blocking voltage capabilities.

Moreover, the development of GaN led to the use of structures, like high-electron-mobility transistors (HEMTs) and Cascodes, due to their self-conducting properties.

The packaging addresses different power and frequency ranges, such as discrete devices, modules, and press-pack. Therefore, the state of the art study has to summarise several investigations of different devices. The literature review keywords are cryogenic, Si, SiC, GaN, IGBT, MOSFET, superjuntion, trenchgate, HEMT, Cascode, physical behaviour in cryogenic temperatures, static and dynamic behaviour or characteristics, blocking voltages ($\leq$650 V, 1200 V,1700 V,4500 V) and cryogenic power electronics.

The device under test (DUT) in the publications mentioned are directly cooled using a cryogenic chamber, and this publication makes an overall comparison and discusses different design ideas to achieve the best practice.

2) KEY PROPERTIES OF SEMICONDUCTORS

The behaviour of semiconductors is dependent on several key properties, such as the band-gap (between the conduction band and valence band), intrinsic carrier concentration (the density of electron/holes in pure silicon), carrier mobility (the drift velocity of carriers is proportional to the electrical field), carrier lifetime and impact ionisation [34, Pages: 11-24]. These temperature-dependent parameters influence semiconductor behaviour under cryogenic conditions. The most characteristic effect is the so-called carrier freeze-out, occurring at temperatures below 77 K in Si-based semiconductors. Nevertheless, carrier freeze-out is a complex mechanism and can be explained due to donor and acceptor energies.

With a temperature ($T_J \leq 77$ K), donor and acceptor energies become removed from the respective band edges. This carrier freeze-out effect is also dependent on doping levels [58, Page: 1067]. The article [59] proved in 1986, for the first time, carrier freeze-out by donor level measurements. Also, the publication [34, Page: 15] states that carrier freeze-out is only observable under a temperature of 77 K for high ($> 8 \cdot 10^{18}$cm^{-3}) and very low ($< 3 \cdot 10^{16}$cm^{-3}) doping levels in Si-based semiconductors.

3) CRYOGENIC BEHAVIOUR OF DIODES

Si-based diodes (ultrafast and superfast) offer a better electrical behaviour in cryogenic conditions than SiC-based Schottky diodes. The R_F, reverse recovery charge (Q_{rr}) and the breakdown voltage (V_{Break}) decrease. Only in the property of V_{Break} the SiC-diode shows better behaviour. Even the Q_{rr} is significantly reduced in Si-based diodes as the temperature drops [31, Pages: 5-6] [36, Page: 3].

In Si-P-i-N diodes, the intrinsic carrier concentration reduces to lower temperatures; therefore, the zero forward voltage drop (V_{F0}) increases and the R_F decreases at cryogenic temperatures [34, Page: 38]. Also, Si-diodes offer a lowering Q_{rr} due to the intrinsic carrier concentration. The mathematical model in the publication [34, Pages: 46-48] proves the ratio of intrinsic carrier concentrations in highly versus lightly doped areas leads to a decrease of the charge in the middle region. The blocking capability falls in combination with lower temperatures mentioned effective impact ionisation.

The best property of Si Schottky diodes is the increasing blocking ability to lower temperatures [34, Page: 36]. The R_F shows excellent characteristics because of the increased electron mobility (25 times increase from 300 K to 77 K). Otherwise, the V_{F0} increases due to two competing temperature mechanisms. There is a decrease in the thermal voltage and a reduction in the saturation current density [34, Page: 27].

4) CRYOGENIC BEHAVIOUR OF Si-BASED MOSFETs

The literature review illustrates that Si-MOSFETs switches offer reduced $R_{DS,on}$ due to the increased carrier mobility (electron mobility and hole mobility) over decreasing cryogenic temperature (to 77 K$\leq T_J$) [34]. Additionally, cryogenic temperatures decrease blocking voltage, slightly increase threshold voltage (V_{Th}), and reduce minor turn-on energy loss per pulse (E_{on}) and turn-off energy loss per pulse (E_{off}).

At lower temperatures than 100 K, $R_{DS,on}$ increases due to the carrier freeze-out [34, Page: 67]. Moreover, the fall of the blocking capability is due to a higher average carrier speed, which leads to more effective impact ionisation [34, Page: 24]. The decreased intrinsic carrier concentration under cryogenic temperatures leads to a slightly increased V_{Th} [34, Page: 71].

Another interesting fact is the behaviour of different device structures under cryogenic temperatures. Publication [39] compares different device structures with each other. A HEXFET®, MDmesh™and a CoolMOS™MOSFET are compared. The doping level affects the behaviour remarkably, as also mentioned above. Additionally, publication [39, Page: 2012] states that every semiconductor has its characteristics under cryogenic behaviour. However, the trends in $R_{DS,on}$, V_{Break}, V_{Th} and switching are nearly similar to other Si-based MOSFETs.

5) CRYOGENIC BEHAVIOUR OF Si-IGBTs

The IGBT combines the advantages of easy control and the enormous current carrier capability due to its internal device structure. Therefore, the properties of Si-MOSFETs and a bipolar transistor are merged in one device. Under low-temperature conditions, the V_{Th} behaviour is similar to Si-MOSFETs. The effect is explainable due to the reduced intrinsic carrier concentration [34, Page: 89] [41, Page: 1901].

Otherwise, the collector-to-emitter resistance (R_{CE}) properties, zero collector-to-emitter voltage (V_{CE0}), V_{Break} characteristics and switching behaviour are related to bipolar transistors. Cryogenic temperatures lead to reduced R_{CE} and increased V_{CE0} due to reduced intrinsic carrier concentration. The device is also affected by carrier freeze-out at temperatures under 77 K. Moreover, the blocking voltage decreases due to impact ionisation. An advantage are the reduced E_{on} and E_{off} [34, Page: 92]. In particular, E_{off} becomes minimal under cryogenic conditions. It can be described by the fact that the recombination current is proportional to the inherent bipolar transistor current gain β. The current gain β decreases by decreasing operating temperature due to the reduction in the lifetime of the minority carrier [34, Pages: 86-87]. A paper [45, Pages: 3-9] emphasises the opportunities of press-packs under cryogenic conditions and includes studies of switching characteristics for megawatt-scale Si-IGBTs.

6) CRYOGENIC BEHAVIOUR OF SiC-MOSFETs

SiC-devices have a highly increased $R_{DS,on}$ due to carrier freeze-out [46, Page: 779] already from 230 K, slightly reduced V_{Break}, an increased V_{Th} and nearly constant switching energy losses. The fallen V_{Break} is also related to the impact ionisation which is degraded [49, Page: 4]. Moreover, publication [47, Pages: 207-208] illustrates the influence of large densities of interface states at the SiO_2/SiC interface on the V_{Th}. Also, the publication [47, Pages: 209] represents another reason for the increased $R_{DS,on}$ under cryogenic conditions (consisting of residual resistance and channel resistance); the dominant mechanism in the channel resistance is the increase in the density of trapped electrons due to lower temperatures in the channel. The residual resistance is prevalent from 300 K to higher temperatures. Otherwise, the channel resistance is dominant in lower temperatures smaller than 300 K.

Another interesting fact is device's structures, e.q.: planar or trench, offer small different characteristics [48, Pages: 712-713].

7) CRYOGENIC BEHAVIOUR OF GaN-HEMT OR GaN CASCODE

The literature review illustrates some exciting investigations of GaN-semiconductors. GaN-HEMTs are complex transistors, which have lateral structures compared to conventional power semiconductors. Compared to Si- and SiC-field-effect transistors, the $R_{\mathrm{DS,on}}$ and breakthrough behaviour under cryogenic conditions is more complicated due to more dependent parameters.

GaN semiconductors have a different structure and physical function than conventional semiconductors. Thus, a few explanations about physical mode of operation are helpful for understanding cryogenic behaviour. The highly doped and non-doped layer interface leads to a two-dimensional electron gas (2DEG). Inside the 2DEG, electron mobility is very high. The layers can be composed of different material combinations; often used materials are n-high doped aluminium gallium arsenide (AlGaAs) and non-doped gallium arsenide (GaAs). Moreover, the interface design between high and non-doped layers, gate structure, and electrical interfaces are challenging. Also, a SiC-substrate can improve thermal conductivity. There are two kinds of HEMTs, a normally-off enhancement-mode HEMT (E-HEMT) and a normally-on depletion-mode HEMT (D-HEMT) [60].

The E-HEMT offers the desired control characteristics for most applications. Therefore, a Cascode device structure combines the D-HEMT with a Si-low-voltage MOSFET. There are a lot of advantages and disadvantages comparing the E-HEMT and Cascode [60].

E-HEMTs have a gate modulation layer (p-Schottky or p-ohmic) to ensure the normally-off mode, and there is not a typical bipolar junction body diode. But by self-biasing due to the drain-source voltage (v_{DS}), reverse conduction is possible. Otherwise, the gate driver can also drive the semiconductor in reverse conduction mode due to the gate signal. Therefore, the HEMTs conduct in both ways without Q_{rr}. Due to the lateral design, the gate-drain and drain-source capacity are smaller than vertical power MOSFETs, leading to more favourable switching behaviour [60] [61, Page: 3].

Thus, the breakthrough mechanism is complex due to the lateral structure. There are the source-drain mechanism (punch-through of electrons injected from source), gate-drain breakdown (high gate-leakage current), vertical breakthrough (poor compensation of the buffer layer) and the impact ionisation (generated holes lead to a decrease of the barrier) [62, Page: 6].

E-HEMTs offer reduced static $R_{\mathrm{DS,on}}$, constant V_{Th} and reduced switching energy losses under cryogenic conditions [50], [51] [53], [54] [56]. Carrier freeze-out as a limitation could not be observed in the publication [54, Page: 7413]. But there are some issues on dynamic drain-to-source resistance ($R_{\mathrm{DS,on,dyn}}$) due to the current collapse effect [52]. The publication [52, Page: 3292] marks a temperature dependency of the current collapse. The study analyses the dynamic characteristics of carbon-doped GaN-D-HEMTs. Current collapse effects are related to the carbon-doping level [52, Page: 3290].

The V_{Break} evaluation is not as clear as in Si- and SiC-devices because of different GaN-manufacturer semiconductor concepts and structures. NASA's publication [56, Page: 11] illustrates the breakdown evaluation of several GaN-devices due to the help of drain-to-source leakage current (I_{dss}) under cryogenic conditions. Some DUTs show a decrease in the I_{dss}; therefore, an increasing V_{Break}. Another DUT points out a slight increase in the leakage current.

Further publications [53, Page: 5291] and [55, Page: 893] on E-HEMTs strengthen the view that the V_{Break} remains constant or improve at a cryogenic levels.

Cascode device structures with a Si-low-voltage MOSFET and high-voltage blocking normal-on D-HEMT enable normal-off device properties. The reverse conduction of a GaN-Cascode is decisively influenced by the typical bipolar junction body diode of the low voltage Si-MOSFET. There is a small Q_{rr}, but it is smaller than HV blocking Si-devices. Minimising parasitic inside the package is very challenging. Parasitics have a major influence on the switching behaviour of semiconductors [63].

The $R_{\mathrm{DS,on}}$ and the V_{Break} decrease at lower temperatures. Moreover, the V_{Th} is slightly increased like the Si-based devices. A reduction in switching energy losses is also observed due to the Q_{rr} [54], [57].

B. INVESTIGATION METHODOLOGY

This subsection describes the requirement perspective of the experimental investigations. There are many exciting questions about the behaviour of semiconductors in cryogenic power electronics, but focus is laid on material and type-independent investigations. HV-blocking semiconductor devices are challenging to handle, and not all devices are commercially available at a comparable voltage and current level. Some compromises have to be made.

1) INVESTIGATED SEMICONDUCTOR MATERIALS

Upcoming WBG semiconductors show advantageous behaviour for high-required power-dense aerospace applications is attractive [1, Page: 84200 - 84206]. The previous section III-A also mentioned that WBG semiconductors have some disadvantages at cryogenic temperatures, especially SiC-devices. Otherwise, using Si-based semiconductors (IGBT and MOSFET) can lead to some advantages at low temperatures and solvable disadvantages.

An overall comparison between Si-IGBT or -MOSFET, SiC-MOSFET, and GaN is conducted to find the best configuration can be found, and give design advice. All chosen semiconductors have diodes — either a pn body diode or an added Si-diode. Commercially available semiconductors are investigated because of their availability and technology readiness level. The semiconductor market is fast-changing, and a technology forecast for the following decades is complicated.

2) INVESTIGATED SEMICONDUCTOR's POWER RATINGS

This publication focuses on the potentials of semiconductors in cryogenic temperature ranges in aircraft applications. For all investigated DUTs, V_{Break} is around 600 V to 650 V for safety reasons, increasing efforts by increasing voltage levels, and their market availability. The chosen nominal device current (at $T_{\mathrm{J}} = 298.15\,\mathrm{k}$) ($I_{\mathrm{Device}}$) is around 40 A (only the evaluated IGBT has a other current value: 40 A at 377.15 K). The first step is to gather experience that will be used in upcoming higher voltage studies. Capturing firsthand experiences in cryogenic power electronics enables rough estimations for higher power ratings. The testbed design should also handle HV levels for future investigations. Moreover, the current is scaleable by parallelising the power electronic devices.

3) EXPERIMENTAL TEMPERATURES

Temperatures above 77 K are useful because under this temperature some disadvantageous behaviour of semiconductors exist, as mentioned in the subsection III-A. Furthermore, the system cooling design defines the cryogenic media's temperature, as analysed in II-C.

Otherwise, the self-heating of semiconductors and the non carrier freeze-out of GaN-devices require lower temperatures than 77 K. Some other cryogenic media can offer deeper temperatures.

LH_2 (temperature at normal boiling point (T_{NBP})=20.3 K, [64, Page: 5]) is challenging in regards of safety regulations [64], and LHe (T_{NBP}=4.2 K, [64, Page: 5]) requires closed-loop cooling systems and a reprocessing system because of its costs [65, Page: 10]. LN_2 is practicable in comparison to H_2 and He. The attractive temperature range (T_{NBP}=77.3 K, [64, Page: 5]) can be achieved by using LN_2. Additionally, LN_2 is a cost-efficient experimental coolant. In ongoing research activities, a closed-loop He cooler must be part of the infrastructure. Another opportunity is using LH_2 to use the proposed aircraft system medium, but high infrastructure efforts are likely to result [64].

4) INVESTIGATED PACKAGES

Tab. 4 below presents all DUTs with their internal structure, material, rated voltage, and rated current levels. Global MFs are focused on several device materials and technologies; therefore, all technologies can not be presented by one.

Moreover, the assembly and connection technology and the insulation coordination inside power electronic devices have to be taken into account. Silicone gel guarantees insulation coordination in typical power electronic modules. There are some disadvantages of using silicone regarding its robustness against very deep temperatures [66, Page: 113]. Therefore, the preferred TO-247-3 package ensures thermal decoupling and fulfils all listed conditions/requirements above.

However, GaN and Si-Superjunction require other package technologies to guarantee the best performances. In upcoming investigations, GaN-HEMTs or other package technologies and blocking voltages can occur. This publication focuses on overall comparison earning experiences to advise for all given semiconductors a possible topology and environmental options (cryogenic and non-cryogenic considerations).

Other package technologies, for example disks, can be involved in further research activities.

TABLE 4. List of DUTs and their parameters at T_{J}= 298.13 K in a transistor outline (TO)247-3 package from different manufacturers (MFs).

Device	Technology	V_{Break} V	I_{Device} A	MF
Si-MOSFET	Superjunction	650	47	A
SiC-MOSFET	Trench Gate	650	39	A
Si-IGBT	Trench Gate	600	96	B
GaN	Cascode	650	35	C

5) SEMICONDUCTOR PARAMETER OF INTEREST

Knowledge about the semiconductor's R_{on} (R_{CE} or $R_{\mathrm{DS,on}}$) and switching energy losses (E_{on} and E_{off}) in cryogenic temperature is fundamental to determining topology-dependent power losses per inverter ($P_{\mathrm{L,Inv}}$). With the help of these parameters (R_{on}, E_{on}, E_{off}) and the heat sink design thermal transfer characteristics, statements can be drawn about self-heating and a possible f_{PWM}. Further essential parameters are the blocking capability and the V_{Th}. As previously mentioned in subsections III-A, some materials show advantages and disadvantages in cryogenic temperatures.

a: ON-RESISTANCE

The knowledge about behaviour at low temperatures is essential for designing high-current conductive power electronics because the conductive-dependent power losses ($P_{\mathrm{L,C}}$) are directly related to R_{on} and the quadratic relation of the current. Additionally, the losses can differ depending on the chosen topology, the modulation level (M) and the power factor ($\cos\varphi$). Furthermore, the V_{CE0} of Si-IGBT devices influences the conducting losses, too.

The focus is a comparison between the different semiconductor materials and types. Upcoming research activities should outline a comparison between different chip sizes and nominal voltages of a selected type to prove the feasibility of different cryogenic approaches.

Furthermore, $R_{\mathrm{DS,on,dyn}}$ is an essential parameter of SiC- and GaN-semiconductors. In upcoming research activities, the $R_{\mathrm{DS,on,dyn}}$ should be investigated in different GaN-systems under cryogenic temperature ranges.

b: BLOCKING CAPABILITY

Knowledge about the behaviour of the blocking voltage is a critical factor that influences the applicable topology under cosmic radiation. A reliable and fault-tolerant design of power electronic devices in cryogenic aerospace applications is required. Cosmic radiation is one essential design criterion. To prevent avalanche generation of particles from primary cosmic rays [67]:

- In-/decrease Chip Temperature (device-dependent) [67]
- Decrease Chip Sizes
- Reduce Off-Time
- Decrease the ratio of DC voltage to device V_{Break}

For the IGBT module produced by ABB, the empirical Eqn. 5 states that a decrease in temperature (277.15 K until 402.15 K) leads to deterioration in breaking through due to cosmic radiations [68, Page: 3]. C_1 to C_3 are characteristic values; for example, C_3 expresses the device characteristic failure in time (λ) rate to nominal conditions. C_1 and C_2 describe the blocking voltage dependency on the λ Rate.

$$\lambda(V_{DC}, T_J, h) = C_3 \cdot e^{\left(\frac{C_2}{C_1 - V_{DC}}\right)} \cdot e^{\left(\frac{302.15 - T_J}{47.6}\right)} \cdot e^{\left(\frac{1-\left(1-\frac{h}{44300}\right)^{5.26}}{0.143}\right)} \quad (5)$$

The publication [67] also illustrates that each device has its cosmic radiation robustness temperature dependency. Another publication shows the temperature behaviour of the λ due to cosmic radiation of controlled axial lifetime (CAL) diodes down to 237.15 K [69, Page: 2034]. For WBG devices, the temperature dependency is currently unknown and has not been part of any published research to date. The publication [39] advises long-term test locations, and in the PhD-Thesis [70], a comparison between Si and SiC devices is made. Decreasing T_J lowers the dielectric strength and the latching sensitivity, but the publication [67] also states that influence of temperature is not well understood yet. Upcoming investigations have to clarify if cryogenic temperatures improve or deteriorate the robustness against cosmic radiation.

However, the designable device voltage level decides which topology is suitable for which kind of semiconductor device. Moreover, the V_{Break} is an important data value for executing experimental investigations under cryogenic temperatures.

c: THRESHOLD VOLTAGE

The V_{Th} is another crucial parameter to control switchable semiconductors. A fault-tolerant design requires understanding threshold temperature drifting mechanisms to adjust the gate driver output voltage to the required level.

V_{Th} measurements are necessary preliminary studies for dynamic experimental investigation. These investigations also help explain the loss mechanism shifting due to varying V_{Th}.

d: SWITCHING LOSSES

A superconductive electrical machine requires small current ripples, as mentioned above II-B3. This system requirement leads to high f_{PWM} of the drive inverter. The $P_{L,S}$ to be dissipated via the heat sink design correlates directly with the f_{PWM}. Indicators for this material and type-independent study are:

- E_{on}
- E_{off}
- rise time (t_{rise})
- fall time (t_{fall})

A testbed must capture E_{on} and E_{off} under cryogenic temperature. The power electronic community has discussed the correct measurement strategy [71]. Significantly, the evaluation of WBG semiconductors involves high-frequency-high-voltage and high-frequency-high-current measurement probes. Another strategy is the usage of a calorimeter [72] or characterising the $P_{L,S}$ due to the evaluating behaviour of parasitic elements [54].

A cryogenic environment requires an electrical measurement of E_{on} and E_{off} under some measurement errors. The so-called double puls test enables verification of the dynamic behaviour.

Therefore, a cryogenic double pulse testbed has to be designed. The testbed should enable temperatures from nearly 77.3 K to room temperature.

The following section III-C describes the design of the developed cryogenic double pulse testbed and experimental procure.

C. EXPERIMENTAL SETUP

This subsection outlines the testbed capabilities for the experimental investigations and procedure.

Several requirements result from the investigation methodology in section III-B, which the testbed design fulfils. The thermal testing principle based on the thermal capacity of the cooler needs a particular procedure.

1) CRYOGENIC DOUBLE PULSE TESTBED

Fig. 9 shows the construction of the developed cryogenic double pulse testbed. The test methodology results in specific testbed requirements.

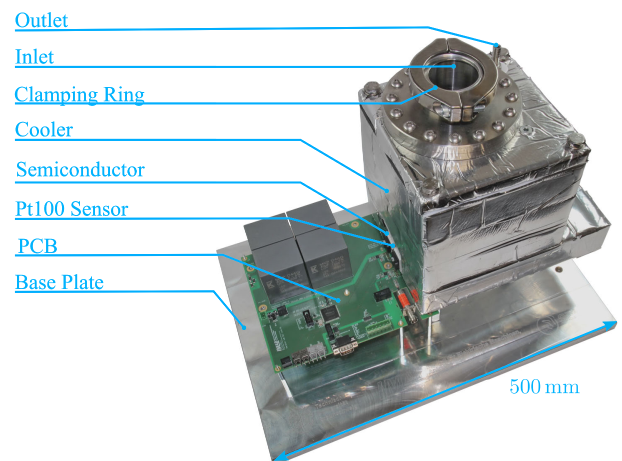

FIGURE 9. Cryogenic double pulse testbed.

The self-developed testbed conducts different semiconductor devices from various manufacturers. Discrete devices assembled in TO-247-3 housings are the focus of the investigation. All mechanical components are placed in such a way

that easy access of measurement probes and electrical contacts are ensured. The measurement probes are not affected by cryogenic temperatures because only the DUTs have a thermal interface to the cryogenic cooler. The temperature drift of the voltage and current measurement is minimised by this design. 3.8 litre of LN_2 can take place inside the L-shape cooler design. This shape possesses two thermal paths (short: 1330 s and long 1625 s) to avoid shocking the semiconductor's assembly and joining technology. The semiconductor thermal interface reaches nearly the LN_2's T_{NBP} of 77.3 K measured by the thermal sensor.

The electronic consists:

- DC link capacitors (1.5 kV)
- Snubber-circuit options
- Two isolated-powered drivers
- Temperature measuring
- Differential-voltage probes
- A current shunt
- field-programmable gate array (FPGA)
- Communication interfaces.

The FPGA especially enables flexibility in controlling the pulse length. A non-saturable spider-web coil with a small load inductance and less parasitic capacities requires small accurate pulse lengths.

2) EXPERIMENTAL PROCEDURE

Fig. 10 illustrates the complete test setup with a 600-litre climate chamber, N container and measurement equipment. On the left side, the N container is displayed. The LN_2 is led through a hose to the heat sink inside the climatic chamber. Due to the use of the climate chamber, adjusting the environmental conditions is practicable. The climate chamber disposes of humidity control, an air dryer and chamber pressure regulation. Both functionalities prevent a strong dewing because of extreme temperature difference (ΔT)s (room temperature to cooler).

FIGURE 10. Cryogenic testbed.

In the first step, the climate chamber controls the humidity and the temperature 282.15 K for approximately 180 s on a constant level to keep the dewing under an acceptable level. The LN_2 gets into the coolant and the DUT interface decreases to 77 K. The coolant has to be filled up five until six times. During the first refilling process, much gaseous N is produced due to the evaporation process of the N caused by the significant ΔT. The gaseous N is led out of the climatic chamber via the designed outlet. After the cooling down process, all measurements are executable during the warming-up progress. Depending on the measurement, different types of equipment are used to measure the R_{on}, V_{Break}, V_{Break}, E_{on} and E_{off}.

The following subsection analyses the results of the experimental investigations.

D. COMPARISON OF THE CAPTURED SEMICONDUCTOR PARAMETERS

This subsection discusses measurement data and compares the collected data parameters with literature values from the comprehensive literature review in section III-A.

A material-independent analysis of different semiconductor materials is possible by the relative tendencies to 273.15 K (0 °C). Moreover, the propagation of uncertainties considers all estimated and specified errors. With the aid of a cubic regression, the data are fitted.

1) COMPARISON OF THE CAPTURED ON-RESISTANCE AND ZERO COLLECTOR-TO-EMITTER VOLTAGE

As mentioned in the subsection III-B, the R_{on} is a crucial parameter and is mainly responsible for the $P_{L,C}$.

Fig. 11 compares the chosen devices against each other, highlighting the relative saving opportunities and giving information about the uncertainties.

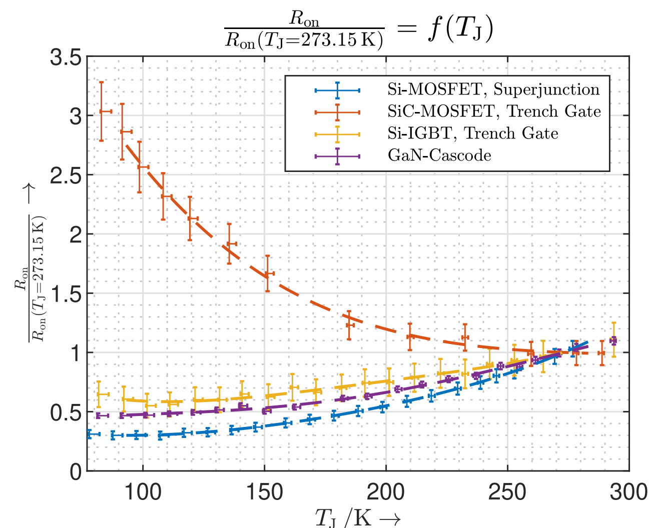

FIGURE 11. Normalised R_{on} ($R_{DS,on}$ or R_{CE}) over temperature.

The Si-superjunction MOSFET emphasises significant relative $R_{DS,on}$ improvements of approximately 70 % from room temperature to cryogenic conditions. The mentioned carrier

freeze-out can be recognized. Comparable results can be found in the publication [39].

The literature review also showed that the $R_{DS,on}$ of SiC-MOSFETs increases significantly by the power of three because of the early-onset carrier freeze-out, as mentioned in the subsection fundamentals III-A. The investigation in the publication [46] illustrates roughly the same relative factor on a 1200 V Si-MOSFET.

The cryogenic condition also leads to a decrease of the R_{CE} in the investigated trench-gate IGBT. Moreover, the V_{CE0} increases due to the reduced carrier concentration, shown in Fig. 12. Carrier freeze-out can be recognized under 100 K.

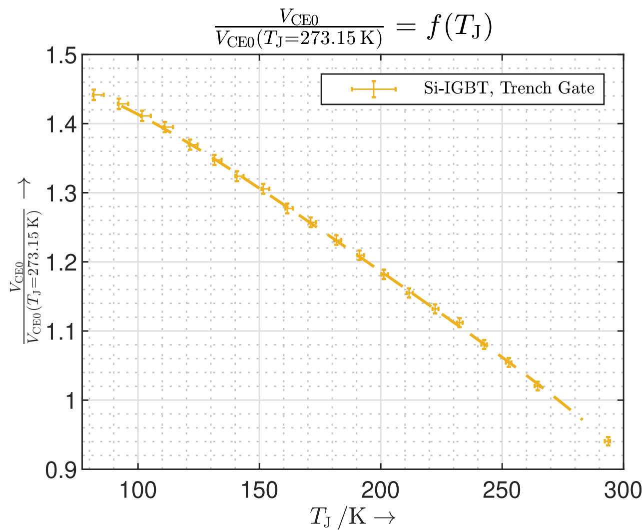

FIGURE 12. Normalised V_{CE0} over temperature.

GaN-Cascodes also have substantial improvements of about 60 % under cryogenic conditions. Publication [54] illustrates comparable results. Furthermore, no slight increase in lower temperature than 100 K is noticeable, and no carrier freeze-out occurs. Nevertheless, an absolute value of the R_{on} is also crucial, not only relative improvements. Tab. 5 shows the captured absolute R_{on} at 273.15 K.

TABLE 5. List of DUTs and their captured and nominal R_{on} [gate-source voltage (v_{GS}) and gate-emitter voltage (v_{GE}) do not comply with the specified values].

Device	Technology	MF	captured R_{on} at 273.15 K mΩ	specified R_{on} at 298.15 K mΩ
Si-MOSFET	Superjunction	A	55	80
SiC-MOSFET	Trench Gate	A	64	60
Si-IGBT	Trench Gate	B	15	15
GaN	Cascode	C	35	50

2) COMPARISON OF THE CAPTURED BREAKTHROUGH VOLTAGE

Subsections III-A and III-B explain the importance of the breakdown evaluation for a power electronic design under cryogenic conditions. Fig. 13 illustrates the relative change to 273.15 K.

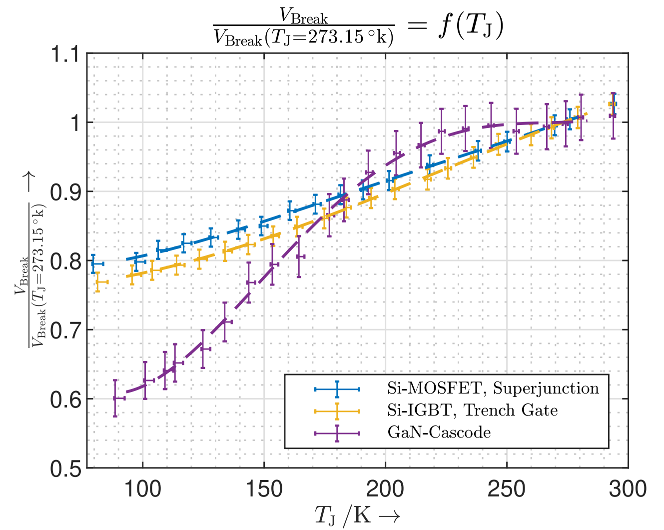

FIGURE 13. Normalised V_{Break} over temperature [For SiC: only a few data points could be collected, the avalanche behaviour is challenging; 5 - 10 % reduction of V_{Break}].

Si-Superjunction MOSFETs offer a lowered blocking voltage capability by around 20 % to 273.15 K. As mentioned in subsection III-A, this effect is related to higher carrier speed, leading to more effective impact ionisation. Publication [38] delivers comparable results.

The investigated SiC-MOSFET possesses rapid onset avalanche behaviour; future studies require a curve tracer with a HV source measurement unit. Only a few data points are captured from cryogenic conditions to room temperature. These measurements confirm that SiC-MOSFETs have only a slight reduction of $5 - 10\,\%$ in the blocking capability, as mentioned in the subsection III-A. The manufacturing of 650 V SiC-blocking devices is complex due to the thickness of the epitaxial layer. The publications [47] reach comparable results.

Si-IGBTs have also lowered blocking voltage capabilities by around 20 % due to the higher carrier speed under cryogenic conditions. Comparable results are given in [43].

The device's architecture of GaN-Cascodes is very complex. Additionally, the subsection III-A describes the breakthrough mechanism of GaN-HEMT. The measurement results illustrate a reduction of around 40 %. The tests on GaN-Cascodes are repeated several times with different starting temperatures in order to exclude the influence of damage. Results of other breakdown evaluations of 650 V GaN-Cascodes are not available under cryogenic conditions.

Nevertheless, the safety or production margin in WBGs is enormous. Additionally, the Tab. 6 gives an overview of the absolute captured breakdown values at 273.15 K.

It can be noticed that more technical/production experiences in the last 50 years exist in Si-devices than in WBGs. However, the absolute values of the blocking voltage capability illustrate the possibilities of WBGs.

TABLE 6. List of DUTs and their V_{Break} at 273.15 K.

Device	Technology	MF	captured V_{Break} at 273.15 K V	Specified V_{Break} at 298.15 K V
Si-MOSFET	Superjunction	A	694	650
SiC-MOSFET	Trench Gate	A	1300	650
Si-IGBT	Trench Gate	B	651	600
GaN	Cascode	C	1828	650

3) COMPARISON OF THE CAPTURED THRESHOLD VOLTAGE

Another crucial parameter is the V_{Th} because it indicates the robustness against a fault switch-on of the device, as mentioned in the subsection III-B. A temperature dependency on cryogenic conditions is also known from the literature review III-A. Normalised and quadratic-regressed measurement values are shown in the Fig. 14.

Si-Superjunction MOSFET, Si-IGBT, and GaN-Cascode slightly increase of the threshold by around 30 % to cryogenic conditions due to the decreased intrinsic carrier concentrations, as reviewed in the subsection III-A. Si-IGBTs and GaN-Cascodes also own a low-voltage Si-MOSFET as a gate control.

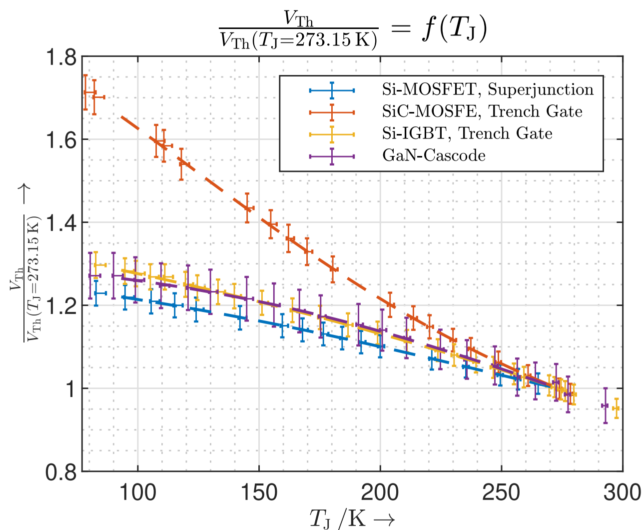

FIGURE 14. Normalised V_{Th} over temperature.

An increase of around 70 % is noticeable in SiC-devices due to enormous degraded concentration of intrinsic carriers, as reviewed in the subsection III-A. The publication [47] represents matching results.

4) COMPARISON OF THE CAPTURED SWITCHING LOSSES

As subsection III-B mentioned, the switching energy losses (E_{on} and E_{off}) decisively determine the applicable f_{PWM}. Furthermore, the switching energy losses are substantial to estimate self-heating under cryogenic conditions. The evaluation is more complicated than over parameters.

Fig. 15 and 16 show the normalised and quadratic-regressed measurement results of E_{on} and E_{off}.

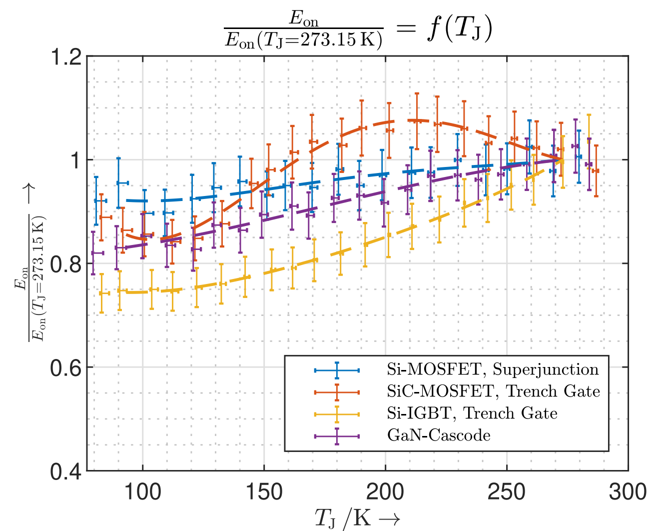

FIGURE 15. Normalised E_{on} over temperature [including Q_{oss} and Q_{rr}].

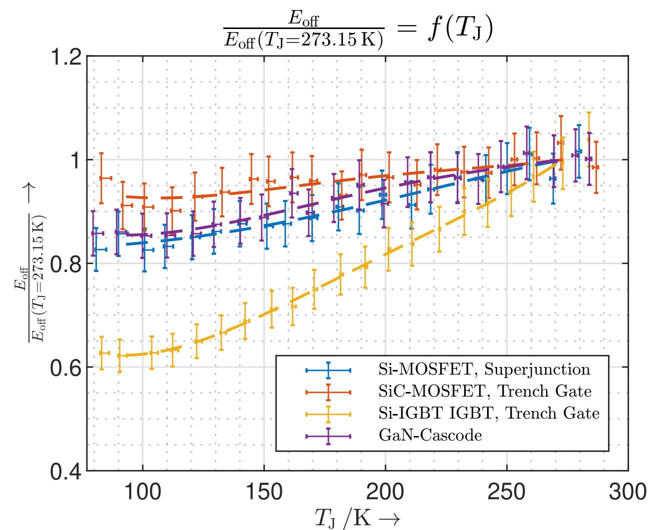

FIGURE 16. Normalised E_{off} over temperature.

The Si-superjunction MOSFET offers lowered switching energy losses (E_{on} and E_{off}) to cryogenic temperatures. However, the measurement can not determine the full potential because this superjunction MOSFET requires a snubber circuit to achieve an acceptable switching behaviour. The increased transdurence due to inversion layer mobility leads to better switching behaviour [40, Page: 1968]. Despite the snubber circuit, comparable results could be reproduced similar to [40].

SiC devices do not offer better switching behaviour (E_{on} and E_{off}) under cryogenic conditions. The E_{off} is slightly improved, as illustrated in the results of Fig. 16. Moreover, Fig. 15 shows an interesting behaviour over the whole investigated temperature range. As investigated in [44, Page: 9109],

the $R_{DS,on,dyn}$ is another interesting parameter and influences the $P_{L,S}$, too.

Taped carriers' freeze-out is mainly responsible for increasing the $R_{DS,on,dyn}$. Furthermore, the effect is device-dependent [44, Page: 9109]. This investigation in this publication comes to the same conclusion as publication [44, Page: 9114] that huge improvements in the switching behaviour are not observable.

Si-IGBTs with an additional Si-diode offer a substantial relative improvement. The decreased Q_{rr} of around 80 % and the increased carrier modulation process to cryogenic conditions lead to better switching behaviour [44, Page: 9109]. Further, the E_{off} is significantly lowered, too. IGBTs have a large tail current under normal conditions. A loss reduction is achieved to better recombination under cryogenic conditions [44, Page: 9112].

GaN-Cascodes have also slightly reduced on-switching losses due to the recombination of the Q_{rr} ($V_{GS} < V_{Th}$) and slightly smaller Q_{oss}. A drop in the switching-off energy losses is also measurable due to the transdurance increase [54, Page: 7415]. The GaN-Cascode inside the TO 247-3 package requires a snubber circuit. Future work will conduct further investigation on E-HEMTs.

Fig. 17 and 18 compare the switching behaviour of the investigated IGBT between 285 K and cryogenic temperature 84 K as an example. From the current and voltage curve in Fig. 17 when switching on, the reduction of the Q_{rr} can be perceived. A massive tail current reduction is noticeable in the switching-off in the current trace in Fig. 18.

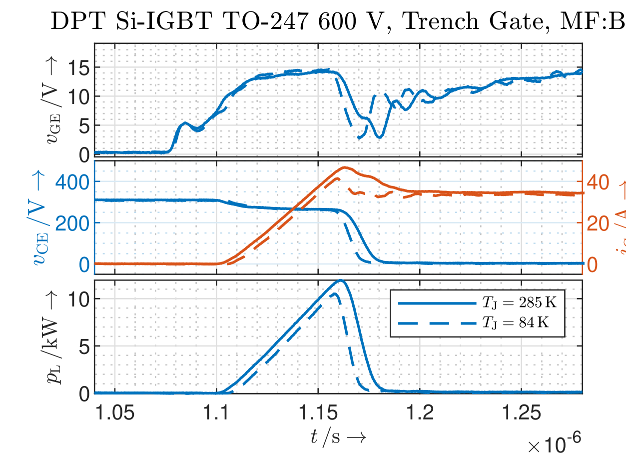

FIGURE 17. Comparison of the on-switching behaviour of the investigated Si-IGBT between $T_J = 285$ K to $T_J = 84$ K.

The following paragraph compares all investigated device parameters against each over and discusses the cryogenic technical prospects.

5) OVERALL COMPARISON AND TECHNICAL PROSPECTS

The spider map in Fig. 19 compares all captured parameters relatively to room temperature and illustrates the prospects powerfully. Therefore, the outer edge represents desirable properties, small R_{on}, high V_{Break}, constant V_{Th}, and lowered

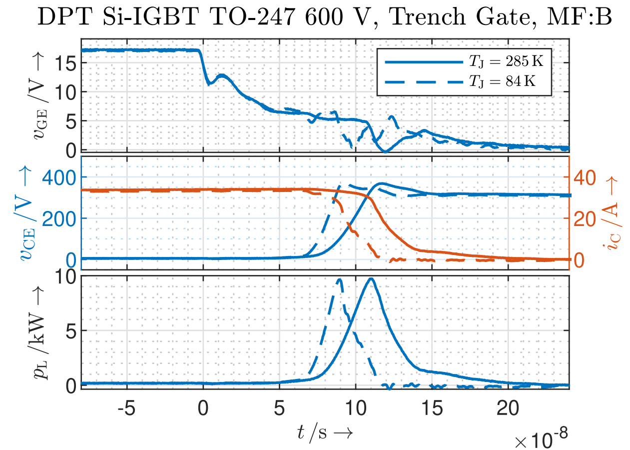

FIGURE 18. Comparison of the off-switching behaviour of the invesigated Si-IGBT between $T_J = 285$ K to $T_J = 84$ K.

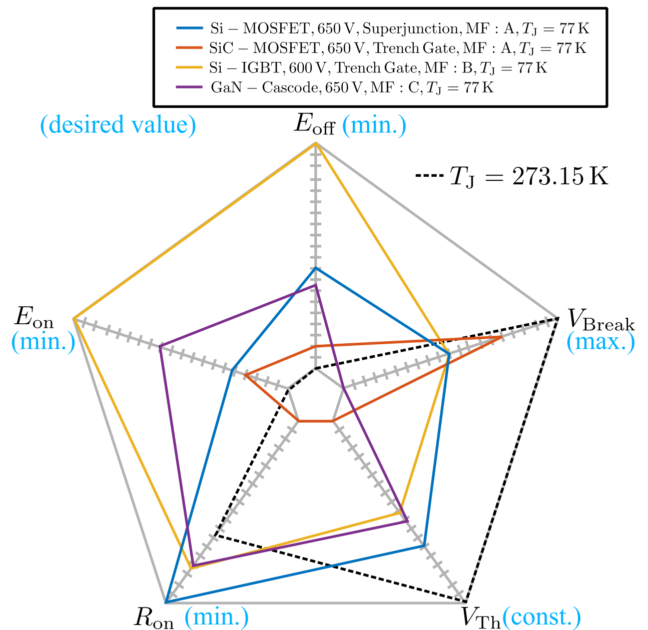

FIGURE 19. Comparison of investigated power electronic devices under cryogenic conditions [the outer corners correspond to the best relative material improvements].

E_{on} and E_{off}. Counters, the inner edge shows poor material properties.

Si-Superjunction MOSFETs offer a significantly decreased R_{on}, a reduced V_{Break}, slightly higher V_{Th} and lowered switching energies. This paper comes to the same material conclusion as mentioned in the subsection fundamentals III-A. Nevertheless, blocking voltage capability limits the design degree of freedom. Nowadays, Si-power MOSFETs are available to 650 V. Thus, two-level topologies are only possible for small bus voltages. Otherwise, due to the small R_{on}, the current-carrying capability is excellent to guarantee huge output currents due to paralleling. Additionally, the carrier freeze-out defines the lowest T_J to above 90 K. Device self-heating or a defined controllable thermal path can drive

the MOSFET in the optimal cryogenic condition. But the device structures and device generation have a profound impact.

SiC-devices have no improvements in cryogenic temperatures. An early-onset carrier freeze-out reduces the possible cryogenic uses, and only the blocking capabilities keep nearly constant at cryogenic temperatures. This technical assessment of the cryogenic behaviour of SiC is confirmed in the literature review III-A. The only way is to use it outside the cryogenic area and take advantage of the enormous ΔT. Around room temperature, SiC offers excellent properties.

In contrast to SiC-MOSFETs, the Si-IGBTs show relative high improvements to cryogenic conditions (to 90 K). Only the blocking capability is badly affected by the lowered temperature. The slightly increased V_{Th} is acceptable. Si-IGBTs in a half-bridge or single configuration are available to HV of 6.5 kV. The use of a two-level topology with high-current carrying and high-voltage capabilities would be possible.

Another WBG-device is investigated in this publication. Compared to SiC offers GaN enormous advantages under cryogenic conditions. The GaN-devices do not suffer under the carrier freeze-out and can be directly cooled. Our investigations show a weakened blocking voltage capability of GaN-Cascodes. However, the breakdown evaluation is difficult due to the complex device structure. Otherwise, as mentioned in the fundamentals, GaN-E-HEMT do not show a weakened blocking capability under cryogenic conditions III-A. But the lateral structure does not allow it to reach the physical properties of GaN. Nevertheless, the lateral structure is essential to achieve good switching properties. Multilevel and interleaving is required to reach higher output powers. The design considering all thermal design aspects will be challenging and could decrease the power density.

Tab. 7 gives an overview of the presented thoughts.

TABLE 7. Recommendation for all DUTs for the operation in cryogenic environments.

Device	Technology	Cryogenic	Power	Cooling
Si-MOSFET	Superjunction	yes	medium	indirect
SiC-MOSFET	Trench Gate	no	high	indirect
Si-IGBT	Trench Gate	yes	high	indirect
GaN	Cascode	yes	medium	indirect
GaN	HEMT	yes	medium	direct

This section sets the important background for designing a power electronic inverter for a cryogenic drive train of a long-distance aircraft. The behaviour of the semiconductor materials is investigated by experiments and validated by a comprehensive literature review. Thus, this section summarises semiconductor materials' technical prospects in cryogenic temperature ranges and introduces recommendations.

The following section describes the design of a power electronic inverter for a cryogenic power train for a long-distance aircraft.

IV. POWER ELECTRONIC INVERTER DESIGN FOR CRYOGENIC POWER TRAIN

This section presents the power electronic design with cryogenic cooler design of a drive inverter for a superconducting electrical propulsion of long-distance aircraft.

The data from system analysis in section II and the experimental semiconductor material investigation in section III add important input to the inverter design. With the aid of understanding the loss mechanism of each semiconductor material in cryogenic temperature ranges, the optimal T_{J} can be defined. Therefore, the optimal T_{J} determines the cooler. Two cooling system concepts (direct H_2 and indirect He) are available, and for both, cryogenic heat sink designs are presented. The challenges are:

- The selection of suitable semiconductor materials and structures with their advantages and disadvantages
- Superconductor and semiconductor interfacing
- The choice of the topology with its influence on the current ripple
- A targeted highly-integrated drive train concept with different thermal resistances avoiding voltage superpositioning
- The integration of the topology into the cooling concept with non-cryogenic or cryogenic working semiconductors
- The cooling design has to guarantee the required temperature range to operate the semiconductors in their advantaging operating temperature under partial load conditions
- A lightweight cooler design to reach high power densities of the overall power electronic inverter (conventional heat sink has a large share of the total mass or volume)

A. POWER ELECTRONIC DESIGN

This subsection shows the state of the art of cryogenic inverter design for a long-distance aircraft, choice of the semiconductor material, topology discussion, the loss model and mass estimations.

The mission profile, mentioned in the system analyses in the section II, requires enormous P_{Shaft}s. Furthermore, several systems specifications must be taken in the inverter design. Based on a material and topology discussion, an inverter loss model delivers essential impacts for the heat sink design. With the aid of a scalable inverter model, a mass assumption of the electrical parts can be calculated.

A 3×3 5.4 MW superconducting electrical machine with three independent stars point needs a $\hat{i}_{\mathrm{s}}$ of 870 A by $V_{\mathrm{DC}} =$ 3 kV. Moreover, the superconducting machine requires a f_{PWM} higher than 10 kHz. The highly defined onboard voltage possesses challenges and advantages. Significantly, the leg current is reduced by a highly defined DC voltage of 3 kV. This is an advantage because the semiconductors do not reach the conductivity of a superconductor even with cryogenic cooling. The connection technology of the power

electronics could only be designed to be weight-reduced if it is superconducting. Directly connecting superconductors to the power electronics semiconductors requires the use of GaN. This essential interfacing topic has to be addressed in future studies.

1) STATE OF THE ART

Publication [15] illustrates the design of a MW-scale cryogenic-cooled three-level inverter ANPC (two ANPC inverters in parallel to 1 MW) based on SiC-MOSFETs with a f_{PWM} of 70 kHz and a ±500 V bus voltage.

Another publication [14] presents the results of an Si-MOSFET-based ANPC three-level inverter with 140 kHz. The bus voltage is also 1000 V. As mentioned in this publication and our studies, the cryogenic temperature can reduce losses for Si-Superjunction MOSFETs. Furthermore, the ANPC reduces electromagnetic compatibility (EMC) filter efforts due to smaller du/dt. The commissioning of the scaled 40 kW inverters is shown, and an efficiency improvement of around 30 % is presented. The inverter reaches absolute efficiency at cryogenic temperature by around 97.8 %.

2) CHOICE OF SEMICONDUCTOR MATERIAL

Currently, the bus voltage of 3 kV makes it challenging to use GaN devices because of their lower blocking voltage capability. Additionally, the multilevel design has to be supplemented by massive paralleling of GaN-devices to reach high power demands. In the future, GaN devices could be an alternative and offer no cooling limits due to the non-appearance of carrier freeze-out. The cooler design could be lightweight.

To face the high bus voltage, HV blocking Si-IGBTs and HV blocking SiC devices are the devices of choice. As investigated in the previous sections, IGBTs offer loss reduction benefits and worse blocking capabilities under cryogenic conditions around 80 K until 120 K. Si reaches its limits, and the cryogenic improvements do not match the values of common cooled SiC. The publication [73, Page: 248] of Cree introduces their investigation on a 6.5 kV chip. This chip offers a tenfold reduction in $P_{\mathrm{L,S}}$s compared to HV blocking IGBTs. Also, with circuit optimisations presented in [74, Page: Page: 117], soft-switching circuits can improve the $P_{\mathrm{L,S}}$s of IGBT-inverters by around 50 %, but this does not reach SiC's values.

3) TOPOLOGY DISCUSSION

The choice of the power electronic topology is dominated by the interaction of machine, electronic properties and electrical system requirements. 2-level and multi-level topologies are feasible for the nine-phase inverter design, but the power density is a crucial design target.

The 2-level inverter has the main advantage of a minimal amount of semiconductors, but it has to use semiconductor devices with 6.5 kV blocking voltages. Due to the high blocking voltage, fast voltage-changing speeds and parasitic capacities, EMC filter efforts increases.

A model-based optimisation in [75] concludes that the ANPC three-level shows higher power density than a two-level voltage source inverter due to a decreased active semiconductor chip size. The ANPC could use semiconductors with a blocking voltage of 3.3 kV by increasing the number of active semiconductor devices. As mentioned in the cryogenic invert's state of the art, the main advantage of the ANPC is the decreased EMC filter efforts. Moreover, the f_{PWM} could be much higher and improve the THD [76]. Dielectric stress due to the fast voltage changing speeds in the electrical machine's windings could be reduced, which leads to reduced insulation lifetime [77]. The increased active semiconductors possess many controlling strategies to improve the loss distribution, hybridise different semiconductor materials, and increase fault tolerance. Otherwise, semiconductors with different behaviours must be combined, and the electrical interaction could be challenging. Additionally, the DC link capacitor is twice as big as the two-level configuration by storing the same energy [76]. The balancing of the DC link capacitor restricts the control.

Nevertheless, the ANPC could possess advantages in several aspects. Model-based investigations, as suggested in [75], and holistic system optimisations as [12] have to clarify beneficial inverter topology under cryogenic power train requirements of a long-distance aircraft. The electric-thermal design is the focus of this scientific contribution. As the first design step, a two-level nine-phase configuration is used.

4) LOSS MODEL

Fig. 20 shows 2-level topology for a drive inverter with the lowest amount of semiconductor devices. In the discussed case, three inverters fed one cryogenic drive. The thermal and electrical interfaces could be challenging in a matter of a non-cryogenic approach.

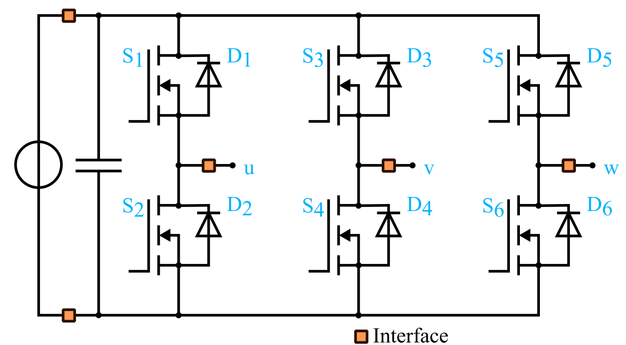

FIGURE 20. Non-cryogenic SiC three-phase two-level inverter.

The analytical loss Eqns. 6 to 13 of the three-phase 2-level inverter controlled via a space vector modulation illustrates the power dissipation of the power electronic.

There are $P_{\mathrm{L,S}}$ and $P_{\mathrm{L,C}}$ for the semiconductor switch (here index: MOSFET) and diode (here index: Diode). Controllable parameters, such as the M, affect the $P_{\mathrm{L,C}}$. Other parameters, such as the $\cos\varphi$ and $\hat{i}_{\mathrm{s}}$, are given by the electrical machine. Additionally, the space vector modulation has a

third harmonic; therefore, the conduction losses require a fourier decomposed factor (F_{svm}) [78, Page: 2838].

The $P_{L,S}$ are proportional to the configurable f_{PWM}. Additionally, the equations offer a linear adjustment to the captured reference value (index: ref) [74, Page: 29].

$$P_{L,S,MOSFET} = \frac{1}{\pi} \cdot f_{PWM} \cdot (E_{on}(T_J) + E_{off}(T_J)) \cdot \frac{V_{DC}}{V_{ref}} \cdot \frac{\hat{i}_S}{I_{ref}} \tag{6}$$

$$P_{L,S,Diode} = \frac{1}{\pi} \cdot f_{PWM} \cdot E_{rec}(T_J) \cdot \frac{V_{DC}}{V_{ref}} \cdot \frac{\hat{i}_s}{I_{ref}} \tag{7}$$

$$P_{L,C,MOSFET} = \frac{R_{DSon}(T_J) \cdot \hat{i}_s^2}{2 \cdot \pi} \cdot \left(\frac{\pi}{4} + M \cdot \left(\frac{2}{3} \cdot \cos\varphi + F_{SVM}\right)\right) \tag{8}$$

$$P_{L,C,Diode} = \frac{V_{F0}(T_J) \cdot \hat{i}_s}{2 \cdot \pi} \cdot \left(1 - \frac{M \cdot \pi}{4} \cdot \cos\varphi\right) + \frac{R_F(T_J) \cdot \hat{i}_s^2}{2 \cdot \pi} \cdot \left(\frac{\pi}{4} - M \cdot \left(\frac{2}{3} \cdot \cos\varphi + F_{SVM}\right)\right) \tag{9}$$

$$F_{SVM} = \frac{6 \cdot \sqrt{3}}{\pi} \sum_{\nu}^{\infty} \left[\frac{\cos(k \cdot \varphi)}{k^5 - 5 \cdot k^3 + 4 \cdot k} - \frac{\cos(l \cdot \varphi)}{l^5 - 5 \cdot l^3 + 4 \cdot l}\right] \tag{10}$$

$$k = 3 \cdot (4 \cdot \nu + 1) \tag{11}$$

$$l = 3 \cdot (4 \cdot \nu + 3) \tag{12}$$

$$\nu = 0, 1, 2, 3, \ldots \tag{13}$$

Currently, only a high-blocking and high power half-bridge module from Mitsubishi [79] is under development. A scaled and fictive device is used based on experiences from the publications [75] and chip data from [73].

Additionally, the temperature dependency is estimated by fitting parameters from own investigations. With the help of the Eqns. 6 to 13, the chip loss can be calculated. All calculations are assumptions to prove the technical implementation feasibility. In the future, better values can also be expected due to HV SiC and packaging development.

The power losses per switch ($P_{L,Switch}$) can be calculated with number of parallel-switched chips per module (n_{Chip}) and the cumulative power losses per chip ($P_{L,Chip}$) of each chip:

$$P_{L,Chip} = P_{L,C,Chip,MOSFET} + P_{L,S,Chip,MOSFET} + P_{L,C,Chip,Diode} \tag{14}$$

$$P_{L,Switch} = \sum_{n=1}^{n_{Chip}} P_{L,Chip} \tag{15}$$

The model data in Fig. 21 shows a decreasing optimal T_J to increase f_{PWM}. The losses are minimal in a temperature range of 250 K to 275 K. SiC has to be used at a particular temperature to minimise losses because the $P_{L,S}$ become dominant for HV-blocking chips at higher f_{PWM}s. Until a T_J of 223 K, a slight increased $R_{DS,on}$ can be recognised from the measurement data in Fig. 11.

Moreover, the thermal path defines which $P_{L,Chip}$ per chip surface can be handled. Using 20 kHz, the power dissipation per chip surface is about $0.8\,\mathrm{W} \cdot \mathrm{mm}^{-2}$. An optimisation of the chip area can reach higher levels dependent on the thermal path. Therefore, the f_{PWM} can be further increased. A further THD reduction, as exemplary presented in the subsection II-B3, is reachable.

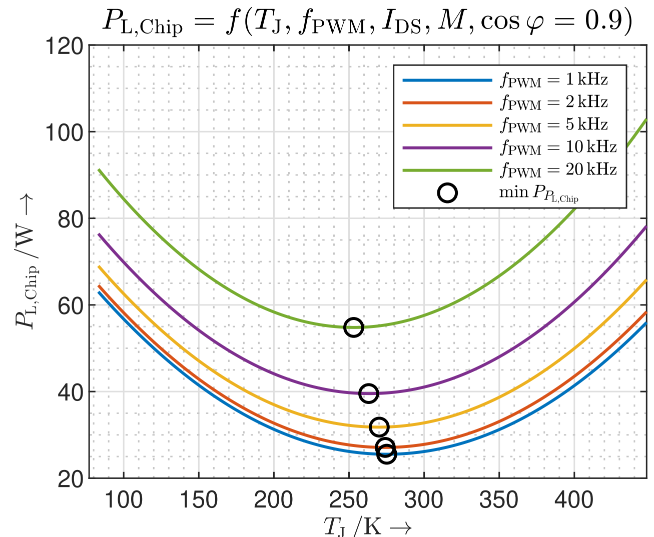

FIGURE 21. **Losses per chip with varied f_{PWM}, I_{DS} = 30 A, M = 0.9, $\cos\varphi$ = 0.9.**

The diagram in Fig. 22 illustrates the partial load loss behaviour of the inverter over the temperature. For LC1, the total $P_{L,Switch}$ is 1.57 kW. The $P_{L,Inv}$ is 28.23 kW. This dissipation leads to estimated efficiency of 99.5 % without auxiliary losses. Further improvements can be reached; an optimum P_{trans} of the superconducting electrical machine and $P_{L,S}$ has to be found in holistic optimisation approach in future studies. In the future, an improvement can be expected due to the development of WBGs.

The single-switch SiC module includes paralleled n_{Chip} = 26. Therefore, the interconnection of the n_{Chip} = 26 can be challenging for the future module. Furthermore, the f_{PWM} is limited to the interconnection. The calculated assumptions do not cover the limitations of the parallel arrangements.

A spreading angle of 45° with a conventional direct bonded copper (DCB), soldering and aluminium matrix with SiC particles (AlSiC) base plate obtain the cooling. The required data and the mathematical description are used from the publication [75]. The thermal resistance from junction to case ($R_{th,J-C}$) for a single chip is calculated with assumed material data, layer thickness and a spreading angle. The cumulated thermal resistance from junction to case ($\sum R_{th,J-C}$) in Fig. 23 consists of multiple parallel chips with their single thermal resistances $R_{th,J-C}$. By increasing the

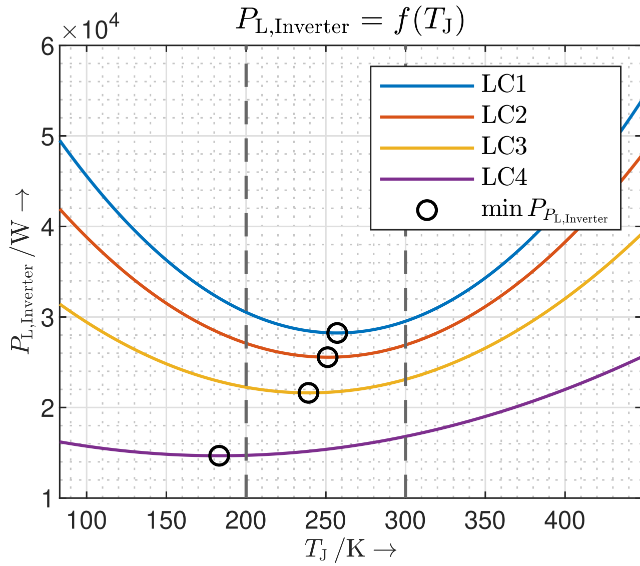

FIGURE 22. In the partial load range (LC1, LC2, LC3, and LC4), the minimised $P_{\mathrm{L,C}}$ lead to lower optimal T_{J}s.

f_{PWM} the $P_{\mathrm{L,S}}$ increases, and the chip current per single chip has to decrease because of the limited power dissipation per chip area. It requires more n_{Chip} and more module area—the $\sum R_{\mathrm{th,J-C}}$ decreases, as presented in Fig. 23. An increased n_{Chip} leads to a quadratic increase of the module area. A f_{PWM} of 20 kHz has a $\sum R_{\mathrm{th,J-C}}$ of 14.3 K·kW^{-1} of one switch with 26 parallel chips.

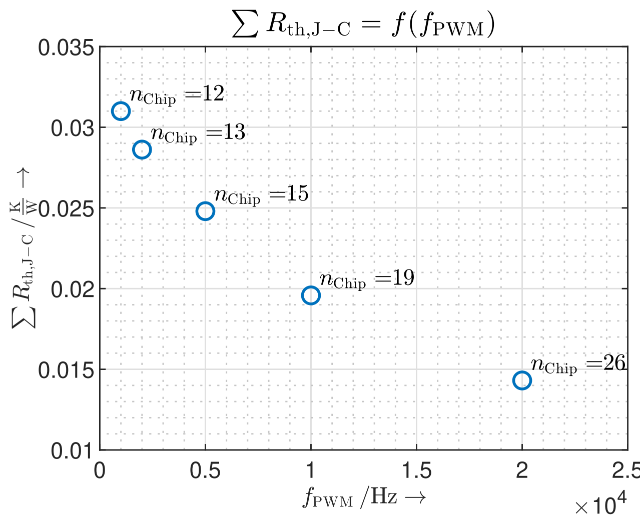

FIGURE 23. Calculated $\sum R_{\mathrm{th,J-C}}$ of multiple parallel chips is dependent on the f_{PWM}.

5) MASS ESTIMATIONS

The mass of a single-switch module (m_{Switch}) can be assumed using material data and estimated Volumina for all module components. Two switches form a half-bridge, and the superconducting electrical machine requires nine phases (3 × 3). The mass of the module (single-switch-configuration) is 0.61 kg and dependent on the f_{PWM}, as shown in Fig 24. The total module mass per inverter is calculated to be 11 kg. Capacitors are estimated to have about 60 kg using equations of the publication [75]. The electrical interconnection is complex because the inverter is outside the cryogenic media. Therefore, a thermal barrier is needed. The interconnection is estimated to weigh per inverter of 45 kg. A weight of 5 kg is approximated for intelligent drivers as proposed in [80] and over auxiliaries. The integration in the fan's housing is strived to lower the mass.

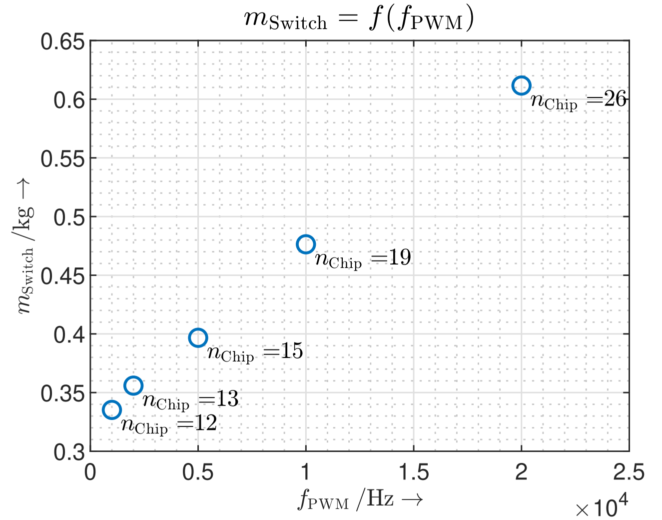

FIGURE 24. Estimated modul mass is dependent on the f_{PWM} (single-switch-configuration).

The following section continues with the design of the power electronics heat sink. Based on the loss model estimations, a heat sink design for both presented cooling concepts has to be discussed.

B. POWER ELECTRONIC COOLER DESIGN

As mentioned in section II, the indirect or direct cooling system has to cope with the media flow of full and partial load conditions. This section presents the ideas for power electronics cooling related to a direct H_2 and indirect concept He.

Referring to Fig. 22, a 5 % tolerance of the losses around the optimal working temperature is introduced, yielding a temperature window from 200 K to 300 K for the optimal operation of the power electronic switches.

The calculations will have a safety margin if the H_2 has left the wet stream region and is an equilibrium gas (para- and ortho-hydrogen with temperature-dependent mass fractions). The losses of the superconducting cables, power electronic inverter and superconducting electrical machines heat the H_2 to certain amount of fuel cell temperature level. The thermophysical properties of H_2 are taken from [27], [81].

1) DIRECT COOLING CONCEPT WITH H

After cooling the superconducting cables, the H_2 will probably enter the electrical machines with 24 K to 34 K. According to Tab 8, the H_2 gas leaves the electrical machine with estimated temperatures. At this current design stage, not

much is known about the losses of the superconducting wiring harness and the heat intruding into the wires from the environment via connectors, valves and flanges. An optimistic scenario is assumed. The exact temperature level is less critical for power electronics because they operate at much higher temperatures than electrical machines and the DC backbone.

TABLE 8. H_2 **temperature based on the mission profile and the assumed losses of DC backbone and electrical machine.**

Load Case		T_{H2} of H_2 K
LC1	Peak Rating	83.7
LC2	Climb	83.7
LC3	Cruising	83.6
LC4	Landing	81.4

Several geometries of heat sink plates are studied. A proposal for an AlSiC cooling plate is given in Fig. 25. The gaseous H_2 with an average working temperature (T_m) of appr. 80 K to 84 K and operating pressure of 2 bar pass through straight channels underneath the MOSFET modules. The cooling plate has the exact dimensions of the base plate of the two single-switch modules (half-bridge).

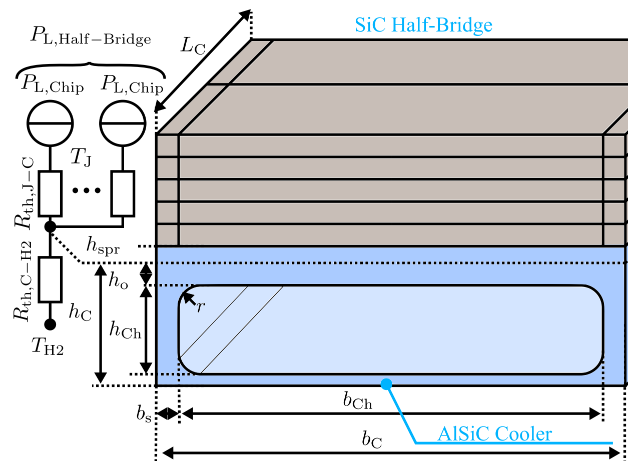

FIGURE 25. **Power electronic cooler design (one half-bridge of nine, two single-switch-configuration).**

There are two strategies to achieve the necessary temperature drop between junction and H_2 temperature—a temperature blocking resistor in the conductive path or a deliberately reduced heat transfer on the gas side.

Strategy I, a 0.15 mm Kapton layer between the case and the heat sink plate may already serve. However, calculations show a considerable spread of temperatures between the LCs peak power (LC1) and landing (LC4). Consequently, optimisation is possible for only one LC, while the others will be far outside the tolerance window.

Strategy II, increasing the temperature drop of the heat transfer to the cooling gas is a more promising approach due to the non- linearity of the reynolds number (R_e) and nusselt number (N_u). Increasing the cross-section of the channels while reducing the effective heat transfer surface (A_r) in the cooler plate, as indicated in Fig. 25, can achieve a reduced velocity, smaller R_e, and small heat transfer coefficients.

Each change of flow momentum causes pressure losses. The impulse occurs by changing cross-sections and any flow through a channel or pipe. The velocity, density, and temperature will also change using a compressible medium. Combined with the temperature-dependent H_2 properties, this leads to highly nonlinear dependencies and requires numerical computational fluid dynamics (CFD) calculation for more exact results. An approximation procedure with the well-known equations for heat transfer and compressible media [27], [28] [81], [82] [83], [84] [85] is used to study the main influencing parameters.

Calculating the temperature drops (Eqn. 16) on the thermal conductive path are trivial, otherwise calculating the heat transfer requires more effort.

$$T_j = T_{H2} + \left(R_{th,J-C} + R_{th,C-H2}\right) \cdot \sum_{2 \cdot n_{chip}} P_{L,Chip} \quad (16)$$

As the $\dot{m}_{H2}$ does not vary from tank to fuel cell, isobaric conditions can be assumed in principle. There are tiny pressure drops along the flow path due to friction and change in channel size, but they are far below 1 %, so this assumption is justified. For exemplarily 2 bar operating pressure, a stepwise calculation of the H_2 mass flow through the cooler plate ($\dot{m}_{cp}$) is conducted. The calculations yield the pressure drops, the velocities, and the flow temperature before and outside the cooler channels. From the velocities and the geometry of the cooling channel with the hydr. diameter (D_h) (Eqn. 17), R_e, N_u and the average coefficient of heat transfer (α_m) are derived [81], [82] [83], [84] [85].

$$D_h = \frac{4 \cdot A_{Ch}}{C_{Ch}} \quad (17)$$

With the cross-section of the cooling channel (A_{Ch}) and the circumference of the channel (C_{Ch}), the D_h can be calculated. This results in A_r:

$$A_r = \pi \cdot D_h \cdot L_{Ch} \cdot n_{ch} \quad (18)$$

The cooler channel length (L_{Ch}) is equal to cooler length (L_C). The following calculated surface is used as a reference for evaluating all channel geometries. The real heat transfer area (A_T) differs from A_r:

$$A_T = C_{Ch} \cdot L_{ch} \cdot n_{ch} \quad (19)$$

With A_T, the temperature drops of heat transfer are calculated. The medium thermal conductivity (λ_m) is found with the thermal conductivity of H_2 (λ_{H2}) at the T_m and the N_u for turbulent or laminar flow:

$$\lambda_m = \frac{N_{u,m} \cdot \lambda_{H2}(T_m)}{D_h} \quad (20)$$

Regarding the short L_{Ch}, the calculation of the medium value of reynolds number ($R_{e,m}$), medium value of nusselt number ($N_{u,m}$) and T_m are considered sufficient in Eqn. 21. These

values are iteratively corrected by heating the H_2 flow, which contributes significantly to T_m.

$$\Delta T = \frac{P_{ch}}{\dot{V} \cdot \varrho_{H2}(T_m) \cdot c_{pH2}(T_m)} \quad (21)$$

$$\Delta T = \frac{P_{ch}}{\dot{m}_{Ch} \cdot c_{p,H2}(T_m)} = \frac{\Delta h}{c_{p,H2}(T_m)} \quad (22)$$

With the aid of power losses per channel ($P_{L,Ch}$), the volume flow ($\dot{V}$), the density of H_2 (ϱ_{H2}) and the thermal capacity of H_2 ($c_{p,H2}$), the ΔT between in- and outlet can be calculated. The converted formula 22 offers the use of mass flow per channel ($\dot{m}_{Ch}$) or enthalpy change (Δh). Additionally, the $T-S$ or $h-S$ diagram provides the temperature-dependent data of the H_2. Calculating the ΔT allows the calculation of the thermal resistance from case to H_2 ($R_{th,C-H2}$) and the T_J of the semiconductor in Fig. 26.

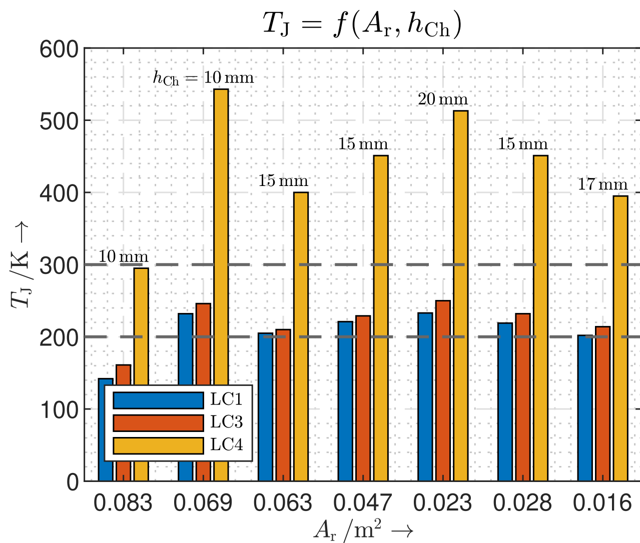

FIGURE 26. T_J **depending on the** A_r **and the thickness of the cooler plate, preferred geometry:** $A_r = 0.016\,m^2$, $h_{Ch} = 17\,mm$**).**

The channel dimensions, channel height (h_{Ch}), channel width (b_{Ch}) and number of cooling channels (n_{Ch}) are varied. Fig. 26 shows the feasibility of reaching the desired temperature window (low and high tolerance temperature, in Fig. 22) by the heat sink design. Tab. 9 illustrates the dimensions of the preferred structure with one cooling channel.

The analyses show a nonlinear dependency that could be traced back to geometrical changes of the channels (difference between A_r and A_T). Moreover, only an integer value of n_{Ch} is possible. Suppose the surface becomes smaller with increasing channel diameter because fewer channels fit into the fixed b_C. In that case, the turbulence decreases, and the $R_{th,C-H2}$ increases.

A significant deviation from the temperature window occurs at LC4 because the $\dot{m}_{H2}$ is so small that the temperature rises to very high values. With some geometries, the flow additionally changes from turbulent to laminar, causing a further temperature rise. A turbulent flow is maintained in the preferred geometry under all LCs. The higher T_J at LC4 is not critical nor dimensioning due to the small losses.

TABLE 9. Dimensions of the preferred exemplary cooling plate.

Dimension	Value Unit of Measurement
L_C	240 mm
cooler width (b_C)	120 mm
cooler height (h_C)	22 mm
hydr. diameter of cooling channel (D_C)	22 mm
h_{Ch}	17 mm
corner radius of the cooler (r)	1.5 mm
upper cover (h_o)	4.3 mm
b_{Ch}	100 mm
side wall (b_s)	10 mm
n_{Ch}	1
$\sum R_{th,J-C}$	$7.15\,K \cdot W^{-1}$
thermal conductivity of AlSiC (λ_{AlSiC})	$173\,W \cdot (m \cdot K)^{-1}$
mass of the cooling plate (m_{Cp})	600 g

The temperature drop between the coolant and channel wall is comparatively high and influenced by the turbulence (where R_e is an equivalent measure) and the poor λ_{H2} at low temperatures. As mentioned in strategy II, the design lifts the T_J to the desired temperature window. The T_Js of the preferred geometry ($A_r = 0.016\,m^2$, $h_{Ch} = 17\,mm$) are within the lower half of the tolerance window and fit neatly with the calculated optimal T_J.

From these data, the m_{Cp} is 600 g, which is relatively low for a single switch element of this size. The relatively short L_{Ch} allows a calculation with average values and a one-dimensional calculation model for the heat flow given in Fig. 25.

2) INDIRECT COOLING CONCEPT WITH He

Due to the high optimal T_J of SiC-devices, a RBCC is not required. The cooling circuit of the power electronics comprises only the cooling plate, the heat exchanger and a fan to serve the necessary H_e mass flow ($\dot{m}_{He}$). Fig. 27 illustrates the indirect cooling system without a RBCC.

With indirect cooling, controlling the fan speed allows a particular variation of the $\dot{m}_{He}$.The calculation procedure is somewhat similar to the one described before. Three heat transfer areas must be considered:

1) The heat transfer from $P_{L,Inv}$ to the He cooling gas flow in the cooler plate
2) The two heat transfers in the heat exchanger: From the He flow to the wall of the cell and from the wall to the $\dot{m}_{H2}$

Slight rises in temperature and pressure are caused by the fan, which increases the enthalpy by the amount of added electrical power (P_{in}). This additional P_{in} must also be transferred to the heat sink.

A counterflow design with a laser-welded construction and a high number of parallel channels or cells is proposed as a heat exchanger in Fig. 28. The pressure in the He circuit is chosen, similar to the pressure of the H_2 side at appr. 2 bar. The low pressure allows a thin walled construction of the heat exchanger.

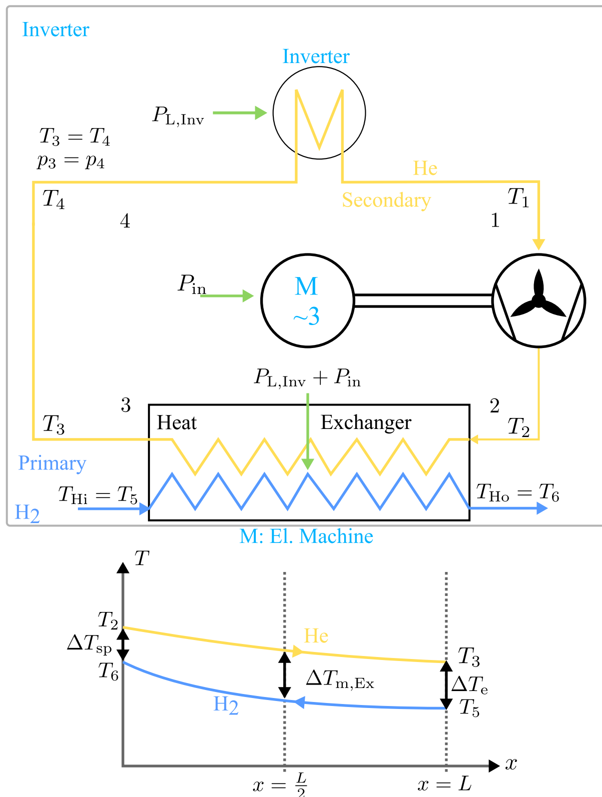

FIGURE 27. The indirect cooling circuit concept for the power electronic inverter does not require a RBCC.

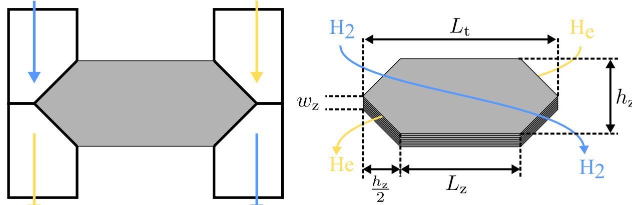

FIGURE 28. Laser-welded heat exchanger construction for power electronic cooling.

The calculation of the heat exchanger follows the known formula apparatus as known from [83], [86] [84], [85] [87]. As an unique feature, a prescribed $\dot{m}_{\mathrm{He}}$ on the primary side can be noticed while the choice of the $\dot{m}_{\mathrm{He}}$ on the secondary side is free in principle. The thermophysical properties of He and H_2 are retaken from [27], [81] [82]. The calculation model can be explained with the help of Fig. 27.

The power balance yields the temperatures T_5 and T_6, and with $\Delta T_{\mathrm{sp}} = T_2 - T_6$ as the free chosen parameter, the temperatures T_1, T_2 and T_3 can be calculated. The Eqn. 23 describes the medium temperature drop in the heat exchange ($\Delta T_{\mathrm{m,Ex}}$) and defines the first condition of the $\dot{m}_{\mathrm{He}}$. It may be noticed that the choice of higher T_{sp} also reduces the $\dot{m}_{\mathrm{H2}}$:

$$\Delta T_{\mathrm{m,Ex}} = \frac{\Delta T_{\mathrm{e}} - \Delta T_{\mathrm{sp}}}{\ln \frac{\Delta T_{\mathrm{e}}}{\Delta T_{\mathrm{sp}}}} \tag{23}$$

As the sum of $\Delta T_{\mathrm{m,Ex}}$ from the heat transfer calculation depends also on the $\dot{m}_{\mathrm{He}}$; a second condition is given. Both conditions must be balanced to calculate the $\dot{m}_{\mathrm{He}}$.

The calculations use the designs mentioned in Fig. 27, and Fig. 28. Tab. 10 presents the heat exchanger's dimensions.

TABLE 10. Dimensions of the heat exchanger.

Dimension	Value Unit of Measurement
length laser-welded heat exchanger (L_z)	400 mm
height laser-welded heat exchanger (h_z)	100 mm
width laser-welded heat exchanger (w_z)	3.3 mm
wall thickness laser-welded sheets (d_z)	0.5 mm
number of channels for each medium (n_{zm})	40
weight of heat exchanger without connecting flanges (m_{Ex})	4.3 kg

The design aimed to achieve a moderate $\dot{m}_{\mathrm{He}}$ for LC1 to reduce the maximum fan power (P_{in}). The $\dot{m}_{\mathrm{H2}}$ varies with the LC allowing a reduced P_{in} if the drive is not operated at full load.

In this exemplary calculation each drive is equipped with cooling circuits for machine and power electronics. This gives a maximum of redundancy in the drive system. The $\dot{m}_{\mathrm{H2}}$ of $0.085\,\mathrm{kg \cdot s^{-1}}$ enters the heat exchanger with $T_5 = 80\,\mathrm{K}$ and is heated up to $T_6 = 109\,\mathrm{K}$. The maximal $\dot{m}_{\mathrm{He}}$ is $0.113\,\mathrm{kg} \cdot s^{-1}$ for LC1, requiring a fan power of 1.9 kW. He enters the heat sink plate with a temperature of $T_3 = 83\,\mathrm{K}$. It is heated up during LC1 to $T_2 = 134\,\mathrm{K}$. With the fan's aid, the temperature rises by 2.6 K.

The heat transfer calculation in the cooler plate is done according to the previous discussion on direct cooling via LH_2. An exemplary construction of a heat sink plate with the dimensions in Fig. 29 is calculated.

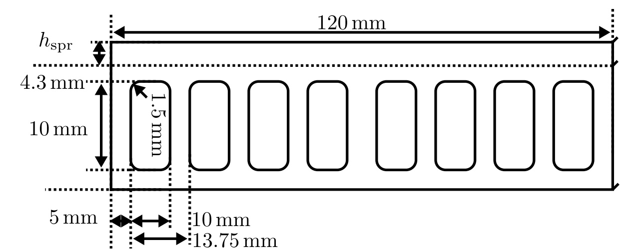

FIGURE 29. AlSiC cooler plate for the He circuit. $240 \cdot 120\,\mathrm{mm}^2$ with eight channels, weight $m_{\mathrm{Cp}} = 0.8\,\mathrm{kg}$.

Tab. 11 shows the calculated T_{J} based on the LCs. Special attention is given to LC4 because the $\dot{m}_{\mathrm{H2}}$ is minimal, causing significantly higher H_2 heating by the $P_{\mathrm{L,Inv}}$ up to 239 K.

TABLE 11. T_{J} based on the mission profile and indirect cooled by He.

Load Case		T_{J} K
LC1	Peak Rating	250
LC2	Climb	247
LC3	Cruise	236
LC4	Landing	332

Fortunately, the He flow stays in the turbulent region with the help of the fan. It lifts all temperatures in the He circuit and requires an adaption of the $\dot{m}_{\mathrm{He}}$ to the elevated temperatures.

The fan power is reduced to 1.4 kW only. Consequently, the T_J in LC4 is outside the tolerance window of 200 K to 300 K. Nevertheless, the power and the losses in LC4 are so small; therefore, this is not critical for the operation of the drive. The following subsection compares the impact of both cooling design proposals on mass estimations. A power density can be assumed under all discussed assumptions.

C. INVERTER MASS COMPARISON

The calculated data from the previous subsections possess a first mass estimation of the power electronic inverter. Both discussed technical cooling opportunities are compared in Tab. 12.

TABLE 12. **Inverter mass estimation (power electronic auxiliary: small magnetic components, current sensors, driver, and control).**

Component	Direct Cooling kg	Indirect Cooling kg
Module mass ($2 \cdot m \cdot m_{\text{Switch}}$)	11	11
Capacitor mass	60	60
Power Electronic Auxiliaries	5	5
Bus bars	45	45
EMC Filter	not estimated	not estimated
Cooler Plates ($m \cdot m_{\text{CP}}$)	5.4	7.2
m_{Ex}	-	4.3
Mechanical Auxiliaries	Not estimated	Not estimated
Fan, motor and inverter	-	2
Overall	127	135

Nevertheless, the weight estimations are subject to certain uncertainties. Other essential components, such as the EMC filter and mechanical auxiliaries, must be considered in future studies. Mechanical auxiliaries include flanges and piping systems. The determination of these missing masses requires further reconciliations at the system level.

Although the estimation does not cover some components' weight, the expected total weight is comparatively low. A gravimetric power density of $40.4\,\text{kW} \cdot \text{kg}^{-1}$ to $42.9\,\text{kW} \cdot \text{kg}^{-1}$ could be achieved. Moreover, the weight difference between direct and indirect cooling not significant, thus indirect cooling is not ruled out.

V. CONCLUSION

This paper illustrates the power electronic design in the cryogenic application of long-distance aircraft. New aircraft designs with better storage capabilities for the volumetric but light-weight liquid hydrogen (LH_2) enable new non-CO_2-producing fuel-cell-driven power train concepts. Hydrogen (H_2) enables technologies such as superconductivity and increases the power density of the superconducting backbone and the superconducting electrical machine. Nevertheless, an electric power train requires a power electronic inverter to drive the electrical machine.

Knowledge of the behaviour of different semiconductor materials under cryogenic temperatures is essential to answer the question: "Are modern power electronics a technology enabler or a bottleneck of the system?" Additionally, the cryogenic power train possesses many challenging aspects. The aircraft design defines the needed mechanical shaft power (P_{Shaft}) per engine. Therefore, power electronics must deliver enormous power values required from the aircraft's mission profile. Also, superconducting machines possess some requirements for the power electronic concerning switching frequency (f_{PWM}) and total harmonic distortion (THD). Superconductivity is not feasible without considering the cooling of the components.

This article is based on requirement-oriented methodology and analyses the aircraft and energy system prospects. Experimental semiconductor material investigations support this methodology to understand the semiconductor material behaviour under cryogenic conditions. Out of the system analyses and experiments investigation, a power electronic design with cooling considerations for cryogenic power trains is possible.

System-level aspects analysed in section II lead to the design conditions of the power electronic drive train inverter. Significantly, installed P_{Shaft}, the needed THD of the electrical machine and the available cooling opportunities impact the power electronic design. Designing power electronics for cryogenic power train also requires a comprehensive comparison of the behaviour of semiconductor materials under cryogenic conditions. Comprehensive experimental investigations in section III on different semiconductor materials indicate the loss-saving junction temperature (T_J) to prove the suitability of the semiconductor materials. This experimental-indicated loss-saving T_J is scaled to the desired power range of the cryogenic power train. The power electronic design in section IV includes the heat sink design to set the T_J considering two cooling system opportunities under different load case (LC)s to the loss-saving temperature window.

The fuel cell-powered cryogenic drive train concept for a blended wing body (BWB) long-distance aircraft can offer some improvements regarding CO_2, NO_x and noise reduction. Moreover, it also can improve the efficiency chain from production-to-thrust. Out of the mission profile combined with the Sustainable and Energy-Efficient Aviation (SE^2A) BWB long-distance aircraft design, the cryogenic power train must deliver a P_{Shaft} of 5.4 MW per drive unit. Additionally, a finite element method (FEM)-based analysis characterises the influence of the current ripple on the hysteresis loss per cycle (Q) of the superconducting material inside the superconducting machine. The transport losses (P_{trans}) can be reduced by the factor of 10 by increasing the f_{PWM} of the power electronic inverter. Two possible cooling concepts are available. The losses of the direct current (DC) backbone, the electrical machine and the electronic power heat the stored LH_2 to the desired fuel cell system temperature partially. A direct cooling approach uses gaseous H_2, and the indirect cooling concept with a secondary circuit is based on helium (He). The suggested drive train concept would be only feasible if the fuel cell's efficiency, temperature and power density increase. Especially the fuel cell system cooling is challenging under an aircraft's laminar flow condition. However, the available H_2 mass flow ($\dot{m}_{\text{H2}}$), the cooling concept

and the semiconductor's behaviour under cryogenic conditions define essential design inputs for the power electronic heat sink design. The experimental investigations show that silicon (Si) and gallium nitride (GaN) offer advantages under deep temperatures. In particular, GaN has no so-called carrier freeze-out and can be used for He temperatures. However, the breakdown voltage (V_{Break}) of GaN devices is currently limited. It is possible that GaN can also handle enormous powers by blocking high voltage (HV) and conducting enormous currents in the future. Si-insulated gate bipolar transistor (IGBT) and superconjuction metal-oxide-semiconductor field-effect transistor (MOSFET) show improvements to 77 K. Under 77 K, carrier-freeze out sets in. For IGBTs, the improvements do not reach the technical possibilities in switching energy reduction of SiC. In particular, high f_{PWM}s are required to reduce THD. Therefore, the magnetisation losses (P_{mag}) and P_{trans} of the superconductor are reduced. The blocking voltage of Si-MOSFETs is limited. Only silicon carbide (SiC) possesses the properties to achieve high power with high f_{PWM}s. In our investigation, the frequency-dependent power losses ($P_{\mathrm{L,S}}$) dominate in 6.5 kV-blocking SiC-MOSFETs, and the optimal T_{J} is about 200 K to 300 K. A slight reduction of E_{off} in experimental data is noticeable. A scalable inverter model uses the measured and referenced semiconductor data to determine the loss-reducing T_{J} under specified LCs. This scalable inverter model uses data from a HV blocking SiC semiconductor with temperature-dependent loss calculations. A T_{J} range from 200 K to 300 K acts loss-reducing because the $P_{\mathrm{L,S}}$ of the SiC inverter dominate the overall losses. Out of the desired temperature window (200 K to 300 K), a heat sink design for both cooling system considerations can be calculated by analytical equations. An analytical optimisations of different direct cooling designs via gaseous H_2 out of the electrical machine analyses the difficulties of fulfilling all analysed LCs out of the mission profile. The suggested heat sink design uses the non-linear dependency of cooling capacity on the $\dot{m}_{\mathrm{H2}}$ to lift the T_{J} to the specified temperature window under different LCs. Only LC4 is out of the desired temperature window, but the power losses per inverter ($P_{\mathrm{L,Inv}}$) are minimal and not critical. Furthermore, the indirect cooling for the power electronic inverter is analysed. The calculations consider the secondary He cooling circuit. The desired temperature window of the SiC inverter (200 K to 300 K) is so high that a reverse brayton cycle cryocoolers (RBCC) arrangement is unnecessary. Only a fan sets the corresponding $\dot{m}_{\mathrm{He}}$. Moreover, a light-weight laser-welded heat exchanger concept to the H_2 is presented. The indirect cooling concept uses the same strategy to lift temperature to the desired temperature level as the direct approach. Both cooling considerations are compared by considering the main parts of each concept. The weight difference between power electronic's direct and indirect cooling concepts is not a criterion for exclusion. Additionally, indirect cooling offers a higher system safety.

A high switching power electronic is more of a technology enabler than a bottleneck, but many challenges must be clarified in the future. For both considered cooling concepts, the power electronic inverter for a cryogenic drive train for a long-distance aircraft is feasible.

Holistic multi-parameter system optimisation in future studies must define the best overall parameter set to reach high power densities. This article indicates and discusses many optimisation parameters. Moreover, the development of vertical GaN structures enables direct cryogenically-cooled HV power electronics. Thus, thermal interfacing problems could be solved. GaN semiconductor material investigations require a closed-loop He testbed to reach temperatures smaller than 77 K.

AUTHORS CONTRIBUTION

Hendrik Schefer: Power Electronic Investigations, Writing, Editorial, Review; Wolf-Rüdiger Canders: Cooling Design, Writing, Review; Jan Hoffman: Discussion on Superconducting Machines; Regine Mallwitz and Markus Henke: Review, Supervision.

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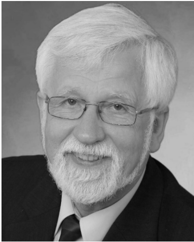

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