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RESEARCH ARTICLE

Accurate Characterization for Continuous-Time Linear Equalization in CMOS Optical Receivers

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ABSTRACT Recently published CMOS optical receivers consist of a limited-bandwidth first-stage transimpedance amplifier (TIA) followed by an equalizer. Limiting the TIA's bandwidth improves the gain and reduces the noise but introduces a significant inter-symbol interference (ISI) that is dealt with by the subsequent equalizer. Continuous-time linear equalizer (CTLE) is a commonly used equalizer in both electrical and optical links. However, recent research reported different findings about CTLE-based optical receivers. Some research papers concluded that CTLEs boost high-frequency noise compared to a full-bandwidth design. Other publications reported that high-frequency noise remains unaffected while white noise is significantly reduced. This work aims to solve this discrepancy by presenting an accurate analysis for CTLE-based optical receivers considering noise, gain, and jitter. We show that the noise performance depends on the pole/zero locations of the limited-bandwidth (LBW)-TIA and the follow-on equalizer. A properly designed CTLE-based receiver achieves a 2.5× higher gain and a 1.74× better noise than the full-bandwidth design. The CTLE is also compared to the well-known decision feedback equalizer (DFE). The noise performance of the CTLE-based receiver lies between that of finite and infinite impulse response DFE-based receivers but achieves better gain than both architectures.

INDEX TERMS Optical receiver, equalizer, transimpedance amplifier, noise, jitter.

I. INTRODUCTION

The increasing demand for bandwidth-intense services such as social networks, online high-definition video streaming, video conferences, online games, mobile internet, and cloud-based storage has caused an exponential growth in internet traffic. Consequently, electrical interconnects in data centers are being replaced by optical interconnects as the former suffer from crosstalk and frequency-dependent losses that increase with speed and distance. In optical links, the transmitted optical modulation amplitude (OMA) must be sufficiently large that despite coupling and fiber losses, the received optical power exceeds the receiver's sensitivity limit. Therefore, receiver sensitivity is a crucial performance metric. However, the design of high-sensitivity optical receivers in scaled CMOS technologies is challenging due to smaller intrinsic gain and more noise compared to SiGe BiCMOS technologies [1], [2].Traditionally, receiver front ends (FEs) are designed with wide bandwidth to support higher data rates. This wide bandwidth directly trades off with the transimpedance gain of the FE [1], [2], [3]. To relax this trade-off, optical receivers with intentionally reduced bandwidth are becoming commonplace. Reducing the bandwidth of the first stage transimpedance amplifier (f_{TIA}) to less than half the targeted data rate improves both gain and noise performance. However, the reduced f_{TIA} introduces inter-symbol interference (ISI) which closes the output eye diagram. Therefore, ISI must be dealt with by a subsequent equalization. Linear and non-linear equalization approaches have been recently used to remove ISI [4], [5],

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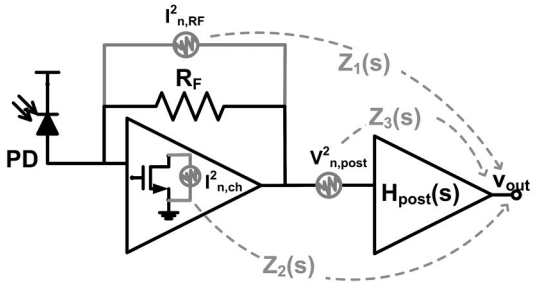

FIGURE 1. General block diagram for all receiver front ends with noise sources and noise transfer functions indicated.

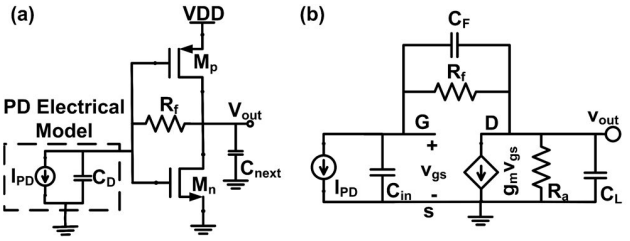

FIGURE 2. Inverter-based TIA (a) circuitry (b) small-signal model.

[6], [7], [8], [9], [10]. Non-linear techniques such as decision feedback equalizers (DFEs) noiselessly remove the ISI but suffer from a timing constraint that limits their speed and increases design complexity at high data rates [4], [5], [6]. Linear approaches such as continuous-time linear equalizers (CTLE) and feedforward equalizers (FFEs), on the other hand, do not suffer from time constraints but significantly impact the noise [7], [8], [9], [10].

Several publications have studied the impact of linear equalization on the noise performance of optical receivers [4], [9], [10], [11], [12]. For example, the analysis in [4] claims that CTLEs boost high-frequency noise. The same claim is also made in [12] for FFEs. In contrast, the study in [9] and [11] suggests that colored noise remains the same while white noise significantly reduces compared to the full-bandwidth design. This paper aims to solve this discrepancy by identifying the conditions that make linear-equalizer-based receivers achieve either better, worse, or the same noise performance as the classical full-bandwidth design and intuitively explain this performance. This paper focuses on continuous-time linear equalizer (CTLE)-based receivers, but the presented methodology also applies to FFE-based receivers.

The rest of this paper is organized as follows: Section II presents the methodology of noise calculation. The conventional full-bandwidth receiver that is used as a reference design for comparison is discussed in Section III. Section IV considers several designs for CTLE-based receivers and compares their performance with the reference design. Section V discusses the role of the CTLE in electrical and optical links and compares CTLE-based with DFE-based optical receivers. Finally, Section VI concludes the work.

II. METHODOLOGY OF NOISE CALCULATION

FIGURE 1 shows a generalized block diagram for all front-end used in this work. The block diagram in FIGURE 1 consists of a shunt-feedback (SF) transimpedance amplifier (TIA) and a subsequent stage $H_{post}(s)$. The SF-TIA is either operated in the full-bandwidth (FBW) mode or in the limited-bandwidth (LBW) mode. $H_{post}(s)$ is realized by a buffer, a main amplifier (MA), or an equalizer, depending on the mode of operation. This section presents a generalized analysis that applies to both the conventional and the equalizer-based receivers.

A. SHUNT-FEEDBACK TRANSIMPEDANCE AMPLIFIER

The SF-TIA exhibits superior noise performance and can operate with a smaller voltage supply compared to the well-known common-gate (CG)-TIA. Therefore, the SF-TIA has become the dominant topology in advanced CMOS technologies. The SF-TIA is extensively employed in recent research where it is operated either in the FBW mode followed by a multi-stage main amplifier [13], [14], [15], [16] or in the LBW mode followed by an equalizer [4], [9], [17], [18]. The CMOS-inverter-based (Inv)-TIA in FIGURE 2(a) is the most common implementation of the SF-TIA thanks to its high transconductance resulting from current reuse, high intrinsic gain even in scaled CMOS technology, and its ease of design. The small-signal model of the Inv-TIA is shown in FIGURE 2(b). In the model, C_{in} is the sum of gate-to-source capacitance C_{GS}, photodiode capacitance C_D, and pad capacitance C_{pad}, respectively. C_F is the gate-to-drain capacitance C_{GD}. C_L is the sum of the drain-to-bulk capacitance C_{DB} and the loading capacitance from the subsequent stage C_{next}. $g_{m,tia}$ and R_a are the combined output resistance and transconductance of the NMOS and the PMOS. R_f is the feedback resistor. Considering this model, the Inv-TIA exhibits a second-order transfer function $Z_{TIA}(s)$ that is characterized by a low-frequency gain of $R_{TIA,0}$, an oscillation frequency ω_{TIA}, and a pole quality factor Q_{TIA} that can be written in circuit parameters as

$$R_{TIA,0} = -\frac{g_{m,tia}R_a}{1+A_0}R_f \tag{1.a}$$

$$\omega_{TIA}^2 = \frac{1+g_{m,tia}R_a}{R_fR_a\left(C_FC_L+C_{in}C_L+C_FC_{in}\right)} \tag{1.b}$$

$$Q_{TIA} = \frac{\sqrt{R_fR_a\left(1+g_{m,tia}R_a\right)\left(C_FC_L+C_{in}C_L+C_FC_{in}\right)}}{R_fC_F\left(1+g_{m,tia}R_a\right)+R_aC_L+\left(R_f+R_a\right)C_{in}} \tag{1.c}$$

Several parameters in this model are coupled. For example, $g_{m,tia}$, C_{GS}, and C_{GD} are coupled by the technology transient frequency, f_T. Also, R_a and $g_{m,tia}$ are coupled by the gain $A_0 = g_{m,tia}R_a$. It should be noted that f_T and A_0 are fixed for a given technology, aspect ratio, and biasing condition. Table 1 summarizes initial values, bounds, and the relationships between coupled parameters. The design space

TABLE 1. TIA's parameters.

Parameter	Description	Values and Bounds	Comment
f_{bit}	Data rate	25 Gb/s	
f_T	Transit frequency at the selected biasing.	$5 \times f_{bit}$	Based on simulation in TSMC-65 nm. The Inv-TIA is biased at $V_{DD}/2$.
A_0	Inverter DC gain	6 V/V	
$g_{m,tia}$	Combined transconductance	10 mS-100 mS	Design variable
R_a	TIA output resistance	$A_0/g_{m,tia}$	
f_A	Core-amplifier's open-loop pole	$\frac{1}{(2\pi R_a C_L)}$	
R_f	Feedback resistor	10 Ω-5 kΩ	Design variable
C_g	Total gate capacitance	$g_m/(2\pi f_T)$	
C_{gs}	gate-to-source capacitance	$4C_g/5$	Based on simulation in TSMC-65 nm
C_{gd}	gate-to-drain capacitance	$C_g/5$	
C_{PD}	Photodiode capacitance	60 fF	
C_{PAD}	Pad capacitance	40 fF	
C_{next}	Input capacitance of the next stage	25 fF	

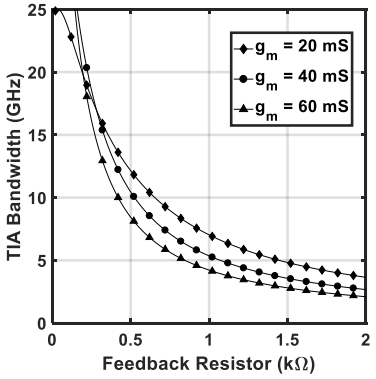

FIGURE 3. TIA's 3dB bandwidth as a function of the feedback resistor for various values of the transconductance.

is now defined by $g_{m,tia}$ and R_f which are swept to plot the TIA's 3 dB bandwidth as shown in FIGURE 3. The plot shows that for a given bandwidth, R_f needs to be reduced toward large $g_{m,tia}$. For a given $g_{m,tia}$ (and hence a give power dissipation), the bandwidth drops toward larger R_f (*i.e.*, larger gain). The gain-bandwidth trade-off is further investigated in Section IV to find the optimal TIA's bandwidth considering both noise, ISI, and jitter.

B. NOISE ANALYSIS

The main noise sources are depicted in FIGURE 1. The TIA's channel and feedback thermal noise sources are shown in FIGURE 1 as $I^2_{n,ch}$ and $I^2_{n,RF}$, respectively. The power spectral densities (PSDs) of these two sources are expressed as: $I^2_{n,ch} = 4kT\gamma g_{m,tia}$ and $I^2_{n,RF} = 4kT/R_f$, where γ, T, and k are the excess noise factor, temperature in Kelvin, Boltzmann constant, respectively. The subsequent stage has an input-referred noise PSD of $V^2_{n,post} = 4kT/g_{m,post}$, where $g_{m,post}$ is the transconductances of the input devices. Each noise source sees a *different* transfer function to the output as indicated in FIGURE 1 by $Z_1(f)$, $Z_2(f)$, and $Z_3(f)$. Therefore, the output squared noise is expressed as

$$V^2_{n,Rf} = I^2_{n,Rf} \int_0^\infty |Z_1(f)|^2 \, df \tag{2.a}$$

$$V^2_{n,ch} = I^2_{n,ch} \int_0^\infty |Z_2(f)|^2 \, df \tag{2.b}$$

$$V^2_{n,post,out} = V^2_{n,post} \int_0^\infty |Z_3(f)|^2 \, df \tag{2.c}$$

where, $V^2_{n,Rf}$, $V^2_{n,Rf}$, and $V^2_{n,Rf}$ are the output noise power in (V^2) due to the feedback resistor, channel, and the subsequent stage, respectively. These analyses are explained as follows: the noise from R_f directly referrers to the input so that it is amplified to the output through the transfer function of the overall FE $Z_1(f) = Z_{TIA}(f)\, H_{post}(f)$. The channel noise $I^2_{n,ch}$ is first converted into voltage by the output impedance of the TIA $Z_{out}(f)$, then amplifier to the output through $H_{post}(f)$, leading to $Z_2(f) = Z_{out}(f)\, H_{post}(f)$. The input-referred noise voltage of the subsequent stage is amplified to the output by its transfer function. That is, $Z_3(f) = H_{post}(f)$. The input-referred noise power in (A^2) is calculated by refereeing the output noise power to the receiver's input by an appropriate gain.

C. INPUT-REFERRAL GAIN

The output noise power can be referred to the input by the midband value of the front-end's amplitude response $Z_{FE,0} = Z_{TIA}(0)\, H_{post}(0)$ only if the FE's bandwidth is sufficiently wide to introduce a negligible ISI. When the FE's bandwidth is reduced relative to the data rate, the signal sees a gain of less than $Z_{FE,0}$ due to the closure in the output eye diagram caused by the ISI. Therefore, the output noise needs to be referred to the input by the same gain seen by the signal to attain equal output and input signal-to-noise ratios (SNRs) [11], [19]. That is,

$$SNR_{out} = \frac{V^2_{signal}}{V^2_n} = \frac{i^2_{pp} \times gain^2}{V^2_n} = \frac{i^2_{pp}}{V^2_n/gain^2} = \frac{i^2_{pp}}{i^2_n} = SNR_{in} \tag{3}$$

where i_{pp} is the peak-to-peak value of the input current pulse. V^2_n and i^2_n are total output noise power and the total input noise power, respectively. The "*gain*" in (3) is the effective gain calculated from the pulse response of the *overall* FE [11]. In FIGURE 4, the FE's response to an input pulse $r(t)$ is

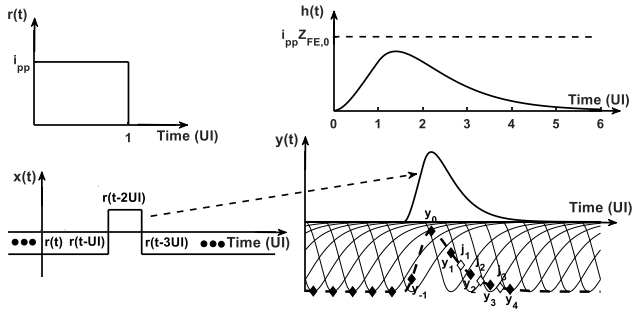

FIGURE 4. Pulse response analysis for effective gain and jitter calculation.

$h(t)$. The input current pulse is characterized by a peak-to-peak value of i_{pp} and a width of a unit interval UI, where $UI = 1/f_{bit}$. Due to bandwidth limitations, $h(t)$ cannot settle at $i_{pp}Z_{FE,0}$. $h(t)$ also lasts for several UIs, causing interference with neighboring pulses. The signal $x(t)$ is an isolated binary one transmitted in a sea of binary zeros. Assuming a linear time-invariant (LTI) operation, $y(t)$ shows the FE's response to the signal $x(t)$. $y(t)$ is called the pulse response and is formed by superimposing, in time, the FE response for each bit in the sequence $x(t)$.

The ISI is quantified by sampling $y(t)$ at the rising edges of a baud rate clock relative to its peak (filled marker points).

This results in a discrete-time sequence $V_{y,m}$ given by $V_{y,m} = y(mT_b)$ for m ranging from $-\infty$ to $+\infty$. The sample at $m = 0$ (*i.e.,* at the peak of the pulse) is denoted as the main cursor sample $V_{y,0}$. The ISI samples $\left(V_{y,m\neq 0}\right)$ are destructively added to $V_{y,0}$, closing the vertical eye opening (VEO) to

$$VEO = V_{y,0} - \sum_{\substack{m=-\infty \\ m\neq 0}}^{\infty} \left|V_{y,m}\right| \tag{4}$$

An effective gain can be calculated from this VEO as $Z_{eff} = VEO/i_{pp}$. This gain is used in noise calculations when the ISI is not eliminated or is only partially eliminated. Therefore, input-referred noise powers due to the feedback resistor, channel, and the subsequent stage are calculated as $i^2_{n,Rf} = V^2_{n,Rf}/Z^2_{eff}$, $i^2_{n,ch} = V^2_{n,ch}/Z^2_{eff}$, and $i^2_{n,post} = V^2_{n,post,out}/Z^2_{eff}$, respectively. All noise sources are uncorrelated. Therefore, the total input noise power, i^2_n, is the sum of noise powers from all individual contributors.

$$i^2_n = i^2_{n,Rf} + i^2_{n,ch} + i^2_{n,post} \tag{5}$$

The rms input-referred noise, $i_{n,rms}$, is the square-root of i^2_n. This methodology of noise calculation, first, accounts for how the stage following the TIA processes the noise of each contributor. Second, the methodology accounts for the residual ISI in the effective gain calculation which is normally less than the low-frequency gain. In the following sections, this methodology is used to explore the noise performance of various receiver architectures. In simulations that follow f_{bit}, i_{pp}, $g_{m,post}$, and γ are fixed at 25Gb/s, 10 μA_{pp}, 10mΩ^{-1}, and 2, respectively.

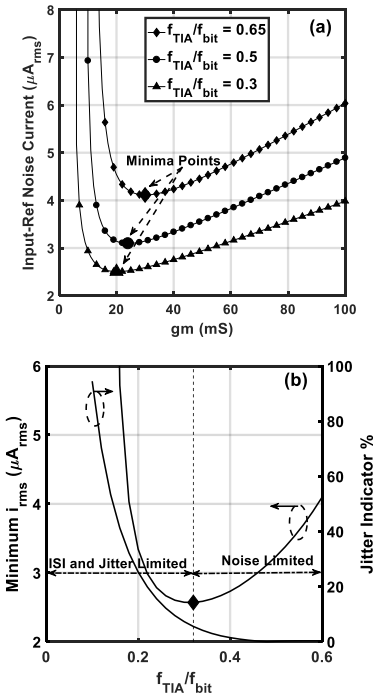

FIGURE 5. Performance of the FBW FE with buffer (a) the input-referred current for various values of f_{TIA}/f_{bit} (b) Minimum i_{rms} and JI as a function of f_{TIA}/f_{bit}.

D. JITTER

Jitter is defined as the deviation of zero-crossing points of the data from their ideal position in time. These points are aligned with falling edges of the clock. Therefore, the output pulse $y(t)$ in FIGURE 4 is also sampled at the falling edges of a baud rate clock relative to its peak (hollow marker points). The sum of the magnitude of these samples relative to the pulse peak is considered a jitter indicator (JI). The defined JI accounts only for the deterministic jitter caused by ringing in the time domain or residual ISI [20].

III. REFERENCE FULL-BANDWIDTH DESIGN

To assess the performance of CTLE-based receivers, it must be related to a reference design point of the conventional design approach.

A. FULL-BANDWIDTH FE WITH BUFFER

In this front-end, $H_{post}(s)$ is implemented by a unity gain infinite bandwidth buffer. $i_{n,rms}$ of this FE is shown in FIGURE 5(a) for various values of f_{TIA}/f_{bit}. f_{TIA} is varied by sweeping $g_{m,tia}$ and R_f. The minima points in

FIGURE 5 (a) are extracted and plotted along with the jitter indicator (JI) in FIGURE 5(b) as a function of f_{TIA}/f_{bit}. The noise reaches a minimum value of 2.5 μA_{rms} at $f_{TIA} = 0.32 f_{bit}$. The JI at this point is only 5.5%. Further reducing f_{TIA} below the optimal value results in ISI and jitter that degrade the noise due to the reduced effective gain. A larger than optimal f_{TIA} increases the output-referred integrated noise voltage also degrading the noise. Frontend

TABLE 2. Front-end summary for optimal noise performance.

f_{bit} = 25 Gb/s	Full-Bandwidth FE		Limited-Bandwidth FE		
	With Buffer **(Reference design)**	With MA	Complex-zero CTLE: case 1	Complex-zero CTLE: case 2	Single-zero CTLE **(Best performance)**
Transconductance	$g_{m,tia}$ = 20 mS and $g_{m,post}$ = 10 mS Both are fixed for fair noise comparison under a constant power dissipation constraint.				
Bandwidth allocation	$f_{TIA} = 0.32 \times f_{bit}$ $f_{buffer} = \infty$ $f_{FE} = 0.32 \times f_{bit}$	$f_{TIA} = 0.32 \times f_{bit}$ $f_{MA} = 0.67 \times f_{bit}$ $f_{FE} = 0.31 \times f_{bit}$	$f_{TIA} = 0.16 \times f_{bit}$ $f_{FE} = 0.32 \times f_{bit}$	$f_{TIA} = 0.16 \times f_{bit}$ $f_{FE} = 0.41 \times f_{bit}$	$f_{TIA} = 0.16 \times f_{bit}$ $f_{FE} = 0.43 \times f_{bit}$
R_f (kΩ)	0.861	0.861	1.809	1.809	1.809
Q_{TIA}	0.505	0.505	0.402	0.402	0.402
JI	5.5 %	4.8 %	5.56 %	4.8 %	
Effective Gain (kΩ)	0.455	1.137	0.987	1.126	1.153
$i_{n,rms}$ (μA_{rms})	2.57	1.68	2.42	1.85	1.474
$i^2_{n,Rf}$ (A^2/Hz)	4.3615e-13	5.5721e-13	2.0766e-13	1.8661e-13	1.8122e-13
$i^2_{n,ch}$ (A^2/Hz)	3.6276e-12	1.8440e-12	3.3637e-12	2.2071e-12	1.6622e-12
$i^2_{n,post}$ (A^2/Hz)	2.5413e-12	4.3027e-13	2.2851e-12	1.0340e-12	3.2938e-13

parameters for optimal noise performance (bold marker point in FIGURE 5(b)) are summarized in Table 2 and the design at this point is considered a reference design for follow-on comparisons.

Conventionally, best receiver sensitivity is achieved when the FE exhibits a Butterworth response and a bandwidth of $2f_{bit}/3$ (Section 4.6 in [21]). However, FIGURE 5(b) and Table 2 show that, even with no equalization, optimal noise performance is achieved at f_{TIA} and Q_{TIA} of $0.32f_{bit}$ and 0.505, repectivelly. The lower f_{TIA} is justified as follows: the noise model in [21] considers only the white noise component while our model accounts for the colored noise, which pushes the noise-optimum bandwidth to a lower frequency to filter out more high-frequency noise. The lower $\boldsymbol{Q_{TIA}}$ is resulted from the limited gain in the TIA's core amplifier (this statement is further justified in Section IV.A).

B. FULL-BANDWIDTH FE WITH MAIN AMPLIFIER

In this design, the FBW TIA is followed by a single-stage main amplifier with a second-order Butterworth transfer function given by [22]

$$H_{post}(s) = A_{MA}(s) = \frac{A_{MA,0}}{\left(\frac{s}{2\pi f_{MA}}\right)^2 + \frac{\sqrt{2}\,s}{2\pi f_{MA}} + 1} \tag{6}$$

where $\boldsymbol{A_{MA,0}}$ and $\boldsymbol{f_{MA}}$ are the DC gain and the 3 dB bandwidth of the MA. It is assumed that the MA exhibits a gain-bandwidth product of $\boldsymbol{2f_{bit}}$, which is realizable in technology with $\boldsymbol{f_T = 5f_{bit}}$, as indicated in Table 1. The MA's bandwidth is made relatively wide so that the receiver's bandwidth is approximately set by the TIA [21]. In FIGURE 6, $\boldsymbol{f_{MA}}$ is swept to plot the input-referred noise and the JI while TIA's parameters are fixed as in the reference design in Table 2. The noise reaches a minimum value of $\boldsymbol{1.68\mu A_{rms}}$ at $\boldsymbol{f_{MA} = 0.66f_{bit}}$, leading to an overall bandwidth of $\boldsymbol{0.31f_{bit}}$. The JI at this point is only $\boldsymbol{4.8\%}$. In comparison to the FBW with buffer, the deployment of the MA increases the order of the noise transfer functions

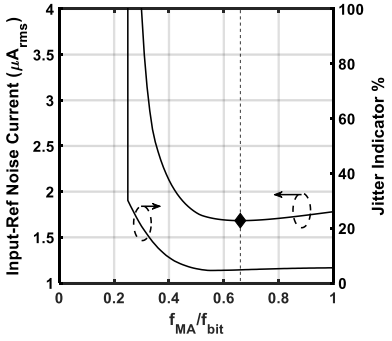

FIGURE 6. Performance of the FBW FE with a main amplifier. TIA's parameters are fixed as in the reference design.

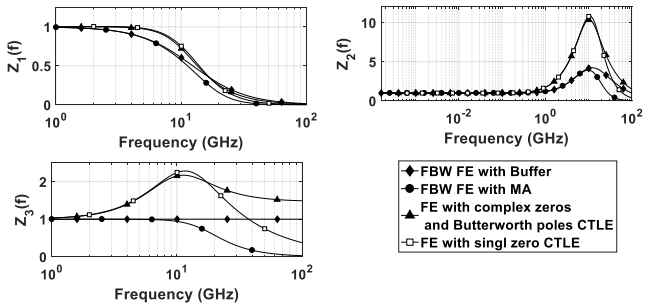

FIGURE 7. Comparison of normalized noise transfer functions.

which filters out more high-frequency noise as shown in FIGURE 7. However, this FE exhibits a smaller $\boldsymbol{f_{FE}/f_{bit}}$ which increases the ISI and reduces the ratio of the effective gain to the DC gain. Combining these two effects, the noise contributions from the channel and MA are reduced while the noise contribution of $\boldsymbol{R_f}$ slightly increases compared to their counterparties in FBW-FE with buffer (see Table 2).

IV. EQUALIZER-BASED FRONT-END

A continuous-time linear equalizer (CTLE) implements a frequency-dependent gain to introduce a high-frequency boost that compensates for the limited-bandwidth

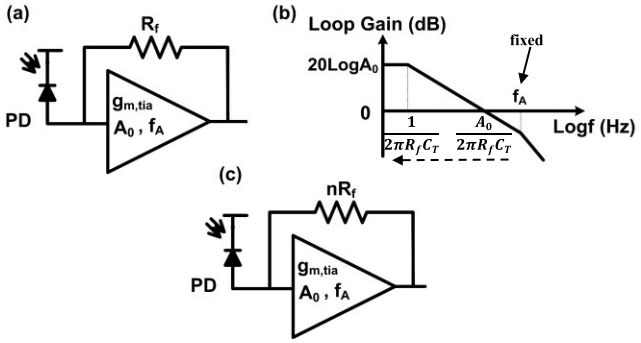

FIGURE 8. Shunt-feedback TIA (a) FBW design, (b) open-loop dynamics, and (c) LBW design.

(LBW)-TIA's high-frequency roll-off. The CTLE can be realized by source degeneration [23], passive [9] or active inductive load [10], or passive network [24]. It can also be realized by continuous-time delay cells [8]. In this work, we consider a general transfer function that can model all different implementations. Equalizer parameters are determined to extend the bandwidth and achieve the best possible noise performance while maintaining a JI of less than 10 %. This JI percentage is arbitrarily chosen and can be changed according to the priority given to the horizontal eye-opening and jitter. This section first discusses the design of the LBW-TIA, then explores several designs for the equalizer.

A. LIMITED-BANDWIDTH TIA

In the LBW-TIA, the bandwidth is shrunk by a factor n compared to that of the FBW-TIA. This is achieved by increasing R_f while fixing $g_{m,tia}$ which allows for a fair noise comparison under a constant power dissipation constraint. For example, in FIGURE 3, when $g_{m,tia}$ is fixed at 20 mS, f_{TIA} is reduced from $f_{TIA} = 0.32 f_{bit} = 8$GHz to $f_{TIA} = 0.16 f_{bit} =$ 4GHz (*i.e.*, $n = 2$) by increasing R_f from 0.861 Ω to 1.82 kΩ.

The feedback resistor is boosted by a factor of 2.11×, approximately equal to the bandwidth shrinkage factor n, indicating a near-linear proportionality between the gain and the bandwidth. This is in contrast to the square-law relation predicted by the transimpedance limit (TL) in [1], [3], and [9]. This is explained as follows: the TL is the maximum gain that can be reached for a given bandwidth and technology. The TL is reached when the TIA exhibits a Butterworth response. However, as R_f increases, the input open-loop pole becomes more dominant compared to the core amplifier's pole f_A (note that once $g_{m,tia}$ is fixed f_A is also fixed) as shown in FIGURE 8(b). As a result, the TIA exhibits a response with Q_{TIA} of less than $1/\sqrt{2}$. The oscillation frequency ω_{TIA} is converted to the corresponding 3 dB bandwidth through a factor $\rho = \sqrt{\sqrt{\left(1 - 1/2Q_{TIA}^2\right)^2 + 1} + \left(1 - 1/2Q_{TIA}^2\right)}$ [3]. Simulation results show that ρ is proportional to $R_f^{-0.5}$. Therefore, the transimpedance limit from [3] can be rewritten as

$$R_f = \frac{(A_0 + 1)}{A_0} \frac{A_0 f_A \rho^2}{2\pi f_{TIA}^2 C_T} \tag{7.a}$$

which implies

$$R_f^2 \sim \frac{1}{f_{TIA}^2} \rightarrow R_f \sim \frac{1}{f_{TIA}} \tag{7.b}$$

This proves that *actual* gain does not reach TL and drops linearly with the bandwidth. This linear relation between the gain and the bandwidth facilities the design of the equalizer but reduces R_f boosting factor to n, instead of n^2 as in [9] which follows the theoretical transimpedance limit. To reach the TL (*i.e.,* to boost R_f by n^2) when the bandwidth is shrunk by a factor n, A_0 and f_A need to be scaled up and down by a factor of n, respectively, to attain a fixed $Q_{TIA} = 1/\sqrt{2}$. Practically, this approach is not realizable since the A_0 of a single-stage CMOS inverter is constant for a given biasing and aspect ratio. Furter, the maximum value of A_0 is limited by the technology node. A cascode transistor is used in [9], [10], and [23] to boost A_0. However, the cascode device becomes the dominant noise contributor at high frequency [23]. In this work, cascode transistors are ruled out to constrain the problem.

An equalizer restores the bandwidth to a finite degree. That is, excessive scaling of the LBW-TIA bandwidth (*i.e.,* large n) requires a large amount of equalizer peaking, increasing gain ripple and group delay variation. This translates to time-domain ringing and jitter which reduces the effective gain and may cancel out noise improvement resulting from limiting the TIA's bandwidth. Further, an equalizer working at its limit suffers from a limited tunability which makes the circuit susceptible to process, temperature, and voltage (PVT) variations [1], [9]. Considering these practical limitations, n is fixed at 2 in the following simulations. The design of the LBW-TIA is summarized in FIGURE 8 (c) in comparison to the FBW-TIA.

B. COMPLEX-ZERO EQUALIZER

In this design, we consider a unity low-frequency gain equalizer that introduces a pair of complex zeros that perfectly match the bandwidth-limiting poles of the LBW-TIA and a pair of complex poles. Two cases for the equalizer's poles are considered as follows:

1) CASE 1) CTLE WITH COMPLEX POLES THAT MATCH THOSE OF THE FBW-TIA

The overall FE (LBW-TIA/CTLE) in this design exhibits a second-order amplitude response characterized by the dc gain of the LBW-TIA and the poles of the FBW-TIA. This case is considered for the sake of comparison with reference works [9], [11]. The noise reaches a minimum value of 2.42 μA_{rms} at $f_{FE} = 0.32 f_{bit}$. The JI at this point is only 5.56%. Compared to FBW-FE with buffer: 1) The equalizer restores the bandwidth by a factor n. As a result, the effective gain improves by a factor of 2.17×, approximately equal to the

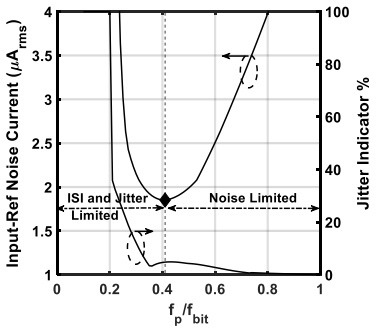

FIGURE 9. Noise performance of the CTLE-based FE where the equalizer introduces a pair of complex zeros that perfectly match the bandwidth-limiting poles of the LBW-TIA and a pair of Butterworth poles at $2\pi f_p$.

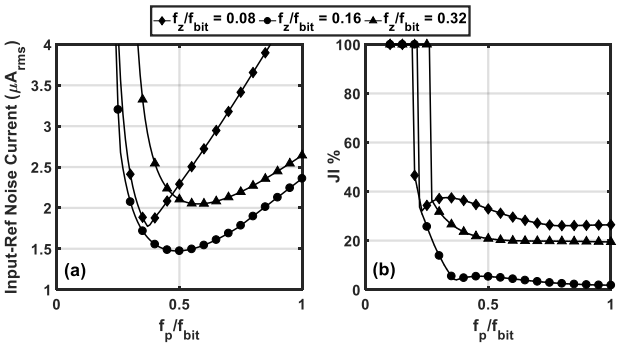

FIGURE 10. Noise performance of the CTLE-based FE where the equalizer introduces a single zero and a pair of Butterworth poles at $2\pi f_z$ and $2\pi f_p$, receptively.

bandwidth shrinkage factor n as explained in Section IV.A. 2) the noise from the feedback resistor sees an identical transfer function $Z_1(f)$ to the output but is referred to the input by a higher effective gain. Therefore, $i^2_{n,Rf}$ improves by a factor of $2.1\times(\cong n)$ as indicated in Table 2. 3) the equalizer introduces a high-frequency boost in the noise transfer functions $Z_2(f)$ and $Z_3(f)$, integrating more noise at the output. However, this is counteracted by the higher effective gain, leading to almost identical input-referred noise powers for both the channel and the subsequent stage.

These conclusions coincide with [9] and [11] where colored noise is unchanged while the feedback noise improves by a factor equals to the gain boosting factor (which is n in this work compared to n^2 in [9]). Despite the improvement in the white noise, $i_{n,rms}$ improves only by 8 % since the total noise is dominated by colored noise. The deployment of the equalizer restores as wide horizontal eye-opening as in the fbw-fe with buffer as evident by the equal JIS (5.56%.) in both front ends.

2) CASE 2) CTLE WITH BUTTERWORTH POLES

The overall FE (LBW-TIA/CTLE) in this design exhibits a second-order transfer function defined by the DC gain of the LBW-TIA and a pair of Butterworth poles at $2\pi f_p$. Therefore, the FE exhibits an overall bandwidth of $f_{FE} = f_p$. FIGURE 9 shows that the noise of this FE reaches a minimum value of 1.85 μA_{rms} at $f_p = 0.41 f_{bit}$ which coincides with [6] on the noise-optimum bandwidth for a Butterworth TIA. The JI at this point is only 4.8%. The equalizer restores the bandwidth by a factor $>n$. As a result, this FE shows a wider bandwidth than the FBW-FE with buffer as shown by $Z_1(f)$ in FIGURE 7. The wider bandwidth improves the gain boosting factor beyond the bandwidth shrinkage factor n. The effective gain improves by a factor of 2.5×. On the other hand, the equalizer introduces a high-frequency boost in the noise transfer functions $Z_2(f)$ and $Z_3(f)$ as shown in FIGURE 7, integrating more noise at the output. Combining these two effects, the input-referred noise power due to all contributors and $i_{n,rms}$ are significantly improved as shown in Table 2.

C. SINGLE-ZERO EQUALIZER

Complex-zero equalizer is not common in optical receivers. Practically, a single-stage equalizer that introduces a single zero is usually employed. Therefore, in this design, we consider a unity low-frequency gain single-stage equalizer that introduces a single real zero and a pair of Butterworth poles at $z_{eq} = 2\pi f_z$ and $\omega_{eq} = 2\pi f_p$, respectively. The transfer function of the overall FE is given by

$$Z_{FE}(s) = \frac{R_{TIA,0}\left(1+\frac{s}{z_{eq}}\right)}{\left(\frac{s^2}{\omega_{TIA}^2}+\frac{s}{Q_{TIA}\omega_{TIA}}+1\right)\left(\frac{s^2}{\omega_{eq}^2}+\frac{\sqrt{2}\,s}{\omega_{eq}}+1\right)} \quad (8)$$

For this experiment, 100 values for f_z and 100 values for f_p in the range $0.1 f_{bit}$ to f_{bit} were chosen, resulting in a total of 10,000 design points. For all combinations, the noise and the JI are calculated, and a sample of the results is shown in FIGURE 10. The noise reaches a minimum value of 1.47 μA_{rms} when f_z and f_p are set to bandwidth of the LBW-TIA ($i.e., f_z = f_{TIA} = 0.16 f_{bit}$) and $0.49 f_{bit}$, respectively. This noise minimum occurs for an overall bandwidth of $f_{FE} = 0.43 f_{bit}$, meaning that the equalizer extended the bandwidth by a factor of 2.7×.

This FE achieves the best noise performance compared to all other FEs investigated so far. That is, this implementation increases the order of all noise transferer functions which filters out high-frequency noise. Moreover, the equalizer restores the bandwidth by a factor greater than the bandwidth shrinkage factor, further improving the effective gain. The input-referred power due to all contributors and $i_{n,rms}$ are significantly improved as shown in Table 2. The equalizer's transfer function shown by $Z_3(f)$ in FIGURE 7 indicates that the equalizer introduces a 7.1 dB of peaking (2.28×) at the Nyquist frequency $f_N = f_{bit}/2$ which is practically realizable [9].

This FE also achieves the highest effective gain of 1.15 kΩ. Therefore, a peak-to-peak voltage $V_O^{PP} = SNR i_{n,rms} Z_{eff} = 23.9\text{mV}_{pp}$ is produced at the output of the FE, where SNR is the required signal-to-noise ratio and equals 14.07 for bit-error-rate (BER) of 10^{-12}. This output is sufficiently large achieve the desired BER when the FE is followed

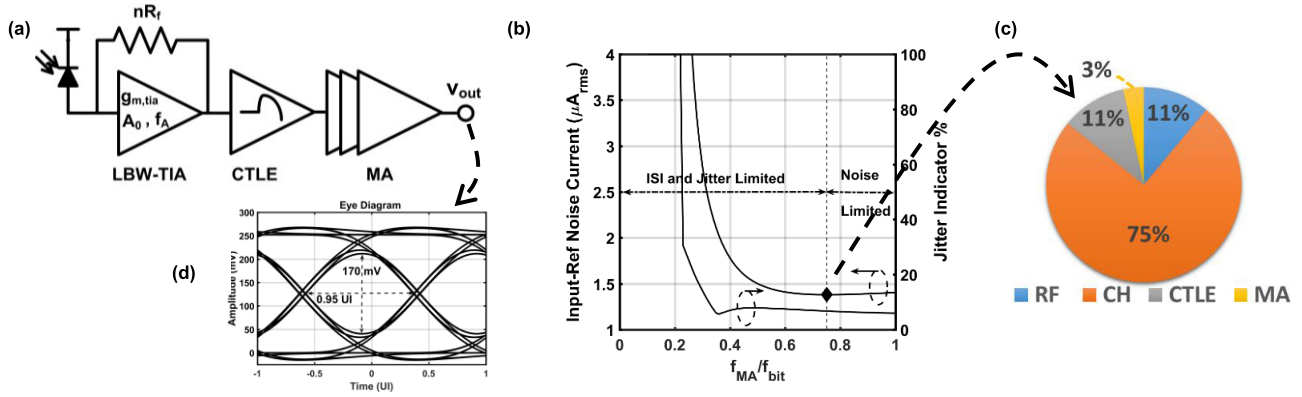

FIGURE 11. Front-end with LBW-TIA, CTLE, and MA (a) block diagram, (b) noise and jitter performance, (c) noise breakdown, and (d) 25 Gb/s eye diagram with input set at sensitivity level.

by an ideal clock-and-data recovery (CDR). Practically, the output voltage of the FE needs to be increased by swing requirements of an actual CDR, V_{CDR}^{PP} to attain the same BER as for the ideal CDR. The incurred power penalty due to finite sensitivity of the practical CDR is calculated as $PP = \left(V_O^{PP} + V_{CDR}^{PP}\right)/V_O^{PP}$. For example, a V_{CDR}^{PP} of 100 mV_{pp} incurs a PP of 7.14 dB. Next, we consider adding a main amplifier to mitigate this PP.

D. CTLE-BASED FRONT-END WITH A MAIN AMPLIFIER

So far, all noise comparisons are performed under a constant power dissipation constraint which requires fixing the number of stages. In this section, the number of stages is increased to mitigate the PP incurred by the voltage amplitude requirements of the CDR. In this FE, the LBW-TIA/CTLE in Section IV.C are followed by a three-stage MA. Each MA stage is described by (6). FIGURE 11 shows the block diagram and summarizes the results of this FE. The MA's per-stage bandwidth is swept to plot the noise and jitter as shown in FIGURE 11 (b). Compared to the FE in Section IV.C, employing the MA increases the effective gain to 2.75 kΩ and slightly improves $i_{n,rms}$ to 1.36 μA_{rms}. Therefore, the PP is reduced to 2.01 dB for $V_{CDR}^{PP} = 100\text{mV}_{\text{pp}}$. FIGURE 11 (b) shows that the noise reaches a minimum value when the MA's per-stage bandwidth is $0.97f_{bit}$,, leading to overall MA and front-end bandwidths of $0.69f_{bit}$, and $0.41f_{bit}$, respectively. The noise breakdown in FIGURE 11 (c) shows that the total input-referred noise power is dominated by the TIA's channel noise (75 %) while the MA's contribution to the input noise is negligible (only 3 %). The JI at the best noise point is only 7.3 %, indicating a wide horizontal eye-opening as evidenced by the simulated eye diagram in FIGURE 11 (d).

V. DISCUSSION

A. COMPARISON WITH DFE

FIGURE 12 (a) shows a general block diagram of a decision feedback equalizer (DFE)-based optical receiver. In principle, DFEs noiselessly cancel post-cursor ISI but not the precursor ISI. Referring to the pulse response in FIGURE 4, and

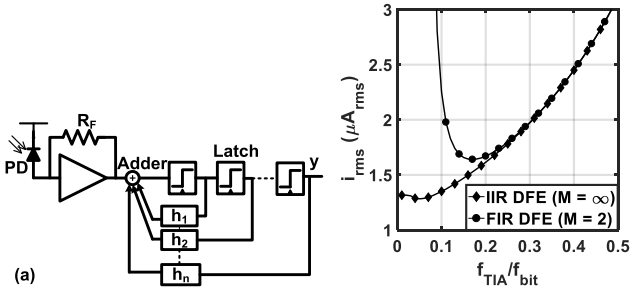

FIGURE 12. (a) Block diagram of a DFE-based optical receiver (b) Noise performance of IIR-DFE and two-tap FIR-DEF-based receivers.

considering an M-tap DFE, the vertical opening of the output eye diagram is calculated as

$$VEO_{DFE} = V_{y,0} - \sum_{m<0} |V_{y,m}| - \sum_{m>M}^{\infty} |V_{y,m}| \qquad (9)$$

Consequently, the effective gain of a DFE-based receiver is calculated as $Z_{eff,DFE} = VEO_{DFE}/i_{pp}$.

FIGURE 12 (b) shows the input-referred noise current of an infinite impulse response (IIR) and a two-tap finite impulse response (FIR) DFE-based receiver as a function of f_{TIA}/f_{bit}.

For the IIR-based receiver, the noise reaches a minimum value of 1.28 μA_{rms} at $f_{TIA} = 0.05f_{bit}$. Further reducing f_{TIA} below this optimal value results in a pre-cursor ISI that degrades the noise due to the reduced effective gain. At this point, the TIA employs a feedback resistor of 5.8 kΩ and achieves an effective gain of $Z_{eff,DFE} = 0.992\text{k}\Omega$. For the FIR case, the residual post-cursor ISI reduces the effective gain to 0.746kΩ which worsens the minimum $i_{n,rms}$ to 1.64 μA_{rms}. This noise minimum occurs at $f_{TIA} = 0.17f_{bit}$.

Compared to the CTLE-based FE in Section IV.C $\left(i_{n,rms} = 1.47\mu\text{A}_{\text{rms}}\right.$ and $\left.Z_{eff} = 1.153\text{k}\Omega\right)$, IIR-DFE-based FE achieves slightly better noise and lower effective gain. That is, IIR-DFEs noiselessly remove post-cursor ISI but have no bearing on the pulse height as seen at the output of the TIA. On the other hand, CTLEs restore a wide bandwidth which allows the pulse at the output of the FE (TIA/CTLE)

to settle at a higher level which improves the effective gain. The residual post-cursor ISI in the FIR-DFE-based receiver worsens the gain, resulting in a worse noise compared to the CTLE-based receiver. The higher gain in the CTLE-based front-end makes it more suitable for the cases where the swing requirements of the CDR incur a significant power penalty.

B. COMPARISON WITH ELECTRICAL LINKS

In electrical Links, CTLEs provide high-frequency peaking to mitigate signal distortion caused by channel loss. That is, the electrical channel acts as a low-pass filter with transfer function $\boldsymbol{G(f)}$. Therefore, the channel's effect on the pulses can be reversed by passing the received signal through a CTLE with a transfer function $\boldsymbol{G^{-1}(f)}$. This way, equalized pulses match those originally launched by the transmitter [25]. In contrast, CTLEs are used in optical receivers to compensate for the ISI introduced by the intentionally reduced TIA's bandwidth. Despite the boost in high-frequency noise, CTLE can be beneficial for noise in optical receivers as shown in Section IV.C.

C. FEEDFORWARD EQUALIZER

The presented methodology can also be used to accurately characterize feedforward equalizer (FFE)-based optical receivers. Each FFE tap produces a delayed, weighted version of the TIA' pulse response. By adding those versions to the TIA's pulse response, pre- and post- cursor ISI can be reduced. FFE filter sums scaled and delayed versions of the same signal, offset in time by UI. To account for noise correlation, the output noise power is calculated by (2) with substituting $H_{post}\,(s)$ by

$$H_{FFE}\,(s) = 1 - \sum_{i=1}^{M} \alpha_i e^{-isUI} \tag{10}$$

where, M is the number of taps and α_i is the weight of the i^{th} tap. The output noise is referred to the input using an effective gain calculated from the equalized pulse response as in (5) to account for any residual ISI. Tap weights appear both in output noise and input-referral gain calculations. Therefore, optimal weights minimize the rms input-referred noise current [11]. Tap weights can also be calculated from the pulse response and noise autocorrelation function [2].

D. UPPER LIMIT OF NOISE INTEGRATION

The upper bounds of noise integration in (2) could greatly impact the results. Due to the low pass response of the front end, the high-frequency noise components beyond the bandwidth of the clock and data recovery unit f_{CDR} are attenuated. Therefore, it becomes sufficient to set the upper limit of noise integration in (2) to f_{CDR} [21]. The comparison in Table 2 is repeated assuming $f_{CDR} = f_{bit}$. Limiting the integration bandwidth filters out the high-frequency noise and reduces the impact of the high-frequency boost introduced by the equalizer. As a result, the best noise performance is achieved in the FE that employs a CTLE with complex zeros and a pair of Butterworth poles (Section IV. B, case 2). This FE also shows a gain advantage over the two FBW designs.

VI. CONCLUSION

In this paper, CTLE-based optical receivers are analyzed and compared with the conventional full-bandwidth and decision feedback equalizer (DFE)-based receivers. The comparison aimed at solving the discrepancy found in literature about how the CTLE impacts the noise. In this comparison, the noise from each contributor is first referred to the output using a proper noise transfer function to account for how the stage following the TIA processes the noise. The output noise is then referred to the input by an effective gain that takes into consideration the residual inter-symbol interference. It has been shown that CTLEs: 1) boost high-frequency noise. 2) restore a wide bandwidth which improves the effective and input-referral gains. Combining both effects, the noise performance of the CTLE-based is better than that of the full-bandwidth receivers and lies between that of a two-tap FIR-DFE and IIR-DFE-based receivers. CTLE-based front end achieves the highest effective gain, making it more suitable for the cases where the swing requirements of the CDR incur a significant power penalty. The presented methodology can be extended to accurately characterize feedforward equalizer (FFE)-based optical receivers.

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REFERENCES

[1] D. Li, L. Geng, F. Maloberti, and F. Svelto, "Overcoming the transimpedance limit: A tutorial on design of low-noise TIA," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 69, no. 6, pp. 2648–2653, Jun. 2022.

[2] B. Radi, D. Abdelrahman, O. Liboiron-Ladouceur, G. Cowan, and T. C. Carusone, "Optimal optical receivers in nanoscale CMOS: A tutorial," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 69, no. 6, pp. 2604–2609, Jun. 2022.

[3] E. Sackinger, "The transimpedance limit," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 57, no. 8, pp. 1848–1856, Aug. 2010.

[4] M. G. Ahmed, "A 12-Gb/s -16.8-dBm OMA sensitivity 23-mW optical receiver in 65-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 53, no. 2, pp. 445–457, Feb. 2018.

[5] J. Proesel, A. Rylyakov, and C. Schow, "Optical receivers using DFE-IIR equalization," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2013, pp. 130–131.

[6] A. Sharif-Bakhtiar and A. C. Carusone, "A 20 Gb/s CMOS optical receiver with limited-bandwidth front end and local feedback IIR-DFE," *IEEE J. Solid-State Circuits*, vol. 51, no. 11, pp. 2679–2689, Nov. 2016.

[7] S. Saeedi, S. Menezo, G. Pares, and A. Emami, "A 25 Gb/s 3D-integrated CMOS/silicon-photonic receiver for low-power high-sensitivity optical communication," *J. Lightw. Technol.*, vol. 43, no. 12, pp. 2924–2933, Jun. 15, 2016.

[8] M. Madani and G. E. R. Cowan, "10 Gb/s optical receiver with continuous-time feed-forward equalization," in *Proc. IEEE 60th Int. Midwest Symp. Circuits Syst. (MWSCAS)*, Aug. 2017, pp. 926–929.

[9] D. Li, "A low-noise design technique for high-speed CMOS optical receivers," *IEEE J. Solid-State Circuits*, vol. 49, no. 6, pp. 1437–1447, Jun. 2014.

[10] D. Abd-Elrahman, G. Cowan, and O. Liboiron-Ladouceur, "Low-noise optical receiver front-end using narrow-bandwidth TIA and cascaded linear equalizer," in *Proc. IEEE 60th Int. Midwest Symp. Circuits Syst. (MWSCAS)*, Aug. 2017, pp. 735–738.

[11] D. Abdelrahman and G. E. R. Cowan, "Noise analysis and design considerations for equalizer-based optical receivers," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 66, no. 8, pp. 3201–3212, Aug. 2019.
[12] A. Sharif-Bakhtiar, M. G. Lee, and A. C. Carusone, "Low-power CMOS receivers for short reach optical communication," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, Apr. 2017, pp. 1–8.
[13] S. Daneshgar, H. Li, T. Kim, and G. Balamurugan, "A 128 Gb/s, 11.2 mW single-ended PAM_4 linear TIA with 2.7 μArms input noise in 22 nm FinFET CMOS," *IEEE J. Solid-State Circuits*, vol. 57, no. 5, pp. 1397–1408, May 2022.
[14] J. Proesel, C. Schow, and A. Rylyakov, "25Gb/s 3.6pJ/b and 15Gb/s 1.37pJ/b VCSEL-based optical links in 90nm CMOS," in *Proc. IEEE Int. Solid-State Circuits Conf.*, Feb. 2012, pp. 418–420.
[15] M. M. P. Fard, O. Liboiron-Ladouceur, and G. E. R. Cowan, "1.23-pJ/bit 25-Gb/s inductor-less optical receiver with low-voltage silicon photodetector," *IEEE J. Solid-State Circuits*, vol. 53, no. 6, pp. 1793–1805, Jun. 2018.
[16] K. Lakshmikumar, A. Kurylak, M. Nagaraju, R. Booth, and J. Pampanin, "A process and temperature insensitive CMOS linear TIA for 100 Gbps/λ PAM-4 optical links," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, Apr. 2018, pp. 1–4.
[17] J. E. Proesel, Z. Toprak-Deniz, A. Cevrero, I. Ozkaya, S. Kim, D. M. Kuchta, S. Lee, S. V. Rylov, H. Ainspan, T. O. Dickson, J. F. Bulzacchelli, and M. Meghelli, "A 32 Gb/s, 4.7 pJ/bit optical link with –11.7 dBm sensitivity in 14-nm FinFET CMOS," *IEEE J. Solid-State Circuits*, vol. 53, no. 4, pp. 1214–1226, Apr. 2018.
[18] S. Saeedi, S. Menezo, G. Pares, and A. Emami, "A 25 Gb/s 3D-integrated CMOS/silicon-photonic receiver for low-power high-sensitivity optical communication," *J. Lightw. Technol.*, vol. 43, no. 12, pp. 2924–2933, Jun. 15, 2016.
[19] D. Abdelrahman. *Modeling and Design of High-Speed CMOS Receivers for Short-Reach Photonic Links*. Accessed: Oct. 18, 2022. [Online]. Available: https://spectrum.library.concordia.ca/id/eprint/988237/1/Abdelrahman_PhD_S2021.pdf
[20] S. Shahramian, H. Yasotharan, and A. C. Carusone, "Decision feedback equalizer architectures with multiple continuous-time infinite impulse response filters," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 59, no. 6, pp. 326–330, Jun. 2012.
[21] E. Säckinger, *Broadband Circuits for Optical Fiber Communication*. Hoboken, NJ, USA: Wiley, 2005.
[22] S. Galal and B. Razavi, "10-Gb/s limiting amplifier and laser/modulator driver in 0.18-μm CMOS technology," *IEEE J. Solid-State Circuits*, vol. 38, no. 12, pp. 2138–2146, Dec. 2003.
[23] Q. Pan, Y. Wang, Y. Lu, and C. P. Yue, "An 18-Gb/s fully integrated optical receiver with adaptive cascaded equalizer," *IEEE J. Sel. Topics Quantum Electron.*, vol. 22, no. 6, pp. 361–369, Nov. 2016.
[24] J. E. Goell, "An optical repeater with high-impedance input amplifier," *Bell Syst. Tech. J.*, vol. 53, no. 4, pp. 629–643, Apr. 1974.
[25] J. F. Bulzacchelli, "Equalization for electrical links: Current design techniques and future directions," *IEEE Solid-State Circuits Mag.*, vol. 7, no. 4, pp. 23–31, Fall 2015.

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