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## RESEARCH ARTICLE

# Investigation of Junctionless Fin-FET Characterization in Deep Cryogenic Temperature: DC and RF analysis

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**ABSTRACT** This work presents the SOI Junctionless Fin-FET characterization in Deep Cryogenic behavior (DC-JLFET). Results show that the JLT device is well-suited for various operations, such as computation, sensing, and communication in the quantum field. The cryogenic transfer characteristics, including bias, and interface trap density, are analyzed over a broad temperature range (300 Kelvin down to 4.2 Kelvin). Cryogenic DC and RF analyses were done on the conventional double-gate JL-FET structure, operating at 300 K and below 4.2 K for different geometries. The suggested study illustrates that cryogenic status in the new technology CMOS can be correctly anticipated by calibrating data using an experimental device.

**INDEX TERMS** Fin-FET, cryogenic, junctionless, quantum computing.

## I. INTRODUCTION

The scaling down of the channel lengths in standard metal-oxide-semiconductor (MOS) Field-Effect transistors (FET) poses several critical challenges, such as reducing SCEs, increasing on-current, and lower power consumption must be addressed [1], [2], [3]. SOI transistors have been broadly used as a good alternative for further downscaling for the low-power FET operations asked by ITRS. SOI wafers have low variability, improved electrostatic control, and lesser short-channel effects (SCEs) [4], [5], [6], [7], [8], [9]. Also, SOI's lower parasitic capacitances and resistances provide good RF and analog Figures of Merits (FoMs). The junctionless FETs (JLFETs) have been suggested as a further effort to solve the SCEs and stringent requirements of an ultra-steep doping characteristic at the metallurgical interfaces as well as complicated heat budgets in standard transistors [10], [11], [12], [13], [14], [15], [16], [17], [18]. The other way to reduce the SCEs is by using the multiple-gate transistors in the scaled MOSFETs [19], [20], [21]. To improve electrostatic integrity, three modes are combined in this work: SOI, multiple gate FET, and junctionless technology. In silicon structures,

creating CMOS-compatible qubits [22], [23] helped us focus on low temperatures of CMOS semiconductor technology for computer operations. MOS transistor structures have been studied at extremely low temperatures since the 1970s to be used in applications and systems, including limited-noise, space devices, energy conversion devices, and so on [24], [25]. Although, despite the various advantages of high-efficiency and low-power information technology [26], cryogenic cooling did not remain in use for computer technology, reversing the pattern established by the ETA-10 liquid-nitrogen-cooled quantum computer [27]. Quantum computers get the theoretical potential, supported by experimental data, to operate in an enormous problem situation and thus can solve several more computer processing issues that traditional computers cannot. Quantum bit (Qubit) manipulation and readout are vital for achieving quantum computers. Another strategy would be to use low-temperature electronics, which perform at/or close to the temperatures at which qubits exist [28], [29], [30], [31], [32], [33], [34]. Aside from quantum computing, the original function for low-temperature devices is dispersed and huge. In the specific situation of Quantum Computers, FinFETs, as the most common logic circuit structure, are the first of many contemporary devices to be investigated for quantum control circuits.

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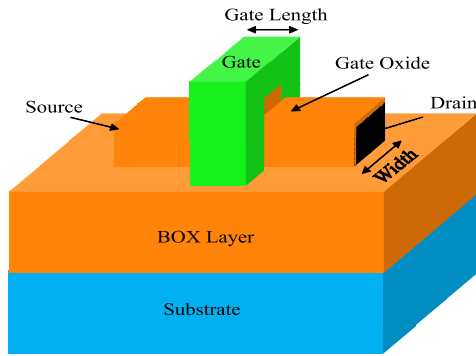


FIGURE 1. A 3-D view of the proposed DC-JLFET.

In this work, we demonstrate that the electrical specifications of junctionless FETs are highly affected by the physical properties of the structures. As a result, the main goal of this study focuses on the effect of temperature decrement on the working of JLFETs down to 4 K in the DC and RF characteristics. The I/V curve, transconductance ( $G_m$ ), subthreshold slope (SS), radio frequency (RF), and interface traps have all been investigated. Also, the influence of different geometries (W/L) on the device characteristics has been analyzed. The goal for comparing 40 and 28 nodes is to investigate the channel length effect on the device features.

## II. DEVICE CHARACTERISTICS

A 3-D schematic of the DC-JLFET is depicted in Fig. 1. First, we have calibrated the simulation data for validation by regenerating the experimental data of a junctionless FET [35], which is demonstrated in Fig. 2. This work is based on an N-type JLFETT structure on  $\langle 100 \rangle$  orientation SOI wafers with a 100 nm thick buried oxide layer (BOX) and an active silicon layer with 5 nm thickness. Uniformly doping of active regions of the device is considered at one  $\times 10^{19} \text{ cm}^{-3}$ . The gate comprises a 5.0 eV work function with an oxide thickness of 1 nm. The gate mask length ranged from 28 nm to 40 nm, and the gate mask width ranged from 1  $\mu\text{m}$  to 2  $\mu\text{m}$ . Surface roughness, coulomb, and phonon scattering have been considered to investigate the impact of scattering effect on mobility.

## III. RESULTS AND DISCUSSIONS

### A. IMPACT OF CRYOGENIC TEMPERATURE ON THE DC CHARACTERISTICS

This paper investigates the cryogenic temperature effects on the RF and DC modes and also analyzes these effects on the subthreshold slope, threshold voltage, and transconductance. Transfer characteristics of the JLFET structure for short channel sizes ( $L = 28 \text{ nm}$  and  $L = 40 \text{ nm}$ ) have been analyzed at various temperatures in the wide range from 4.2–300 Kelvin, as shown in Fig. 3. The widely known point of crossing, which is known as the zero-temperature coefficient (ZTC) [17], [36], [37], has not to rely on the temperature owing to the heat recompense impacts of carrier mobility and threshold

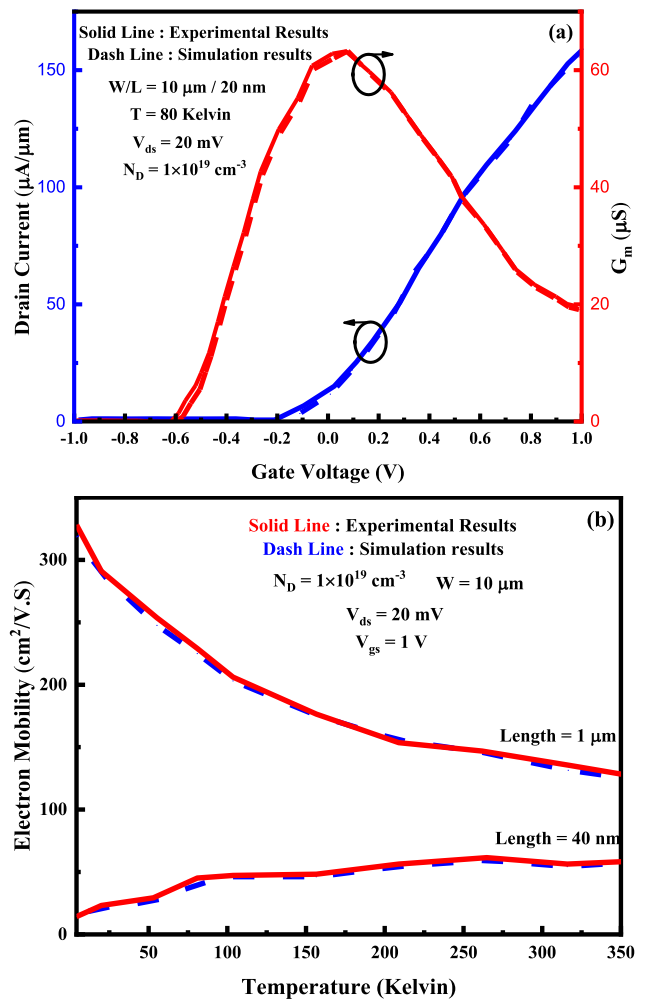


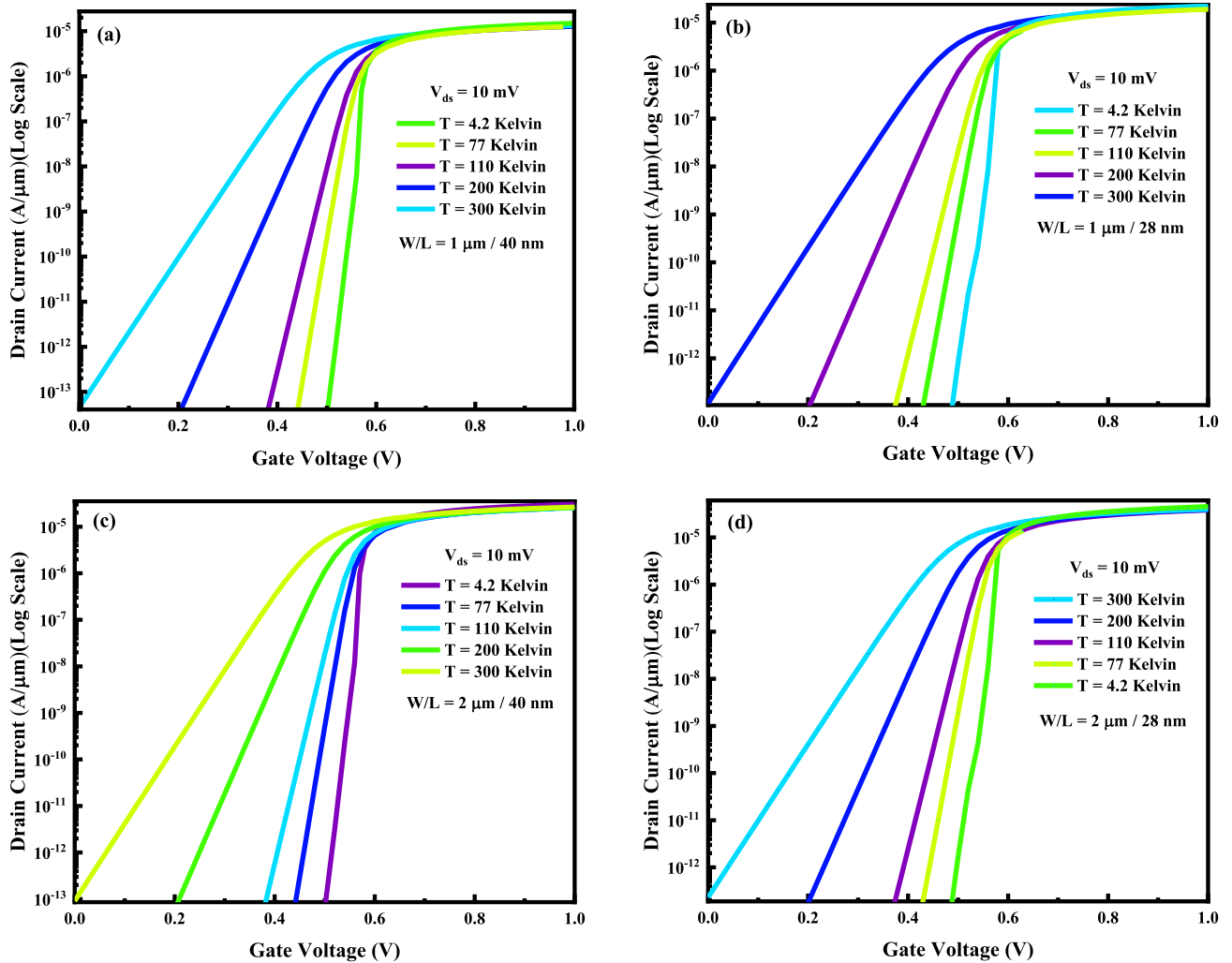
FIGURE 2. Calibration of (a) transfer characteristic and (b) electron mobility of the JLFET with experimental results [35] for validation of the simulation data.

voltage ( $V_{th}$ ) [35]. The ZTC phenomenon is defined by the fact that for large gate sizes,  $V_{th}$  and electron mobility have both been enhanced at lower temperatures [35], whereas those differed in reduction of temperature for short gate length and increment of mobility is not high.

The subthreshold slope  $SS$ , described as  $\eta kT/q (\ln 10)$  (mV/dec), decreases the thermal voltage at 77 and 4.2 Kelvin for all structures. As demonstrated in Fig. 4, the  $SS$  reduces to 4.5 mV/dec in 4.2 K for  $L = 40 \text{ nm}$ ; however, this reduction is smaller than the predicted amount, which is 0.8 mV/dec at extremely low temperatures; this is due to insufficient dopant ionization. Also, the  $SS$  is 4.8 mV/dec when the gate size is  $L = 28 \text{ nm}$ .

The  $I_{on}$  increases slightly at 4.2 Kelvin for the small-length structures but rises for the extensive-length designs, as shown in Fig. 5. It could be defined by the expression of the electron current [30]:

$$J_n = q\mu_n \left( nE + \frac{n\nabla kT}{q} \right) \quad (1)$$



**FIGURE 3.** Transfer characteristic curve (a)  $W/L=1 \mu\text{m} / L=40 \text{ nm}$  (b)  $W/L=1 \mu\text{m} / L=28 \text{ nm}$  (c)  $W/L=2 \mu\text{m} / L=40 \text{ nm}$  (d)  $W/L=2 \mu\text{m} / L=28 \text{ nm}$  of the JLFET at  $V_{ds} = 10 \text{ mV}$  with different temperatures.

The current density is proportional to the temperatures at low drain voltages, and field-assisted ionization is poor, but at high drain voltages, the current density rises with lowering the temperature due to carrier mobility, and field-assisted ionization is significant in this channel size. The  $G_m$  improves at 4.2 Kelvin ( $\sim \times 2$ ,  $W/L = 2 \mu\text{m} / 28 \text{ nm}$ ), as illustrated in Fig. 6.

For JLFET structures, the  $G_m$  curve was plotted in Fig. 6, with different  $W/L$  geometries at  $V_{ds} = 10 \text{ mV}$ , while the  $G_m$  show high degradation in large  $V_{gs} < V_{fb}$  in regards to increasing the series resistance  $R_{Se}$ . The oscillations observed in  $G_m$  curves credit this impact to the quantum transport in such Structures [38]. When the  $V_{gs}$  of an n-type transistor is raised, electrons may fill the possible sub-band step by step, causing the current to behave step-like. In particular, at extremely small  $V_{ds}$ , the quantization of energy states in the conduction band is seen [39] because the total energy at larger voltages is substantially more than the band gap among two quantized energy states.

In a short channel DGJLFET, the  $V_{th}$  can be described as [15] (2), as shown at the bottom of the next page, where;

$$\beta = \frac{-1 + e^{-\frac{L_{gate}}{\lambda}}}{2 \sinh(\frac{L_{gate}}{\lambda})}$$

$$\delta = \frac{V_{ds} - \omega \left( -1 + e^{-\frac{L_{gate}}{\lambda}} \right)}{2 \sinh(\frac{L_{gate}}{\lambda})}$$

$$\gamma = \frac{1 - e^{-\frac{L_{gate}}{\lambda}}}{2 \sinh(\frac{L_{gate}}{\lambda})}$$

$$\theta = \frac{-V_{ds} + \omega \left( -1 + e^{-\frac{L_{gate}}{\lambda}} \right)}{2 \sinh(\frac{L_{gate}}{\lambda})}$$

$$\lambda = \sqrt{\frac{t_{si}(4\epsilon_{si} + C_{ox}t_{si})}{8C_{ox}}}$$

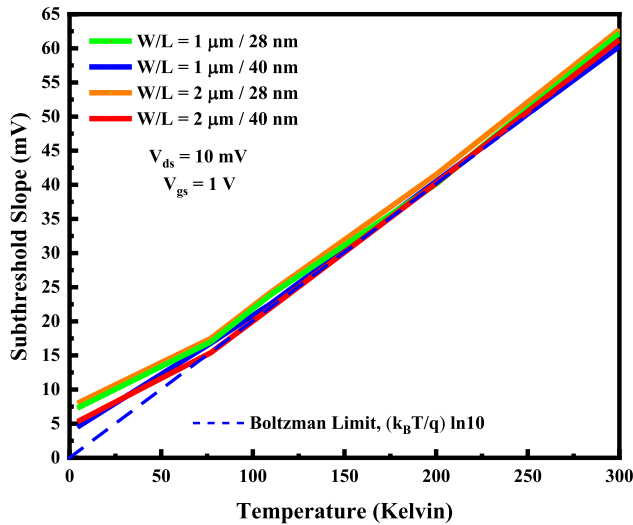


FIGURE 4. Variation of SS versus different temperatures and W/L geometries.

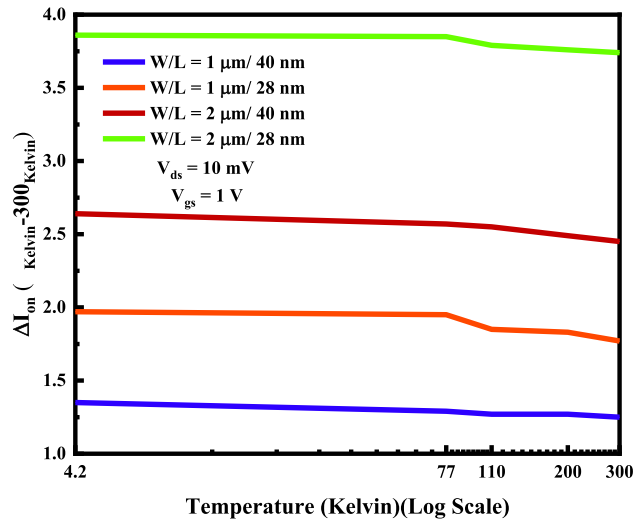


FIGURE 5. Impact of the temperature on the  $I_{on}$  of JLFET versus different temperatures.

$$\omega = V_{fb} - \frac{qN_D t_{si}}{2C_{ox}} - \frac{qN_D t_{si}^2}{8\epsilon_{si}} \quad (3)$$

where the  $\lambda$  is the natural length and  $V_{fb}$  is the flat band voltage. We must note that the  $\beta$  and  $\gamma$  are zero in long channel lengths. Eq. (3) shows that the only temperature-dependent parameter is the  $V_{fb}$ . Besides, the  $V_{th}$  shifts to higher gate voltages at 4.2 Kelvin versus 300 Kelvin because of incomplete ionization. Indeed, larger drain voltages are necessary to absorb enough electrons to the top to form the inversion area. The  $V_{th}$  variation with different temperatures

is shown in Fig. 7 with various W/L geometries. It is worth noting that the maximum  $V_{th}$  change has been illustrated in W/L = 1  $\mu$ m / 28 nm ( $\Delta V_{th} = 0.15$  V).

Fig. 8 shows that until reaching 77 Kelvin, the  $\eta$  remains close to the value at 300 Kelvin. From 77 Kelvin down to 4.2 Kelvin, the slope factor increases sharply.

### B. INFLUENCE OF INTERFACE CHARGE DENSITY ON THE JLFET I-V CURVE IN THE DEEP CRYOGENIC TEMPERATURE

The charge density for every unit area measured in interface states  $Q_f$  is [40]:

$$Q_f = \int_{E_i}^{+\infty} N_f(E) f(E) dE \quad (4)$$

In this equation,  $N_f$  denotes the overall distribution of interface traps across the energy. In cryogenic conditions, the concentration of dangling bonds at the junction does not increase considerably. The clear temperature-dependent rise of the rate of  $N_f$  value (for example, in charge-pump calculations [40]) is because, at very low temperatures, the Fermi level covers a large section of the energy bandgap. This logarithmic rise in trap intensity at the band edge was also required to account for the bend of the I-V curve and the SS degradation caused by conduction-band or valence-band tails [41]. Depending on the type (acceptor/donor) and the placement of the Fermi level in the bandgap, Interface density  $N_f$  can be either charged or uncharged. Their charge contribution varies with the surface potential,  $\psi_s$ . Fig. 9 depicts the transfer characteristics of JLFET in the deep cryogenic temperature and RT with and without interface charge density.

The interface traps play an essential role in determining the  $V_{th}$ , the  $\mu_{ch}$ , and the  $G_m$  of FETs, and their effect is especially evident in the SS of the transfer characteristics. Fig. 10 demonstrates the influence of the various  $N_f$  on the SS &  $V_{th}$  in the deep cryogenic temperature.

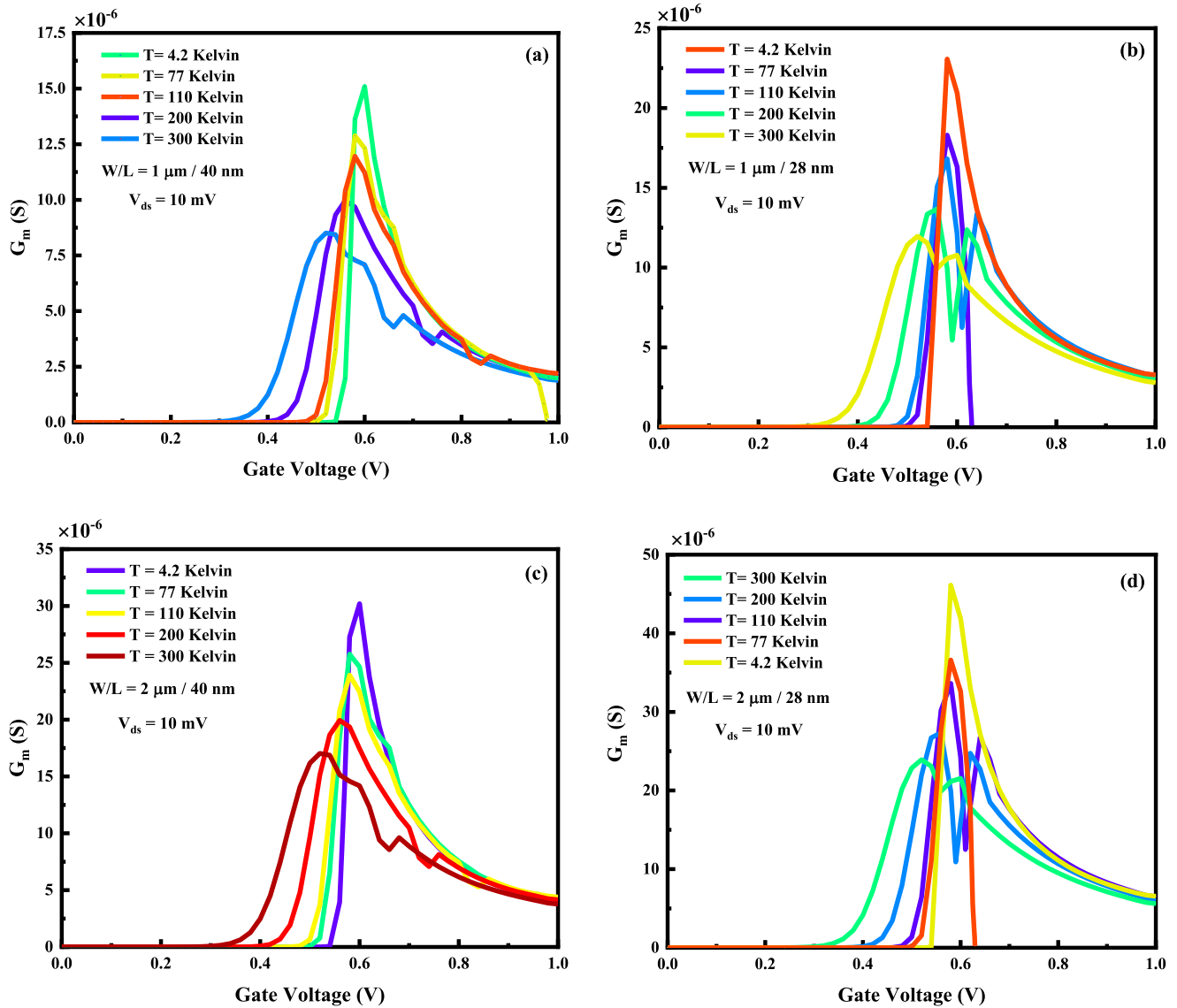
Fig. 11 shows the JLFET  $G_m$  curve in deep cryogenic temperatures with various  $N_f$ . To analyze the effect of the  $N_f$  on the SS can be expressed [7]:

$$SS = \frac{kT}{q} \ln(10) \left[ 1 + \frac{C_f}{C_{ox}} + n \right] \quad (5)$$

where  $C_f = qN_f$  is the capacitances of the  $N_f$  at the gate oxide,  $C_{ox}$  is the gate oxide capacitance,  $C_{Si}$  is the active regions capacitance, and  $N_f$  represents the interface trap density at the gate oxide. The  $n$  is the body factor, defined by  $n = (C_{ox} + C_f + C_{Si})/C_{ox}$  for an SOI structure. The impacts of traps related to the BOX layer have been neglected.

Fig. 12 illustrates the influence of  $V_{ds}$  on the I-V curve of JLFET in the deep cryogenic temperature. As demonstrated in Fig. 12, at higher drain voltages, current density rises

$$V_{th} = \frac{2(\delta\gamma + \beta\theta) + \omega + \sqrt{((2(\delta\gamma + \beta\theta) + \omega)^2 - (1 - 4\beta\gamma)(\omega^2 - 4\delta\theta))}}{(1 - 4\beta\gamma)} \quad (2)$$



**FIGURE 6.** Characteristic of the  $G_m$  curve (a)  $W/L=1 \mu\text{m}/L=40 \text{ nm}$  (b)  $W/L=1 \mu\text{m}/L=28 \text{ nm}$  (c)  $W/L=2 \mu\text{m}/L=40 \text{ nm}$  (d)  $W/L=2 \mu\text{m}/L=28 \text{ nm}$  of the JLFET at  $V_{ds} = 10 \text{ mV}$  with different temperatures.

with reducing the temperature through mobility, and field-assisted ionization is critical in the channel. We understand that  $N_f$  increases with lowering the temperature, achieving  $10^{13} \text{ cm}^{-2}$  at deep cryogenic temperatures.

**C. RF ANALYSIS**

Fig. 13 shows the impact of the Transconductance Generation Factor (TGF) versus  $V_{gs}$  in various cryogenic temperatures. TGF has been described as  $G_m/\text{drain-current}$  relation and represents the power losses of the structure in digital operations. The higher TGF leads to smaller power losses.

Plotting TGF, which gives a detailed perspective of the analyzed device, from low-frequency (depletion/partial depletion) application where high gain is obtained to high-frequency (flat band/accumulation) application where higher

drive current is needed, seems to be a constructive analysis solution that enables for a first world admiration of the device under research for analog analysis. In the green regime (depletion/partial depletion), TGF is inversely proportional to the SS. On the purple side (flat band/accumulation), It would be proportionally to  $\mu_n \cdot C_{ox}/n$  (where  $\mu_n$  is electron mobility,  $C_{ox}$  is gate oxide capacitance, and  $n$  is body factor). On the other hand, A device’s analog/RF efficiency is mainly restricted by intrinsic terminal capacitances. The effect of temperature on parasitic capacitances versus  $V_{gs}$  can be seen in Fig. 14.

The transit frequency ( $f_T$ ) of FETs is achieved as follows() [42]:

$$f_T = \frac{G_m}{2\pi (c_{gs} + c_{gd})} \tag{6}$$

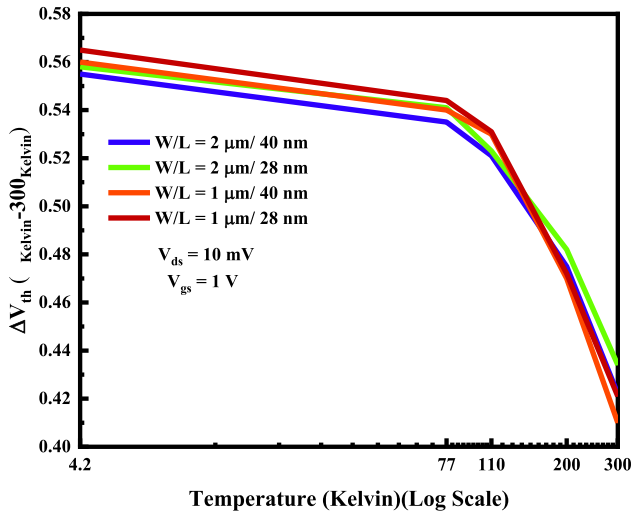


FIGURE 7. Variation of  $V_{th}$  versus different temperatures and W/L geometries.

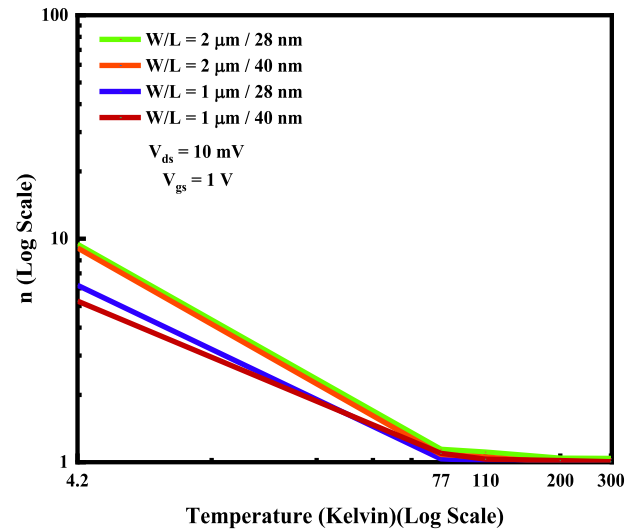


FIGURE 8. Impact of the temperature on the  $n$  of JLFET.

and is calculated from the current gain ( $H_{21}$ ) and shown in Fig. 15 as one of the main RF FoMs. Due to the lower parasitic capacitances and higher  $G_m$ , the  $f_T$  improves, and the maximum  $f_T$  is achieved, about 563 GHz. Because of the lower variation of capacitances in cryogenic temperatures, the transit frequency  $f_T$  follows the increment in the  $G_m$ , as demonstrated in Fig. 7. This rise may be offset by decreased power usage, which is also advantageous for thermal losses from the management system to the quantum bits. This increment becomes particularly significant in shorter channel lengths.

We analyzed the influence of the various temperatures on the unilateral-power-gain (UPG), ( $f_{max}$ ) is the frequency where UPG becomes unity, or zero dB, and the transit time ( $\tau$ ) of JLFET. These ratios have been achieved from the

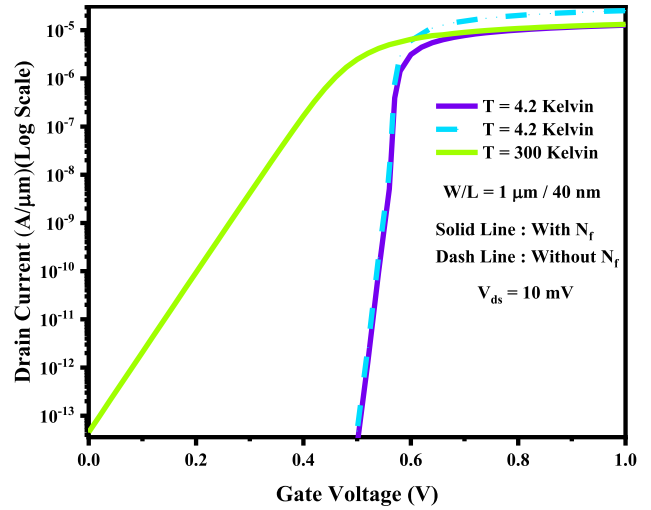


FIGURE 9. Effect of  $N_f$  on the on-current ( $I_{on}$ ).

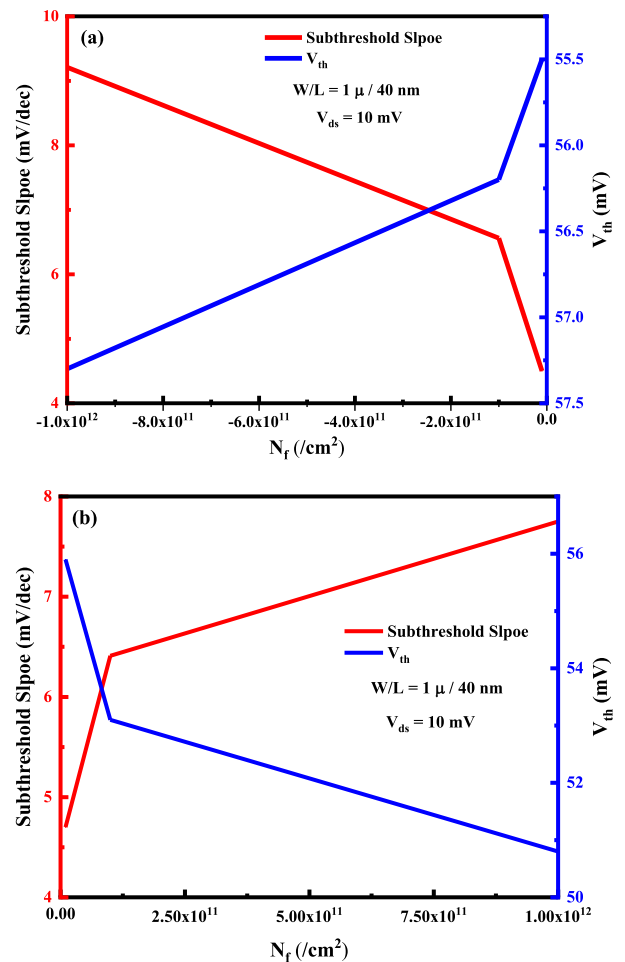


FIGURE 10. Impact of the various  $N_f$  on the SS &  $V_{th}$  in the 4.2 Kelvin temperature (a) Negative (b) Positive.

equations [43], [44]:

$$f_{max} = \frac{f_T}{2} \sqrt{\frac{R_{ds}}{R_g}} \quad (7)$$

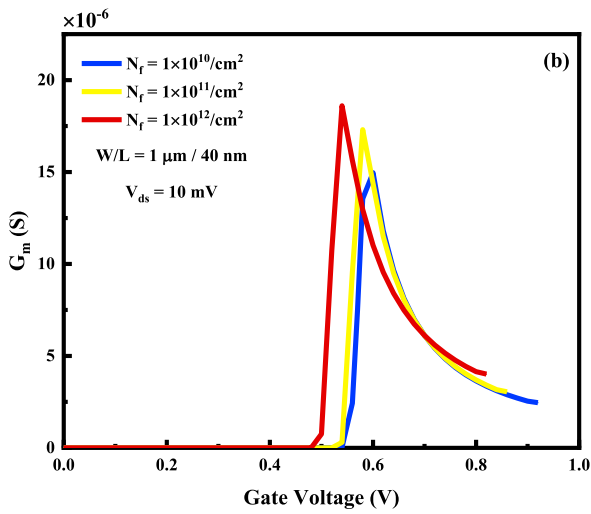
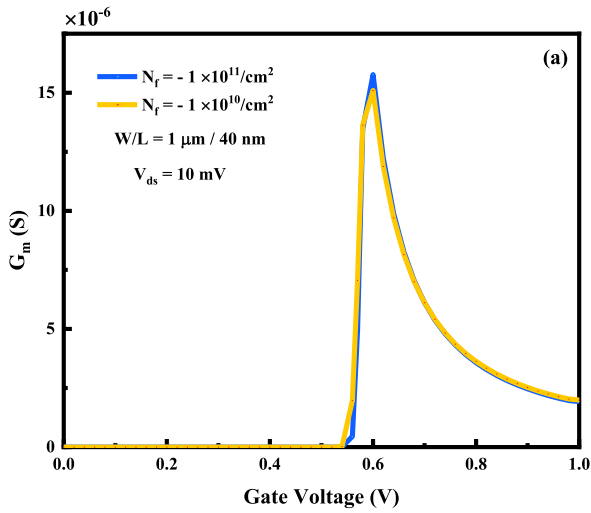


FIGURE 11. Impact of the various interface charge density on the  $G_m$  curve at the 4.2 Kelvin temperature (a) Negative (b) Positive.

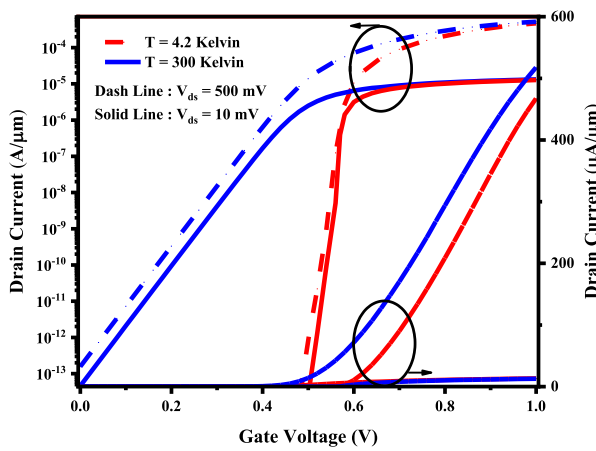


FIGURE 12. Impact of  $V_{ds}$  on the JLFET I-V curve in the various temperatures.

$$\tau = \frac{1}{2\pi fT} \quad (8)$$

$$UPG = \left(\frac{f_{max}}{f}\right)^2 \quad (9)$$

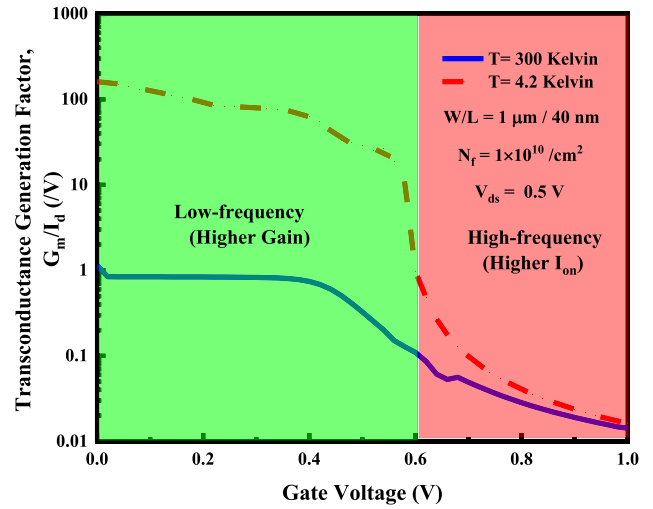


FIGURE 13. Impacts of TGF on the various temperatures.

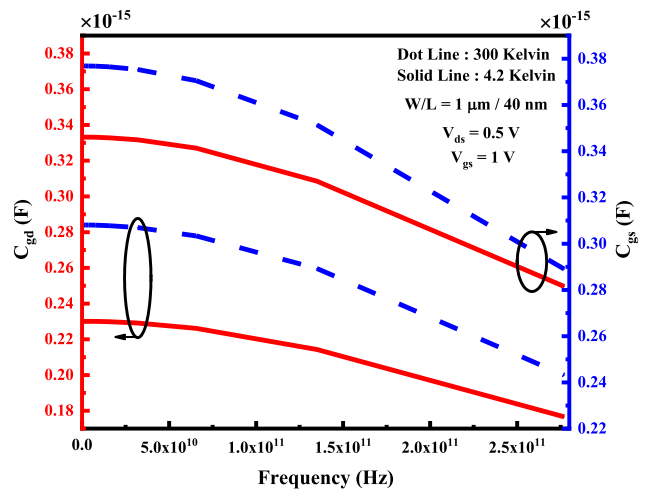


FIGURE 14. Impact of various temperatures on parasitic capacitance.

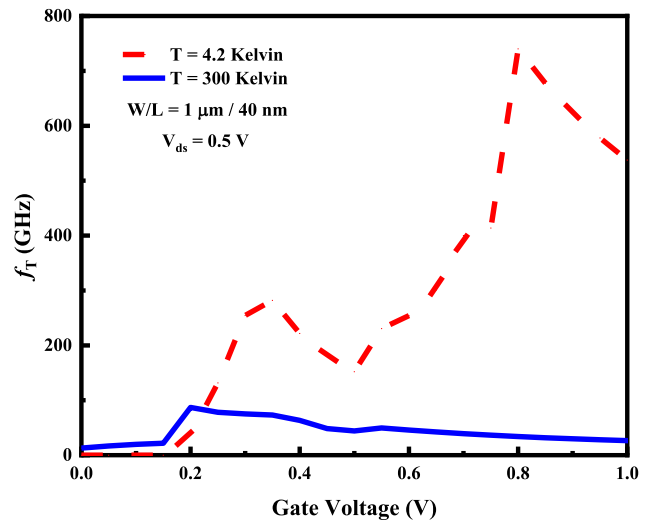


FIGURE 15. Impact of various temperatures on the  $f_T$ .

The obtained results above equations are illustrated in Fig. 16. The gate resistance ( $R_g$ ) decreases because of the reduced

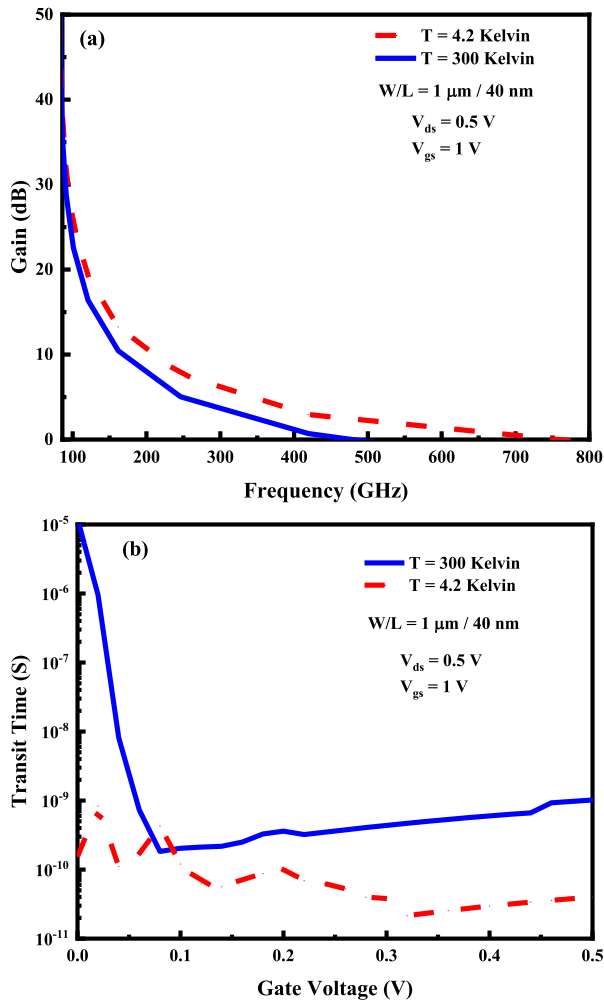


FIGURE 16. Influence of several temperatures on the (a) UPG and (b) transit time.

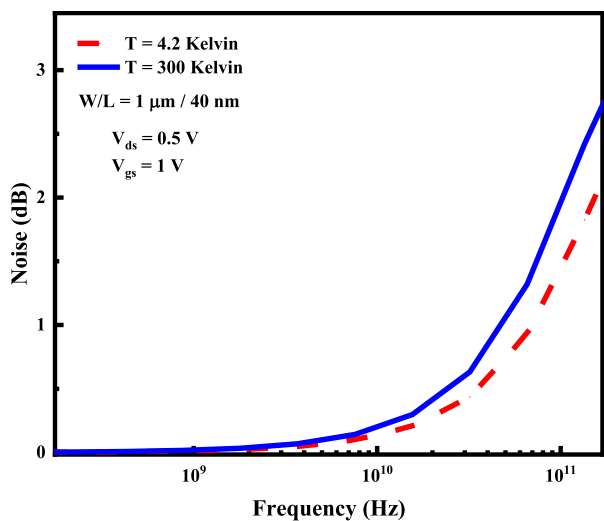


FIGURE 17. Impact of various temperatures on the noise.

resistivity of gate metal contact at the cryogenic temperature, and due to the higher  $f_T$  at 4.2 Kelvin,  $f_{max}$  increases. It can be inferred that the 4.2 Kelvin temperature leads to better

performance and reduces transit time. Improvement in  $G_m$  and  $f_T$  enables a reduction in transit time. Charge carriers have a very low transit time in the ON-condition.

The NF of FETs can be obtained as follows:

$$NF = 1 + 5\pi f C_{gs} \sqrt{\frac{R_S + R_G}{G_m}} \quad (10)$$

Fig. 17 shows the impact of various temperatures on the Noise Figure (NF). By reducing parasitic capacitance and due to higher  $G_m$ , the value of NF reduces at lower temperatures.

#### IV. CONCLUSION

The effect of cryogenic temperature on an ( $L = 28$  nm and  $L = 40$  nm) Junctionless SOI Fin-FET innovation for quantum information management systems is presented in this paper. Starting with a deep study of the physical structures at extremely low temperatures, actually promoting changes in the essential analog design specifications are achieved, even though increment in the slope factor at very low temperatures decreases the predicted current savings; however, this increase is not significant. The suggested study illustrates that cryogenic status in the new technology CMOS may be correctly anticipated by calibrating data using an experimental device. This is an attractive idea for future small cryogenic models for silicon-based quantum information structures.

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