Received 11 November 2022, accepted 29 November 2022, date of publication 7 December 2022,
date of current version 13 December 2022.

Digital Object Identifier 10.1109/ACCESS.2022.3227442

RESEARCH ARTICLE

Analysis of the Zero Overvoltage Switching Phenomenon

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This work was supported by the Research Program LuFo VI of the German Federal Ministry for Economic Affairs and Climate Action.

ABSTRACT In common understanding, the fast switching speed of wide-bandgap devices leads to high overvoltage and oscillations, if no countermeasures are taken. Those countermeasures were introduced in the past, and include methods such as build-in gate resistors or low-inductive power modules. There is, however, a physical limit for the reduction of the parasitic inductance in the commutation cell. This is one of the reasons why the full potential of wide-bandgap devices cannot be entirely utilized. In contrast, the Zero Overvoltage Switching (ZOS) phenomenon can be used to theoretically unleash unlimited switching speed with no switching losses and voltage overshoots. This method triggers the inherent parasitic oscillating elements of a commutation cell to perform an ideal current commutation. This article investigates the physical effects and usage of this technology in real-world applications. The model of an ideal commutation cell is adapted to reality by introducing damping factors as well as the nonlinear behaviour of the parasitic capacitances. An extended ZOS area is presented, including the parasitic capacitances of two wide-bandgap devices. It allows today's silicon carbide power modules to make use of the ZOS technology and perform at different power levels. Measurements with a commercially available power module were taken to verify the theoretical analysis and the derived equations.

INDEX TERMS Silicon carbide (SiC), SiC MOSFET, unlimited switching speed, wide-bandgap, zero overvoltage switching.

NOMENCLATURE

ZOS	Zero Overvoltage Switching.
L_σ	Parasitic inductance of the commutation cell.
T_1	Bottom connected transistor.
T_2	Top connected transistor.
C_{ds1}	Parasitic drain-source capacitance of transistor T_1.
C_{ds2}	Parasitic drain-source capacitance of transistor T_2.
D_1	Body diode of transistor T_1.
D_2	Body diode of transistor T_2.
I_{TO}	Turn-off current to achieve ZOS.
$I_{TO,n}$	Turn-off current including extended ZOS area.
$t_{ZOS,n}$	Required commutation time during ZOS.
i_{Cds2}	Current through parasitic capacitance C_{ds2}.
v_{Cds2}	Voltage across parasitic capacitance C_{ds2}.
v_{mp}	Midpoint voltage.
$v_{L\sigma}$	Voltage across the parasitic inductance L_σ.
f_{res}	Resonant frequency of the parasitic resonant tank.
E_Q	Required energy for moving charge into the parasitic capacitances.
E_C	Stored energy in the parasitic capacitances.
Q_{ZOS}	Amount of required charge to achieve ZOS.
t_{sl}	Time until the current ramp reaches its end value.

The associate editor coordinating the review of this manuscript and approving it for publication was Francesco G. Della Corte.

I. INTRODUCTION

With wide-bandgap transistors such as silicon carbide (SiC)-based MOSFETs, it is possible to increase the operating switching frequency f_{sw} of a power converter compared to silicon-based transistors [1], [2]. Generally, a higher

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switching frequency is preferred since it effectively leads to a decreased physical size of passive components. Due to very short turn-on and turn-off events, wide-bandgap devices are capable of reducing the switching losses. However, during the turn-off event, the high di/dt within the parasitic inductance of the commutation cell induces a voltage that could lead to severe overvoltage spikes. Untreated, the appearing overvoltages may exceed the blocking voltage of the transistor, leading to its destruction. Also, the high frequency ringing in the voltage and current caused by the parasitic elements effectuates greater electromagnetic interferences [3].

A. STATE OF THE ART

In today's power electronic circuits, a trade-off between high dv/dt and di/dt for low switching losses and the overvoltage on a transistor is crucial. Different solutions have been proposed for limiting the overvoltages and ringing after switching events.

One approach is to reduce the parasitic inductance in the commutation cell to a minimum [4]. According to [5] the parasitic inductance in the commutation cell is the main contributor to ringing and overvoltages. With the increasing usage of SiC transistors, different optimization methods are presented to reduce the parasitic inductances in power modules [6], [7]. An optimized busbar design between the DC-link and the power modules can reduce the effective parasitic inductance of the commutation cell [8], [9].

The authors of [10] proposed the integration of an additional snubber ceramic capacitor on the direct bonded copper (DBC) substrate of the power module. This effectively reduces the size of the commutation cell and thereby the effective parasitic inductance. A measurement methodology was proposed to visualize the current distribution within the power module and the actual influence of the snubber capacitors. Also, article [10] provides a comparison of a power module with and without integrated snubber capacitors. In [11] ceramic capacitors were embedded into a power module. Measurements were provided, to show the difference between the power modules with and without embedded ceramic capacitors. However, by implementing a snubber capacitor in the power module, it is possible that oscillations between the external DC-link and snubber capacitors are introduced. To avoid this, a Si-RC element compared to a ceramic capacitors can be implemented. In [12] a Si-RC device is placed physically close to the transistors, in order to reduce the effective parasitic inductance of the commutation cell as well as damping voltage oscillations.

An alternative method is to control the di/dt of the transistor by the external gate resistors. By inserting gate resistors, the gate drive current is reduced. This directly lengthens the switching transition of the transistor and therefore increases the duration of the commutation. This method is resulting in lower overvoltage, but also in higher switching losses. Fig. 6 in [13] exhibits the turn-on and turn-off behavior of SiC MOSFETs with different gate resistances. The presented waveforms suggest an increasing overvoltage by lowering the gate resistance. An active gate driver as proposed in [14] uses a multistage gate resistance control concept to reduce the voltage overshoots.

Another option according to [15] is to use different techniques of controlling the dv/dt as well as di/dt. By electronically adjusting the Miller capacitance, the dv/dt of a MOSFET can be controlled. However, applying this method in a half-bridge topology also leads to increased switching losses due to longer-lasting switching transitions.

B. FUNDAMENTALS OF ZOS

The work that follows proposes a different approach that combines the advantage of fast switching wide-bandgap devices without the drawback of high overvoltages and ringing. Zero Overvoltage Switching, firstly introduced in [16], is a method that allows an infinitely fast turn-off of the transistor's channel, resulting in minimum switching losses at no occurring overvoltages on the transistors. This is done by utilizing the parasitic elements of the circuitry as an active design parameter. This article provides a theoretical and experimental analysis of this method.

The ZOS phenomenon is particularly presented for the turn-off event. However, several options for lossless turn-on methods were proposed in [16]. It was mentioned that the ZOS technique can be used in several topologies.

In the following, the ZOS phenomenon is analyzed on the basis of a symmetrical half-bridge topology, as seen in Fig. 1. The low-side voltage V_{LS} and the phase inductor L_{ph} are shown to complete the half-bridge topology, but will not play an active part in this article's analysis. They are given to indicate the origin of the phase current i_{ph}. The commutation cell forms a resonant circuit, consisting of the parasitic inductance L_σ, the parasitic drain-source capacitances C_{ds1} and C_{ds2}, and the body diodes D_1 and D_2 of the transistors T_1 and T_2. S_1 and S_2 represent the ideal transistor as a switch without parasitic elements. All parasitic inductances in the commutation cell are combined into one parasitic inductance L_σ.

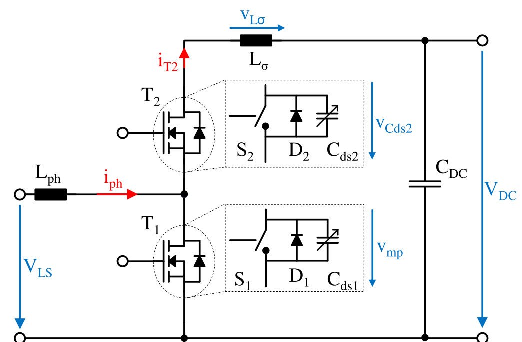

FIGURE 1. Half-bridge topology with parasitic elements.

To derive the following equations, the circuit in Fig. 1 is modified to an equivalent circuit, depicted in Fig. 2. The equivalent circuit is derived in two steps. The circuit on the left side includes the phase current I_{ph} which is assumed to be constant for the entire commutation. The current i_{ch} acts as

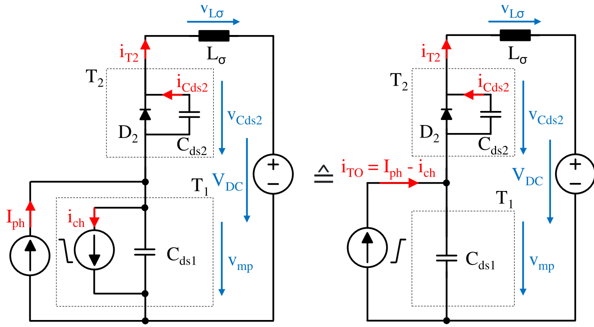

FIGURE 2. Two-step derivation of the commutation cell's equivalent circuit.

a current sink, which resembles the turn-off switching event of the channel inside the transistor T_1. The equivalent circuit on the right side combines both current sources into one step current source. The step current i_{TO} is the difference between the phase current I_{ph} and the transistor's channel current i_{ch}. The step current source represents the channel's turn-off event inside the transistor T_1. In this article the equivalent circuit on the right is used to derive the formulas. The commutation starts at the time t_{start}, where the current I_{TO} passing through the channel of the transistor T_1 is pinched off infinitely fast. It should be noted that the equivalent circuit is only valid during the time of the commutation. The commutation ends when the body diode D_2 becomes the current carrying device. The capacitance C_{DC} in Fig. 1 is magnitudes larger than the parasitic capacitances. Therefore, for the high frequent oscillations, the capacitance C_{DC} does not play an active part in the analysis and V_{DC} is assumed to be an ideal voltage source in Fig. 2.

ZOS is only achievable if the following two conditions are met. The first condition mentioned in [16] is that a specific current, the turn-off current I_{TO}, must be switched off by the transistor T_1 for exciting the resonant circuit. In [16] the formula of the turn-off current is given with the assumption that the two parasitic capacitances are equal. In contrast, the turn-off current I_{TO} to achieve ZOS for two variable parasitic capacitances is derived as follows. The required energy to move electric charge into the parasitic capacitances during commutation is compared to the stored energy in the parasitic capacitances at the DC-link voltage V_{DC}. The energy E_{Q} that moves a specific amount of charge into the parasitic capacitances to achieve ZOS is given by

$$E_{\mathrm{Q}} = \int_0^{Q_{\mathrm{ZOS}}} v_{\mathrm{DC}}\, dq_{\mathrm{ZOS}} = \frac{1}{2}\frac{Q_{\mathrm{ZOS}}^2}{C_{\mathrm{ds1}} + C_{\mathrm{ds2}}}. \tag{1}$$

For ZOS, the required charge is determined for half a period of the resonant frequency of the parasitic resonant tank. This correlation is best seen in Fig. 3. The parasitic resonant tank consists of the parasitic capacitances C_{ds1} and C_{ds2} and the parasitic inductance L_σ. The amount of charge for achieving ZOS is expressed by

$$Q_{\mathrm{ZOS}} = \int_0^{\frac{1}{2}t_{\mathrm{res}}} i_{\mathrm{TO}}\, dt = \frac{1}{2} t_{\mathrm{res}} I_{\mathrm{TO}} \tag{2}$$

where

$$t_{\mathrm{res}} = 2\pi \sqrt{L_\sigma \frac{C_{\mathrm{ds1}} C_{\mathrm{ds2}}}{C_{\mathrm{ds1}} + C_{\mathrm{ds2}}}}. \tag{3}$$

Substitution of (3) into (2) and then (1) yields

$$E_{\mathrm{Q}} = \frac{1}{2}\pi^2 L_\sigma \frac{C_{\mathrm{ds1}} C_{\mathrm{ds2}}}{(C_{\mathrm{ds1}} + C_{\mathrm{ds2}})^2} I_{\mathrm{TO}}^2. \tag{4}$$

The stored energy E_C in the parasitic capacitances is determined by

$$E_{\mathrm{C}} = \int_0^{V_{\mathrm{DC}}} v_{\mathrm{DC}}\, (C_{\mathrm{ds1}} + C_{\mathrm{ds2}})\, dv_{\mathrm{DC}} = \frac{1}{2}\, (C_{\mathrm{ds1}} + C_{\mathrm{ds2}})\, V_{\mathrm{DC}}^2. \tag{5}$$

Equalizing (4) and (5) and re-arranging leads to the equation

$$I_{\mathrm{TO}} = \frac{V_{\mathrm{DC}} \sqrt{\frac{(C_{\mathrm{ds1}}+C_{\mathrm{ds2}})^3}{C_{\mathrm{ds1}} C_{\mathrm{ds2}} L_\sigma}}}{\pi} \tag{6}$$

to determine the required turn-off current and operate with ZOS. The parasitic capacitances in this derivation are assumed to be constant, i.e. voltage dependent.

The second condition for achieving ZOS is that the transistor T_1 must be switched off as fast as possible. It was stated that the turn-off event must be shorter than a period of the resonant frequency. This condition is further addressed in chapter III-B.

In [16] it was claimed that if identical transistors are used in a half-bridge topology, the symmetry of the parasitic capacitances may be easily obtained. For each DC-link voltage V_{DC} there is a specific operating point, at one turn-off current I_{TO}, where ZOS is ideally achievable. To select the desired turn-off current I_{TO} for a specific application, one must vary either the parasitic inductance L_σ or the parasitic capacitances. Increasing the parasitic inductance can be attained by increasing the distance to the DC-link capacitors, and therefore increasing the commutation cell size. However, a more practical approach might be adding a capacitor in parallel to the transistors to increase the total effective drain-source capacitance.

In the simulation of Fig. 3 only the parasitic inductance L_σ as well as the parasitic capacitances C_{ds1} and C_{ds2} are considered. The drain-gate and the gate-source parasitic capacitances of both transistors are not considered. The capacitances C_{ds1} and C_{ds2} are assumed to be linear, whereas in reality the drain-source capacitances show nonlinear behaviour, depending on the applied voltage. The figure shows the current through the transistor T_2, as well as the

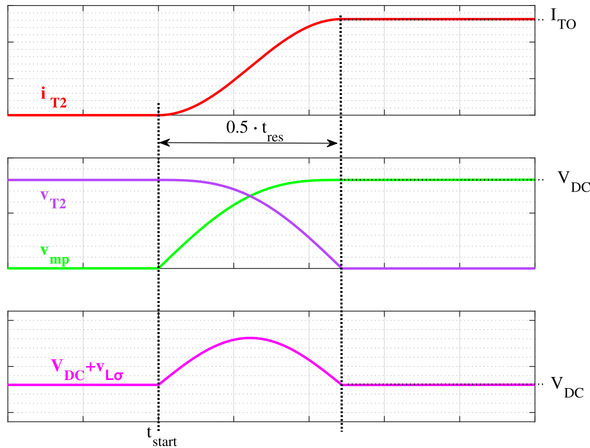

FIGURE 3. Simulated waveforms for a ZOS operating point using the equivalent circuit of Fig. 2.

voltage across T_2. Also, the midpoint voltage v_{mp} and the voltage across the parasitic inductance is shown. It should be noted that the commutation ends after half a period of t_{res}. At that time the current through the transistor T_2 reaches the value of the turn-off current I_{TO}. Oscillations appear neither on the current i_{T2}, nor on the voltage v_{mp}.

In [17] the ZOS phenomenon was encountered during double pulse measurements with SiC MOSFETs. It was stated that, in contradiction to the expected switching behaviour and by decreasing the gate resistor towards zero, the appearing overvoltages decrease as well. A closer analysis of the different correlations and influential factors were not given. In [18] a simulation model was presented to examine the turn-off transient behaviour of SiC MOSFETs. It was observed that the overvoltage was reduced by adjusting the turn-off speed. The ZOS phenomenon was also mentioned in [19, pp. 70 ff.] referred to as ‘‘minimum overshoot switching’’, particularly for gallium nitride-based power integrated circuits.

While the existence of the ZOS phenomenon was already experimentally proven, various aspects were not investigated. In the first publications of ZOS in [16] and [20] it was assumed to be an ideal effect. Transferring this into real-world applications, different aspects need to be examined. Therefore, this article analyzes the ZOS phenomenon further mathematically, including considerations of damping factors as well as nonlinearities of the parasitic capacitances and their effect on ZOS. Furthermore, in this article it is theoretically and experimentally proven that several ZOS operating points for a set DC-link voltage V_{DC} exist. Finally an experimental chapter in which measurements, comparable to the well-known double pulse tests, are conducted. The measurements with different hardware variations verify the derived equations. The goal in this article is not to design a power module, particularly for the ZOS operating area, but to use a commercially available power module and enable it to operate with ZOS and achieve higher efficiency for power electronic systems. The results of the measurements are discussed and an outlook is given.

II. EXTENDED ZOS AREA

In [16] and [20] it was presented that the ZOS phenomenon can be used only for one specific turn-off current I_{TO}, depending on the parasitic elements of the commutation cell and the applied DC-link voltage. In contrast, this chapter shows that ZOS is applicable not only for one, but for multiple turn-off currents $I_{TO,n}$. Contrary to [21], the extended ZOS area is shown for separate parasitic capacitances, as well as experimentally proven in chapter IV. Also, a detailed examination of the influential factors for the extended ZOS area is provided. Fig. 4 shows the simulated waveforms for a ZOS operating point in the extended ZOS area. The first possible ZOS operating point for $n = 1$ can be reached after the time $t_{ZOS,n}$, described by

$$t_{ZOS,n} = \frac{1}{2} \cdot n \cdot t_{res} \tag{7}$$

with t_{res} as the period of the resonant circuit. Every period where the current i_{T2} equals $I_{TO,n}$, a theoretical ZOS operating point exists. During the commutation time $t_{ZOS,n}$, the current i_{T2} is equal to the current i_{Cds2} through the parasitic capacitance C_{ds2}. Depending on the required turn-off current $I_{TO,n}$, the voltage v_{mp} reaches the voltage V_{DC} after $t_{ZOS,n}$. During this time, the voltage v_{Cds2} across the transistor T_2, and therefore the parasitic capacitance C_{ds2} is reduced down to zero. In Fig. 4 the simulated waveforms for $n = 5$ are depicted. At the time $t_{ZOS,5}$ the voltage v_{mp} reaches the DC-link voltage V_{DC} with no overvoltage oscillations. At that point, the anti-parallel diode D_2 shorts the parasitic capacitance C_{ds2} and becomes the current carrying device. It must be pointed out that the current through the parasitic capacitance is physically the same current as through the body diode D_2. The commutation process ends after the time $t_{ZOS,n}$.

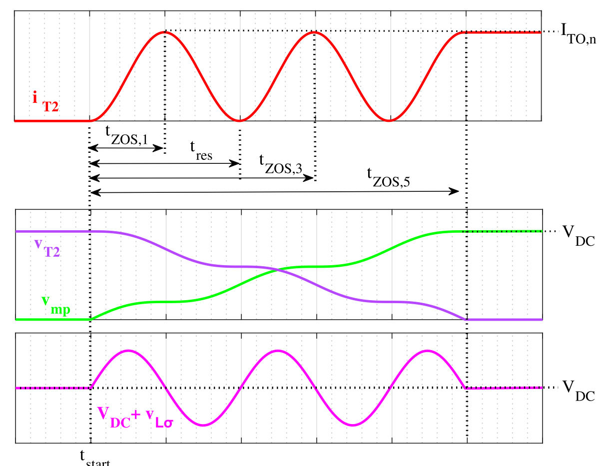

FIGURE 4. Simulated waveforms of an operating point in the extended ZOS area for $n = 5$ using the equivalent circuit of Fig. 2.

To calculate the turn-off current $I_{\mathrm{TO},n}$ of the extended ZOS area, the original equation (6) is extended to

$$I_{\mathrm{TO},n} = \frac{V_{\mathrm{DC}}\sqrt{\frac{(C_{\mathrm{ds1}}+C_{\mathrm{ds2}})^3}{C_{\mathrm{ds1}}C_{\mathrm{ds2}}L_\sigma}}}{n\pi} \tag{8}$$

with $n = 2 \cdot i + 1 : i \in \mathbb{N}_0$. Equation (8) is only valid for linear capacitances. The impact of nonlinear capacitances on the ZOS operating point will be addressed in section III-C. In the consideration of Fig. 2, the value of the step current source equals $I_{\mathrm{TO},n}$ determined by (8). With more than one operating point where ZOS is possible, the field of applications where the ZOS technique can be used is broadened. In Fig. 5, the different operating points in the extended ZOS area are depicted, calculated with an exemplary circuit of $C_{\mathrm{ds1}} = C_{\mathrm{ds2}} = 2\,\mathrm{nF}$ and $L_\sigma = 15\,\mathrm{nH}$ at various DC-link voltages V_{DC}.

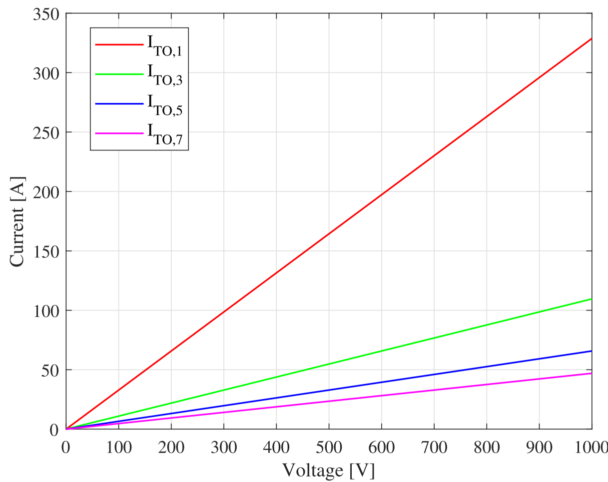

FIGURE 5. Visualization of the turn-off currents in the extended ZOS area.

In power converters, an active power control is crucial. Applying the initial ZOS technique of [16] in power converters means that, for each voltage V_{DC}, only one turn-off current I_{TO} is possible. In that case, only one operating point with constant power can be obtained. In the extended ZOS area, several operating points with the corresponding current $I_{\mathrm{TO},n}$ can be achieved. Other techniques of power control to obtain ZOS in a power converter were given in [16], which include methods such as the usage of burst-mode or valley skipping. However, multiple operating points in the extended ZOS area will simplify the control of power converters. For an usual buck- or boost-converter with a symmetrical half-bridge topology, the boundary conduction mode was proposed.

A. MATHEMATICAL ANALYSIS

In the following, the equations for an analytical description during the commutation time are derived. For this analysis, only the devices that play an active part as depicted in Fig. 2 are considered. The current $i_{\mathrm{Cds2}}(t)$ through the parasitic capacitance C_{ds2} can be calculated with

$$i_{\mathrm{Cds2}}(t) = \frac{2 \cdot I_{\mathrm{TO},n} C_{\mathrm{ds2}} \cdot \sin^2\left(\sqrt{\frac{0.25 \cdot (C_{\mathrm{ds1}}+C_{\mathrm{ds2}})}{C_{\mathrm{ds1}}C_{\mathrm{ds2}}L_\sigma}}\, t\right)}{C_{\mathrm{ds1}} + C_{\mathrm{ds2}}}. \tag{9}$$

The voltage $v_{\mathrm{mp}}(t)$ can be expressed by

$$v_{\mathrm{mp}}(t) = \frac{I_{\mathrm{TO},n}\,(C_{\mathrm{ds2}} \cdot \sin(t\,\omega) + C_{\mathrm{ds1}} t\,\omega)}{C_{\mathrm{ds1}}\,(C_{\mathrm{ds1}} + C_{\mathrm{ds2}})\,\omega} \tag{10}$$

with

$$\omega = \sqrt{\frac{C_{\mathrm{ds1}} + C_{\mathrm{ds2}}}{C_{\mathrm{ds1}}C_{\mathrm{ds2}}L_\sigma}}. \tag{11}$$

The voltage over the parasitic capacitance C_{ds2} can be used as an indicator of how long the commutation process requires to end. After the voltage v_{Cds2} crosses the threshold voltage of the diode, the diode shorts the parasitic capacitance C_{ds2}. This occurs after the time $t_{\mathrm{ZOS},n}$ for an ideal ZOS operating point. The equation for the voltage v_{Cds2} is expressed by

$$v_{\mathrm{Cds2}}(t) = V_{\mathrm{DC}} - \frac{I_{\mathrm{TO},n}\,(t\omega - \sin(t\omega))}{(C_{\mathrm{ds1}} + C_{\mathrm{ds2}})\,\omega}. \tag{12}$$

The voltage across the parasitic inductance is expressed by

$$v_{\mathrm{L}\sigma}(t) = \frac{I_{\mathrm{TO},n}}{C_{\mathrm{ds1}}\omega} \cdot \sin(t\omega). \tag{13}$$

The equations (9) to (13) are only applicable for $t_{start} < t < t_{\mathrm{ZOS},n}$ and for the assumption of an ideal current step of an infinite slope. During this time, the current through the diode D_1 is negligible. After the commutation time $t_{\mathrm{ZOS},n}$, the diode D_2 shorts the parasitic capacitor C_{ds2} and ends the commutation process.

The optimal ZOS operating point can only be obtained if the matching turn-off current $I_{\mathrm{TO},n}$ is set. Voltage oscillations can be expected when the turn-off current $I_{\mathrm{TO},n}$ cannot be reached. If the turn-off current $I_{\mathrm{TO},1}$ is considered to be the maximum appearing current, the highest possible overvoltage is present for $n = 2$. The maximum appearing overvoltage of v_{mp} results in equation

$$V_{\mathrm{mp,max}} = V_{\mathrm{DC}} + I_{\mathrm{TO},2}\sqrt{\frac{L_\sigma}{C_{\mathrm{ds1}}}}. \tag{14}$$

Fig. 6 visualizes the expected overvoltages at v_{mp} around the extended ZOS operating points. The overvoltages were calculated with an exemplary circuit, where $C_{\mathrm{ds1}} = C_{\mathrm{ds2}} = 2\,\mathrm{nF}$ and $L_\sigma = 15\,\mathrm{nH}$, and a DC-link voltage of $V_{\mathrm{DC}} = 800\,\mathrm{V}$. For even numbers of n the calculated turn-off current $I_{\mathrm{TO},n}$ results in local maxima of overvoltage, and for odd numbers of n ZOS is achieved, resulting in no overvoltages at v_{mp}.

After the commutation time $t_{\mathrm{ZOS},n}$, the parasitic capacitor C_{ds2} is shorted by the diode D_2, which results in a change of the resonant frequency. The resonant frequency for the time $t > t_{\mathrm{ZOS},n}$ can be calculated by

$$f_{\mathrm{res}} = \frac{1}{2\pi\sqrt{L_\sigma C_{\mathrm{ds1}}}}. \tag{15}$$

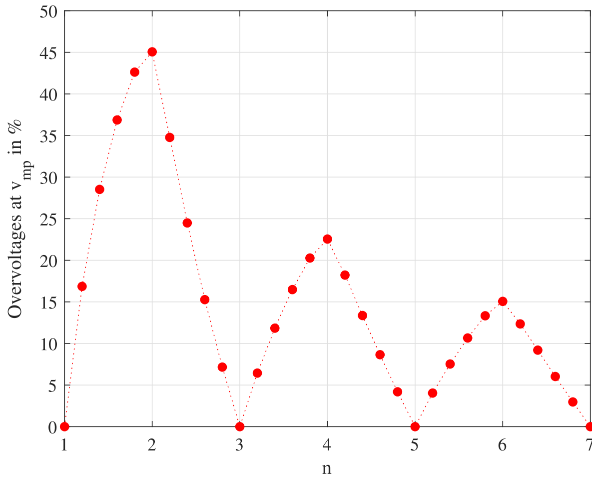

FIGURE 6. Visualization of the expected overvoltages in between ideal ZOS operating points.

The previous equations suggest that different values of parasitic capacitances can also be used. For an unsymmetrical use of the parasitic capacitances C_{ds1} and C_{ds2} (8) still determines the turn-off current, which leads to the least possible overvoltage. However, in the case of unsymmetrical parasitic capacitances, some overvoltage oscillations are inevitable. For the case where $C_{ds2} > C_{ds1}$, the current through the parasitic capacitor $i_{Cds2}(t_{ZOS,n})$ at the end of the commutation is greater than the turn-off current $I_{TO,n}$, which leads to high overvoltages. For $C_{ds2} < C_{ds1}$, the current $i_{Cds2}(t_{ZOS,n})$ is smaller than $I_{TO,n}$ which also creates overvoltages, but at lower levels than the former case.

III. INFLUENTIAL FACTORS FOR ACHIEVING ZOS

In the following, additional aspects that influence ZOS are examined. The equivalent circuit depicted in Fig. 2 is extended to a more realistic circuit with damping factors and nonlinear behaviour of the parasitic capacitances. A more realistic switching speed of the transistor compared to the instantaneous step current source is also examined. Each aspect is analyzed individually.

A. ANALYSIS OF A DAMPED CIRCUIT

Firstly, the influence of a damping factor in the form of an ohmic resistance is examined. The ohmic resistance inherently exists due to copper traces on the PCB and busbars as well as the R_{dson} of the MOSFETs and the equivalent series resistance (ESR) of the DC-link capacitor. For this analysis an equivalent resistor R_{DC} is placed between D_2 and L_σ, depicted in Fig. 7.

The derivation of the current through the parasitic capacitance C_{ds2} in this set-up is also derived with the use of an ideal current step and leads to

$$i_{Cds2,R}(t) = \frac{I_{TO,n} C_{ds2} e^{-\zeta t}\left(e^{\zeta t} - \cos(\frac{t\omega_R}{2})\right)}{C_{ds1} + C_{ds2}} - \frac{I_{TO,n} C_{ds2} R_{DC} e^{-\zeta t} \sin(\frac{t\omega_R}{2})}{L_\sigma \omega_R (C_{ds1} + C_{ds2})} \quad (16)$$

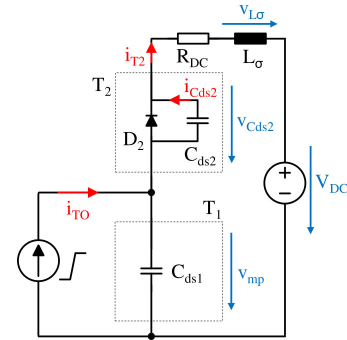

FIGURE 7. Equivalent circuit during commutation with damping factor.

where

$$\omega_R = \sqrt{\frac{4\,(C_{ds1} + C_{ds2})}{C_{ds1} C_{ds2} L_\sigma} - \frac{R_{DC}^2}{L_\sigma^2}} \quad (17)$$

and $\zeta = \frac{R_{DC}}{2L_\sigma}$. The influence of the introduced resistance R_{DC} on the current $i_{Cds2,R}$ through the parasitic capacitance C_{ds2} is displayed in Fig. 8. The waveforms are calculated with an exemplary circuit, consisting of $C_{ds1} = C_{ds2} = 2\,\text{nF}$ and $L_\sigma = 15\,\text{nH}$ in the extended ZOS area with $n = 5$. The DC-link voltage V_{DC} was set to 800 V.

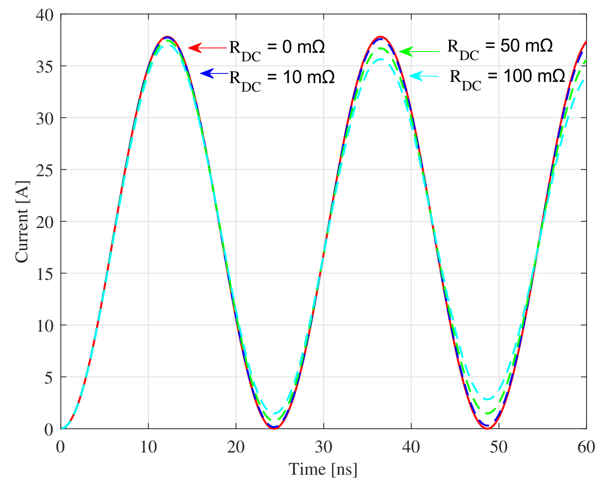

FIGURE 8. Calculated waveforms of $i_{Cds2,R}(t)$ at different values for R_{DC}.

The voltage over the parasitic capacitance C_{ds2} is represented by the following equation

$$\begin{aligned} &v_{Cds2,R}(t) \\ &= V_{DC} - \frac{I_{TO,n} e^{-\zeta t}}{L_\sigma \omega_R (C_{ds1} + C_{ds2})^2} \\ &\quad \times \Bigg[\left(C_{ds1} C_{ds2} R_{DC}^2 - (2C_{ds2} + 2C_{ds1})\, L_\sigma\right) \sin(\frac{t\omega_R}{2}) \\ &\quad + [(C_{ds2} + C_{ds1})\, L_\sigma t - C_{ds1} C_{ds2} L_\sigma R_{DC}]\omega_R e^{\zeta t} \\ &\quad + C_{ds1} C_{ds2} L_\sigma R_{DC} \omega_R \cos(\frac{t\omega_R}{2}) \Bigg]. \end{aligned} \quad (18)$$

The commutation time $t_{ZOS,n}$ changes when a resistance is introduced in the circuit of Fig. 2. For this reason, the commutation time with a resistance is expressed by $t_{ZOS,n,R}$. The difference between $t_{ZOS,n}$ and $t_{ZOS,n,R}$ is best seen by numerically evaluating the required time until $v_{Cds2,R} = 0\,V$ and $v_{Cds2} = 0\,V$. A universal derivation for the damping influence on the time $t_{ZOS,n,R}$ is not provided. Differential equations of third order do not have a general solution. As an approximation, the third order differential equation can be reduced to a second order differential equation to estimate the effective damping factor. However, in this article, the influence of damping factors is shown with an exemplary circuit. Considering the influence of a damping factor, for ZOS operating points of a higher order of n, a certain overvoltage is inevitable since the matching turn-off current $I_{TO,n}$ cannot be reached. In real applications the value of R_{DC} is kept to a minimum for small conduction losses. However, to design a ZOS switching cell it needs to be considered as well. An approximation for the appearing overvoltages, dependent on the mismatch in $I_{TO,n}$, can be calculated by simulation or a numerical approach. For a numerical approach, the equations during and after commutation must be derived, while also considering the difference in the time $t_{ZOS,n,R}$. The direct effect on the appearing overvoltage depending on the introduced resistance R_{DC} is displayed in Fig. 9. In contrast to Fig. 6, only the appearing overvoltages at the ZOS operating points for odd numbers of n are calculated and depicted for a better visibility.

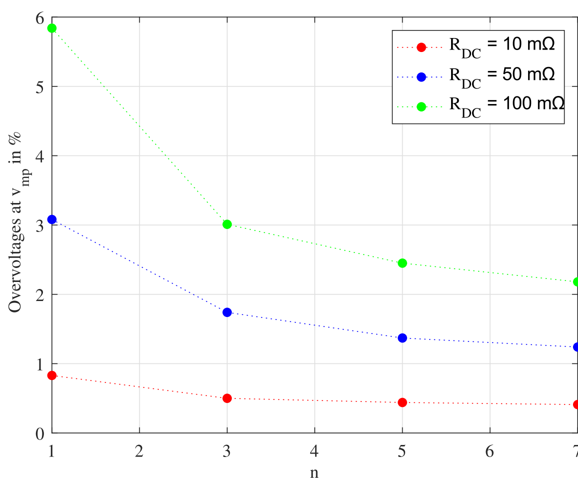

FIGURE 9. Appearing overvoltage dependent on introduced resistance R_{DC}.

B. INFLUENCE OF THE SWITCHING SPEED

The ZOS operating points highly depend on the switching speed of the transistors. The switching speed of the transistors depends on the current capability of the gate driver unit and the external and internal gate resistors. During a turn-off event, the gate capacitance of the transistor needs to be discharged. The required time for discharging the gate capacitance defines how fast the turn-off event of the transistor is. In the previous chapters the switching speed of the transistors were assumed to be infinite. Therefore, the equations in II-A were derived with an ideal current step. In the following, the current step is altered to a current ramp, which resembles the current waveform of a transistor's turn-off event more realistically. The current slope is expressed by using the Laplace transform of the following function

$$I_{sl}(s) = \frac{I_{TO,n}}{t_{sl}s^2}\left(1 - e^{-s\cdot t_{sl}}\right) \tag{19}$$

where t_{sl} defines the time until the current ramp reaches its end value $I_{TO,n}$. In the time domain, this corresponds to the following equation

$$i_{sl}(t) = \frac{(I_{TO,n}t_{sl} - I_{TO,n}t)\Phi_{(t-t_{sl})} + I_{TO,n}t}{t_{sl}} \tag{20}$$

with Φ as the Heaviside step function. The equation for the current $i_{Cds2,sl}$ can be derived with the aforementioned current slope and results in

$$\begin{aligned} i_{Cds2,sl}(t) = &\frac{-I_{TO,n}C_{ds2}}{\omega_{sl}t_{sl}\left(C_{ds1} + C_{ds2}\right)} \\ &\times\left[\Phi_{(t-t_{sl})}\sin(\omega_{sl}\left(t_{sl} - t\right)) + \sin(\omega_{sl}t)\right. \\ &\left.+\left((\omega_{sl}t - \omega_{sl}t_{sl})\,\Phi_{(t-t_{sl})} - \omega_{sl}t\right)\right] \end{aligned} \tag{21}$$

where

$$\omega_{sl} = \sqrt{\frac{C_{ds1} + C_{ds2}}{C_{ds1}C_{ds2}L_\sigma}}. \tag{22}$$

Fig. (10) uses (21) to show the impact on the current through the parasitic capacitance C_{ds2} with different current slopes, represented by t_{sl}. For the calculation, the same values as in the previous examples are used: $C_{ds1} = C_{ds2} = 2\,nF$ and $L_\sigma = 15\,nH$ at $V_{DC} = 800\,V$ at a ZOS operating point with $n = 5$. It needs to be considered that the variation of the slope t_{sl} influences the ZOS operating points. No noticeable current oscillations at the current $i_{Cds2,sl}(t)$ for a current $i_{sl}(t)$ with a slope of $t_{sl} = 24.3\,ns$ are observed. Also, $i_{Cds2,sl}(t)$ reaches half the value of the desired turn-off current $I_{TO,5}$.

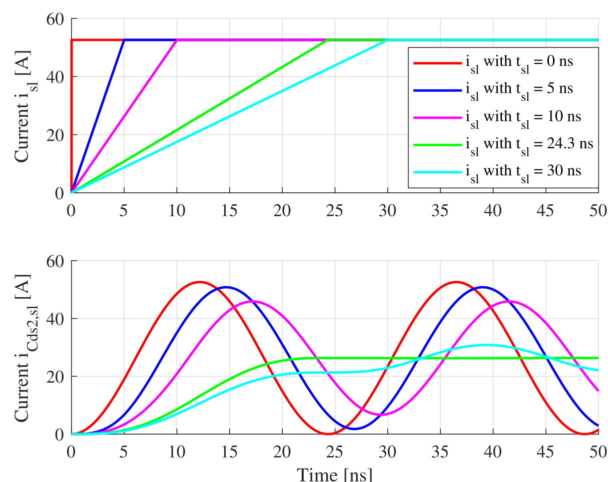

FIGURE 10. Calculated waveforms of $i_{Cds2,sl}(t)$ with different current slopes, represented by t_{sl}.

However, the resulting overvoltage in v_{mp} is still present, since the reached turn-off current does not match the required turn-off current $I_{\mathrm{TO},n}$. This implies that the turn-off event must be completed before the time duration of one period of the resonant frequency t_{res} as defined in (3). The steeper the current slope is, the higher the peak value of the current $i_{\mathrm{Cds2,sl}}$ will become, which results in lower overvoltage ringing. This corresponds directly to the requirement of a specific gate driver unit for enabling ZOS. The gate driver needs to be able to turn off the transistor as fast as possible. Therefore, a gate driver unit with a high current sink ability and a low impedance path is required.

C. CONSIDERATION OF THE NONLINEAR CAPACITANCES

In the previous chapters the capacitances C_{ds1} and C_{ds2} were considered to be linear. In transistors such as SiC MOSFETs, those parasitic capacitances are greatly nonlinear. This nonlinearity needs to be examined in terms of its influence on the ZOS phenomenon. As a consequence of including the nonlinear capacitances in the circuit, the differential equations cannot be solved analytically. This limitation is bypassed by simulating an adjusted circuit with the program LTspice.

The capacitance characteristics of transistors are usually given in the datasheets, provided by the manufacturer based on a standardized measurement procedure. In the following, the nonlinear capacitances of the SiC power module FS03MR12A6MA1B by Infineon [22] are used. In the datasheet, the input capacitance C_{iss}, the output capacitance C_{oss} and reverse transfer capacitance C_{rss} are provided. For the output capacitance C_{oss} the following relation applies: $C_{\mathrm{oss}} = C_{\mathrm{ds}} + C_{\mathrm{gd}}$. The drain-source capacitance C_{ds} can therefore be determined by $C_{\mathrm{ds}} = C_{\mathrm{oss}} - C_{\mathrm{rss}}$, since the reverse transfer capacitance C_{rss} equals the gate-drain capacitance C_{gd}. In the following, only the drain-source capacitance will be considered.

To simulate the nonlinear parasitic capacitors in the simulation program LTspice, some adjustments need to be made. LTspice allows the representation of nonlinear capacitances by using an equation that describes the electric charge. In this case, the electric charge Q_{Cds} is calculated from the extracted information of C_{ds} over the applied voltage V_{ds}. The parasitic drain-source capacitances' charge $Q_{\mathrm{Cds}}(v_{\mathrm{ds}})$ for the Infineon SiC power module is interpolated by

$$Q_{\mathrm{Cds}}(v_{\mathrm{ds}}) = 79 \cdot (\tilde{V}_{ds} + 1)^{0.5}\,\mathrm{nC} \tag{23}$$

with $\tilde{V}_{\mathrm{ds}} = \frac{V_{\mathrm{ds}}}{1\,\mathrm{Volt}}$. The dimensionless value of $\tilde{V}_{\mathrm{ds}}$ is added by one, to eliminate a calculating error in LTspice that occurs for $\tilde{V}_{\mathrm{ds}} = 0$. In [22] the information of the capacitances were only given up to a drain-source voltage of 600 Volt. For that reason, the graphs of the extracted values of C_{ds} and Q_{ds} are not exceeding 600 Volt. Fig. 11 shows the difference between the extracted values of C_{ds} from the datasheet and the corresponding charge Q_{Cds} that was calculated, as well as the approximated charge calculated with (23). The approximated function of the electric charge is used as input for the LTspice simulation.

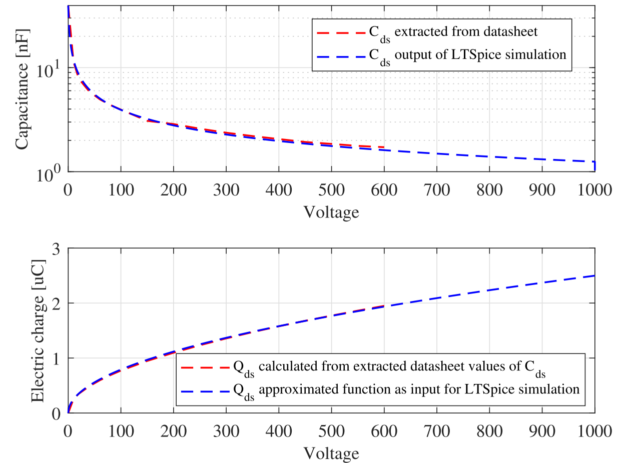

FIGURE 11. Datasheet values of the SiC power module and implemented function of nonlinear capacitances in LTspice.

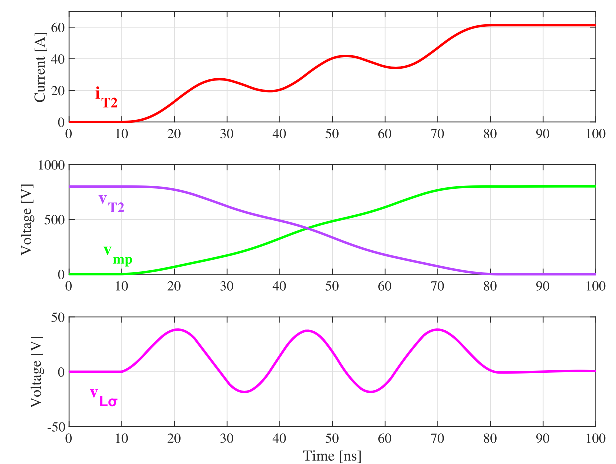

FIGURE 12. Simulated waveforms for a ZOS operating point at $I_{\mathrm{TO,5}}$ with nonlinear capacitances.

Fig. 12 displays the results of the LTspice simulation with the approximated nonlinear capacitances, with $L_{\sigma} = 15\,\mathrm{nH}$ and $n = 5$ at $V_{\mathrm{DC}} = 800\,\mathrm{Volt}$. Comparing the results of the simulation to Fig. 4, it is noticeable that the current i_{T2} is ramping up by each period and not returning to zero. The nonlinear behaviour of the parasitic capacitance, depending on the applied drain-source voltage of the transistor, suggests that the initial equation (8) is not precisely calculating the required turn-off current $I_{\mathrm{TO},n}$ for a ZOS operating point. Converting (8) by only replacing the capacitances C_{ds1} and C_{ds2} with the voltage-dependent electric charge is not sufficient. Equation (8) only applies if the resonant frequency of the commutation cell is constant. In case of nonlinear capacitances, the resonant frequency varies depending on the applied voltage over the capacitances. For a lower voltage the capacitance is higher, resulting in a lower resonant frequency. For a higher voltage, the capacitance is lower, resulting in a higher resonant frequency. In the example of the Infineon SiC power module, the capacitance varies from 33.55 nF to 1.44 nF, which leads to a resonant frequency

range of 7.09 MHz to 34.24 MHz with the aforementioned $L_\sigma = 15$ nH.

Fig. 13 points out the difference of the turn-off current $I_{\mathrm{TO},n}$ calculated by the initial equation (8) and the simulated turn-off current that is necessary when the circuit is modeled with nonlinear capacitances. The value of the linear capacitances of C_{ds1} and C_{ds2} is set to 1.69 nF, which is taken from the datasheet of the aforementioned SiC power module. It can be observed that the initial equation (8) is not leading precisely to the value of the required turn-off current $I_{\mathrm{TO},n}$. The required turn-off current can be better predicted by following the proposed approach, where the datasheet values are used and implemented into a simulation tool. The experimental verification of this approach will be shown in chapter IV-D.

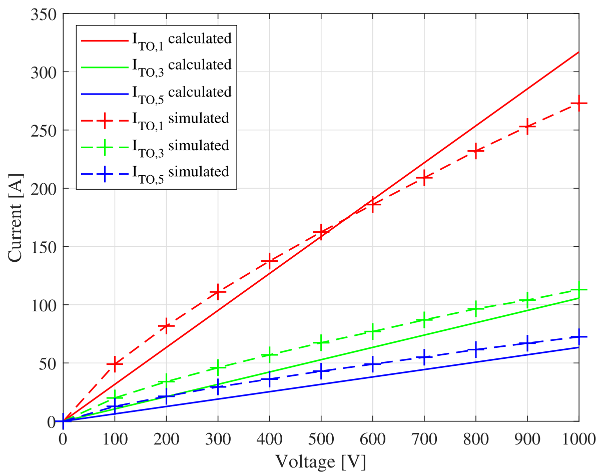

FIGURE 13. Difference of calculated and simulated turn-off current $I_{\mathrm{TO},n}$ without and with nonlinear capacitances.

D. ADDITIONAL INFLUENCES

1) INFLUENCE OF SELF- AND MUTUAL INDUCTANCES

In the previously used equivalent circuit of Fig. 2, the parasitic inductance L_σ was modeled as a single inductance, which is sufficient for the analysis, but excludes the differentiation between self- and mutual inductance. In [23] it is stated that the self-inductance can be considered to be constant in high frequencies. The mutual inductance is not depending on the frequency, but presents a challenge to model accurately. In [24] the mutual inductance between parallel current paths is analyzed in detail. Especially for a parallelization of transistors in a power module, an enhanced parasitic inductance model is required. In [25] a power module with parallel transistors is examined, pointing out that the DBC layout effectuates the switching behaviour of the transistors. It was stated that a current coupling effect leads to a variance in the gate-source voltage of each of the paralleled transistors. It was proposed to modify the layout of the power module by adjusting the length of the wire bonds, and connecting the transistor bare dies individually to the DBC. Therefore, the parasitic inductance of each transistor was severally adapted.

It is certain that a more profound model of the parasitic inductance L_σ is beneficial for a more precise calculation of the turn-off current $I_{\mathrm{TO},n}$, especially to design a power module that specifically uses the ZOS technique. The extension of the parasitic inductance model with an analysis of self- and mutual inductances is part of future work.

2) INFLUENCE OF FORWARD VOLTAGE OF THE BODY DIODE

The body diode of the SiC MOSFET has characteristically a high forward voltage. The forward voltage of the exemplary SiC power module FS03MR12A6MA1B is between 4.42 Volt to a maximum of 6.15 Volt, depending on the drain current. The forward voltage of the diodes has a direct impact on the calculation of the turn-off current $I_{\mathrm{TO},n}$. When the forward voltage of the body diode is considered, (8) must be adjusted to

$$I_{\mathrm{TO},n} = \frac{(V_{\mathrm{DC}} + V_{\mathrm{F}})\sqrt{\frac{(C_{\mathrm{ds1}}+C_{\mathrm{ds2}})^3}{C_{\mathrm{ds1}}C_{\mathrm{ds2}}L_\sigma}}}{n\pi} \tag{24}$$

with V_{F} as the forward voltage of the body diode.

3) OTHER PARASITIC ELEMENTS AND INFLUENCES

The influences of additional parasitic capacitances, such as the gate-source and gate-drain capacitances as well as the parasitic capacitances from each transistor to the heatsink were not assessed.

Another influence for ZOS operating points is the varying temperature. This aspect was not focused on in this article. A changing temperature during operation impacts a variety of parameters.

IV. MODEL VERIFICATION

In this chapter, the previously derived models and mathematical analysis are verified by experimental measurements. The aforementioned Infineon SiC power module is used. A gate driver unit was developed, that considers the specific requirements for a low impedance and high current sink ability mentioned in chapter III-B. Fig. 14 shows the used test setup. The measurements only investigate the turn-off event. Therefore, the current is ramped up only once and then switched off by the transistor T_1.

Table 1 lists the used equipment and its maximum available bandwidths for the measurements. The current probe measures the current through the inductor of the test setup. The Rogowski probe measures the current through the transistor T_1 at the DC- terminal. Both current measurements were used to measure the turn-off current $I_{\mathrm{TO},n}$. The voltage probe measures the voltage v_{mp} across the low side transistor T_1. The DC-link capacitance C_{DC} is designed to connect all three phases of the SiC power module to the DC-link capacitor PCB. However, for the pulse tests, the other two phases were physically isolated from the DC-link capacitor PCB. The capacitance C_{DC} is built out of 21 parallel capacitors (manufacturer product number: B32676T8205K000 by EPCOS - TDK Electronics), which gives a total capacitance of 42 μ F.

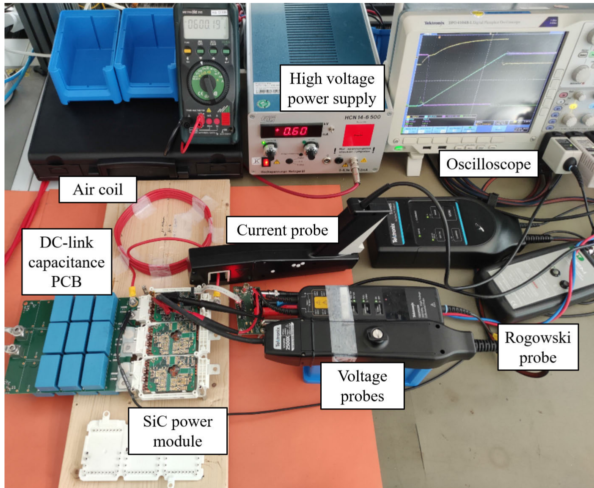

FIGURE 14. Test setup for pulse-test measurements.

TABLE 1. Used measurement equipment.

Equipment	Device name	Bandwidth
Oscilloscope	Tektronix DPO4104B-L	1 GHz
Voltage probe	Tektronix TIVH05	500 MHz
Rogowski probe	CWTUM/6/R	30 MHz
Current probe	Tektronix TCP0150	20 MHz
Impedance analyzer	Agilent 4294A	/
Milliohmmeter	Sefelec MO1	/

An air coil was used due to no saturation, with an inductance of 8.7 μ H.

The ESL and ESR of the DC-link capacitor PCB is measured with an impedance analyzer. This is done to adjust the value of the parasitic inductance L_σ in the simulation. This allows the comparison of the measurement results directly with the simulation results. With the impedance analyzer, the ESL of the DC-link capacitor PCB is determined to be 15.7 nH with an ESR of 1.926 mΩ. The value of the stray inductance of the SiC power module is given in the datasheet with 8.5 nH, but it is not clearly stated which pathway of the power module is included. Therefore, the parasitic inductance is experimentally determined. A pulse test at a DC-link voltage of $V_{DC} = 600$ V was performed and the resonant frequency was measured. With the information of the resonant frequency in combination with the datasheet value of $C_{ds1} = C_{ds2} = 1.69$ nF at 600 Volt, the parasitic inductance is calculated to a value of $L_\sigma = 21.1$ nH. This value includes the ESL of the capacitor, as well as the parasitic inductance of the power module. Comparing the results that were measured with the impedance analyzer and adding the datasheet value of the stray inductance, the experimentally evaluated value of L_σ matches. It should be noted that for the following tests, the turn-off gate resistance of the gate-driver circuit is set to zero, with a gate-source voltage of +20 Volt and −8.2 Volt. This ensures that the transistor T_1 is turned off as fast as possible.

A. EXPERIMENTAL VERIFICATION OF EXTENDED ZOS AREA

In the following, the indicator for achieving ZOS is the measured midpoint voltage v_{mp}. Also, two additional measurements were included to show the impact and importance of reaching the required turn-off current $I_{TO,n}$. The turn-off current was changed to ten percent above and ten percent below the optimal turn-off current $I_{TO,n}$. In Fig. 15, the measurement results for $I_{TO,1}$ at a DC-link voltage $V_{DC} = 800$ V are shown. It can be observed that there are still voltage oscillations on v_{mp} present. However, the existence of the ZOS phenomenon becomes plainly evident.

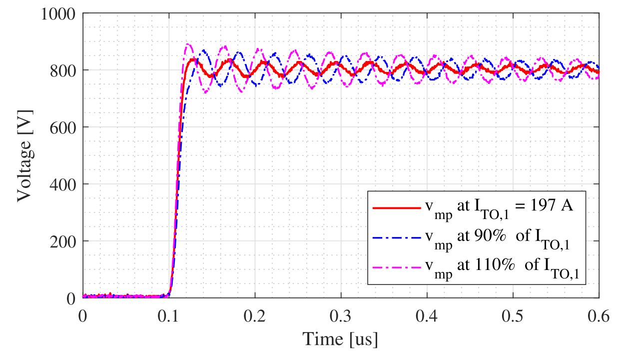

FIGURE 15. Measured midpoint voltage v_{mp} at different values around $I_{TO,1}$.

Fig. 16 and Fig. 17 show the measurement results for $I_{TO,3}$ and $I_{TO,5}$ respectively. It can be seen that, for turn-off currents in the extended ZOS area, the voltage oscillations are further decreased compared to the measurement results at the turn-off current $I_{TO,1}$.

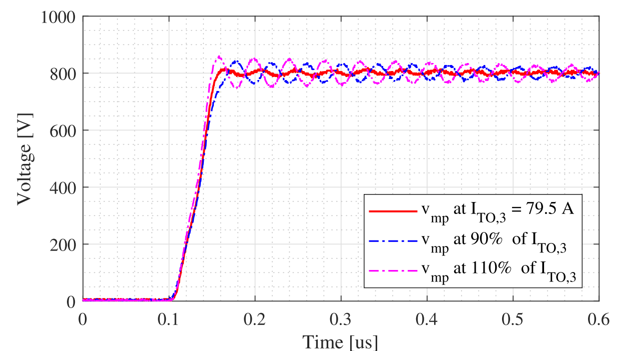

FIGURE 16. Measured midpoint voltage v_{mp} at different values around $I_{TO,3}$.

Fig. 18 shows the midpoint voltage for the turn-off current at $I_{TO,1}$and $I_{TO,2}$. It can be observed that a lower value of $I_{TO,2} = 126$ A compared to $I_{TO,1}$ results in a maximum overvoltage. At a higher turn-off current $I_{TO,1} = 197$ A, the appearing overvoltage is at a local minimum. This verifies the theory of the expected overvoltage for even numbers of n in between the ZOS operating points, as shown in Fig. 6.

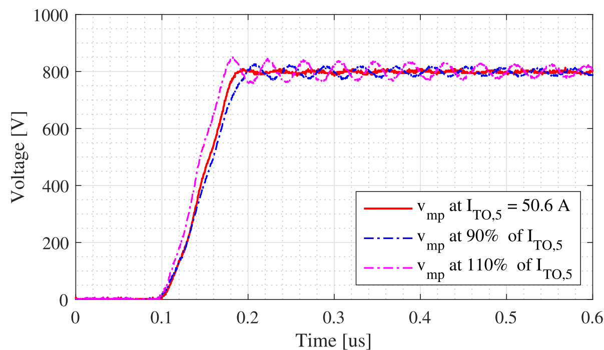

FIGURE 17. Measured midpoint voltage v_{mp} at different values around $I_{TO,5}$.

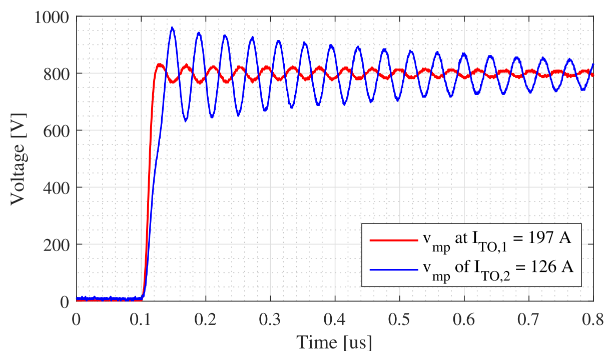

FIGURE 18. Measured midpoint voltage v_{mp} at $I_{TO,1}$ and $I_{TO,2}$.

B. INFLUENCE OF DAMPED CIRCUIT

The total DC-resistance of the commutation cell is determined by measuring the copper resistance and the ESR of the DC-link capacitors, and by taking into account the values of the R_{dson} given by the datasheet. A total resistance of $R_{DC} = 12.36\,\text{m}\Omega$ is measured. To measure the copper resistances, a milliohmmeter MO1 with a precision of 0.05% is used. With this value it is possible to calculate the theoretically appearing overvoltage, introduced by the DC-resistance. Referring to Fig. 9, it can be assumed that for $R_{DC} = 12.36\,\text{m}\Omega$ the appearing overvoltage solely affected by the damping of the DC-resistance is under 1%. The measurements show that the DC-resistance is not the only damping influence. In Fig. 19, the midpoint voltage v_{mp} is measured at a voltage of $V_{DC} = 600\,\text{V}$ for a turn-off current $I_{TO,2}$. The overvoltage for this turn-off current reaches a maximum. For the same operating points, a simulation is performed with the influence of nonlinear capacitances and an introduced DC-resistance of $R_{DC} = 12.36\,\text{m}\Omega$. The envelope curve is calculated with the value of the DC-resistance and determined with a parasitic inductance of L_σ =21.1 nH. The envelope curve only fits for the simulated waveform of v_{mp} and not for the measured waveform. The measured waveform of v_{mp} shows a greater damping. However, it can be observed that the peak overvoltage for the simulated as well as the measured values of v_{mp} are comparable.

It can be assumed that a greater damping factor is present. At high frequencies, the combination of the skin and proximity effects leads to a shifting current distribution in

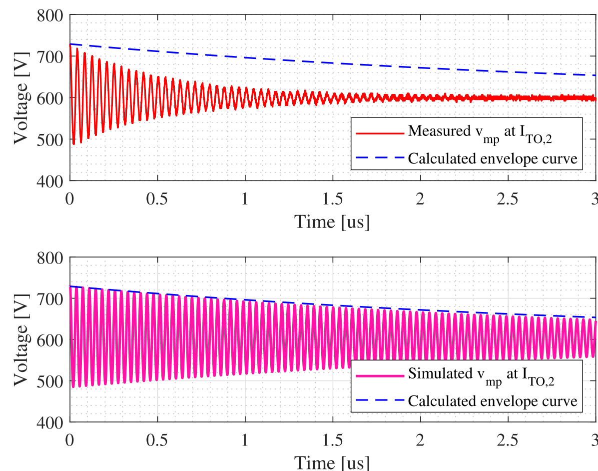

FIGURE 19. Measured and simulated voltage ringing of v_{mp} to investigate influence of damping.

the copper planes, which increases the effective damping factor. Additionally, as mentioned in chapter III-D1, a different model for the parasitic inductance would improve the analysis. Both mentioned influencing factors will be examined as a part of future work.

C. INFLUENCE OF THE SWITCHING SPEED

As mentioned in chapter III-B, to apply ZOS it is essential to have a specific gate driver unit that is able to turn-off the transistor T_1 as fast as possible. To show the impact and necessity of a capable gate driver unit, the turn-off process is slowed down by adding external gate resistors R_{off} of different values. Fig. 20 shows the measured midpoint voltages v_{mp} for the same turn-off current $I_{TO,1}$. It can be observed that even with an external gate resistor of $R_{off} = 1\,\Omega$, the ZOS operating point cannot be reached. For $R_{off} = 0\,\Omega$ an overvoltage peak of 5% is still present. One influencing factor is the internal gate resistor within the SiC power module of $R_{gate,int} = 0.23\,\Omega$.

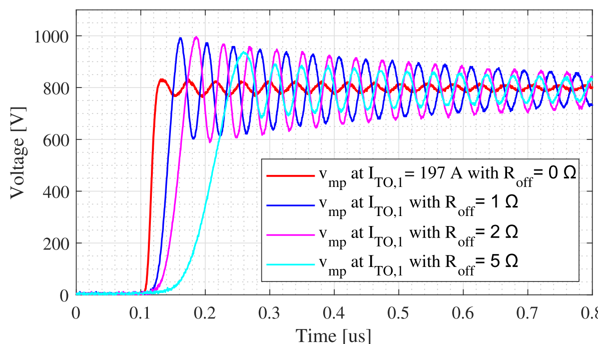

FIGURE 20. Measured midpoint voltage v_{mp} with varied external gate resistors R_{off} at $I_{TO,1}$.

Fig. 21 depicts the measured midpoint voltages v_{mp} for a turn-off current $I_{TO,3}$ in the extended ZOS area.

D. EXAMINATION OF NONLINEAR CAPACITANCES' IMPACT

The influence of the nonlinear behaviour of the parasitic capacitances can be experimentally demonstrated. In Fig. 22,

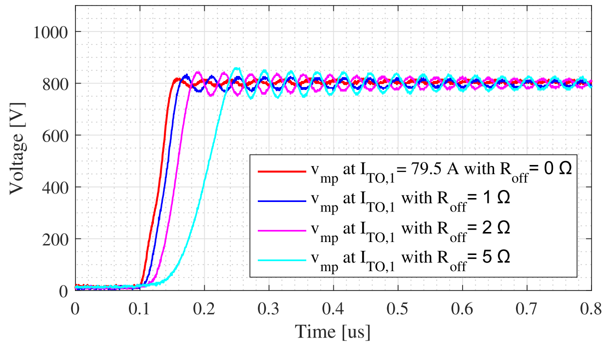

FIGURE 21. Measured midpoint voltage v_{mp} with varied external gate resistors R_{off} at $I_{TO,3}$.

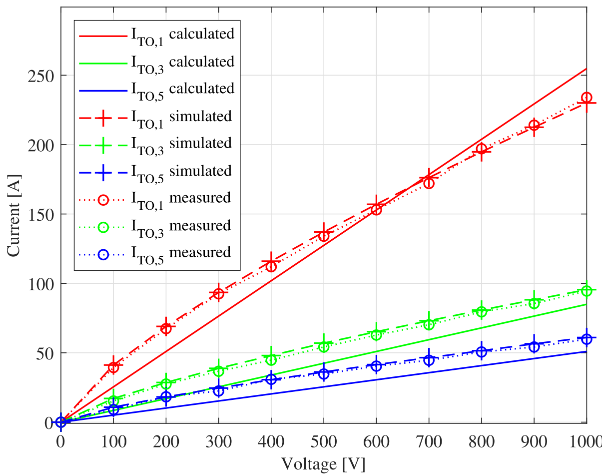

FIGURE 22. Visualization of extended ZOS area with the results of simulation and measurements.

the actual required turn-off currents $I_{TO,n}$ for operating with ZOS over a wide range of the DC-link voltage V_{DC} are measured and compared to the calculated turn-off current and to the simulated turn-off currents, which include the nonlinear behaviour of the capacitances. For the nonlinear capacitances the previously introduced approach in chapter III-C is used. The value of the parasitic inductance in the simulation is adjusted to $L_\sigma = 21.1\,\text{nH}$. The turn-off currents, calculated with (8), use linear capacitances. The value of the linear capacitances were set to $C_{ds1} = C_{ds2} = 1.69\,\text{nF}$, as given in the datasheet. Firstly, in Fig. 22 the difference between the calculated and the measured values can be traced back to the difference of using linear capacitances for the calculated turn-off currents, whereas in reality those parasitic capacitances show nonlinear behaviour. Secondly, the approach of chapter III-C, where the nonlinear capacitances are included in the simulation, can be confirmed by the measurements. The simulated and the measured turn-off currents are matching closely across the wide range of the DC-link voltage V_{DC}.

E. DISCUSSION OF MEASUREMENTS

In the experimental measurements of [20] and [21] the parasitic inductance is enlarged with external wires. In this article's presented measurements, no external parasitic inductances are introduced. In contrast, the aim was to design a low inductance DC-link capacitor PCB to reach high turn-off currents, for better usability in real-world applications. By using low parasitic inductances, it can be ensured that, in an operating point where ZOS cannot be achieved due to faulty control, the appearing overvoltage does not reach a destructive level. Using an increased parasitic inductance as proposed in [21] decreases on the one hand the time when the transistor must be turned off, which lowers the requirement for a special gate driver. On the other hand, increasing the parasitic inductance lowers the maximum turn-off current $I_{TO,n}$ and as mentioned, would lead to great voltage overshoots and oscillations if the turn-off current $I_{TO,n}$ is not reached.

It is also possible to increase the turn-off current by adding ceramic capacitors close to the DC terminals of the module, which effectively leads to a lower parasitic inductance. In doing so, the turn-off currents can be increased by 10 A. However, the introduction of the ceramic capacitors leads to a second resonance, measurable on the midpoint voltage v_{mp}. For this article's measurements, the ceramic capacitors are not used in order to provide clearer measurements.

The measurements, that show the impact of the nonlinear capacitances in Fig. 22, are measured up to 1000 V. At this DC-link voltage for $I_{TO,1}$, the overvoltage peak reaches 1060 V. With an overvoltage of 6%, it can be assumed that by applying ZOS, a wider voltage range of the transistor can be used since the safety margin to the blocking voltage can be reduced.

V. CONCLUSION

This article investigates different influential factors of ZOS. An analytical approach for an equivalent circuit is provided, deriving the formula for the extended ZOS area with individual parasitic capacitances. The influential factors, such as the introduction of a damped circuit and a varying switching speed, are also analyzed. With the developed gate driver unit, it is experimentally proven that multiple ZOS operating points exist. In addition, the importance of a suitable gate driver is shown, by varying the switching speed with adjusted external turn-off gate resistors. The necessity of considering the nonlinear capacitances is also shown. A simulation approach is proposed, which includes the datasheet values of the nonlinear parasitic capacitances. This enables a better prediction of the required turn-off currents to achieve ZOS.

The theoretical aspects are validated with measurements using a commercial SiC power module. The measurements prove, for the first time, that a commercially available SiC power module can be enabled to operate with ZOS. The measurements of the midpoint voltage v_{mp} in the extended ZOS area are shown, confirming that those operating points in the extended ZOS area are usable for real-world applications. It is possible to use the full advantage of ZOS in those additional operating points, with negligible switching losses and voltage overshoots. Diminishing the switching losses enables the design of a more efficient power converter. Also, a higher power density can be achieved, since the active cooling of the power modules can effectively be reduced.

Power converters using the ZOS technique yield lower voltage overshoots and oscillations due to cleaner switching transitions. This leads to a decrease in filtering requirements and achieves EMI compliance with reduced effort. However, to fully benefit from the mentioned advantages of ZOS in a converter, a ZOS-specific power control is required.

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