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RESEARCH ARTICLE

Capacitor-Current-Feedback With Improved Delay Compensation for LCL-Type Grid-Connected Inverter to Achieve High Robustness in Weak Grid

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ABSTRACT To attenuate the resonance of the *LCL* filter, capacitor-current-feedback (CCF) active damping has been extensively adopted in *LCL*-Type grid-connected inverters. Owing to the appearance of a negative damping region caused by the digital control delay, however, the damping performance has significantly deteriorated, thus the system is susceptible to being unstable under weak grid operation. To address this issue, this paper proposes an improved delay compensation method, which can effectively extend the boundary frequency of the positive equivalent resistance region from $f_s/6$ to $f_s/4$. Furthermore, the resonance frequency forbidden region of the *LCL* filter can be eliminated. In doing so, strong robustness against the grid impedance variation and high noise immunity can be achieved. To guarantee the system stability and obtain good control performance after compensation, a detailed parameters design procedure for the current regulator and the CCF coefficient is further presented. At last, experimental results are provided to confirm the theoretical analysis and verify the effectiveness of the proposed delay compensation method.

INDEX TERMS Active damping, grid-connected inverter, LCL filter, delay compensation, weak grid.

I. INTRODUCTION

NOWADAYS, driven by the increasing concern about energy shortage and environmental pollution problems, distributed power generation systems (DPGSs) are attracting growing attention. As the power conversion interfaces between the DPGSs and the public grid, in which, inverter plays a key role in injecting stable and high-quality current into the grid [1], [2].

To reduce the switching harmonics content in the output current, an *L* or *LCL* filter has been widely used, while the total volume required for the *LCL* filter is smaller for the same harmonic attenuation performance [3]. However, an inherent resonance problem is introduced by *LCL* filter, which might lead to system instability. To address this issue, damping methods must be adopted to suppress the resonance peak [4], [5], [6], [7], [8], [9], [10]. Passive damping is a direct way to dampen the *LCL* resonance by inserting a passive resistor in series or parallel with the filter network [4], [5]. This is a simple and effective way while it also introduces into considerable power loss, which is not cost-effective. Compared with passive damping, active damping features high efficiency and flexibility, and it can be implemented in two ways. One is based on digital filters, which are cascading with the current regulator [6]. The other way is based on filter state variables feedback [7], [8], [9], [10]. This article adopts the capacitor-current-feedback (CCF) active damping method, which is extensively used in industry due to its simplicity and effectiveness [10].

For obtaining high flexibility, the grid-connected inverter is most digitally controlled. Considering the influence of digital control delay [11], however, the CCF active damping performance is weakened [12], [13], [14], [15], [16]. As revealed in [12], it is no longer equivalent to a pure

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resistance but an impedance that varies with the frequency of the system. In [13], one-sixth of the sampling frequency $f_s/6$ is regarded as the critical frequency, signed as f_{cri}, which is the boundary frequency of the positive equivalent resistance region. When the actual resonance frequency is higher than the critical frequency, the open-loop unstable poles would be introduced into the control loop, leading to nonminimum-frequency behavior. Note that, if the resonance frequency is too close to the critical frequency, the system is apt to be unstable due to the inadequate gain margin. So, f_{cri} and its vicinity can be defined as the resonance frequency forbidden region [14]. In particular, when the resonance frequency is equal to $f_s/6$, the system stability cannot be maintained [16]. Therefore, the digitally controlled grid-connected inverter with CCF active damping is susceptible to instability under weak grid conditions.

To mitigate the adverse effect of digital control delay on the CCF active damping, numerous solutions are proposed [12], [17], [18], [19], [20], [21], [22], [23], [24], [25], [26], [27], [28], [29], [30], [31], [32], [33], which can be classified into two types. One is to directly reduce the digital control delay. In [12] and [17], the computation delay is reduced by shortening the time interval between the signal sampling instant and the PWM reference update instant. However, signal aliasing and switching noises might be introduced. To overcome this drawback, the real-time computation scheme is proposed in [18] by immediately updating the computed PWM reference. Nevertheless, it is highly dependent on DSP computation performance. In [19], the multiple sampling scheme is proposed, which is equivalented to reducing the computation delay by increasing the sampling frequency. Nevertheless, it is also susceptible to aliasing and switching noise.

Another method is to use the model-based predictive control [20], [21], [22] or the model-free phase-lead compensator [23], [24], [25], [26], [27], [28], [29], [30], [31] to compensate the digital control delay. In [20], the smith predictor is proposed to alleviate the delay effect, which is effective and more readily implemented. However, it is sensitive to the variation of system parameters and operating conditions. State observer can also be used to calculate the next beat of system state variables for compensating the computation delay [21], [22]. However, it also needs modeling error mitigation, which imposes extra computation burdens. In [23] and [24], the *RC* damping and the *RLC* damping are respectively proposed by feeding back capacitor current with a first-order high-pass filter (HPF) and a second-order one, which can extend the boundary frequency of the equivalent resistance region from $f_s/6$ to $f_s/3$. Nevertheless, it is subject to noise amplification, which is introduced by the HPF. Based on the graphical evaluation, Lu et al. [25] investigate several phase-lead compensators, e.g., linear predictor [26], first-order phase-lead compensator [27], [28], second-order generalized integrator [29] and propose a novel phase-lead compensator. Those above-mentioned compensators are revealed that can compensate a maximum time delay of half-sampling period. The characteristic of them are that the higher phase compensation, the higher gain in high frequency region. To compensate more phase-lag resulting by the digital control delay, a second-order phase-lead compensator is respectively inserted into the CCF path and the feedforward path [30], [31], which has significant phase-lead performance and higher magnitude response near the Nyquist frequency. However, those delay compensation methods put more attention on the phase-lead performance of the compensator while neglecting the high magnitude response in high frequency region, which introduces significant noise amplification and increases the difficulty of control parameters design.

In this paper, an improved delay compensation method with better noise immunity performance is proposed. After compensation, the positive equivalent resistance can cover the range of $(0, f_s/4)$, and the resonance frequency forbidden region is eliminated. Thus, the system robustness against the grid impedance variation is enhanced and noise amplification can be relieved.

The rest of this paper is organized as follows. In Section II, the configuration of the system is described and the mathematical model in discrete-domain is presented. In Section III, the effect resulting by digital control delay on the damping performance is investigated. In Section IV, an improved delay compensation method with better noise immunity performance is proposed and the stability analysis of the system after compensation is further analyzed detailedly. For obtaining good control performance, the detailed parameters design procedure is also presented. In Section V, the experimental results are shown to verify the validity of the proposed delay compensation method. Finally, Section VI concludes this paper.

II. MODELING THE DIGITAL CONTROLLED LCL-TYPE GRID-CONNECTED INVERTER

Fig. 1 shows the configuration of a digital controlled single-phase *LCL*-Type grid-connected inverter, in which V_{in} is the DC voltage, and v_g denotes the grid voltage. L_1 is the inverter-side inductor, C is the capacitor filter, and L_2 is the grid-side inductor, which constitutes the *LCL* filter. H_{i1} and H_{i2} are the sense coefficient of the capacitor current i_c and the grid-side current i_g, respectively. The main purpose is to regulate i_g to be sinusoidal and synchronized with the voltage at the point of common coupling (PCC). So, the demanded amplitude I^*, which is generated by the outer voltage loop, and the phase θ extracted by the Phase-locked loop (PLL) from v_{PCC} constitute the current reference i_{ref}. The grid impedance at PCC composes of resistance and inductance. Since grid resistance can contribute to damping to some degree, thus grid resistance is ignored to emulate the worst situation. A proportional-resonant (PR) current controller G_R is applied to achieve zero steady-state error tracking.

According to Fig. 1, the continuous-domain control block diagram of the digitally controlled *LCL*-Type grid-connected inverters is given in Fig. 2(a), where $1/T_s$ is represented

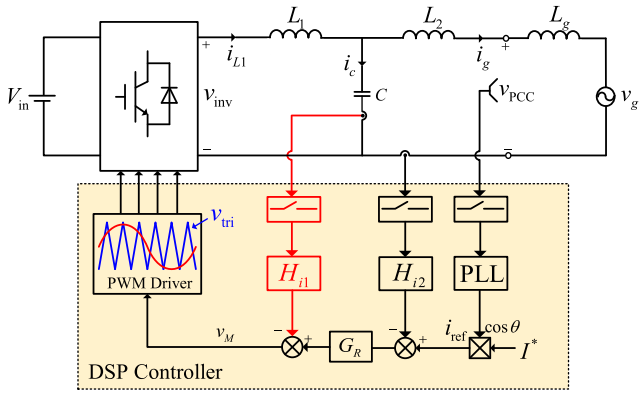

FIGURE 1. Digitally controlled single-phase LCL-Type grid-connected inverter and digital control block diagram.

the sample [32]. K_{PWM} is equivalent to the inverter bridge gain, which can be approximated as $v_{\mathrm{inv}}/v_{\mathrm{tri}}$. v_{inv} and v_{tri} are respectively the inverter bridge output voltage and the amplitude of the triangular carrier. The digital control delay contains computation delay and PWM delay [33]. In order to avoid multiple intersections between the modulation signal and the carrier signal, there is one sampling period delay between the current loading instant and the current sampling instant, which is the computation delay. In s-domain, the computation delay can be expressed as

$$G_d(s) = e^{-sT_s}. \tag{1}$$

The modulation signal should remain unchanged and compare to the triangular carrier, this process can be modeled by ZOH, which is written as follows

$$G_{\mathrm{ZOH}}(s) = \frac{1 - e^{-sT_s}}{s} \approx T_s e^{-0.5\,sT_s}. \tag{2}$$

According to (2), a half sampling period delay $0.5T_s$ is introduced by the PWM process. Therefore, the total delay in the control loop will be $1.5T_s$, which consists of computation delay (one sampling period delay) and PWM delay ($0.5T_s$). $G_R(s)$ is the PR current controller, expressed as

$$G_R(s) = K_P + \frac{2K_r\omega_i s}{s^2 + 2\omega_i s + \omega_o^2} \tag{3}$$

where K_p is the proportional gain and K_r is the resonant gain, $\omega_o = 2\pi f_o$ is the fundamental angular frequency. ω_i is the resonant cutoff frequency, due to the typical $\pm 1\%$ fluctuation of the grid fundamental frequency f_o, ω_i is set as π.

The transfer function from the grid-side current and the capacitor current to the inverter bridge output voltage can be respectively obtained as

$$G_{ig}(s) = \frac{i_g(s)}{v_{\mathrm{inv}}(s)} = \frac{1}{sL_1\left(L_2 + L_g\right)C} \cdot \frac{1}{s^2 + \omega_r^2} \tag{4}$$

$$G_{ic}(s) = \frac{i_c(s)}{v_{\mathrm{inv}}(s)} = \frac{1}{L_1} \cdot \frac{s}{s^2 + \omega_r^2} \tag{5}$$

where ω_r is the inherent resonance angular frequency, expressed as

$$\omega_r = \sqrt{\frac{L_1 + L_2 + L_g}{L_1\left(L_2 + L_g\right)C}}. \tag{6}$$

Fig. 2(b) shows the control block diagram of the digitally controlled *LCL*-Type inverter with the CCF active damping in z-domain. $G_{ig}(z)$ and $G_{ic}(z)$ can be respectively derived by Z-transform to (7) and (8) with ZOH as

$$G_{ig}(z) = \frac{\omega_r T_s\left[z^2 - 2\cos(\omega_r T_s)z + 1\right] - \sin(\omega_r T_s)(z-1)^2}{\omega_r(L_1 + L_2 + L_g)(z-1)\left[z^2 - 2\cos(\omega_r T_s)z + 1\right]}. \tag{7}$$

$$G_{ic}(z) = \frac{\sin\left(\omega_r T_s\right)}{\omega_r L_1} \cdot \frac{z-1}{z^2 - 2\cos\left(\omega_r T_s\right)z + 1} \tag{8}$$

According to Fig. 2(b), the discrete-domain open-loop gain can be derived as (9), shown at the bottom of next page, and the discrete expression of $G_R(z)$ can be obtained as

$$G_R(z) = K_P + \frac{2K_r\omega_i T_s(z-1)}{z^2 + \left(\omega_o^2 T_s^2 + 2\omega_i T_s - 2\right)z - 2\omega_i T_s + 1}. \tag{10}$$

III. IMPACTS OF THE CONTROL DELAY ON THE CAPACITOR-CURRENT-FEEDBACK ACTIVE DAMPING PERFORMANCE

In order to analysis the effect of control delay on the CCF active damping, control block diagram in continuous-domain and its equivalent transformation is shown in Fig. 3. Replacing the feedback variable $i_c(s)$ with $u_c(s)$, and moving the feedback node from the output of $G_R(s)$ to the input of $1/sC$. By means of the equivalent transformation, the CCF active damping can be equivalent to a virtual impedance Z_{eq} paralleled with the filter capacitor [34], expressed as

$$Z_{eq}(s) = \frac{L_1 e^{1.5sT_s}}{H_{i1}K_{\mathrm{PWM}}C}. \tag{11}$$

Substituting $s = j\omega$ into (11), yields

$$Z_{eq}(\omega) = \frac{L_1 e^{1.5j\omega T_s}}{H_{i1}K_{\mathrm{PWM}}C} = R_{eq}(\omega)//jX_{eq}(\omega). \tag{12}$$

According to (12), Z_{eq} can be represent as a parallel connected between a resistor R_{eq} and a reactor X_{eq}, expressed as

$$R_{eq}(\omega) = \frac{L_1}{H_{i1}K_{\mathrm{PWM}}C\cos(1.5\omega T_s)} \tag{13}$$

$$X_{eq}(\omega) = \frac{L_1}{H_{i1}K_{\mathrm{PWM}}C\sin(1.5\omega T_s)}. \tag{14}$$

According to (13) and (14), the frequency characteristics of R_{eq} and X_{eq} can be drawn in Fig. 4. As seen, $R_{eq} > 0$ when $f_r \in (0, f_s/6)$, $R_{eq} < 0$ when $f_r \in (f_s/6, f_s/2)$, and $R_{eq} = 0$ when $f_r = f_s/6$. Obviously, $f_s/6$ is the boundary frequency of the positive equivalent resistance region, which can be defined as the critical frequency f_{cri}. With respect to X_{eq}, $X_{eq} > 0$ when

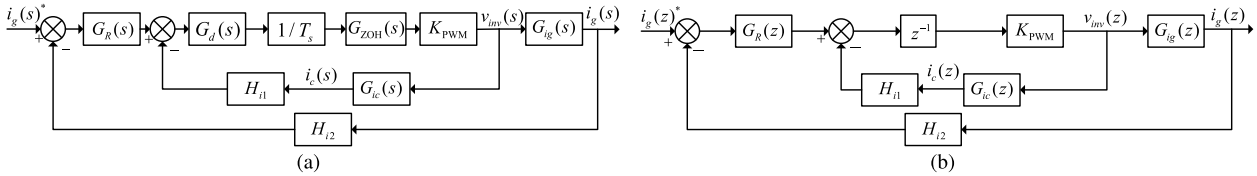

FIGURE 2. Control block diagram of the digitally controlled *LCL*-Type inverter with the CCF active damping. (a) In s-domain. (b) In z-domain.

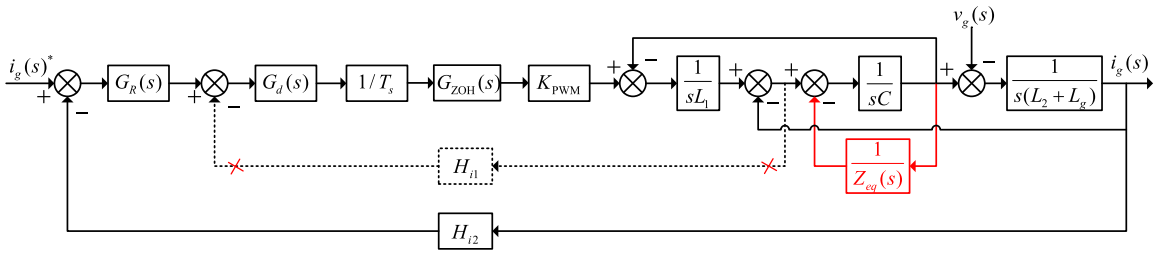

FIGURE 3. Control block diagram in continuous-domain and its equivalent transformation.

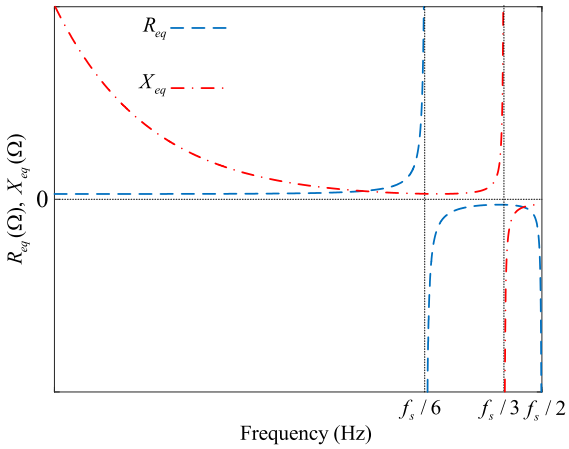

FIGURE 4. Frequency characteristics of R_{eq} and X_{eq}.

$f_r \in (0, f_s/3)$, which is inductive. $X_{eq} < 0$ when $f_r \in (f_s/3, f_s/2)$, which is capacitive. Note that, when $X_{eq} > 0$, f_r increases with the increase of H_{i1}. Thus, a higher actual resonance frequency is yielded, signed as f_r'. When $X_{eq} < 0$, f_r' is lower than f_r. According to (9), the Bode diagrams of the loop gain $T_D(z)$ with $G_R(z) = 1$ for different f_r are shown in Fig. 5. According to Fig. 5 and the research in [12], the stability criterion for digitally controlled grid-connected inverter with the CCF active damping can be summarized in Table 1, where the subscript (+) and (-) represent $-180°$ crossing in the direction of phase raising and phase falling, respectively. P is the number of the open-loop unstable poles, PM is the phase margin, GM_1 and GM_2 are respectively the gain margin at f_r and $f_s/6$, and H_{ilc} is the boundary of H_{i1} when $f_r \in (0, f_s/6)$. If $f_r \in (0, f_s/6)$ and $H_{i1} > H_{ilc}$, a pair of right half-plane open-loop poles might arise. The expression of H_{ilc} can be given as

$$H_{ilc} = \frac{\omega_r L_1 \left(2\cos\left(\omega_r T_s\right) - 1\right)}{K_{PWM} \sin\left(\omega_r T_s\right)}. \tag{15}$$

According to the aforementioned analysis, it is recommended to obtain a relatively low resonance frequency, which is lower than one-sixth of the sampling frequency. However, it needs a larger volume capacitor or inductor which is not cost-effective and would cause the slow dynamic performance of the inverter owing to the influence of the weak grid. Moreover, it is noticed that the gain margin requirement for case 2 conflicts with case 4. Since f_r decreases as the L_g increases, the actual resonant frequency f_r' might be close to the critical frequency, which leads to system instability due to the inadequate gain margin. Besides, when $f_r = f_s/6$, the inverter will never be stable. Hence, the critical frequency and its vicinity can be defined as the resonance frequency forbidden region. Due to this characteristic, the robustness against grid impedance variation of the system is weakened. So, it is desirable to obtain a wider positive region of R_{eq} and eliminate the resonance frequency forbidden region.

IV. CAPACITOR-CURRENT-FEEDBACK DAMPING WITH IMPROVED DELAY COMPENSATION METHOD

A. THE IMPROVED DELAY COMPENSATION METHOD

In order to relieve the influence of the digital control delay, the phase-lead compensator $G_c(z)$ is added into the capacitor current feedback path. The expression of $G_c(z)$ is

$$G_c(z) = \frac{2(2 - z^{-1})}{1 + z^{-1}}. \tag{16}$$

$$T_D(z) = \frac{H_{i2} G_R(z) K_{PWM}}{\omega_r \left(L_1 + L_2 + L_g\right)(z-1)} \cdot \frac{\omega_r T_s \left[z^2 - 2\cos\left(\omega_r T_s\right) z + 1\right] - (z-1)^2 \sin\left(\omega_r T_s\right)}{z\left[z^2 - 2\cos\left(\omega_r T_s\right) z + 1\right] + (z-1)\frac{H_{i1} K_{PWM}}{\omega_r L_1} \sin\left(\omega_r T_s\right)} \tag{9}$$

TABLE 1. Stability criterion for digitally controlled grid-connected inverter with the CCF active damping.

Cases	f_r	H_{i1}	P	-180° crossing	Gain margin requirement	Phase margin requirement
1	$(0, f_s/6)$	$(0, H_{ilc}]$	0	$f_{r(-)}$	GM_1>0dB	PM>0°
2	$(0, f_s/6)$	$(H_{ilc}, +\infty)$	2	$f_{r(-)}, f_s/6_{(+)}$	GM_1>0dB,GM_2<0dB	PM>0°
3	$f_r = f_s/6$	None	2	None	Unstable	Unstable
4	$(f_s/6, +\infty)$	$(0, +\infty)$	2	$f_s/6_{(-)}, f_{r(+)}$	GM_1<0dB,GM_2>0dB	PM>0°

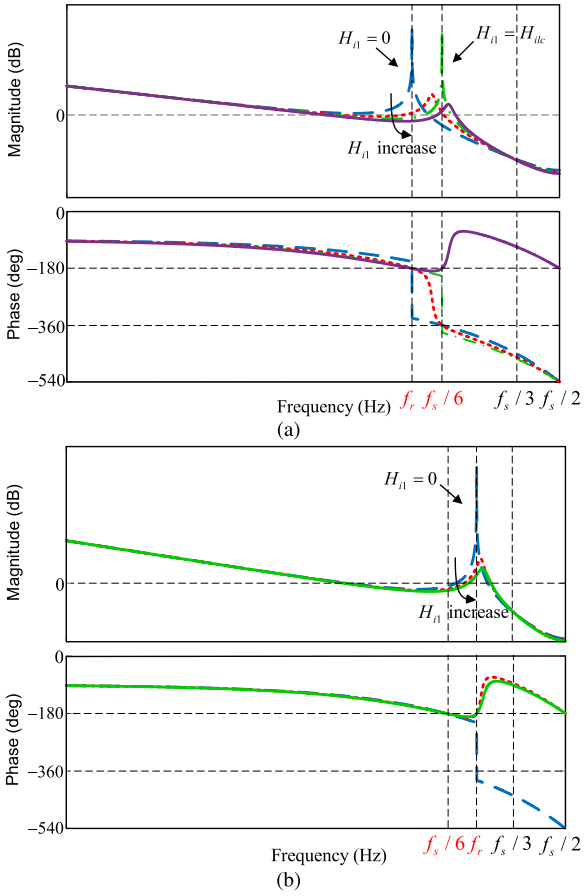

FIGURE 5. Bode diagrams of the open-loop gain with $G_R(z) = 1$. (a) $f_r \in (0, f_s/6)$ (b) $f_r \in (f_s/6, f_s/2)$.

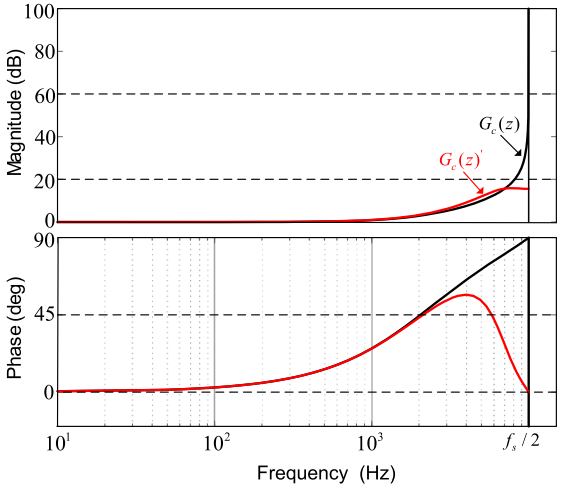

FIGURE 6. The Bode plots of $G_c(z)$ and $G_c(z)'$.

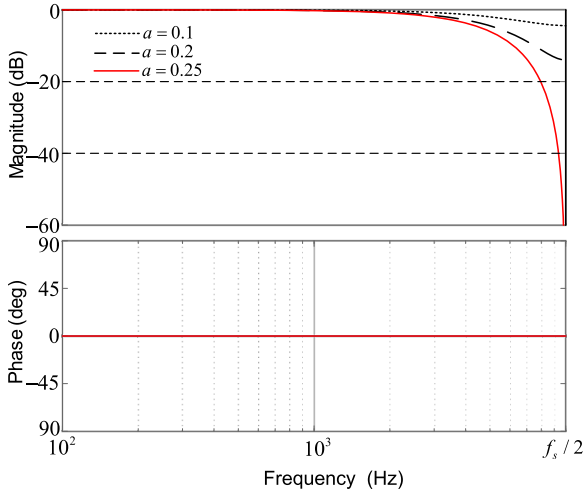

FIGURE 7. Frequency characteristic diagram of $G_{low}(z)$ with different a.

The Bode plots of $G_c(z)$ can be presented in Fig. 6. As shown, the desired 90° can be obtained at Nyquist frequency. However, the magnitude response increases with frequency to infinite at Nyquist frequency, which may cause system instability. For explaining this, (16) can be expanded as

$$G_c(z = e^{j\omega T_s}) = \frac{e^{j0.5\omega T_s}(2 - e^{-j\omega T_s})}{\cos(0.5\omega T_s)}. \tag{17}$$

According to (17), the phase of $G_c(z)$ can be calculated as

$$\angle G_c\,(z) = 0.5\omega T_s + \arctan\left(\frac{\sin(\omega T_s)}{2 - \cos(\omega T_s)}\right). \tag{18}$$

When $\omega = \omega_s/2$, the phase of 90° can be obtained, and the magnitude response will be infinite due to $\cos(0.5\omega_s T_s/2) = 0$, which is in agreement with Fig. 6. However, an ideal phase-lead compensator should only raise the phase of the system while retain the amplitude relatively unchanged. Therefore, a first-order zero-phase-shift digital low filter $G_{low}(z) = az + b + az^{-1}$ is proposed, which $b = 1 - 2a$ should be met [35], [36]. However, $G_{low}(z)$ has a "z", which is hard realized in the digital system. Fortunately, the term "z" in $G_{low}(z)$ can be eliminated by integrating into the term "z^{-1}" in the denominator of $G_c(z)$. Substituting

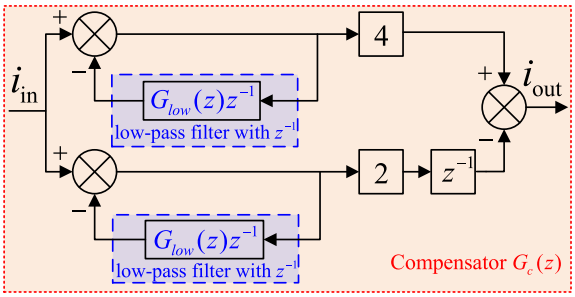

FIGURE 8. Block diagram of the improved phase-lead compensator.

$b = 1 - 2a$ and $z = e^{j\omega T_s}$ into $G_{low}(z)$, it can be derived as

$$G_{low}\left(e^{j\omega T_s}\right) = 2a\cos\left(\omega T_s\right) + 1 - 2a. \tag{19}$$

When $\omega = \omega_{s/2}$, the value of it is $1 - 4a$. If $20\lg\left|G_{low}\left(e^{j\omega T_s}\right)\right|_{\omega=\omega_s/2} = -\infty$, the digital low filter has maximum attenuation at $f_s/2$, so $a = 0.25$, $b = 0.5$ are selected in this paper. The frequency characteristic of $G_{low}(z)$ with different a is shown in Fig. 7. As shown, when $a = 0.25$, the maximum attenuation at Nyquist frequency with zero-phase-shift is obtained. The improved phase-lead compensator expression can be written as

$$G_c(z)' = \frac{2\left(2 - z^{-1}\right)}{1 + G_{low}(z)z^{-1}}. \tag{20}$$

The bode plots of $G_c(z)$ and $G_c(z)'$ is shown in Fig. 6. It can be seen that the high magnitude response of $G_c(z)$ is effectively attenuated at the expense of the phase in high frequency region gradually decreased to zero. According to the expression of $G_c(z)'$, the block diagram of the improved phase-lead compensator can be presented in Fig. 8. According to (9), the discrete-domain loop gain $T_D(z)'$ with $G_c(z)'$ can be obtained as (21), shown at the bottom of the page.

After compensation, the virtual equivalent impedance is changed, expressed as

$$Z_{eq}(\omega)' = \frac{L_1}{H_{i1}K_{\mathrm{PWM}}C}\frac{\left[1 + G_{low}\left(e^{j\omega T_s}\right)e^{-j\omega T_s}\right]e^{1.5j\omega T_s}}{2(2 - e^{-j\omega T_s})} \tag{22}$$

Same as the mentioned discussion, Z'_{eq} can also be represented as a parallel connection of a resistor R'_{eq} and a reactor X'_{eq}, which can be written as

$$\begin{cases} R_{eq}(\omega)' = \dfrac{L_1}{2H_{i1}K_{\mathrm{PWM}}C}\dfrac{A^2 + B^2}{AD} \\ X_{eq}(\omega)' = \dfrac{L_1}{2H_{i1}K_{\mathrm{PWM}}C}\dfrac{A^2 + B^2}{BD} \end{cases} \tag{23}$$

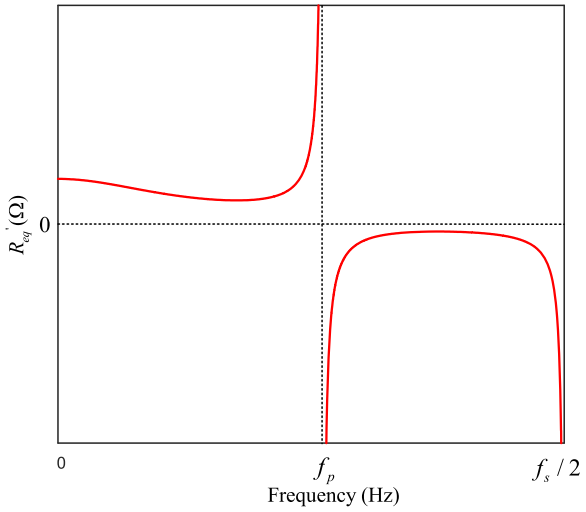

FIGURE 9. Frequency characteristic plot of $R_{eq}(\omega)'$.

where

$$\begin{cases} A = 2\cos^2\left(0.5\omega T_s\right)\cos\left(0.5\omega T_s\right) \\ \quad +[2 - \cos^2\left(0.5\omega T_s\right)]\cos\left(1.5\omega T_s\right) - \cos\left(2.5\omega T_s\right) \\ B = 2\cos^2\left(0.5\omega T_s\right)\sin\left(0.5\omega T_s\right) \\ \quad +[2 - \cos^2\left(0.5\omega T_s\right)]\sin\left(1.5\omega T_s\right) - \sin\left(2.5\omega T_s\right) \\ D = 5 - 4\cos\left(\omega T_s\right). \end{cases} \tag{24}$$

Combining (23) and (24), the frequency characteristic plot of $R_{eq}(\omega)'$ can be shown in Fig. 9. As seen, the boundary frequency of the positive equivalent resistance region after compensation can be defined as f_p, which is extended from $f_s/6$ to $f_s/4$.

B. STABILITY ANALYSIS OF THE SYSTEM AFTER COMPENSATION

After compensation, the system stability might be changed, so it need to be further analyzed. The poles $z = 0$ and $z = 1$ in (21) are inside the unit circle and not right half-plane open-loop poles, which can be ignored here. Therefore, the characteristic equation of $T_D(z)'$ can be expressed as

$$\left[4z^2 + (z+1)^2\right]\left[z^2 - 2\cos\left(\omega_r T_s\right)z + 1\right] + \frac{8H_{i1}K_{PWM}}{\omega_r L_1} \cdot \sin\left(\omega_r T_s\right)(z-1)(2z-1) = 0. \tag{25}$$

For the simplicity of analysis, (25) can be mapped from z domain to ω domain by $z = (1+\omega)/(1-\omega)$, resulting in

$$a_0\omega^4 + a_1\omega^3 + a_2\omega^2 + a_3\omega + a_4 = 0 \tag{26}$$

$$T_D(z)' = \frac{H_{i2}G_R(z)K_{PWM}}{\omega_r(L_1 + L_2 + L_g)z(z-1)} \cdot \frac{\left[4z^2 + (z+1)^2\right]\left\{\omega_r T_s\left[z^2 - 2\cos(\omega_r T_s)z + 1\right] - (z-1)^2\sin(\omega_r T_s)\right\}}{\left[4z^2 + (z+1)^2\right]\left[z^2 - 2\cos(\omega_r T_s)z + 1\right] + \dfrac{8H_{i1}K_{PWM}}{\omega_r L_1}\sin(\omega_r T_s)(z-1)(2z-1)} \tag{21}$$

where

$$\begin{cases} a_0 = 4[1+\cos(\omega_r T_s)] + 4H \\ a_1 = 8[1+\cos(\omega_r T_s)] - 5H \\ a_2 = 12[1-\cos(\omega_r T_s)] + H \\ a_3 = 8[1-\cos(\omega_r T_s)] + H \\ a_4 = 8[1-\cos(\omega_r T_s)] \\ H = \dfrac{8H_{i1}K_{PWM}\sin(\omega_r T_s)}{\omega_r L_1}. \end{cases} \tag{27}$$

The Routh table of (27) can be obtained as

$$\begin{array}{l} \omega^4 : a_0 \ a_2 \ a_4 \\ \omega^3 : a_1 \ a_3 \\ \omega^2 : b_1 \ a_4 \\ \omega^1 : b_2 \\ \omega^0 : a_4 \end{array} \tag{28}$$

where $b_1 = (a_1a_2 - a_0a_3)/a_1$, $b_2 = (b_1a_3 - a_1a_4)/b_1$.

In order to ensure the controllability of the system, f_r should lower than $f_s/2$, then $\omega_r T_s < \pi$ is obtained [37]. Since H_{i1} is defined higher than zero, so $\sin(\omega_r T_s) > 0$ and $1 - \cos(\omega_r T_s) > 0$ can be derived. According to Routh criterion, the first row in the Routh table should retain the same sign for ensuring the system stability. So $a_1 > 0$, $b_1 > 0$ and $b_2 > 0$ are required. According to this requirement, H_{ilc1}, H_{ilc2} and H_{ilc3} can be derived, respectively. So H'_{ilc} can be defined as the minimum among them, expressed as

$$H'_{ilc} = \min\{H_{ilc1}, H_{ilc2}, H_{ilc3}\}. \tag{29}$$

According to (21), the Bode diagrams of $T_D(z)'$ with $G_R(z) = 1$ can be shown in Fig. 10. The $-180°$ crossing frequency in the direction of phase falling and rising can be respectively defined as f_1 and f_2. As seen in Fig. 10(a), when $f_r \in (0, f_p)$ and $H_{i1} < H'_{ilc}$, with the increases of H_{i1}, f_1 keeps on deviating to the left side of f_r. If $H_{i1} > H'_{ilc}$, with the increases of H_{i1}, f_1 deviates to the left side of f_r while f_2 deviates to the right side of f_p. As seen in Fig. 10(b), when $f_r \in (f_p, f_s/2)$, with the increases of H_{i1}, f_1 deviates to the left side of f_p while f_2 deviates to the right side of f_r. As the discussed above, f_1 is never equal with f_2, and satisfies the characteristic, i.e.

$$\begin{cases} f_1 < \min\{f_r, f_p\} \\ f_2 > \max\{f_r, f_p\}. \end{cases} \tag{30}$$

Therefore, the improved delay compensation method can extend the boundary frequency of the positive equivalent resistance region to $f_s/4$ and eliminate the forbidden region of the *LCL* filter resonance frequency. Then, the robustness against the grid impedance varying in a wide region is enhanced.

C. PARAMETER DESIGN

In order to ensure that inverter can operate stably varying with L_g, the CCF coefficient and the current regulator parameters need to be reasonably designed.

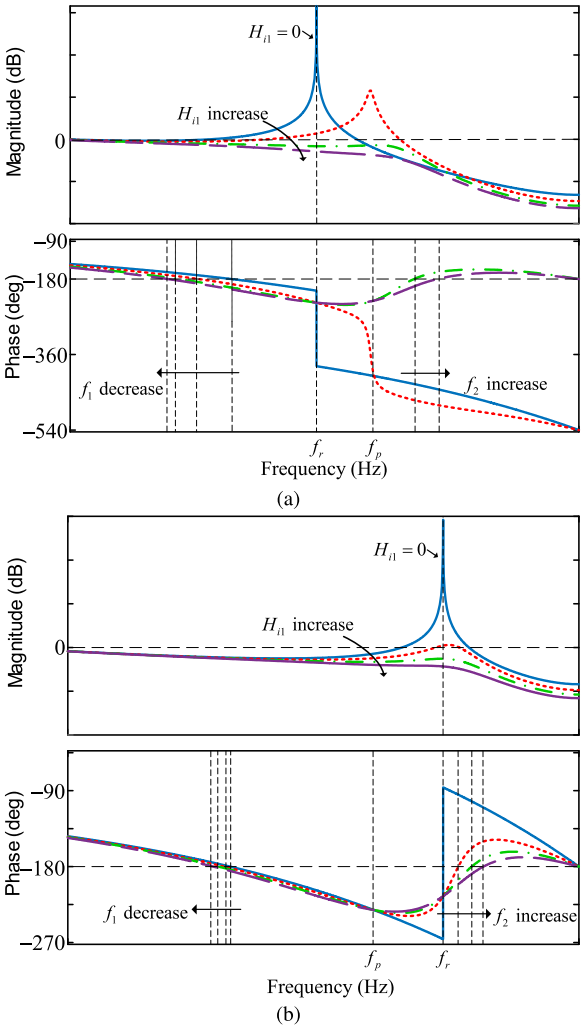

FIGURE 10. Bode diagrams of $T_D(z)'$ with $G_R(z) = 1$. (a) $f_r \in (0, f_p)$ (b) $f_r \in (f_p, f_s/2)$.

Derived by Fig. 3, the open loop gain after compensation in s-domain can be given in

$$T_D(s)' = \frac{1}{sL_1(L_2+L_g)C} \frac{H_{i2}K_{\mathrm{PWM}}e^{-1.5\,sT_s}G_R(s)}{s^2 + \dfrac{1}{CZ_{eq}(s)'}s + \omega_r^2}. \tag{31}$$

Due to the capacitor filter has less impact on the loop gain at or beyond the crossover frequency f_c, so the loop gain at f_c can be approximately as

$$\left|T_D(j2\pi f_c)'\right| \approx \left|\frac{H_{i2}K_{\mathrm{PWM}}G_R(s)}{s(L_1+L_2)}\right|. \tag{32}$$

Because f_c is far great than f_o, thus $|G_R(j2\pi f_c)| \approx K_p$ can be obtained. Substituting it and $\left|T_D(j2\pi f_c)'\right| = 1$ into (32), yields

$$K_P \approx \frac{2\pi f_c(L_1+L_2)}{H_{i2}K_{\mathrm{PWM}}}. \tag{33}$$

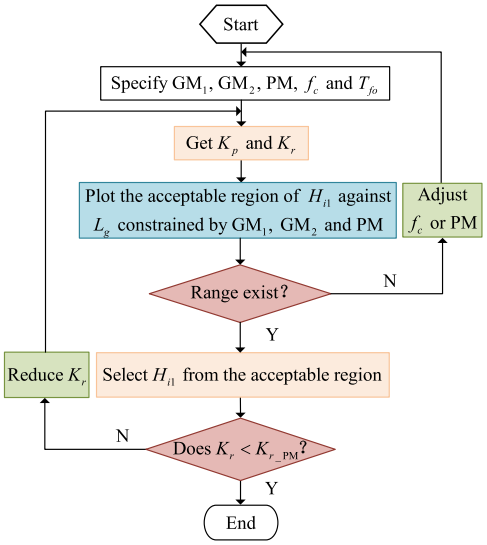

FIGURE 11. Flow chart of the design procedure.

T_{fo} is the loop gain at the fundamental frequency f_o, which is related to the steady state error. It can be derived as follow

$$T_{fo} = 20\lg \frac{H_{i2}K_{\mathrm{PWM}}(K_p + K_r)}{2\pi f_o\,(L_1 + L_2)}. \tag{34}$$

Substituting (33) into (34), the resonant gain of PR current controller under the constraint of T_{fo} is presented as

$$K_{r\_T_{fo}} = (f_o 10^{\frac{T_{fo}}{20}} - f_c)\frac{2\pi(L_1 + L_2)}{H_{i2}K_{\mathrm{PWM}}}. \tag{35}$$

Since f_c is much higher than f_o and f_i, substituting $s = j\omega f_c$ into (3) can obtain $G_R(j2\pi f_c) \approx K_P + 2K_r\omega_i/j2\pi f_c$, then substituting it and $s = j\omega f_c$ into (31) with simplification, PM can be written as

$$\begin{aligned}\mathrm{PM} = {} & \arctan\frac{f_c H_{i1}K_{\mathrm{PWM}}BD + \pi L_1\left(f_r^2 - f_c^2\right)\left(A^2 + B^2\right)}{f_c H_{i1}K_{\mathrm{PWM}}AD} \\ & - 3\pi f_c T_s - \arctan\frac{K_r\omega_i}{\pi f_c K_p}.\end{aligned} \tag{36}$$

According to (36), the resonant gain of PR current controller under the restriction of PM can be derived as (37), shown at the bottom of the page.

Substituting (33) and (35) into (31), the damping coefficient under the constraint of PM can be obtained as (38), shown at the bottom of the page. As the analysis above, the loop gain at f_1 and f_2 should have enough gain margins. So, expressions can be given as

$$\begin{cases}\angle T_D(j2\pi f_1) = -180^\circ \\ GM_1 = -20\lg|T_D(j2\pi f_1)|\end{cases} \tag{39}$$

$$\begin{cases}\angle T_D(j2\pi f_2) = -180^\circ \\ GM_2 = -20\lg|T_D(j2\pi f_2)|\end{cases} \tag{40}$$

According to (39) and (40), (41) and (42) can be respectively derived, i.e., (41) and (42), as shown at the bottom of the next page, where

$$\begin{cases} Q_1 = \dfrac{\dfrac{K_r\omega_i}{\pi f_1 K_p} + \tan(3\pi f_1 T_s)}{1 - \dfrac{K_r\omega_i}{\pi f_1 K_p}\tan(3\pi f_1 T_s)} \\ Q_2 = \dfrac{\dfrac{K_r\omega_i}{\pi f_2 K_p} + \tan(3\pi f_2 T_s)}{1 - \dfrac{K_r\omega_i}{\pi f_2 K_p}\tan(3\pi f_2 T_s)}. \end{cases} \tag{43}$$

Based on the above analysis, the design procedure is shown in Fig. 11, which can be elaborated as follows

1) Specify the requirements of T_{fo}, PM, GM_1, GM_2, and f_c for satisfying system steady-state error, phase margin, gain margin and control bandwidth. Then K_p and $K_{r\_T_{fo}}$ are obtained from (33) and (35), respectively. It is noticed that the selection of K_r needs to be slightly larger than $K_{r\_T_{fo}}$ for reducing the effect of the reduction of fundamental frequency gain owing to the grid impedance variation.
2) According to (38), (41), and (42), curves of H_{i1} against the variation of L_g can be obtained, and check if there is a selectable region that satisfies the requirements of PM, GM_1 and GM_2 vary with L_g over the entire region. If not, the specification of f_c or PM is too strict, and need to be adjusted.
3) Selecting H_{i1} from the acceptable region and substitute into (37), and check if K_r is lower than K_{r_PM}. If it is

$$K_{r\_\mathrm{PM}} = \frac{\pi f_c{}^2\,(L_1 + L_2)}{K_{\mathrm{PWM}}H_{i2}f_i}\cdot\frac{\left[\dfrac{\pi L_1(f_r{}^2 - f_c{}^2)\left(A^2 + B^2\right)}{f_c H_{i1}K_{\mathrm{PWM}}} + BD\right] - AD\tan\left(3\pi f_c T_s + \mathrm{PM}\right)}{\left[\dfrac{\pi L_1(f_r{}^2 - f_c{}^2)\left(A^2 + B^2\right)}{f_c H_{i1}K_{\mathrm{PWM}}} + BD\right]\tan\left(3\pi f_c T_s + \mathrm{PM}\right) + AD} \tag{37}$$

$$H_{i1\_\mathrm{PM}} = \frac{\dfrac{\pi L_1\left(f_r{}^2 - f_c{}^2\right)\left(A^2 + B^2\right)}{f_c K_{\mathrm{PWM}}}\left[\pi f_c{}^2 - 2\pi f_i\left(10^{\frac{T_{fo}}{20}}f_o - f_c\right)\tan(3\pi f_c T_s + \mathrm{PM})\right]}{2\pi f_i\left(10^{\frac{T_{fo}}{20}}f_o - f_c\right)[BD\tan(3\pi f_c T_s + \mathrm{PM}) + AD] + \pi f_c{}^2\,[AD\tan(3\pi f_c T_s + \mathrm{PM}) - BD]} \tag{38}$$

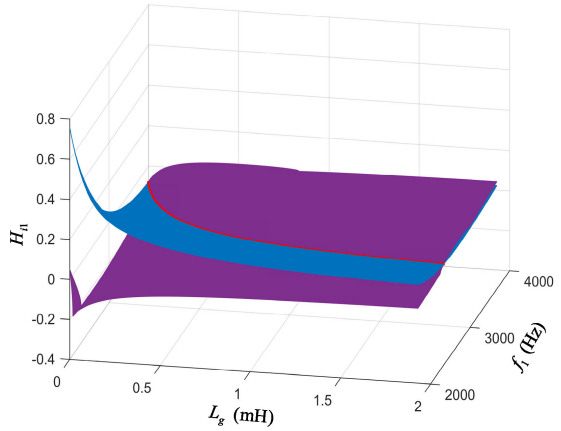

FIGURE 12. Relationships between L_g, GM_1 and H_{i1}.

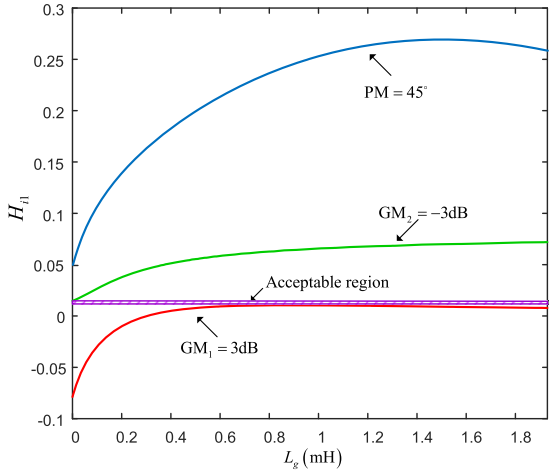

FIGURE 13. Curves of H_{i1} against varying L_g constrained by PM, GM_1 and GM_2.

satisfied, the design is over. Otherwise, reduce K_r and iterate the design procedure.

D. DESIGN EXAMPLE

For better verifying the effectiveness of the above parameters design procedure and the proposed delay compensation method, a design example is illustrated. Table 2 gives the main parameters of a 2kW single-phase *LCL*-Type grid-connected inverter.

TABLE 2. Systems parameters.

Parameter	Symbol	Value
Input voltage	V_{in}	180V
Grid voltage	V_g	110V
Output power	P_o	2kW
Inverter-side inductance	L_1	800μH
Filter capacitance	C	5μF
Grid-side inductance	L_2	140μH
Resonance frequency	f_r	6.5kHz
Sampling frequency	f_s	20kHz
switching frequency	f_{sw}	10kHz
Grid current sampling gain	H_{i2}	0.15
Damping coefficient	H_{i1}	0.013
Proportional gain	K_p	0.85
Resonant gain	K_r	170

According to the aforementioned design procedure, step 1 is to specify the desired parameter as $T_{fo} > 73$dB, PM $> 45°$, $GM_1 > 3$dB and $GM_2 < 3$dB. The *LCL* filter with resonance frequency $f_r = 6.5$kHz is applied and the initial f_c is set as 1300Hz. According to (33) and (35), K_p and $K_{r\_T_{fo}}$ can be respectively calculated as 0.85 and 147, for reducing the impact of the weak grid on the fundamental frequency gain, K_r is taken as 170.

Due to f_1 and f_2 cannot accurately obtain, so two three-dimensional graphs of equation (41) can be drawn in Fig. 12. In the three-dimensional coordinate system with L_g as the x-axis, f_1 as the y-axis, and H_{i1} as the z-axis. Next, the common line of the three-dimensional graphs is projected onto the xoz plane. This projection is the curve of H_{i1} under the constraint of GM_1 with the variation of L_g. In this way, the curve of H_{i1} under the constraint of GM_2 with the variation of L_g can also be obtained. By using (38), (41) and (42), curves of H_{i1} varying with L_g from 0 to 1.93mH constrained by PM,

$$\begin{cases} H_{i1GM_1} = \dfrac{\pi L_1 (f_r{}^2 - f_1{}^2)(A^2 + B^2)}{Q_1 f_1 K_{\mathrm{PWM}} AD - f_1 K_{\mathrm{PWM}} BD} \\ H_{i1GM_1} = \dfrac{\pi L_1}{K_{\mathrm{PWM}} f_1 D} \cdot \\ \left[\left(f_1^2 - f_r^2\right) B + \sqrt{\left(f_r^2 \dfrac{f_c}{f_1} 10^{\frac{GM_1}{20}}\right)^2 \left(A^2 + B^2\right) - \left(f_1^2 - f_r^2\right)^2 A^2} \right] \end{cases} \tag{41}$$

$$\begin{cases} H_{i1GM_2} = \dfrac{\pi L_1 (f_r{}^2 - f_2{}^2)(A^2 + B^2)}{Q_2 f_2 K_{\mathrm{PWM}} AD - f_2 K_{\mathrm{PWM}} BD} \\ H_{i1GM_2} = \dfrac{\pi L_1}{K_{\mathrm{PWM}} f_2 D} \cdot \\ \left[\left(f_2^2 - f_r^2\right) B + \sqrt{\left(f_r^2 \dfrac{f_c}{f_2} 10^{\frac{GM_2}{20}}\right)^2 \left(A^2 + B^2\right) - \left(f_2^2 - f_r^2\right)^2 A^2} \right] \end{cases} \tag{42}$$

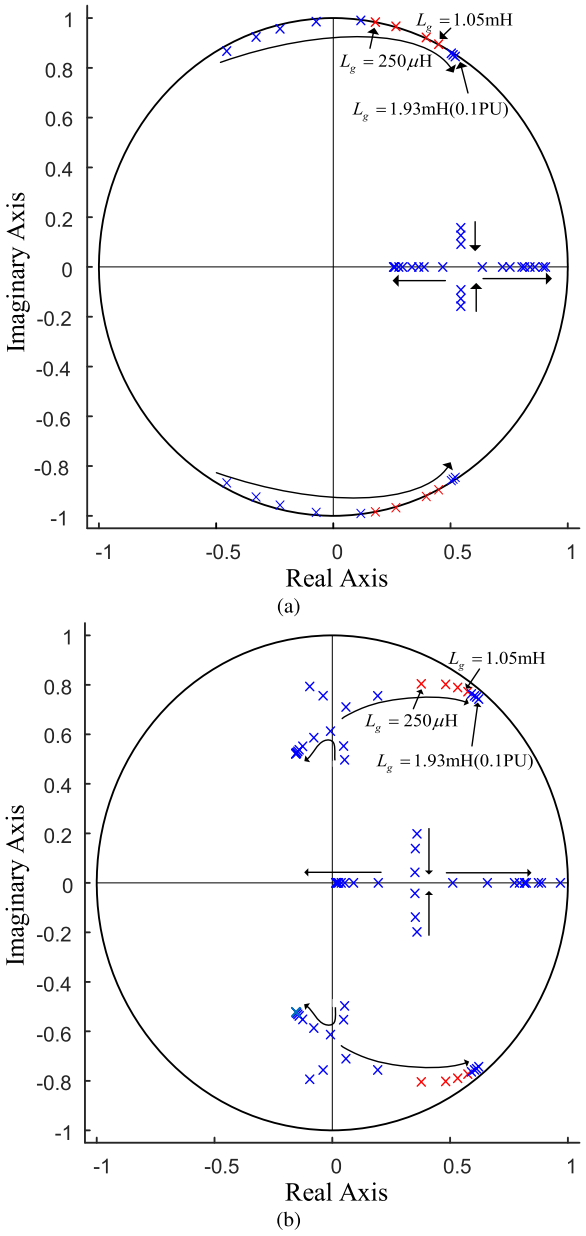

FIGURE 14. Close-loop pole maps with the grid impedance variation. (a) Before compensation (b) After compensation.

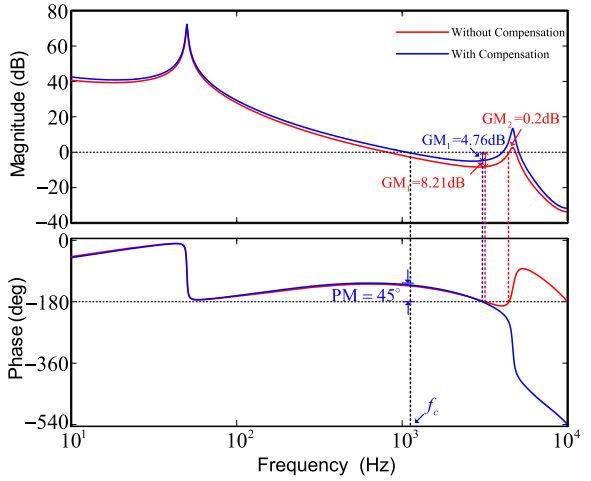

FIGURE 15. Bode diagrams of the open loop gain against $L_g = 250\mu$H with and without compensation.

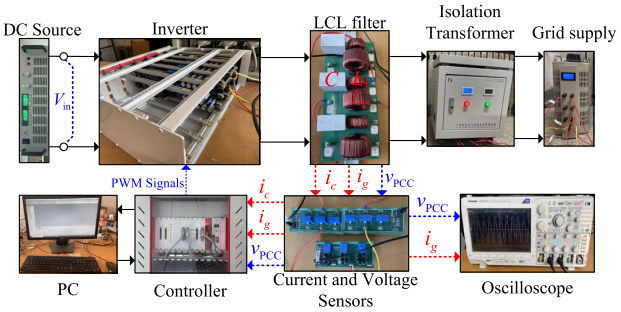

FIGURE 16. Configuration of the experimental setup.

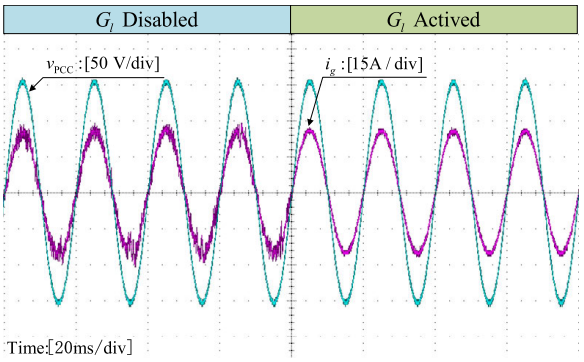

FIGURE 17. Experimental results when altering from $G_c(z)$ to $G_c(z)'$.

GM_1 and GM_2 can be obtained in Fig. 13. It can be seen that the acceptable range of H_{i1} ranges from 0.0118 to 0.0135, so $H_{i1} = 0.013$ is selected. Substituting H_{i1} into (37), the $K_{r\_PM} = 189$ can be calculated, and $K_r < K_{r\_PM}$ is satisfied.

With the parameters given in Table 2, the close-loop pole maps with the grid impedance variation before and after compensation are shown in Fig. 14(a) and Fig. 14(b), respectively. As shown in Fig. 14(a), the close poles will move outside the unit circle when grid impedance varies from 250μH to 1.05mH, which fall into the resonance frequency forbidden region. When the proposed delay compensation is adopted, the resonance frequency forbidden region is eliminated. So the close poles shown in Fig. 14(b) can be trapped within the unit circle, which verifies the feasibility of the parameters design and the effectiveness of the proposed delay compensation method.

The Bode diagrams of the loop gain against $L_g = 250\mu$H with and without delay compensation can be shown in Fig. 15. Before compensation, the actual resonance frequency falls into the resonance frequency region and the gain margin are respectively $GM_1 = 8.21$dB and $GM_2 = 0.2$dB, which is not stable due to the inadequate stability margin. Then, the open-loop unstable poles is removed owing to the extension of the positive equivalent resistance region. So, just one $-180°$ crossing exists, and corresponding gain margin is $GM_1 = 4.76$dB. In Fig.15, the $f_c = 1300$Hz and PM $= 45°$ are clearly

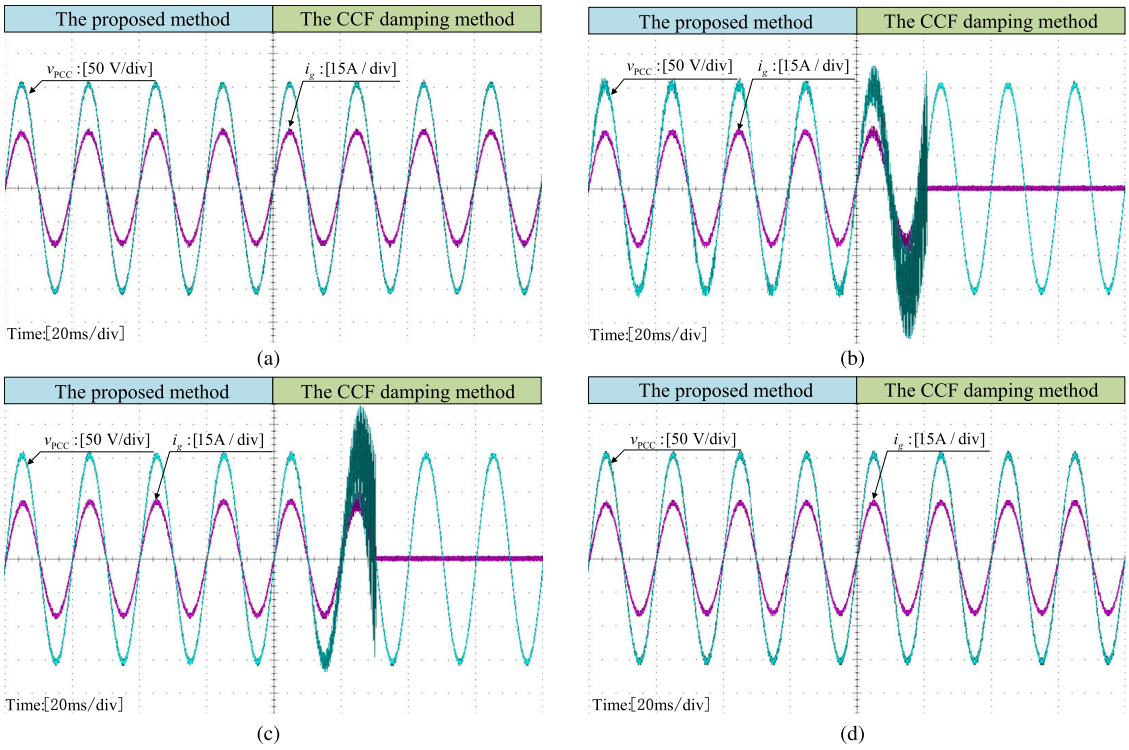

FIGURE 18. Experimental results when altering from the proposed method to the conventional CCF damping method. (a) $L_g = 0$ (b) $L_g = 250\mu$H (c) $L_g = 1.05$mH (d) $L_g = 1.93$mH.

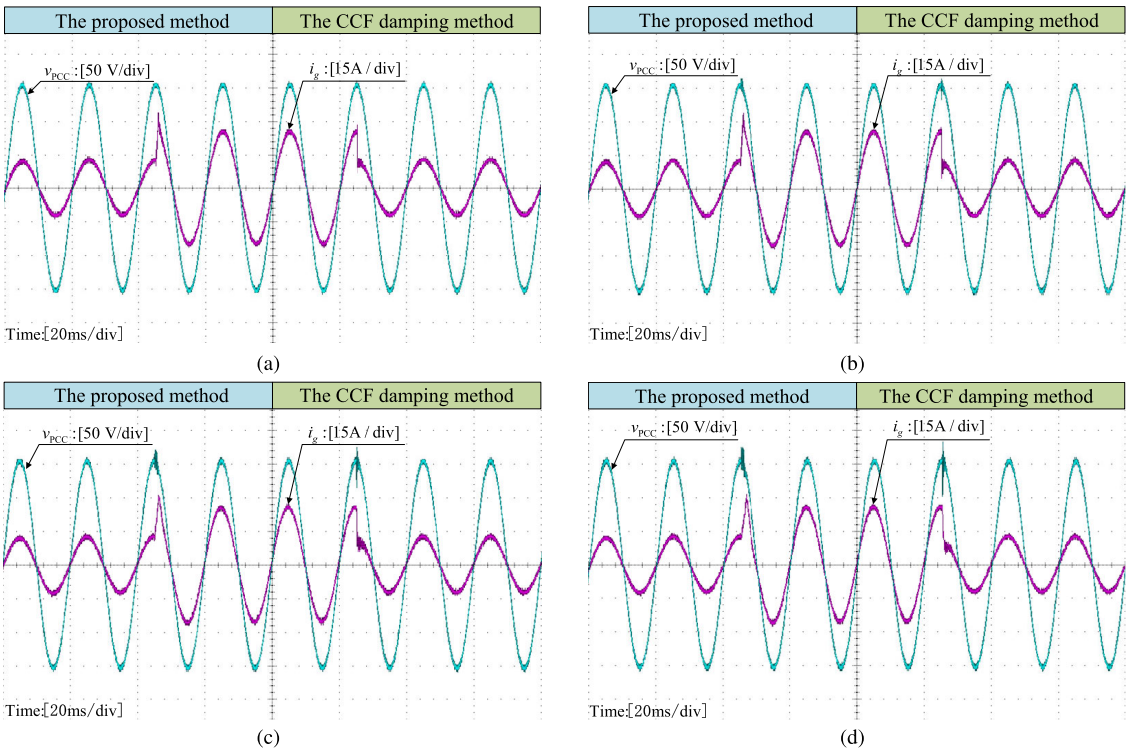

FIGURE 19. Experimental results with the proposed method when the grid current changes between half- and full-load. (a) $L_g = 0$ (b) $L_g = 250\mu$H (c) $L_g = 1.05$mH (d) $L_g = 1.93$mH.

identified. Therefore, the control system has a good control performance after compensation.

V. EXPERIMENTAL RESULTS

To confirm the effectiveness of the proposed method, a 2-kW experimental set up is constructed, which is shown in Fig.16. The main parameters are given in Table 2 and the controller is implemented in a TI TMS320C28346 DSP. Furthermore, the grid impedance L_g is emulated by an external inductor.

In order to make a straightforward comparison, the experimental waveform is altered from one method to another one. The experimental waveforms when altering from $G_c(z)$ to $G_c(z)'$ is shown in Fig. 17. As shown, the grid-side current is significantly distorted due to the noise amplification while the current is stable when alternation is occurred, which is agree with Fig. 7. The noise amplification is effectively reduced when the digital low filter is added. Furthermore, Fig. 18 presents the experimental results when altering from the proposed method to the conventional CCF damping method against different grid impedance, in which v_{PCC} presents the PCC voltage and i_g presents the grid-side current. As seen, when $L_g = 0$, the inverter remains stable with either the proposed method or the conventional CCF damping method. However, when the damping method altering from the proposed method to the conventional CCF damping method under $L_g = 250\mu$H or 1.05mH, which f_r' falls into the resonance frequency forbidden region. The grid-side current and the PCC voltage arise significantly oscillation and further trigger protection. Moreover, when $L_g = 1.93$mH, the actual resonance frequency is away from the resonance frequency forbidden region. So, the inverter is constantly stable. The experimental results are consistent with the analysis given in Section IV. Thus, it is meaning that the proposed delay compensation method can improve the *LCL*-Type grid-connected inverter robustness against the grid impedance variation and significantly relieve the noise amplification.

For verifying the feasibility of the parameters design procedure given in Section IV. The experimental results with the proposed method when the grid current reference i_{ref} step between half- and full-load against different grid impedance is shown in Fig. 19. To exhibit the worst situation, the step action is occurred at the peak of i_g. As seen, the inverter features good dynamic performance and stability with the grid impedance varies from 0 to 1.93mH. The experimental results demonstrate that the parameters design procedure is valid.

VI. CONCLUSION

Owing to the digital control delay effect, the *LCL*-Type grid-connected inverter with the CCF active damping is apt to be unstable when the grid impedance varies in a wide range. To address this issue, this paper proposes an improved delay compensation method which is inserting a phase-lead compensator with a digital low-pass filter into the CCF path. Accordingly, the boundary frequency of the positive equivalent resistance region is boosted from $f_s/6$ to $f_s/4$ and the resonance frequency forbidden region is completely eliminated, which the inverter robustness against the grid impedance variation is enhanced. Moreover, the improved phase-lead compensator provides both substantial phase compensation and does not introduce excessive amplitude gain in the high frequency domain, which relieves the noise amplification. For obtaining good control performance of the inverter, a parameters design procedure is further presented. Finally, a 2kW prototype is built and the experimental results verify the validity of the theoretical analysis and the proposed method.

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