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TOPICAL REVIEW

Low Voltage Switched-Capacitive-Based Reconfigurable Charge Pumps for Energy Harvesting Systems: An Overview

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ABSTRACT Conventional SC-based charge pump with fixed conversion ratio is predominantly adopted in energy harvesting (EH) systems, which becomes a bottleneck for attaining high power conversion efficiency (PCE) with wide dynamic range (WDR). This article reviews and explores the SC-based reconfigurable charge pump (RCP) as an alternative voltage-boosting element for the EH system. An overview of the RCP structure is established, followed by a comprehensive review of CP reconfigurable topologies along with state-of-art architecture. Design consideration of the RCP in terms of dynamic range, PCE, and VCE is provided to give a clear insight into the future development of RCP architecture for the EH system.

INDEX TERMS Energy harvesting (EH), reconfigurable charge pump, wide dynamic range, capacitive-based converter, dc-dc converter, CMOS.

I. INTRODUCTION

Nowadays, the demands for high-efficiency, miniaturized, low-powered devices such as healthcare wearables [1], biomedical implants [2], and IoT wireless sensor nodes (WSNs) [3] have increased expeditiously due to the vast social needs in pursuing a healthy and wellness lifestyle. Since these devices are generally implemented as system-on-chips (SOC) solutions with miniaturized size, conventional bulky battery-based power supply has become impractical. Besides, self-sustainability features also come into consideration where battery replacement is unrealistic in implantable medical devices.

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The limitations of battery usage in low-powered devices have prompted micro-energy harvesting to become an alternative solution. Examples of energy sources that can be harvested by the EH system include radio frequency (RF) [4], [5], solar [6], thermal [7], and vibration [8], [9]. Despite the power autonomy features, the EH system suffers from low input voltage (tenth to the hundredth microvolt) due to irregular ambient energy density in the environment [10]. Implementing a DC-DC boost converter in the EH system is essential to boost the low harvested DC voltage to a higher DC output voltage for load application while maintaining an optimal voltage conversion efficiency (VCE) and power conversion efficiency (PCE).

Compared with an inductor-based converter, a capacitive-based converter, widely referred to the literature as a charge pump (CP), is preferable in the EH system since no bulky

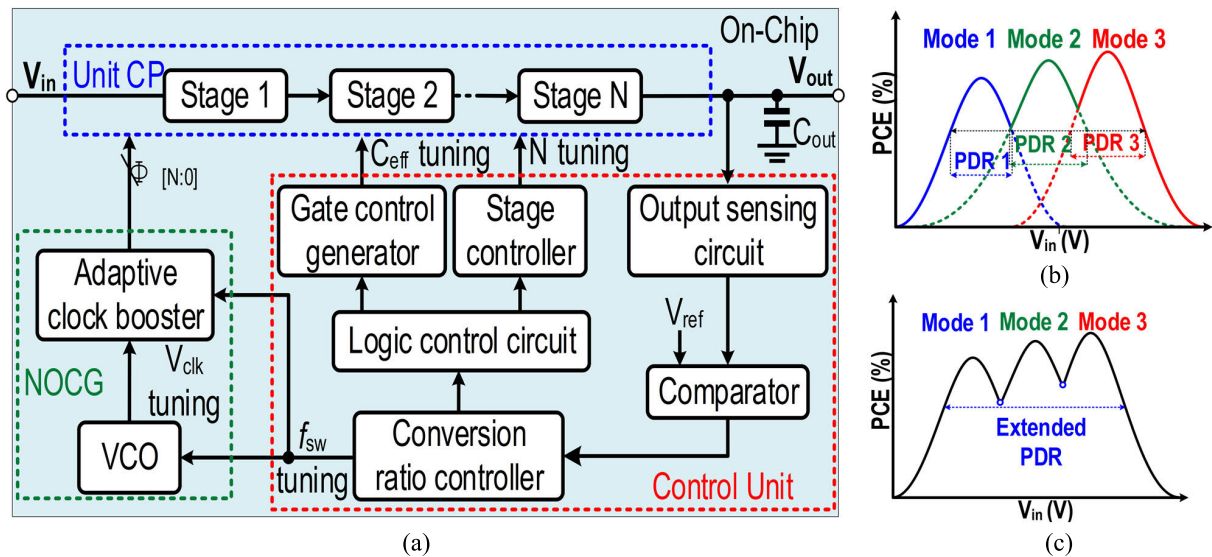


FIGURE 1. (a) General block model of reconfigurable charge pump with N , C_{eff} , V_{clk} , and f_{sw} tuning (b) Limited power dynamic range in conventional CP (c) Extended power dynamic range in reconfigurable CP.

off-chip inductor is required [11]. However, conventional CP with a fixed voltage conversion ratio (CR) has a critical drawback where it has a narrow optimal operating range and is only efficient at discrete ratios of input-to-output voltages [12], [13], resulting in a low PCE when the harvested input voltage is constantly fluctuating. Moreover, the varying input voltage level will lead to a wide variation in the output voltage, which is inadequate in voltage-sensitive loads such as biomedical sensor nodes (BSNs) [2]. These bottlenecks in a conventional CP have made the reconfigurable CP a promising solution as it can provide hybrid CRs by reconfiguring the circuit operation depending on the environment condition while maintaining a relatively high PCE over a wide dynamic range operation.

Depending on the motivation of implementation, prior art reconfigurable CP focused on the CR configuration in which the design is driven by 1) delivering desired constant V_{out} over WDR input voltage and 2) attaining high PCE in extended input operating range. The block diagram of a general reconfigurable CP system is shown in Figure 1(a). Apart from the clock generator, reconfigurable CP usually comes with additional peripheral control circuits such as comparators, sensing circuits, and conversion ratio controllers [14], [15]. By comparing the output voltage (V_{out}) with a reference voltage (V_{ref}), reconfigurable CP tunes its boosting capability or CR by reconfiguring the circuit structure or parameters such as the number of active stages, stage capacitances, switching frequency, and clock amplitude. The changes in these parameters ensure the CP is capable to generate the desired output in the most power-efficient manner without any critical power loss [14], [16]. As the CP reconfigures, the PCE curve of the CP also shifts accordingly respective to the input voltage due to the changes in the circuit characteristics such as power consumption and output

transient response [15]. The dynamic shifting of the PCE curve ensures the CP operates with a high PCE in an extended WDR input voltage, whereas the conventional CP can only attain a high PCE in a particular narrow input range depending on the threshold voltage of the device, technology node, and operating frequency. As a result, the CP performance is improved with high PCE across WDR of V_{in} as shown in Figure 1(c). This article presents a comprehensive review of low voltage capacitive-based reconfigurable CP system topologies for EH. First, a background research of various ambient energy densities is presented in section II. Next, a general overview of the reconfigurable CP system block is presented in section III. Section IV provides a review of the commonly used reconfigurable topologies along with state-of-art architecture with a summary table. A discussion is summarized in section V to provide an extensive review of the significance and limitations of different reconfigurable topologies, along with the systematic CP design approaches and trade-off for the EH system. Finally, section VI concludes the paper.

II. BACKGROUND RESEARCH

To study the necessity of reconfigurable CP in EH harvesting, background research of different ambient energy densities is conducted according to various published articles as well as some authoritative databases such as World Bank's World Development Indicator (WDI), NASA's Surface meteorology and Solar Energy (SSE), along with National Oceanic and Atmospheric Administration (NOAA). The background research aims to provide a general view of the irregularity in the ambient energy density (PV, RF, TEG) at different geographical locations along with the average power density for the different types of EH sources.

Mean Total RF Power Density in Different Country

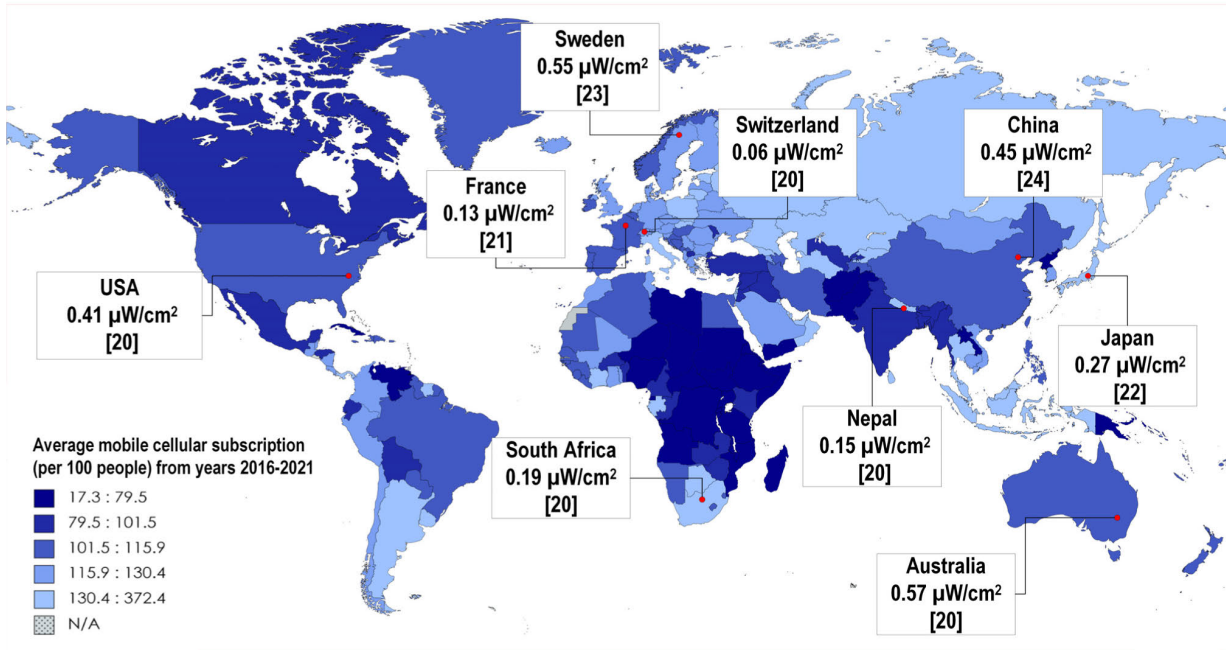


FIGURE 2. Mean total RF power density in different country with different average value of mobile cellular subscriptions [20], [21], [22], [23], [24].

TABLE 1. Summary of average and maximum power density in different frequency bands [17], [18], [19].

Band	Frequency Range (MHz)	Average Power Density ($\mu\text{W}/\text{cm}^2$)	Maximum Power Density ($\mu\text{W}/\text{cm}^2$)
DTV	471-610	0.00089	0.46
GSM900 (MTx)	880-915	0.00045	0.039
GSM900 (BTx)	925-960	0.036	1.93
GSM900 (MTx)	1710-1785	0.0005	0.02
GSM900 (BTx)	1805-1880	0.084	6.39
3G (MTx)	1920-1980	0.00046	0.066
3G (MTx)	2110-2170	0.012	0.24
Wi-Fi 2G	2400-2500	0.00018	0.006

For RF harvesting, the irregularity arises from the different energy levels carried by different frequency bands. For example, Table 1 shows the average power density of different frequency bands that are commonly used for mobile communication, radio or TV broadcasting, and wireless network [17], [19]. The mean value of RF energy density in several countries [20], [24] with different ranges of average cellular subscription has been plotted in Figure 2 to provide an overview of RF EH feasibility. Theoretically, countries with higher average cellular subscription values tend to have a higher RF energy density due to the higher amount of call traffic and signal transmission. However, exceptions have been observed in Figure 2, where some countries with higher cellular subscriptions are having lower RF power density. This is because RF energy density can be easily degraded if the propagation of the RF wave travels for a long distance or

is blocked by obstacles such as terrain constraints or high-rise buildings. Besides, the frequency bands allocated for cellular services are different in the respective countries depending on the countries’ regulatory authorities despite the international telecommunication union (ITU)’s efforts for common frequency usage in telecommunication applications, resulting in a high irregularity of RF power density.

In PV harvesting, the power density is proportional to the solar intensity. A world map of global horizontal solar irradiation which indicates the total solar radiation incident on a horizontal surface is shown in Figure 3. Based on the map, it is observed that most of the regions with high solar irradiation are located at lower latitudes. This is because at higher latitudes the solar radiation angle is smaller, resulting in the energy spreading over a larger surface area. Note that even in the same latitudes, the amount of solar irradiation will

World Map of Global Horizontal Solar Irradiation (GHI)

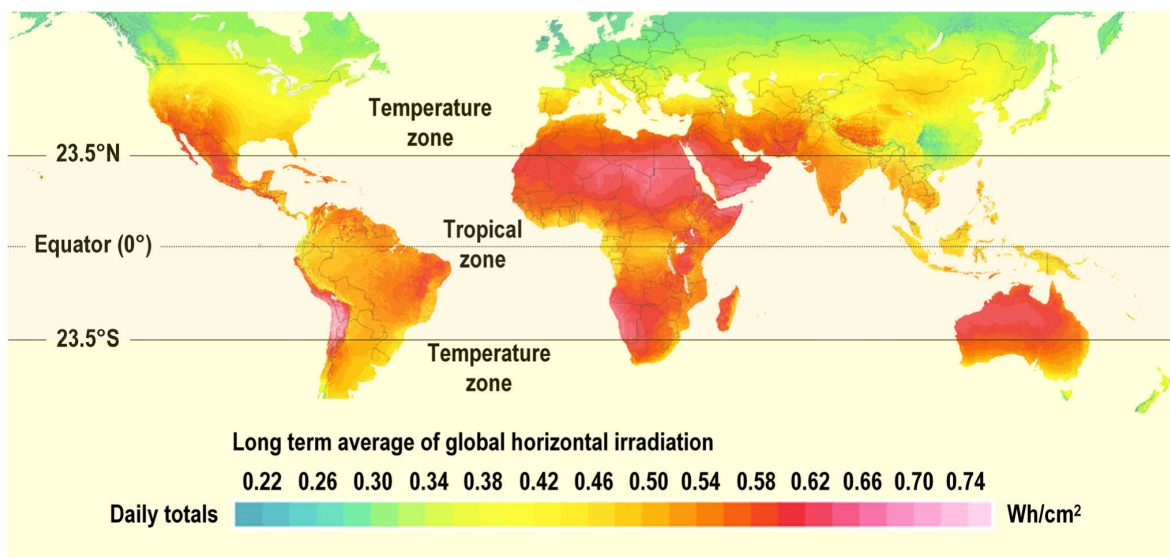


FIGURE 3. World map of long term average global horizontal solar irradiation (GHI).

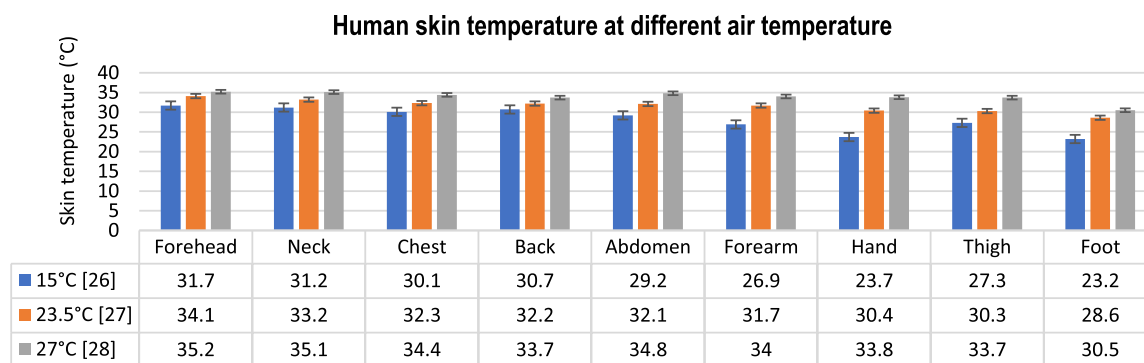


FIGURE 4. Comparison of different part of human skin temperature at 15°C, 23.5°C and 27°C.

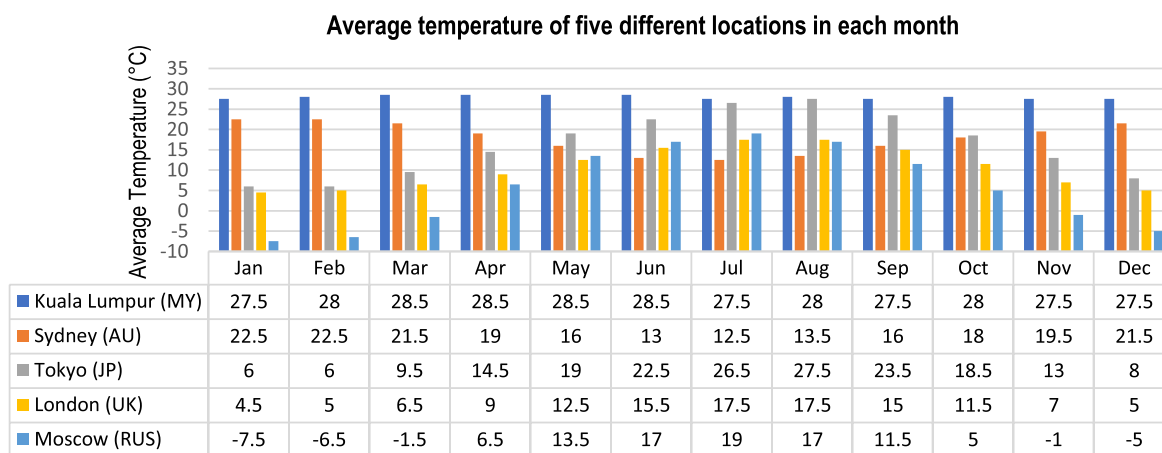


FIGURE 5. Comparison of the average air temperature at different region in respective month [sources from NOAA database].

not be identical due to atmospheric conditions such as cloud cover, air pollution, and land terrain [25].

From the perspective of TEG harvesting, one of the factors that affect the TEG output power is the temperature difference

between the hot and cold surfaces. In this case, we assume the TEG harvesting for body sensor nodes (BSNs) application where the hot region is the human skin temperature, and the cold side is the air temperature. In reference to Figure 4,

it is observed that the human skin temperature varies in different air temperatures and the skin temperature for a different body part also has significant variations between each other [26], [28]. Besides, the temperature of a region can be highly dynamic throughout the year. According to the monthly average temperature data the year. According to the monthly average temperature data of NOAA as in Figure 5, Moscow recorded a maximum temperature variation of 26°C in January and July, while London, Sydney, and Tokyo recorded a temperature variation in the range of 10-20°C, Singapore recorded the lowest average temperature variation of only 1.5°C due to its location in the equator. Hence, the output power of TEG is highly-dependent on geographical and seasonal factors.

Throughout the research work, it is observed that the distribution of ambient energy is significantly dependent on the environment. Hence, it is impossible to design a “once and for all” power-boosting circuit that can maintain optimal PCE for all conditions as the circuits are usually designed and optimized only for certain predetermined input voltage ranges. Hence, the ability to self-reconfigurable has become vital as it is the key to improving the circuit’s adaptivity to environmental changes.

III. RCP MODEL/ARCHITECTURE

A. CHARGE PUMP

The CP circuit is considered the core circuit in the entire RCP system. In an EH system, a step-up CP is responsible to boost up the low DC input voltage harvested from the EH transducer to a sufficiently high output DC voltage for load usage. Occasionally, step-down, or fractional CP [29], [30] has also been implemented in the EH system to generate a fractional CR for higher configurable resolution.

Generally, a step-up CP circuit is constructed by cascading the Nth stage of the voltage doubler cell. Figure 6 shows the simplified schematic of an ideal CP circuit, which comprises MOSFET switches S_i (i = 1,2,3...N+1), pump capacitor C_{pump}(pump = 1,2,3...N), load capacitor, and load resistor that represent the loading circuit. By alternating the non-overlapping clock signal Φ₁ and Φ₂, the odd and even switches S_i is turned on/off sequentially and the charge is pumped along the stages where C_{pump} are successively (dis-) charged during each clock cycle [10]. Switches S_i not only act as power transfer switches across stages, but it also serves the purpose of preventing the charge from flowing in the reverse direction (from N+1 stage to N stage). These switches can be driven by either peripheral circuits such as gate controllers or other pre-charged nodes presented in CP [31].

In loaded condition, the steady-state value of CP final output voltage V_{out}, voltage gain per stage ΔV and voltage loss due to output current per stage V_{loss} can be written as (1), (2) and (3).

$$V_{out} = V_{in} - V_{th} + N \left[\frac{C_{pump}}{C_{pump} + C_{par}} \cdot V_{clk} - V_{th} - V_{loss} \right] \tag{1}$$

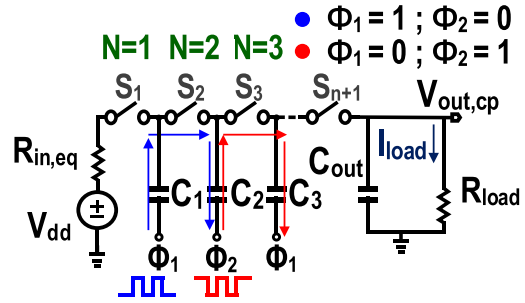


FIGURE 6. Simple scheme of basic charge pump circuit.

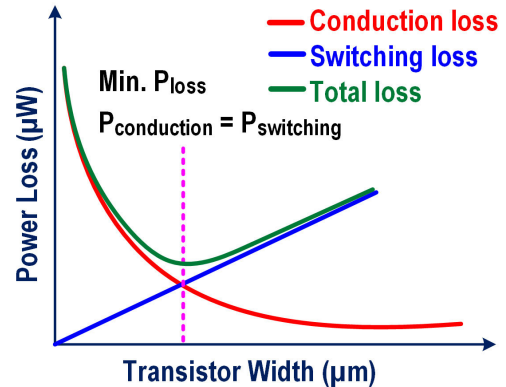


FIGURE 7. Conduction and switching loss with respect to transistor width.

TABLE 2. Type of losses in charge pump circuit.

Type of losses	Details
Redistribution loss	Power loss due to undesirable charge sharing between the capacitors
Conduction loss	Power loss for turning on the transistor with on-resistance Ron
Reversion/leakage loss	Occur when undesired current flow reversely from the high voltage node to low voltage node in CP (Nth stage to (N-1) th stage)
Short circuit loss	Power loss when shoot through current is happened due to temporary shorted in transistor switches
Switching loss	Power loss due to the charge and discharge of parasitic capacitance during the switching process

$$V_{loss} = N \frac{I_{load}}{f_{sw}(C_{pump} + C_{par})} \tag{2}$$

$$\Delta V_{stage} = V_{CLK} \cdot \frac{C_{pump}}{C_{pump} + C_{par}} - \frac{I_{load}}{f_{sw}(C_{pump} + C_{par})} \tag{3}$$

Based on (1), it is observed that four parameters control the maximum output voltage of CP: 1) number of stage N, 2) switching frequency f_{sw}, 3) pumping capacitor capacitance C_{pump}, 4) clock voltage amplitude V_{clk}. The parasitic capacitance C_{par} and threshold voltage V_{th} are not considered as they are the associated parasitic element during the design

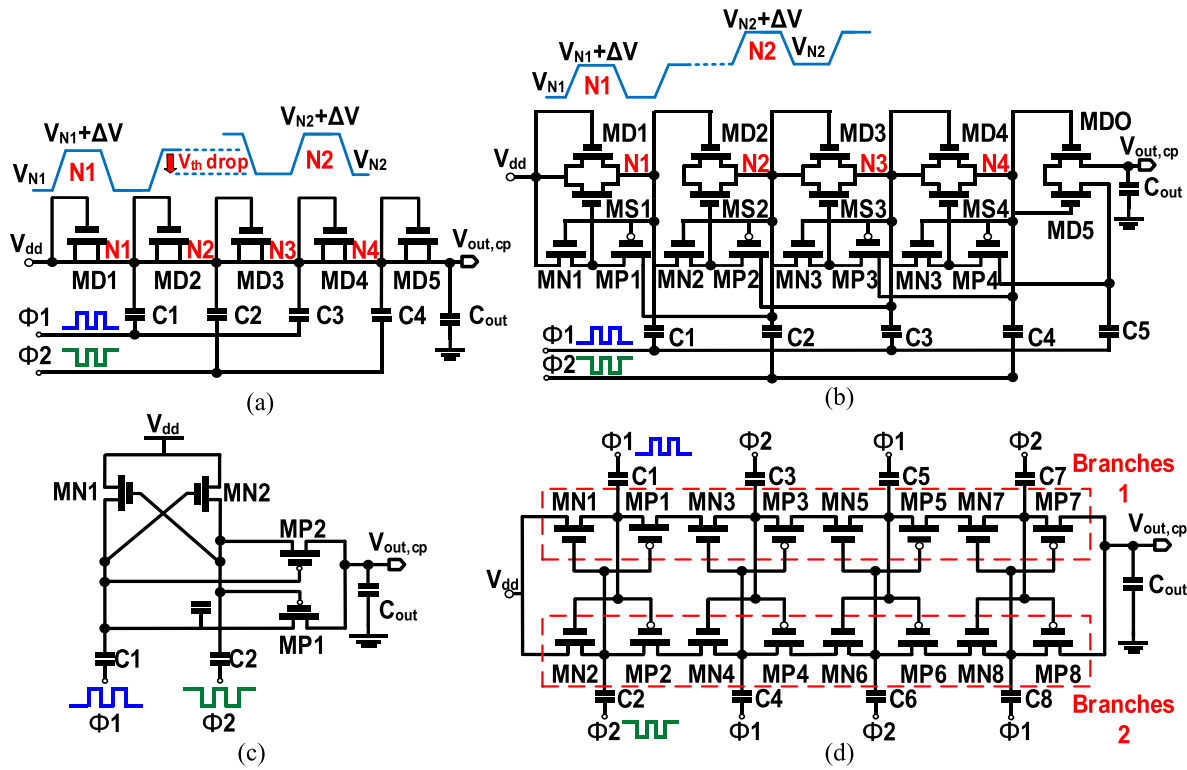


FIGURE 8. State of art charge pump topologies (a) Conventional Dickson [38] (b) Charge Transfer Switch (CTS) II [31] (c) Cross-coupled [43] (d) Dual Branch Latch [48].

implementation and can be minimized by optimizing the mentioned four parameters. In conventional CP circuits, these four parameter values are usually fixed and unconfigurable since they are well-optimized during the design phase to achieve optimum circuit performance in a predetermined condition.

In a practical case, the actual CP output performance is further degraded as it suffers from various power losses during the pumping process. The common loss that is encountered in CP includes redistribution loss [12], conduction loss [32], [33], reversion loss [34], [35], short circuit loss [36] and switching loss [32]. For low voltage CP, reversion, conduction and switching losses are periodized to be eliminated or minimized as they are the main factors deteriorating the CP performance compared to other losses [37]. The total power loss due to conduction and switching loss can be minimized if the condition $P_{conduction} = P_{switching}$ is met as depicted in Figure 7. This can be achieved by carefully selecting the optimal transistor width which can be expressed as (4) where C_{ox} and C_{ov} are the oxide capacitance per unit area and the overlap capacitance per unit width respectively [32].

$$W = \sqrt{\frac{I_{load}^2 L}{f_{sw} V_{dd} \mu C_{ox} (5LC_{ox} + 6C_{ov}) [V_{out} - V_{dd} - |V_{th}|]}} \quad (4)$$

Throughout the years, various CP topologies and improvement techniques have been proposed by researchers to

improve CP performance in terms of PCE, VCE, and dynamic range. Dickson topology is well-known for its simple circuit structure with adequate voltage boosting and current drivability [38], [39]. Yet, the diode-connecting transistors in the Dickson topology induced an inevitable V_{th} to drop across the charge transfer switches (CTS) due to the body effect [39]. As the pumping stage number increased, the difference in the CTS source-bulk voltage also gradually increased, resulting in a higher V_{th} drop and further degrading the PCE. Hence, traditional Dickson topology is not favorable in low-voltage EH applications.

To mitigate this issue, proper CP improvement techniques such as gate and bulk biasing [32], [40], [41] are employed for V_{th} cancellation. For example, the four-phase clock scheme CP with gate boosting techniques and dynamic gate biasing is presented in [40] and [42] which not only delivers a higher PCE in ultra-low input voltage range (33% and 43.1% @ 100mV V_{in}), but also reduces the undesirable reverse leakage between the stages. Yet, the PCE improvement in such low voltage region comes with the cost of additional chip area as [40] employs a bulky LC-based start-up circuit and [42] employs additional NMOS-PMOS transistor pair at each stage that acts as dual control switches. Similar approaches are done in the CTS (II) charge pump [31] shown in Figure 8(b) where additional pass transistors MN_{1-4} and MP_{1-4} are used to achieve dynamic backward control of the CP. As a result, MS_{1-4} can be completely turned on/off, minimizing any power loss due to reverse leakage. Still, these

techniques often come with an additional cost of a special transistor such as triple well CMOS devices to withstand the high voltage on its gate-oxide across each node or require additional auxiliary peripheral circuits such as clock generator and bootstrapping circuit for proper biasing, which bottlenecks to higher power consumption and larger chip area. In other words, the high-power consumption affects the peak as well as WDR PCE of the EH system.

Alternatively, cross-coupled CP, also referred to as latched CP [43], [46] features a very low voltage drop across each charge transfer stage due to a cross-compensation of the threshold voltage. The latch structure of cross-coupled CP also helps in minimizing the switching loss and output ripple [47]. For most applications, a low output ripple is desired since a large output ripple degrades the circuit performance. Still, cross-coupled CP suffers from reversion loss during the overlapping rise and fall transition time of the clock, which leads to a degradation in PCE [48].

To mitigate this issue, CP with dual transfer switches and transfer block techniques has been proposed in [34] and [49] which uses an additional auxiliary transistor to cut off the reversion path and improve the current driving capability. In [50], two pairs of the non-overlapping clock signal are used to precisely turn on and off the charge transfer path and prevent any undesired charge leakage and transfer occurred. While [51] utilized a complementary branch scheme that uses the two-phase signal to prevent simultaneous conduction on the rising edge.

Gate-oxide voltage overstress is another concern in CP circuits as it limits the maximum output voltage and degrades the MOS device's lifetime [52]. This issue worsens with advanced transistors with smaller technology nodes as the gate-oxide thickness is gradually scaled down [52]. Figure 8(d) shows the circuit structure of dual branch CP [48] which can overcome the reliability issue caused by gate oxide overstress in the CP switches. By splitting the single CP into two paths that operate in an interlaying manner, the gate oxide stress encountered by charge transfer switches in each branch is significantly reduced compared to single branch CP [51], [53]. Moreover, the lower gate-oxide stress in each stage allows the usage of smaller switches and capacitor size, which enables an increase in the switching frequency, and reduces the output voltage ripple. Still, the penalty lies in a higher number of transistors used and a larger chip area.

To cope with the low input voltage, CP with a cascaded self-oscillating voltage doubler cell has been introduced in [53] where the cell can self-start from an ultra-low voltage as low as 0.14V and generates a clock signal internally, thus eliminating unnecessary power overhead from clock generator and level-shifter. Although the self-supplied strategy features a very low start-up condition, it comes with a tradeoff between the complex circuit and low efficiency due to the absence of gate-driving circuitry. On the other hand, certain topology focuses on extending the dynamic range of CP using the self-reconfiguration method. For example, [54] proposed a CP topology that can switch between linear and

Fibonacci structures to enhance the current driving capability in different voltage ranges. According to the derivation and simulation result in [54], the Fibonacci structure provides a higher output current when the input voltage is lower than 270mV, while the linear structure is better for input voltage in the range of 270mV and above.

In brief, designing a lossless CP topology is an impractical endeavor. Unlike traditional CP topologies that are solely used to achieve high PCE and VCE, the selection of the reconfigurable CP architecture for EH purposes should also take into consideration the targeted application condition, which in this case high PCE, wide dynamic range, low start-up condition, high reconfigurable resolution, and broad CR range.

B. PERIPHERAL CIRCUITRY

In a reconfigurable charge pump system, the reconfiguration process does not solely dependent on the CP but also on the peripheral circuits such as the CR controller, voltage control oscillator (VCO), non-overlap clocking (NOC), comparator, and so on. A CR controller circuit is responsible for controlling the CP operation by generating a suitable decision control signal so that the CP CR is dynamically changed to obtain optimal PCE.

The control scheme of an RCP can either be purely analog [54], digital [16], [53], or a combination of both [14], [44]. The analog-based control schemes have been dominantly adopted by conventional static CP systems with the advantage of simpler circuit structure and cost-efficiency. However, adaptive control in RCP remains inherently difficult using a purely analog system. On the other hand, a digital control scheme with an intensive analog-digital signal converter, and logic gate usage offers higher flexibility in the control process and is capable to handle a more complex control process compared to an analog control scheme. Typically, a digital control system is easier to be designed than an equally tasked analog control system in terms of total component count and circuit scale. In short, the control scheme of CP has progressively switched from pure analog-based to a combination of analog and digital due to the increasing complexity and adaptive control process.

Unlike conventional CP circuits with only some simple and common peripheral circuits, the reconfigurable CP peripheral circuit has a huge variation from each other since different reconfigurable topologies are used. The primary peripheral circuitry will be discussed in the next sections.

1) COMPARATOR

A comparator is a widely used component in the RCP and is essential in the CP control circuitry for circuit-level decision-making. One of the common use of the comparator in RCP is to act as a sensing circuit or analog-to-digital converter (ADC) [55], [59]. By periodically comparing the varying voltage signal either from the CP input or output path with a predetermined fixed voltage reference [14], [15], [60], the comparator generates a two-state logic output voltage as

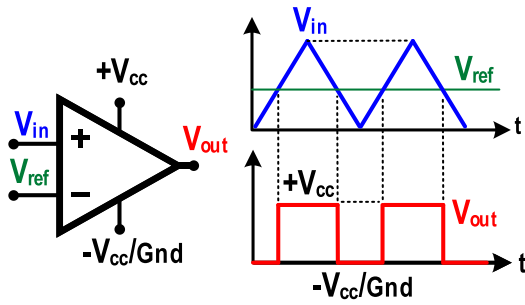


FIGURE 9. Basic schematic of voltage comparator and two-state logic output waveform of comparator with analog V_{in} signal.

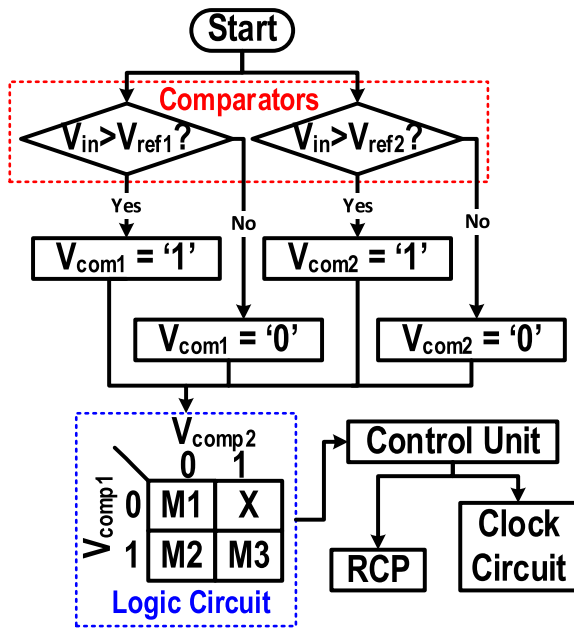


FIGURE 10. Configuration flowchart of common RCP design with 2 comparators and 3 configuration modes (M1, M2, M3).

shown in Figure 9 which will then feed into the corresponding decision-making control circuits, such as the CR controller. Based on the result, these control circuits decide the suitable CP operation mode for the next cycle to achieve the desired CR for optimal output conditions. To reduce the noise effect encountered in the input line, the hysteresis comparator/Schmitt trigger is widely adopted. The hysteresis comparator is a comparator with positive feedback that produce two separate trip points to prevent a noisy input from producing false transitions [61].

2) CONVERSION RATIO CONVERTER

The conversion ratio controller is the most crucial control circuitry in RCP as it acts as the decision maker for the overall CP operation. The goal of the CR controller is to determine the suitable CR value so that the desired CP output can be attained with an optimal PCE under different input voltages. Based on the output result from the decision-aids circuitry, the controller reconfigures the CP CR by modifying the CP system operation mode by tuning one or more system

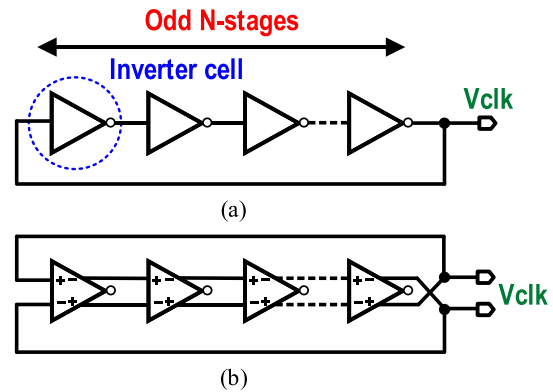


FIGURE 11. Type of R-VCO (a) Single-ended (b) Differential.

operating parameters such as switching frequency, effective capacitance, pump clock amplitude, and the number of active stages. Figure 10 illustrates the reconfiguration process in common RCP designs. A sensing unit, usually a comparator is used to detect the current circuit state and generates a two-state signal (1/0) accordingly [14], [15], [60]. For example, if $V_{in} < V_{ref}$, the comparator output will be '0' and vice versa. Based on this signal, the control unit/logic circuit generates the respective control signal, which further controls the overall CP operation to achieve different configuration modes. For configuration which involves more operation mode, additional comparators are used [14], [15], [60]. Worth noting that the RCP lack of capability to identify which configuration is optimal, instead, it operates according to the control logic. In other words, the RCP can continuously operate under optimal configuration as long it follows the control logic/algorithm which is predetermined in the design phase. The commonly used regulation technique includes active block enable scheme [16], pulse-frequency modulation (PFM) [15], pulse-skip modulation (PSM) [62], pulse-width modulation (PWM) [63], capacitance redistribution [64] and dynamic clock boosting [16]. To attain a finer CR tuning in the reconfiguration process, some architectures may also implement more than one regulation technique to improve the reconfiguration performance in terms of tuning flexibility and resolution [15], [16], [62].

3) VOLTAGE-CONTROLLED OSCILLATOR (VCO)

A VCO serves as a clock signal generator for the RCP circuit where the generated clock signal frequency is determined by the modulated result from the controller circuit. In RCP, VCO is commonly implemented if frequency modulation is performed as the frequency generated from VCO can be easily controlled by varying the supply voltage, which further controls the overall system operating frequency.

Generally, monolithic VCOs can be classified into two major types: LC-VCO and Ring-VCO (R-VCO). Compared to LC-VCO, R-VCO is best suited for EH applications as it features a wide tuning range, low power consumption, and design simplicity [10]. LC-VCO is omitted in this discussion

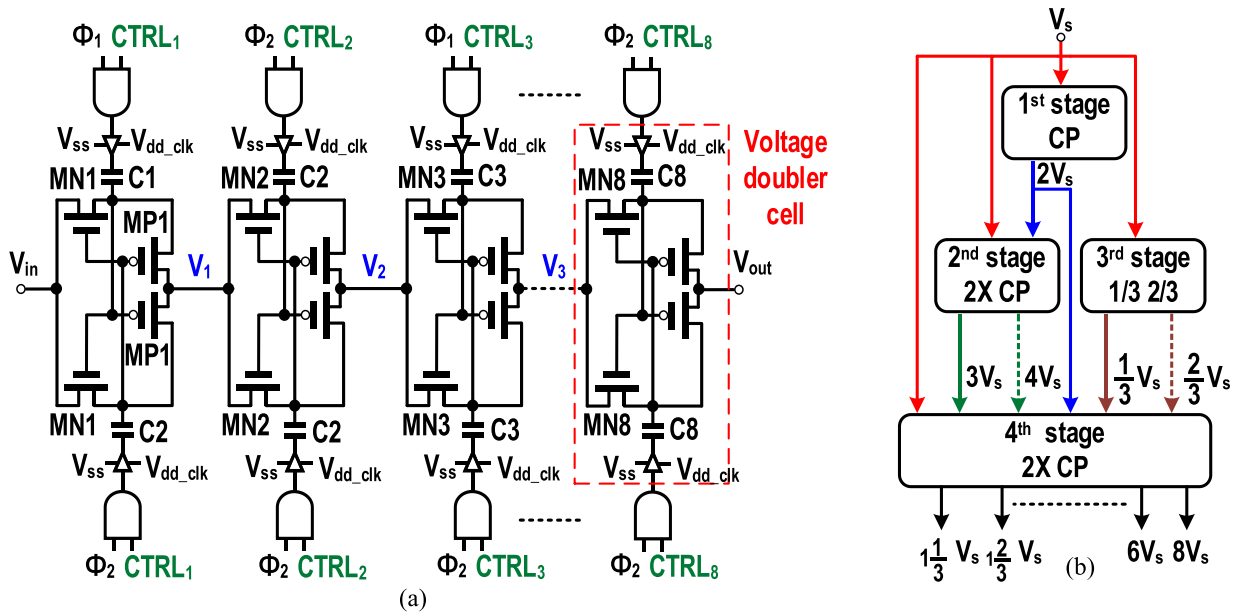


FIGURE 12. (a) RCP circuit architecture with optimal stage selection [16] (b) Conceptual nested cascaded charge pump structure [14].

as it is barely used in the CP for EH application due to the bulky inductor implemented [65], [69]. As depicted in Figure 11, the R-VCO is composed of a series feedback loop of odd-number inverters and can be classified into single-ended and differential ring oscillators. In general, the single-ended RO offers a simpler circuit design and is usually demanded when a small form factor and low power consumption are the primary consideration, whereas differential RO is adopted when noise performance and stability are the primary consideration [70], [71]. The RO operating frequency can be expressed as a function of the propagation delay and the number of inverters stages as described in (5). Based on (5), the VCO frequency f_{vco} can be increased by reducing the inverter stage number $N_{inverter}$ or propagation delay t_{delay} , where t_{delay} can be reduced by increasing the VCO input voltage.

$$f_{vco} = \frac{1}{2N_{inverter} \times t_{delay}} \quad (5)$$

IV. REVIEW OF RECONFIGURABLE TOPOLOGY

A. OPTIMAL STAGE SELECTION

Optimal stage selection (OSS) is a widely adopted reconfigurable technique due to its relatively effective control mechanism and simplicity in implementation. In the OSS mechanism, the number of active CP stages is dynamically adjusted to attain the desired output under different inputs with maximum PCE [14], [16], [72], [73]. By changing the number of active stages, the input voltage is boosted efficiently with the least amount of pump stage involved to avoid unnecessary power loss and operate with optimal PCE [74]. Moreover, a configurable stage number provides a coarse selection of discrete output levels, which is essential in some

applications that require wide-range variable output such as MEMS [16].

Figure 12(a) depicts the RCP architecture with the OSS scheme presented in [16]. In this work, the number of active CP stages is controlled by dynamically enabling or disabling the clock signal fed into each cascaded CP stage. For each CP stage, a pair of AND logic gates controlled by enabling signal $CTRL_i$ ($i=1,2,3,\dots,8$) is employed at the clock signal path where the CP stage can be disabled by setting corresponding $CTRL_i$ low. When $CTRL_i$ is low, the clock signal is prevented from entering the particular CP stages, thus stopping the switching of the capacitor by the clock. As a result, the stage acts as a voltage follower and does not contribute to the overall voltage-pumping process. Consequently, reducing the number of active pump stages as well as the overall CR. Although this work attains a wide tunable output voltage range of up to 10.1V, a significant drop in PCE and output voltage is observed when the clock voltage V_{dd_clk} is below 0.4V. Besides, additional power consumption and parasitic effect are expected in the charge transfer path due to the extra logic circuit implemented.

To mitigate this issue, several works have been reported to minimize the adverse effect caused by the additional component in the charge transfer path. In [72], a stage-selective negative CP with grounded bypass switches is presented so that the stage control process is achieved without adding additional switches in the signal path. In [73], a single pole double throw (SPDT) voltage level shifter circuit is proposed and employed in the stage selection circuit to ensure the maximum voltage across each transistor terminal is kept within normal supply voltage V_{dd} . As a result, both [72] and [73] achieve a high PCE above 50% across a wide output range.

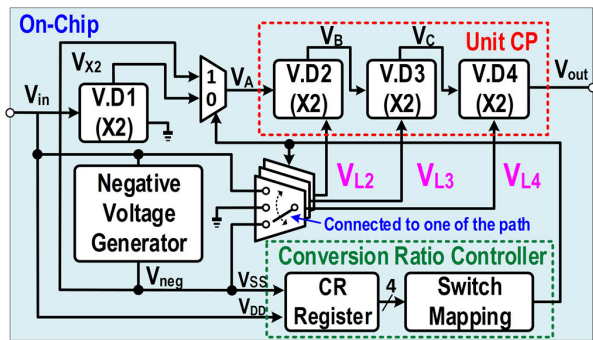


FIGURE 13. System architecture of reconfigurable charge pump using bottom voltage switching [53].

TABLE 3. Stage gain and VCR at Stage Nth for V_{low} = V_{in}, Gnd, V_{neg} [53].

V _L	Stage N th Gain	Stage N th VCR
V _{in}	2(V _{n-1} + V _{in}) - V _{in}	(x2) - 1
Gnd	2(V _{n-1} + V _{in})	x2
V _{neg}	2(V _{n-1} + V _{in}) + V _{neg}	(x2) + 1

Nevertheless, both works suffer from low CR resolution as they can only provide either integral or fractional CRs.

A solution for low CR resolution is presented in [14] where multiple CP cells are cascaded in a nested structure as shown in Figure 12(b). One of the advantages of this cascaded nested structure is the high CR configure resolution with the least number of switches and capacitors usage. By carefully selecting the input connection of each CP cell using a two- or four-way demultiplexer, a wide CR range from 1 1/3x to 8x can be achieved. Additionally, the ability to generate both integral and fractional CR offers a higher configuration resolution which is essential in fine CR tuning. Similar to previous work, the cascaded nested cell can also be bypassed depending on the desired CR. For example, the 3rd stage can be bypassed if fractional CR is not required to reduce power consumption. One of the downsides of this work is that it requires extensive logic control units such as two- or four-way demultiplexer for proper input stage selection which potentially leads to higher power consumption.

B. ADAPTIVE CLOCK VOLTAGE SCALING

In SC-based CP, voltage boosting is achieved by constantly charging and discharging the flying capacitor in each stage through an interlaying clock voltage signal. Based on equations (1) and (3), it is apparent that the CP voltage gain is dominated by the total number of CP stage N and clock signal amplitude V_{clk}. Hence, configuring the V_{clk} is an alternative effective way for CRs tuning besides stage number control. Unlike clock boosting techniques that are commonly used in CP improvement for rising time and stage number reduction [75], the adaptive clock voltage scaling features higher boosting flexibility where the clock drive level is dynamically adjusted based on the control signal from the

controller circuit. The V_{clk} tuning can be realized by implementing an adaptive clock booster circuitry which is usually composed of a two-phase non-overlapping generator, input sensing comparator, gate control generator level shifter, and adaptive clock booster [16], [53]. Ideally, the adaptive clock scheme can be designed to have a wide range of V_{clk} for an extended CR range. However, a high V_{clk} amplitude will cause severe reverse leakage loss, especially in the initial CP stages as the transistors' V_{source} is far higher than the V_{drain}. To mitigate this issue, the gate control circuit is usually implemented with the adaptive clock gain scheme to provide a proper gate biasing for the CTS. The work [76] proposed a dynamic reconfigurable linear CP that exploits the clock amplitude reduction to improve the circuit PCE, while maintaining the speed. The clock amplitude reduction is achieved by implementing a clock amplitude reducer (CKAR) where V_{clk} is set to V_{dd} in transparency mode or half V_{dd} in reduction mode. The implementation of the CKAR in the CP reduces the power loss by more than 35% compared to the original CP design without the penalty in the CP speed. However, power consumption is a concern as additional sub-circuits such as clock scaling circuits and gate control circuits are implemented for optimal circuit operation. Since the implementation of adaptive clock booster/reducer circuitry leads to a complex circuit structure that results in higher power consumption, [53] proposed a simpler V_{clk} tuning technique using a bottom voltage switching mechanism. As depicted in Figure 13, the bottom voltage V_{L2}, V_{L3}, and V_{L4} of CP doubler cells VD2, VD3, and VD4 are switched among V_{in}, Gnd and V_{neg} individually to control the overall CR gain. For V_L connected to Gnd, V_{neg} and V_{in} path, a stage voltage gain of 2x, 2x+1, and 2x-1 is expected as shown in Table 3. Since each CP cell can be connected to a different voltage path individually, a wide CR range can be achieved in a binary manner and generate any CR ratio from 9x - 23x. Here, no clock generator is used as the clock signal is generated internally in the self-oscillating voltage doubler. The elimination of the clocking circuit reduces the power overhead and allows the RCP system to operate in the low input voltage range of 0.14-0.5V. Nevertheless, it suffers from low efficiency (50% peak @ 0.45V input) due to the separate reconfiguration loop and simple cascade connection.

C. FREQUENCY MODULATION

A variable pumping frequency scheme is a reconfiguration technique that alters the CP circuit characteristic by dynamically adjusting the switching frequency depending on the input voltage or load condition. Unlike previous optimal stage selection and adaptive clock scaling schemes that can extend the CP dynamic range through direct CR configuration, frequency tuning is typically implemented in RCP as an associated tuning mechanism to improve the CP transient performance such as output ripple reduction and faster rise time. A common application of frequency tuning in RCP is to act as an impedance tuning mechanism when maximum power point tracking (MPPT) is performed in the EH system.

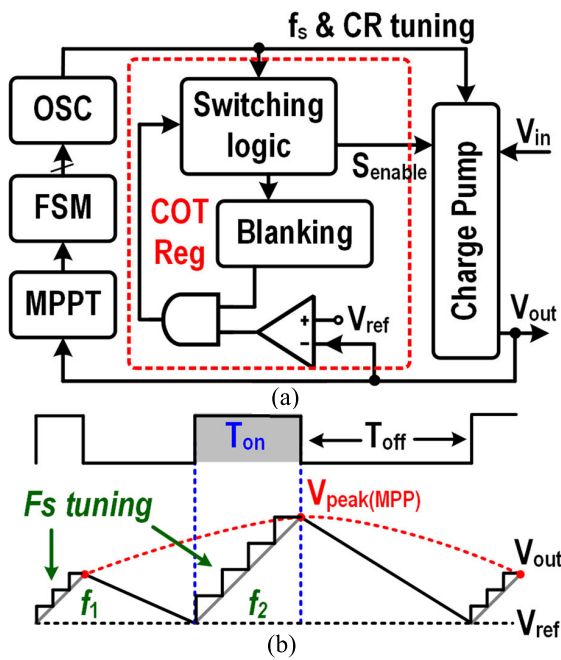


FIGURE 14. (a) System architecture of RCP with COT regulation scheme with f_{sw} and CR tuning [14] (b) CP T_{on} with respect to different f_s [14].

In brief, the goal of MPPT in the EH system is to ensure maximum power extraction from the energy sources [77], [80] by performing impedance matching between the energy source and the harvesting system [81], [83].

In general, the f_{sw} tuning can be achieved by altering the clock signal generator/VCO supply voltage or the number of inverter stages as discussed in section II. Tuning the VCO supply voltage is considered a better approach as the number of inverter stages is usually fixed in the CP circuit [14], [84], [88]. To achieve fine CR tuning and further improve the PCE in WDR input voltage, [14] proposed a two-dimensional MPPT reconfigurable CP topology where the RCP can tune two variables i) number of active CP stage N and ii) switching frequency f_{sw} by utilizing constant on time (COT) regulation as shown in Figure 14(a). As depicted in Figures 14(a) and (b), the COT circuit controls the CP on duration according to the modulated switching frequency f_{sw} to achieve the peak V_{out} defined by the MPPT arbiter. For a high f_{sw} frequency, the CP on time T_{on} will be shorter and vice versa. The implementation of the COT scheme not only features better power utilization as the CP operation time can be dynamically adjusted, but it also eliminates the presence of a power-hungry analog sensing circuit as the power feed into the COT circuit can be reused in the MPPT arbiter. Yet, this kind of two-dimensional tuning comes with the trade-off in complex dedicated power measuring circuits which incur large power overhead [89].

For an EH system that operates in heavy duty cycle, conventional frequency modulation techniques such as pulse frequency modulation (PFM) [37], [62] and pulse skip modulation (PSM) [37] are commonly implemented in RCP as an

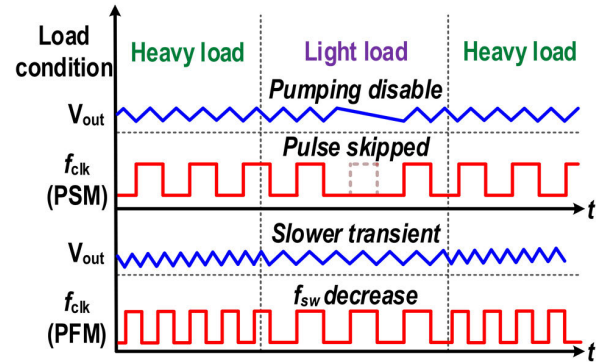


FIGURE 15. PSM and PFM output voltage waveform under different load condition [37].

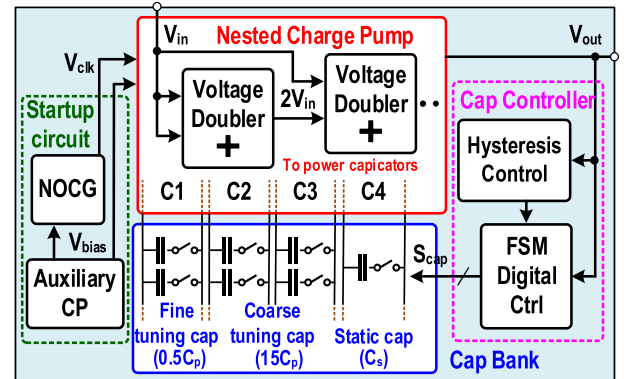


FIGURE 16. System architecture of RCP with capacitance modulation [90].

output regulation mechanism to reduce power consumption in light load or idle condition. As depicted in Figure 15, when the EH system is in light load or idle condition with no extensive output power required, the PFM slows down the CP operation by decreasing the switching frequency, hence conserving the power, and reducing switching loss. Similarly, PSM reduces power consumption by disabling the clock operation and skips some of the clock pulses. As a result, both PFM and PSM offer PCE improvement in terms of lower power overhead even if no direct CR reconfiguration is done. Although PSM and PFM come with the advantage of lower power consumption in light load conditions, they have a trade-off in slower transient response and larger output ripple due to lower frequency. The output ripple can be expressed as (6).

$$V_{out(ripple)} = \frac{I_{load}}{f_{sw} C_{out}} \quad (6)$$

D. CAPACITANCE MODULATION

Similar to frequency modulation, capacitor value modulation is an alternative configuring method to tune the CP impedance in achieving maximum power extraction for the MPPT process. To achieve impedance tuning through capacitance modulation, a capacitor bank is usually required which consists of multiple switched capacitor arrays with different capacitance values [85], [90], [91]. By carefully adjusting the

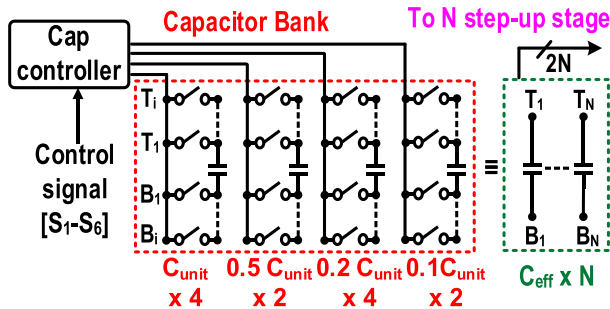


FIGURE 17. Capacitor bank of reconfiguration CP which composed of different capacitance weightage arrays [93].

capacitance configuration network in the capacitance bank, the effective stage capacitance is altered.

The work [90] presented an RCP architecture with MPPT using a capacitance modulation technique. As depicted in Figure 16, the power capacitors C1-C4 of voltage doubler cells are digitized into a bank of multiple-value capacitor arrays. The capacitor bank consists of a static part with static capacitance C_s for minimum usable power delivery and a programmable part with tunable capacitance C_p for impedance tuning. The programmable part of the capacitor bank is further split into a coarse-tuning part that consists of 15 identical capacitors with a total capacitance of $15C_p$ and a fine-tuning part with 1/2 tuning resolution of standard unit capacitor capacitance C_p . Based on the control signal from the MPPT module, the programmable part C_p is configured accordingly to dynamically adjust the effective stage capacitance, and attain an impedance tuning for the MPPT process, where an increase in effective capacitance leads to a decrease in CP impedance and vice versa [90], [92]. Although this work reported a high PCE of up to 80%, it requires a relatively high input voltage range of 1V to 1.5V, which is not favorable for low EH applications with only a hundredth millivolt of input.

A similar approach is demonstrated in [93] but targeting low-voltage EH applications. In this work, a capacitor bank with various weighted capacitance arrays is employed in the RCP where each capacitor array has a different capacitance tuning resolution (C_{unit} , $0.5 C_{unit}$, $0.2 C_{unit}$, $0.1 C_{unit}$) as shown in Figure 17. The capacitance tuning in each array is achieved with the aid of transmission gate switches T_i and B_i that points at the top and bottom sides of each unit capacitor. By enabling or disabling T_i and B_i through control signals S1-S6, the effective stage capacitance is reconfigured and distributed to the corresponding N stages. Compared to prior work [90], this design offers a lower input range from 0.27V to 1V with a peak PCE of 64%. Besides, since all on-chip capacitors are utilized regardless of CP conversion gain, this design features an optimized silicon area utilization compared to the previous design. Still, the bulky capacitor bank remains valid. To eliminate the size-occupied capacitor bank, [64] proposed a different approach of capacitance modulation that can redistribute the capacitance among two charge pump stages, where the first stage stores the excessive power using

TABLE 4. Configuration of charge pump mode under different sunlight intensity and the outcome of each mode [92].

Condition	Mode	Outcome
Strong sunlight	Parallel	Maximum output current with least voltage level boosted
Moderate sunlight	Series parallel	Balance between voltage level boosted and output current
Weak sunlight	Series	Maximum voltage boosting, but lowest output current

MPPT techniques, and the second stage is used for load-powering. The system architecture of the proposed RCP is depicted in Figure 18(a). The proposed RCP consists of 16 sub-modules with CR of $2x$ and is controlled by gate control circuits and digital LDO such that the capacitance is redistributed among two charge pump stages to cope with different output power requirements. The system operation is depicted in Figure 18(b). When in light load condition (sleep mode), 14 sub-modules are distributed to the first stage of CP to maximize the power storing process with the aid of MPPT, and only two CP modules are used to deliver power to the output load. The sub-modules in the first stage are dynamically activated and deactivated by the MPPT circuit to adjust the CP input impedance and achieve maximum power extraction from the PV cell. Conversely, when the light intensity is low or harvested energy is insufficient to cope with the power requirement, the system will turn into active mode and all 16 submodules are distributed to stage two for powering the load. Through the dynamic CP cell reallocations and adaptive energy transfer scheme, a high PCE can be achieved without implementing a large capacitor bank. However, the limited CR in this architecture could restrain its adaptation to the dynamic ambient environment [94].

Besides MPPT impedance tuning, capacitance modulation can be used for CR tuning by adjusting the amount of capacitor involved in the charge transfer path [95], [96]. One of the commonly used methods is to switch the connection of the capacitor between series and parallel form to modify the total effective capacitance and the amount of charge stored in the respective flying capacitors [64], [86], [97], [99]. Figure 19 depicts the proposed RCP architecture in [99], where the RCP can dynamically change its circuit structure between series, parallel and series-parallel modes according to the sunlight intensity variation to achieve different circuit outputs. During the charging phase, all the capacitors that share the same capacitance value are charged to a voltage level of V_{cap} . When discharged, the capacitors are connected either directly to the output node or in series with other capacitors, as shown in Figure 19(b)-(d), resulting in an output voltage V_{out1} , V_{out2} , V_{out3} equal to $V_{in} + V_{cap}$, $V_{in} + 2V_{cap}$ and $V_{in} + 4V_{cap}$. Hence, by simply changing the capacitor connection, different CR can be achieved without adding any extra components to the circuit. However, this configuration process required a significant number of switches and

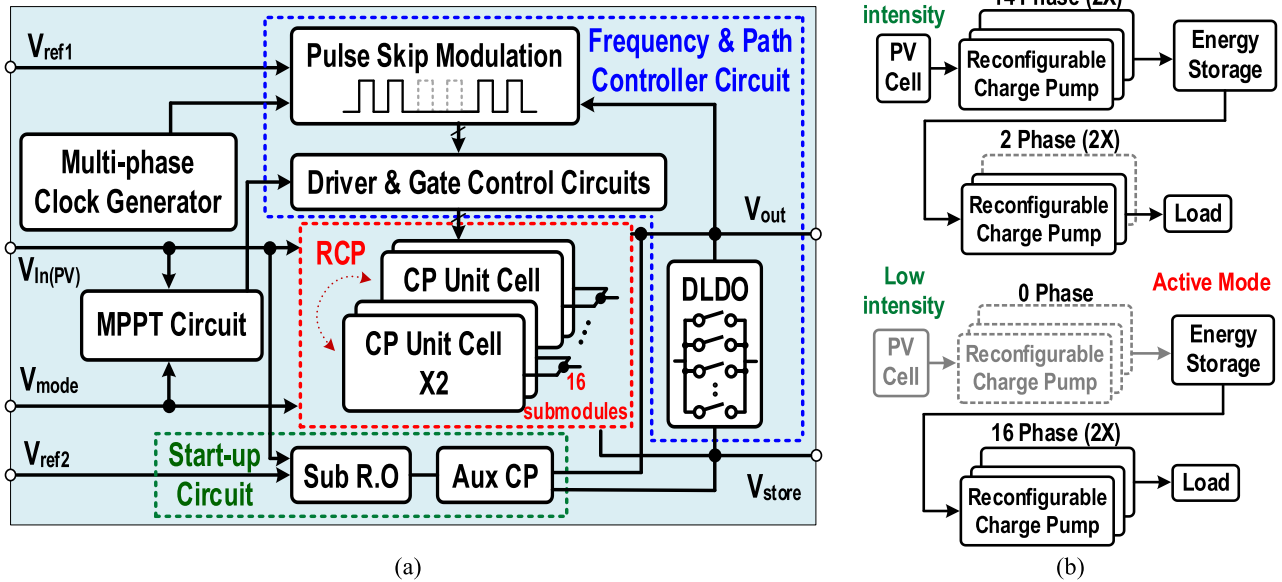


FIGURE 18. (a) System architecture of RCP using capacitance redistribution scheme [64] (b) Sub-modules redistribution under sleep and active mode at different sun intensity [64].

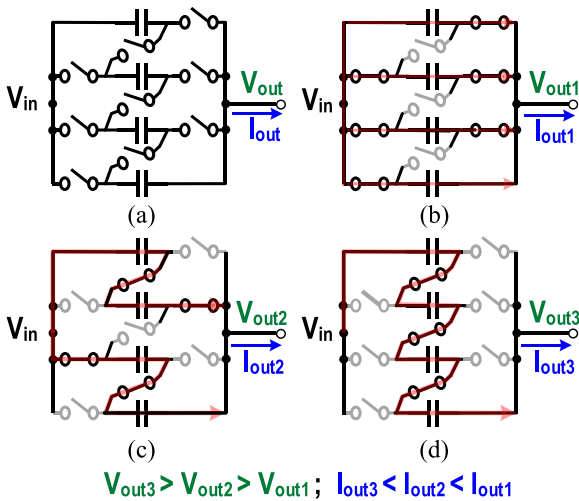


FIGURE 19. Configuration of the circuit structure under (a) Idle (b) Parallel (c) Series parallel (d) Series [99].

additional switches controller to precisely control the state of individual switches.

V. DISCUSSION

In this section, a compressive review will be presented in the context of the advantages and limitations of different reconfigurable topologies. In brief, the CP reconfigurable topology can be categorized based on the tuned parameters during the reconfiguration process: the number of active pump stage N , clock amplitude V_{clk} , switching frequency f_{sw} and effective capacitance C_{eff} . Compared to other topologies, the optimal stage number selection features the most direct and effective CR configuration in terms of the control mechanism. Unlike V_{clk} tuning which usually requires power-starving adaptive clock-boosting circuitry, N can be easily tuned by disabling

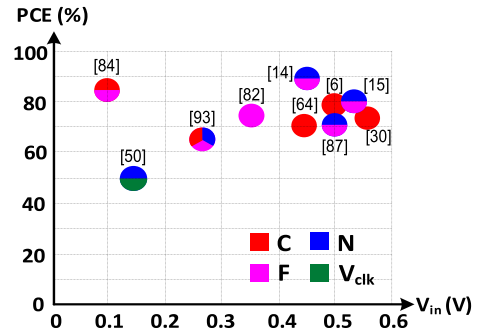


FIGURE 20. Comparison chart of different RCP design performances in Table 5 in terms of V_{in} and PCE.

the clock switching in the CP stages by disconnecting the clock signal path. Furthermore, the PCE of the circuit can also be improved as disabling the CP stage also eliminates all the power consumption, switching loss, and conduction loss contributed by the associated transistors or parasitic elements in the stage [100]. However, low CR tuning resolution is expected in the stage number control scheme as the minimum tunable CR resolution is equal to the CR gain in one CP stage. In other words, N tuning is more amiable when it comes to coarse CR tuning applications. Increasing the total number of CP stages is not an optimal solution as this will lead to the use of more components with a larger chip area and higher power consumption. The CP current consumption concerning N can be expressed as (7), where the optimal N for minimum current consumption is derived as (8) [100].

$$I_{consump(CP)} = [(N + 1) + \alpha \frac{N^2}{(N + 1) V_{dd} - V_{out}}] V_{dd} I_{load} \quad (7)$$

$$N_{optimum} = \left(1 + \sqrt{\frac{\alpha}{1 + \alpha}} \right) \left(\frac{V_{out}}{V_{dd}} - 1 \right) \quad (8)$$

It is also worth noting that increasing the stage number will result in a slower transient response. The relationship between the CP settling time T_{settling} and the number of stages is derived in [101] and expressed as (9).

$$\frac{T_{\text{settling}2} \frac{N_2^2}{f_{\text{sw}} C_{\text{CP}}} \left(\frac{C_{\text{CP}}}{3} + C_L \right)}{T_{\text{settling}1} \frac{N_1^2}{f_{\text{sw}} C_{\text{CP}}} \left(\frac{C_{\text{CP}}}{3} + C_L \right)} = \left(\frac{N_2}{N_1} \right)^2 \quad (9)$$

As a numerical example, a double in the number of the stage ($N_2 = 2N_1$) will result in a 4 times longer settling time ($T_{\text{settling}2} = 4T_{\text{settling}1}$) assuming all other parameters remain unchanged. Such speed degradation is unfavorable in the certain load that requires fast system response, for example, IoT nodes for data logging [76]. Hence, the N tuning is usually implemented in association with frequency tuning to overcome the speed reduction.

Alternatively, V_{clk} tuning offers a higher CR resolution without sacrificing the speed performance. Since V_{clk} amplitude can be dynamically adjusted using an adaptive clock booster/reducer circuit [16], [76], a lesser stage number is required to achieve the same CR gain compared to an equally tasked CP with N tuning topology. The decrease in total CP stage number used in V_{clk} tuning not only benefits in a faster rise time and smaller chip area, but it also improves the overall CP PCE as lesser power loss is induced for fewer stage numbers. However, an additional power-consuming peripheral circuit such as a gate voltage generator is usually required in V_{clk} tuning to provide proper gate biasing for transistors in the charge transfer path so that they do not fall into the cut-off region ($V_g - V_s < V_{\text{th}}$; $V_s = V_{\text{clk}}$) for the case V_{clk} is boosted higher than V_g . Also, a larger transistor with a thicker oxide layer is usually required to withstand the boosted V_{clk} and prevent permanent breakdown. The use of larger transistors not only increases the total area usage but also limits the maximum switching speed due to the increase in the transistor's gate capacitance.

Unlike N and V_{clk} tuning which preserves the original CP circuit connection, C_{eff} tuning directly reconfigurable the circuit network by actively changing the charge transfer path to achieve different CR [30], [64], [97], [102]. Compared to N tuning which suffers from low CR resolution, or V_{clk} tuning which requires a power-consuming boosting circuit, C_{eff} tuning features more flexibility in terms of CR tuning and offers a lower start-up requirement. Still, the penalty lies in the additional switch usage to effectively reconfigure the circuit connection and precisely control the charge transfer path. Besides, the irregular structure also limits the circuit's future reconfigurability. Worth noting that the potential of leakage loss arises significantly following the significant increase in switch number and circuit operation complexity.

Since the impedance of RCP changes continuously respective to the reconfiguration, it raises concerns in impedance mismatch between the RCP and the harvester, which potentially degrades the overall EH performance. To mitigate this issue, some RCP designs are implemented with an MPPT mechanism to dynamically adjust the CP impedance [14],

[30], [64], [87], [93], where RCP impedance tuning is achieved by tuning the circuit switching frequency [14], [30] and effective capacitance [64], [80], [93] as highlighted in section IV. (C) and (D). In low voltage applications, the CP equivalent resistance can be expressed as (10) assuming the CP operates within the slow switching limit (SSL) where all the charge is fully transferred across one and the other stages.

$$R_{\text{CP}} = \frac{1}{CR^2} \cdot \sum_{i \in \text{caps}} \frac{(a_{c,i})^2}{f_{\text{sw}} C_T} \quad (10)$$

By inspection of (9), adjusting the switching frequency f_{sw} or total capacitance C_T contributes the same weightage on the CP equivalent resistance R_{CP} . However, frequency modulation is more amenable for impedance tuning in MPPT applications for size-constrained on-chip integration as capacitance modulation usually requires a large capacitor bank that leads to a high area penalty [14]. On the other hand, frequency modulation features an area-compact solution for MPPT impedance tuning in RCP as the frequency can be easily tuned by configuring the existing VCO.

Besides the MPPT application, frequency tuning is also useful when used as an associated tuning mechanism for fine CR tuning in RCP. For the EH system that operates in heavy-duty-cycles, frequency tuning is used as an output regulation mechanism to minimize unnecessary power consumption in idle/light load conditions by reducing the CP operation frequency. A low switching frequency is usually preferable to attain an optimal PCE as it reduces the CP switching losses and the power consumption in VCO. However, the decrease in switching frequency will result in a larger ripple voltage which potentially causes noise distortion in the RCP circuit and degrades the CP transient response.

Throughout the paper, we have provided an extensive overview of various reconfigurable CP topologies as well the circuit architectures in terms of the tuning process. For ease of understanding, Figure 21(a) provides an illustrative overview of RCP design consideration in the attempt to achieve i) WDR ii) high PCE, and iii) high VCE for EH application. As depicted in the figure, any attempt in optimizing one of the mentioned targets leads to a certain contradicting trade-off in other aspects. For example, an RCP with a WDR usually suffers from a lower peak PCE compared to an RCP with a narrower dynamic range. This is because more power consumption is induced at the additional peripheral control blocks to achieve a WDR [103], [104]. Similar to VCE and PCE, a high VCE does not guarantee a high PCE as the high output voltage usually comes with low current output, resulting in a low output power [104]. Hence, the designer must identify the primary target and find the optimal balance between the design goal and the associated trade-off. The best design outcome is to achieve the primary target satisfactorily with reasonable degradation in other aspects. After all, it is an impractical endeavor to design a perfect CP with optimal performance in every aspect.

Apart from this, Figure 21(a) also provides lists of commonly tuned parameters including clock amplitude [10], [16],

TABLE 5. Summary table of state-of-the-art RCP for energy harvesting.

Ref	Tech (nm)	EH source	Topology	Tuned variable	Fully integrated	MPPT	CR	Vin (V)	Vout (V)	PCE (%)	Area (mm ²)
[6]	130	Solar / PV	Multi-step split merge CP	C	Yes	No	N/A	0.5	2.79	78.6	0.98
[14]	180	PV / TEG	RCP with COT regulation scheme	N,F	Yes	Yes	$1\frac{1}{3} - 8$	0.45	3.3	89	1.84
[15]	180	PV	RCP with TFM scheme	F, N	Yes	No	2,2.5, 3	0.53	1.2	80.8	4.04
[30]	65	PV, Piezo	Multiple input single output RCP	C	Yes	Yes	$\frac{1}{3} - 5\frac{1}{3}$	0.55	2.5	74.6	0.47
[53]	180	PV	Self-oscillating doubler cell with bottom voltage switching	Vclk, N	Yes	No	9-23	0.14	2.2	50	0.86
[87]	180	PV	RCP with thyristor based VCO	N, F	Yes	Yes	1,2,4	0.5	1.8	72	0.55
[93]	130	TEG	Cascaded step-up stage with 3-D MPPT	F,N,C	Yes	Yes	1-6	0.27	1	64	0.84
[64]	180	PV	Dual mode capacitor redistribution scheme	C	Yes	Yes	2,3,4	0.45	1.5	69.5	1.69
[82]	180	PV	Dual output VBC with medium and high voltage generator	F	Yes	Yes	3,9	0.35	0.86	75.8	1.75
[84]	180	TEG	Dual mode PMU with FCS scheme	C, F	No* (External Battery)	Yes	N/A	0.1	0.75	85.4	3.89
[90]	180	PV	Nested CP with digital controlled capacitor bank	C	Yes	Yes	3	1	3	88.7	2.25
[96]	250	N/A	Switch-controlled serial parallel reconfiguration	C	Yes	No	0.25-2	1.7	3.6	93.8	1.7
[75]	65	N/A	Dual branches RCP with clock voltage scaling	Vclk, N	Yes	No	N/A	0.45	1.2	73	0.023
[103]	180	N/A	Hybrid 4/6 stages CP using parasitic	N	Yes	No	3-6	1	3	58	0.5

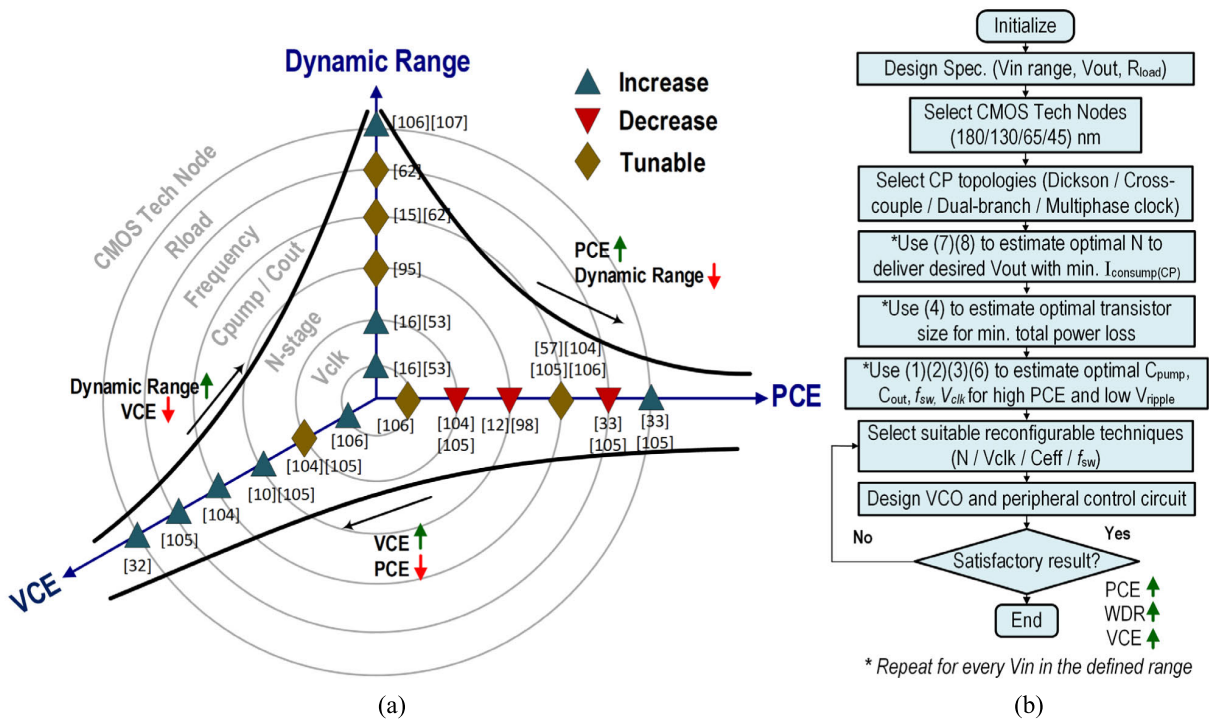


FIGURE 21. (a) Charge pump design consideration and approaches for achieving wide dynamic range, high PCE and VCE (b) RCP design flowchart.

[53], [105], N-stage [53], [103], [104], C_{pump} or C_{out} [10], [12], [95], frequency [15], [62], R_{load} [32], [33] and CMOS technology node [32], [106]. Here, R_{load} and CMOS technology node are included as one of the tunable parameters since both of them can be defined by the designer during the design process even though they are barely discussed in previous sections. The design approach for each of these parameters is summarized in a form of whether to increase, decrease, or tunable depending on the desired goal. Taking N-stage as an example, considering in normal condition, a higher number of N-stage usually guarantee a higher output voltage and better VCE since more pumping stage is involved [16]. Similar to dynamic range, a higher number of N-stage is required to attain a wide dynamic range as the designer can have higher flexibility to configure the CP circuit. Furthermore, the increase in stages indicates a higher resolution in terms of the CR reconfigurable process, allowing fine-tuning process which can greatly improve the circuit sensitivity [16], [53]. However, a higher number of N-stage indicates a larger amount of component count used such as transistor switches and pumping capacitors, resulting in a higher power loss due to parasitic element and body effect [53], [104]. Hence, the N-stage number has to be kept minimal if PCE is desired to be enhanced or increased when VCE and dynamic range is targeted as shown in Figure 21(a).

A parameter with a tunable sign indicates no consistent design approach (increase or decrease) to attain the design goal. Taking frequency as an example, although decreasing the frequency offers a lower power consumption which

improves the PCE, however, the low frequency will result in a large ripple voltage and potential noise distortion in the CP operation, which ultimately degrades the PCE. On the other hand, increasing the frequency helps in reducing the output ripple. Yet, the high frequency might lead to higher power consumption as well as various power loss such as switching loss and incomplete charge transfer. Thus, the best approach is to perform trial and error to determine the optimum value.

A systematic design flow is depicted in Figure 21(b) to aid the designer in designing the RCP effectively. First of all, the designer must identify the design specifications such as the expected dynamic range of V_{in} , desired V_{out} and R_{load} . After the design goals are set, the designer can decide on the technology node and CP topology to be used according to the requirement. Next, the optimal N, C_{pump} , C_{out} , V_{clk} , f_{sw} , transistor width for each V_{in} in the defined input range are estimated from the equations (1)-(4), (6)-(8) accordingly as depicted in Figure 21(b). Once the circuit characteristic and optimal parameters in each defined V_{in} are obtained, the designer can have the freedom of selecting suitable reconfigurable techniques and peripheral control circuits for WDR. The performance of the RCP system is achieved by selecting the optimal parameters in CP peripheral circuits from the given design consideration as shown in Figure 21(a).

Although many works on high PCE, wide dynamic range RCP have been reported, most of these designs exhibit optimal performance for a minimum input voltage, V_{in} ranging from 0.3V to 0.8V, which is less attractive compared to the conventional charge pump with fixed voltage conversion ratio

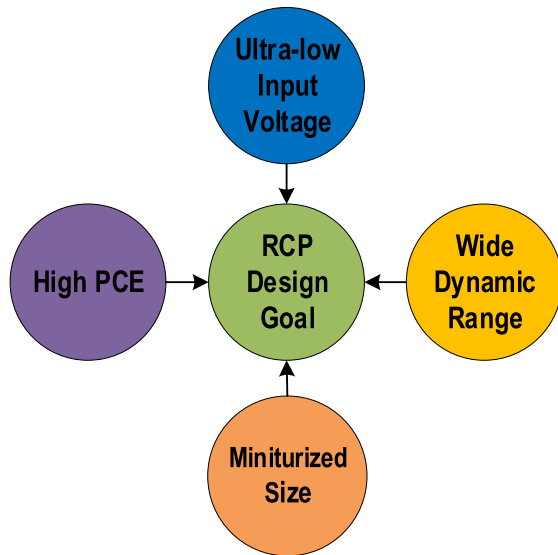


FIGURE 22. Future design goal of RCP in EH application.

in the context of cost and design complexity. The reported work with a minimum V_{in} of less than 0.3V [53], [84] usually suffers from low PCE or requires an external voltage source, which is not favorable for miniaturized EH applications. The PCE degradation is mainly due to insufficient supply voltage for the transistor's operation and higher overall power consumption in RCP due to additional control circuits. To improve the RCP performance and competitiveness for EH applications, the future design direction of RCP should focus on the ultra-low voltage region (0.1-0.25V). In particular, the research goal is to design an RCP that can operate in ultra-low voltage region (0.1-0.25V) abstaining from the integration of external voltage sources while maintaining a reasonably high PCE in a wide dynamic range, as depicted in Figure 22.

VI. CONCLUSION

In conclusion, this article has provided an overview of the reconfigurable charge-pump circuit for EH systems. A summary of the state-of-art charge-pump design for the EH application, specifically in the reconfigurable system has been considered. A review of reconfigurable charge-pump circuits has been presented which has discussed various prior state-of-art architectures in the aspect of tuning mechanisms, design techniques, and trade-offs. Considering a wide input voltage and a wide range of high PCE charge-pump circuit designs, a visualized design trade-off chart of RCP has been demonstrated to aid the designer to have an overall view of the design approach and consideration when designing a high-reliability reconfigurable CP in terms of PCE and wide dynamic range.

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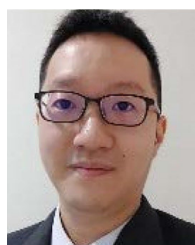
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