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RESEARCH ARTICLE

Evaluation of New Grid Codes for Converter-Based DERs From the Perspective of AC Microgrid Protection

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ABSTRACT The ever-increasing penetration levels of converter-based distributed energy resources (DERs) in medium and low voltage (MV/LV) distribution networks necessitate new and revised standards or connection requirements of generating units. These standardized connection requirements to be met by DERs are called grid codes. This paper reviews new European and IEEE grid codes of MV/LV converter-based DERs and presents an evaluation of selected grid codes applicable for AC microgrid protection. The selected grid codes are evaluated for both grid-connected and islanded modes of AC microgrid operation. The standardized settings of different protection schemes including symmetrical components-based protection schemes are evaluated for quick fault detection and isolation during the most challenging unbalanced faults in grid-connected and islanded modes. The extent of dynamic reactive power (Q) injection by DERs according to European grid codes is evaluated and the effect of Q-injection on fault detection and protection coordination is observed. The generic grid-forming DER model with coupled dq-control has been enabled to provide enough reactive current during the unbalanced faults with the help of an additional Q-source. It is concluded that the grid code requirement of dynamic Q-injection can be met by converter-based DERs with an additional Q-source of minimum capacity equal to twice the apparent power of individual DER in the grid-connected mode. The same extent of Q-injection is also useful for fault detection and reliable directional element design in the islanded mode. A new five-cycle overvoltage ride-through (OVRT) curve is also suggested for smooth transition to the islanded mode.

INDEX TERMS Grid codes, converter-based DERs, AC microgrid protection, symmetrical components.

I. INTRODUCTION

The strong desire to reduce carbon emissions and exploit the benefits of sustainable renewable energy sources (RES), the integration of distributed energy resources (DERs) in the distribution networks has been accelerated during the last decade. The DERs include wind turbine generators (WTGs), photovoltaic (PV) systems and other small-scale combined heat and power (CHP) micro-sources and energy storage systems (ESS). The integration of the DERs close to the load centers offers multiple advantages like the deferral of grid expansion, the reduction of distribution losses, the increased reliability and the continuity of uninterrupted power supply during grid outages. However, the connection of different individual DERs close to the load centers may cause some adverse operational problems like protection coordination and sensitivity problems, local voltage-rise, reduced power quality, over frequency, over loading of lines and transformers, and reactive power unbalance in the local distribution systems. Therefore, new mitigation measures are required to overcome these new challenges. One promising way to tackle these challenges is to plan the future smart distribution networks comprised of multiple individual self-managed and controlled building

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blocks called microgrids. A microgrid with different DERs, loads and ESS could be controlled locally using a microgrid management system (MMS) and thus could interact with the local distribution grid in an acceptable manner either as a net producer or a net consumer of the electrical energy. A microgrid can operate in the islanded mode during main grid outages, thus increasing the reliability of supply to the consumers [1], [2].

The grid-connected mode of operation of the DERs is the usual practice around the world except on distant geographical islands with no connection to the transmission and distribution grids. The diesel and gas generators are usually used there as the main energy sources along with WTGs, PVs and CHP units. For example, the Hailuoto island in Finland uses the diesel generator along with the WTGs and PVs systems for the islanded mode of operation during the grid outages [3]. The extensive use of the diesel and gas generators in this new era of clean and renewable generators is not much accepted and they are likely to be replaced with the BESS or operated only as a final resort when the rest of energy resources are completely depleted.

Currently, the islanded mode of operation of the DERs and microgrids is usually prohibited in the distribution networks due to technical limitations and safety concerns. The islanded mode of operation will, however, enhance the reliability level of the existing distribution networks if planned well with suitable grid-forming DERs and ESS [1], [2].

The behavior of the converter-based DERs is usually different from the behavior of the conventional synchronous generators. On the one hand, the converter-based DERs lack the inertia of rotating machines due to their decoupling with the electric grid through the frequency converters. On the other hand, the converter-based DERs provide the limited short-circuit current contribution due to the limited current ratings of the converters because of the economic reasons to employ highly over-rated converters. However, the converter-based DERs are very quick to operate and control within milliseconds (ms) thanks to the fast power electronic switches. Therefore, the behavior of the converter-based DERs can be easily and quickly controlled in any mode of operation, grid-connected or islanded mode [2].

The grid-connected and the islanded modes of operation of AC microgrid require adaptive overcurrent (OC) protection schemes with at least two setting groups of different current thresholds or sensitivities. This is required due to the increased fault current contribution from the main grid in the grid-connected mode and the reduced or limited fault current contribution from the converter-based DERs in the islanded mode even during the balanced three-phase (3Ph) or LLL faults. The most challenging unbalanced shunt faults like line-to-line (LL) and single-line-to-ground (SLG) faults and the series or open circuit faults result in fault current of less than or equal to load current. Therefore, symmetrical components-based protection schemes may also be required for detection of these faults. Additionally, the distribution lines with DERs on both sides and the ring or looped network topology require the reliable directional schemes for the maintenance of protection selectivity.

The symmetrical components analysis is usually used to find the magnitude of positive-, negative- and zero-sequence components of fault currents and voltages in a three-phase power system. During the normal operation of three-phase distribution system and a balanced ungrounded short-circuit fault (LLL-fault), only the positive-sequence (Pos-Seq) current flows from the sources or generators to the loads which is identical to the rms current. The occurrence of an unbalanced shunt fault like LL-fault between any two live conductors of a distribution line gives rise to both the Pos-Seq and negative-sequence (Neg-Seq) current. The zero-sequence (Zero-Seq) current only increases when there is a shunt fault to the ground, like the SLG, double-line-to-ground (LLG) or three-phase-to-ground (LLLG) faults. The Zero-Seq current may only be available locally depending on the transformer connection type of delta and star (grounded/grounded) at its primary and secondary side. A series fault also known as an open circuit fault generates both the Neg-Seq and Zero-Seq components. The Neg-Seq component is present in all fault types except the balanced LLL-fault and can be used for the detection of broken conductors on transmission or distribution lines and open/close failure of breaker on one or two poles. Any presence of the Neg-Seq and Zero-Seq components during the normal fault-free operation is an indication of unbalanced line impedances, source voltages or load currents [4], [5].

Traditionally, the phase OC or Pos-Seq OC function (51P) clears the most short-circuit faults within the preset coordinated tripping time intervals. The Neg-Seq OC function (51Q) and Zero-Seq OC function (51G) can be used as backup for the detection of those faults which are difficult to be detected by using only 51P protection function (e.g., LL, LG, LLG faults) [6]. The coordination of Neg-Seq and Zero-Seq OC functions can also be done in definite-time or inverse-time just like the Pos-Seq OC function [5], [7] and at least for a local backup to 51P function.

The setting of thresholds and tripping time intervals of the Neg-Seq and Zero-Seq OC functions (51Q and 51G) for the protection of distribution networks with lines and cables may vary depending on the type of grounding schemes, the type of faults and the resistance or impedance of the faults to be detected. These issues are usually addressed separately.

The setting of the tripping threshold of the Pos-Seq or phase OC function (51P) is usually selected above the maximum expected magnitude of load current or inrush current whichever is applicable. The setting of the tripping threshold of the Zero-Seq or ground OC function (51G) is usually selected above the value observed during the highest possible load unbalance [4]. The tripping threshold of 51Q function should be set above any standing load unbalance observed at the relay. For 3Ph motor loads a good level of sensitivity of 51Q function is achieved due to the balanced nature of loads. However, a large 1Ph load on transformer may compromise the sensitivity of 51Q function [8].

Directional discrimination is also required for proper selectivity or coordination of forward and reverse faults in ring-networks or networks with generators on both sides. This can be accomplished with the directional OC function (ANSI 67) with either definite-time or inverse-time characteristic.

The directional OC function not only requires the tripping threshold of the current but also requires the direction of the fault if the fault is in front of the relay (forward fault) or behind it (reverse fault). The directional coordination or discrimination of forward faults in the tripping direction and reverse faults in the non-tripping direction is done using different methods or principles which are usually different for balanced and unbalanced faults.

The directional element (67P) for the balanced fault is usually designed based on phase comparison of Pos-Seq voltage and Pos-Seq current using voltage as the reference or polarizing quantity and the current as the operating quantity. Depending on the set criteria if the phase angle enters the operating area, the fault direction is declared as the forward or the reverse. This scheme may fail due to close-in three-phase short-circuit fault which causes voltage of all phases to fall to a zero magnitude, therefore the magnitude of Pos-Seq voltage is also zero [9]. Hence, the stored memory of the voltage before the fault is usually required for this scheme to work properly for the detection of fault direction [10]. There are also other methods reported in [10], [11], [12], and [13] that use the current-only polarization for the estimation of fault current direction. These schemes can be useful in situations when either the voltage transformer (VT) is not available, or the extra cost of VT is to be avoided.

Using the Neg-Seq voltage and current, it is possible to design a reliable directional element (67Q) for all unbalanced faults in traditional distribution networks. For the ground faults, the Zero-Seq voltage and current can be used to design a ground directional element (67G). The principle of finding the direction can be based on traditional phase comparison of voltage and current or impedance-based directional element [4]. The details about the directional element design and evaluation can be found in [14]. The traditional Neg-Seq directional element and Neg-Seq impedance directional element are discussed in more details in [15].

The converter-based DERs behave as sources of the limited constant current of 1-2 p.u. during the faults irrespective of the design and control of their converters as voltage source converters or current source converters. The converter-based DERs typically provide negligible magnitude of Neg-Seq or Zero-Seq current. Most controllers of the converter-based DERs are usually designed to regulate Pos-Seq current and suppress the Neg-Seq current partially or entirely during the faults [16], [17]. The results from [18], [19], and [20] show the mis-operation of the Neg-Seq directional relays due to the different Neg-Seq fault current characteristics of the converter-based DERs (including type-4 WTG) compared with synchronous generators. However, this impact will be reduced in future as new grid codes require the converter-based DERs to supply a certain amount of Neg-Seq reactive current during the voltage steps or faults. The injection of Neg-Seq short-circuit current by the WTGs proportional to the Neg-Seq voltage is proposed in [17] particularly for the detection of LL-faults.

This requirement may vary according to different national and regional grid codes as reported in [21]. The reactive current support during the short-circuit faults up to the rated current of the DER is required by the latest EN grid code [22] as reviewed in the section II of this paper.

Different regions and countries of the world with increasing penetration levels of the DERs in transmission and distribution networks have set rules and regulations for the connection of DERs, called as ''grid standards'' or ''grid codes'' of DERs. These grid codes define the operational behavior of different types of DERs during the steady-state and fault conditions in order to avoid the adverse effects to the grid assets as well as to the local consumers in the grid-connected operation.

This paper reviews and evaluates the latest active IEEE standards and the common European standards/grid codes (abbreviated as EN) for the converter-based DERs connected at medium voltage (MV) and low voltage (LV) distribution networks for the grid-connected and islanded mode of operation. Particularly, the latest approved European standards EN 50549-1:2019 [23] and EN 50549-2:2019 [22] for generating plants to be connected in parallel with the LV and the MV distribution networks, respectively. The IEEE standard closely related to these European standards is the IEEE standard 1547-2018 [24] which deals with the interconnection and interoperability of the DERs with the associated electric power system (EPS). The impact of the IEEE standard 1547-2018 on the smart inverters is already evaluated in the technical report PES-TR67 of the IEEE power and energy society [25] which is considered as a guide in this review.

The IEEE standard 1547.4-2011 [26], which deals with the DER island system, has also been reviewed briefly to cover the islanded mode operation of the AC microgrid. Related to the different modes of AC microgrid operation like grid-connected, islanded and transition modes the change of DER controls are necessarily required to maintain the stability of the AC microgrid. Therefore, the IEEE standard 2030.7-2017 [27] which defines the specification of microgrid controllers has also been reviewed.

In this paper, the evaluation of EN 50549-1-2019 and EN 50549-2-2019 grid codes have been investigated from the perspective of the protection of AC microgrid. In this regard, symmetrical current- and voltage-based protection schemes have been evaluated for fault detection and protection coordination with a certain amount of reactive current injection by the grid-forming DER during the LL unbalanced faults. The additional amount of reactive current at DER terminals is injected only during the LL unbalanced faults to enhance the Neg-Seq component of fault current. For this purpose, an additional fast acting thyristor switched capacitor (TSC) has been suggested at LV terminals of DER. The TSC is

TABLE 1. Limits for thresholds for type B, C and D power generating modules [28].

Synchronous area	Limit for max capacity threshold from which on a power gen module is of type-B	Limit for max capacity threshold from which on a power gen module is of type-C	Limit for max capacity threshold from which on a power gen module is of type-D
CE	1 MW	50 MW	75 MW
GB	1 MW	10 MW	30 MW
Nordic	1.5 MW	10 MW	30 MW
IE and NI	0.1 MW	5 MW	10 MW
Baltic	0.5 MW	10 MW	15 MW

gen = generating, MW = Megawatt, CE = Continental Europe, GB = Great Britain, IE = Ireland, NI = Northern Ireland.

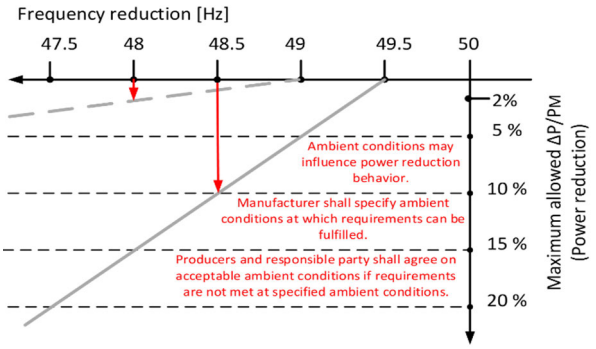

FIGURE 1. Maximum allowable power-reduction in case of UF [22].

switched only in continuous ON or OFF states when the fault condition becomes activated or deactivated by the control.

The use of additional TSC helps to detect the unbalanced shunt and series (open phase) faults using Neg-Seq OC and ratio of Neg-Seq OC and Pos-Seq OC protection functions particularly in the islanded mode of operation. The additional reactive current is evaluated at the DER terminals according to the EN 50549-2-2019 grid code. The DERs are modelled in MATLAB/Simulink using the synchronous frame of reference or dq-control with a limited amount of Neg-Seq current provision capability in the absence of TSC. The symmetrical components-based directional elements are also designed and evaluated during the LL unbalanced faults for the maintenance of protection selectivity before and after Q-injection.

The rest of the paper is organized in a way that Section 2 presents the review of the European EN grid codes for the converter-based DERs, and Section 3 gives review of the IEEE grid codes/standards for the converter-based DERs. Section 4 evaluates the protection related grid codes using the simulations performed with MATLAB/Simulink. Section 5 gives the discussion and Section 6 concludes the paper.

II. EN GRID CODES FOR CONVERTER-BASED DERS

This section reviews the two recently approved EN grid codes i.e., EN 50549-1:2019 [23] and EN 50549 2:2019 [22] for generating plants to be connected in parallel with the LV and MV distribution networks, respectively. Both of these grid codes cover the generating plants up to and including type-B. In conformance to the network code on requirements for grid connection of generators (NC RfG), type-A category of power generating modules have connection point below 110 kV and the maximum capacity of 0.8 kW or more. The type-B, type-C and type-D generating plants/modules are defined in Table 1 [28]. For example, in the Nordic synchronous area type-B generating plants have the active power (P) capacity range of 1.5-10 MW, type-C generating plants have the active power capacity range of 10-30 MW and type-D generating plants have the active power capacity range of 30 MW or more. From the context of this paper, the converter-based generating plants are referred to as DER plants or simply DERs.

A. CONTINUOUS OPERATING FREQUENCY AND VOLTAGE LIMITS

The considered EN grid codes of the DERs in general are comprised of two main parts, one-part deals with the steady-state operating conditions of the DERs and the second-part deals with the operating conditions of DERs during the fault events and other contingency or disturbance conditions. For the steady-state operating conditions, the normal or continuous operating ranges of voltage and frequency of the DERs are defined with respect to the different operational time durations to avoid the possible voltage and frequency instability of the well synchronized power system.

The continuous operating frequency range for the DERs connected to the LV and MV networks is defined as 49-51 Hz [22], [23]. The operation of DERs below the frequency of 49 Hz is considered as underfrequency (UF) operation and over the frequency of 51 Hz the operation is considered as the overfrequency (OF) operation.

During the operation below 49.5 Hz frequency in the grid-connected mode of operation, a maximum active power reduction (ΔP) of 10% of the maximum active power (P_M) per 1 Hz reduction of the frequency is allowed by default for the DER plants connected to the LV or MV networks. However, the most stringent requirement is to reduce only 2% of the maximum active power per 1 Hz reduction of the frequency (see Fig. 1) [22], [23]. Fig. 2 gives the minimum and stringent time periods for the DER operation during the UF and OF situations. The same operating ranges are applicable for the DERs connected to the LV and MV networks.

The continuous operating voltage range capability of the DER plants connected to LV networks is 85–110% of U_n where U_n is the nominal voltage [23] and the continuous operating voltage range capability of the DER plants connected to MV networks is 90–110% of U_c where U_c is the voltage at the connection point [22].

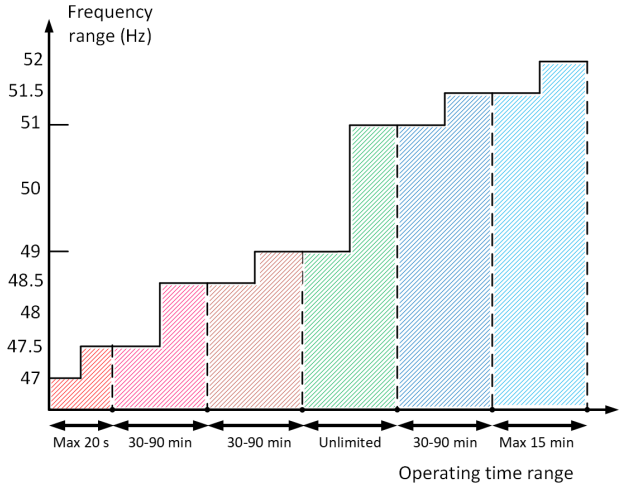

FIGURE 2. Operating time range vs frequency range [22], [23].

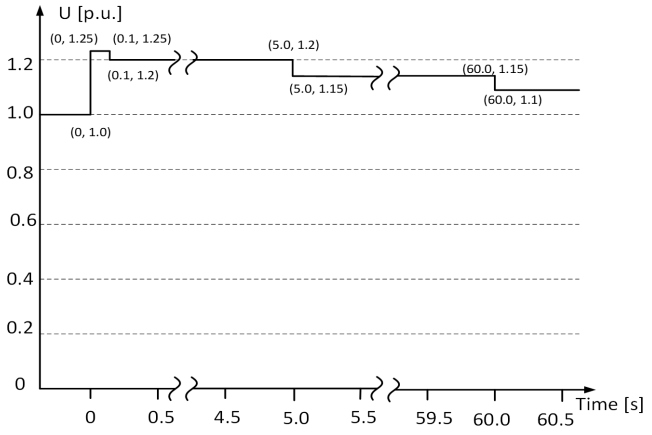

FIGURE 3. The OVRT curve of the DER plants for connection to the LV and MV networks [22], [23].

B. IMMUNITY TO THE FREQUENCY AND VOLTAGE DISTURBANCES

Beyond the continuous allowable voltage and frequency ranges the variations of the voltage and frequency are considered as *the disturbance operating conditions*. The immunity to disturbance operating conditions is required by the DER plants to prevent their unnecessary disconnection for maintaining the stability of the network, particularly with the high penetration level of the DERs in LV and MV networks. Three types of the immunities to disturbance are defined in both standards EN 50549-1-2019 [23] and EN 50549-2-2019 [22]: The first immunity is the rate-of-change-of-frequency (ROCOF) immunity, the second one is the undervoltage (UV) or LV ride-through (UVRT/LVRT) also called fault ride-through (FRT) immunity and the third one is the overvoltage (OV) or high voltage ride-through (OVRT/HVRT) immunity.

The ROCOF immunity means that the DER plant shall stay connected with the distribution network if the frequency of the distribution network changes with a specified ROCOF threshold. For a ROCOF equal to or greater than the specified value, the DER plant modules shall have ROCOF immunity. If the ROCOF threshold value is not specified, then 2 Hz/s for the non-synchronous DER plants including the converter-based DERs and 1 Hz/s for the synchronous DER plants shall apply. A sliding measurement window of 500 ms is considered for defining the ROCOF immunity. However, for the control action dependent on frequency measurement shorter than 500 ms measurement periods and for the small isolated distributed networks on islands higher than the specified ROCOF immunity values may be necessary. The ROCOF is used as a method for the detection of loss of mains condition in some European countries [22], [23]. Related to the ROCOF is the previous technical report [29] prepared by the U.S National Renewable Energy Laboratory (NREL) which suggests that the ROCOF method is fairly effective for the synchronous generators and not effective for the converter-based DERs. For the converter-based DERs it is recommended to use the active loss of mains detection methods.

The UVRT immunity means that during times of low voltages or faults (1ph, 2ph, 3ph) causing the low voltages, the DER plants should stay connected to the distribution network and not tripped. The DER plants should behave according to the defined UVRT voltage-time curve. The DER plants shall stay connected if the minimum voltage, phase-to-neutral (ph-N) or phase-to-phase (ph-ph), at the point of connection remains above the voltage-time curve. The default and the most stringent voltage-time curves of the UVRT requirement for the converter-based DER plants as defined in [22] and [23] are reproduced and compared in [34], hence not mentioned more in this section.

The OVRT immunity means that the DER plants shall stay connected to the LV and MV distribution networks if the highest voltage (ph-N or ph-ph) at the point of connection stays below the defined voltage-time curve of the OVRT capability (Fig. 3).

The grid code EN 50549-1-2019 [23] for the connection requirements of the LV distribution networks, excludes the micro-generating DERs with nominal current not exceeding 16 A per phase from OVRT requirement. Like the previous ROCOF and UVRT immunities, the OVRT immunity is also independent of the interface protection settings which always overrule the technical capabilities and decides about the connection or disconnection of the DER plant [22], [23].

C. THE SHORT-CIRCUIT CURRENT REQUIREMENT FOR THE CONVERTER-BASED DER PLANTS

The DER plants are required to have the capability of providing an additional amount of the reactive current for voltage support during the network faults and sudden voltage steps. This requirement is in addition to the default reactive power (Q) requirement of 33% of the design active power (P_D) and the stringent reactive power requirement of 48.4% of P_D when active power is above 20% of P_D during the normal continuous operating voltage and frequency limits [22]. For the DER plants connected to the LV networks, the additional amount of reactive current for voltage support is not required due to the potential interference with the grid

protection equipment [23]. However, if the reactive power during the network faults is required for the type-B DER plants connected to LV networks by the distribution system operator (DSO) then it will be according to the requirements defined in [22] for the DER plants connected to the MV networks which are reviewed in this section. For the voltage below 15% of U_c, no reactive current supply is required even for the DER plants connected to the MV networks.

The additional reactive current (I_Q) has to be supplied by the DER plants when there is sudden voltage change or jump and this requirement applies to voltage steps in both the Pos-Seq and the Neg-Seq components of the fundamental voltage. It means the voltage steps in Pos-Seq voltage will require additional reactive current in Pos-Seq and the voltage steps in Neg-Seq voltage will require additional current in Neg-Seq. The requirement of providing the additional reactive current should in principle be according to Fig. 4 up to the current limitation of the DER plant and at least up to the rated current (I_r). The additional reactive current in the Pos-Seq (ΔI_{Q1}) is set by the gradient k_1 according to equation (1):

$$\Delta I_{Q1} = k_1 \cdot \Delta U_1 \tag{1}$$

ΔU_1 in (1) is the sudden voltage jump or change for the Pos-Seq defined by equation (2):

$$\Delta U_1 = (U_1 - U_{11min})/U_c \tag{2}$$

U_1 in (2) is the actual voltage of the Pos-Seq and U_{11min} is the 1-minute average of the pre-fault voltage of the Pos-Seq or the RMS value. During the normal operation the Pos-Seq is almost identical to the RMS value. The additional reactive current in the Neg-Seq (ΔI_{Q2}) is set by the gradient k_2 according to equation (3):

$$\Delta I_{Q2} = k_2 \cdot \Delta U_2 \tag{3}$$

ΔU_2 in (3) is the sudden voltage jump or change for the Neg-Seq defined by equation (4):

$$\Delta U_2 = (U_2 - U_{2\_1min})/U_c \tag{4}$$

U_2 in (4) is the actual voltage of the Neg-Seq and U_{21min} is the 1-minute average of the pre-fault voltage of the Neg-Seq or zero. During the normal operation the Neg-Seq current is equivalent to zero. The gradients k_1 and k_2 shall be set in the range of 2-6 with a minimum step size of 0.5. The insensitivity range (Fig. 4) defined in terms of the sudden voltage jump can be in the range of ΔU_{1min} = 0-15% for both the Pos-Seq and the Neg-Seq components.

The step response of the additional reactive current should be "no greater than 30 ms" and the settling time of the additional reactive current should be "no greater than 60 ms." The same values of the step response and settling time are also valid for the inception of the fault and the fault clearance or any voltage step in the duration of the fault but apply only to the controlled reactive current. For the provision of an additional reactive current, the Pos-Seq and Neg-Seq components are limited to the same extent such that the asymmetry of the

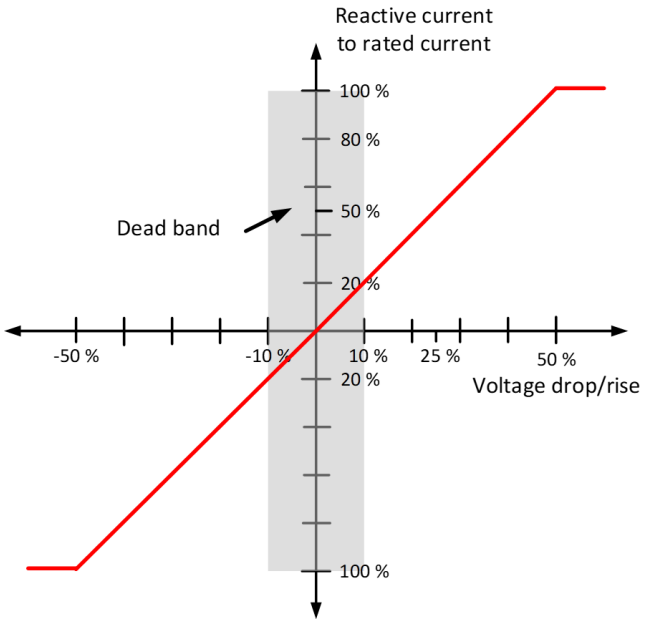

FIGURE 4. Principle of voltage support during faults and voltage steps [22].

support is maintained in case of an asymmetrical fault. Moreover, it is allowed to reduce the active current component to maximize the reactive current, but the reduction should be as small as possible.

The short-circuit current requirement could either be implemented in DER units or in an additional equipment in the DER plant. In this regard, the accuracy of the injected current and the response and settling time is evaluated at the clamps of the DER unit or at the clamps of the additional equipment if applicable due to high dynamic of the requirement. The function of the dynamic reactive current provision can be activated when one or more ph-ph voltages are outside the static voltage range (80-100% of U_c for UV and 100-120% of U_c for OV) or a sudden change in voltage occurs. This function can be deactivated after the re-entry of all ph-ph voltages into static range and after 5 s if the sudden voltage change does not result in any voltage exceeding the static voltage range [22].

D. THE INTERFACE PROTECTION REQUIREMENTS

There are three main objectives of the interface protection mentioned in [22] and [23] which include the prevention of an OV situation due to the power production of the DER plant, the detection of an unintentional island situation and disconnecting the DER plant in this case and providing the assistance to the distribution network in the restoration of the controlled state in case of voltage and frequency deviations beyond the regulated values. It is neither the primary objective of the interface protection to disconnect the DER plant from the distribution network in case of any short-circuit faults internal to the DER plant nor to prevent damages to the DER plant due to short-circuit faults on the distribution network. However, the interface protection may help preventing the

TABLE 2. Voltage and frequency functions for the interface protection [22], [23].

Protection function	Threshold	Operating time
UV[1] [27]	Stage 1: [27 <] (0.2-1) U_n adjustable by steps of 0.01 U_n Stage 2: [27 <<] (0.2-1) U_n adjustable by steps of 0.01 U_n	0.1-100 s adjustable in steps of 0.1 s 0.1-5 s adjustable in steps of 0.05 s
OV[1] [59]	Stage 1: [59 >] (1.0-1.2) U_n adjustable by steps of 0.01 U_n Stage 2: [59 >>] (1.0-1.3) U_n adjustable by steps of 0.01 U_n	0.1-100 s adjustable in steps of 0.1 s 0.1-5 s adjustable in steps of 0.05 s
OV 10 min mean[2]	(1.0-1.15) U_n adjustable by steps of 0.01 U_n	Start time ≤ 3 s not adjustable Time delay setting = 0 ms
UF[3] [81<]	Stage 1: [81 <] (47.0-50.0) Hz adjustable by steps of 0.1 Hz Stage 2: [81 <<] (47.0-50.0) Hz adjustable by steps of 0.1 Hz	0.1-100 s adjustable in steps of 0.1 s 0.1-5 s adjustable in steps of 0.05 s
OF[3] [81>]	Stage 1: [81 >] (50.0-52.0) Hz adjustable by steps of 0.1 Hz Stage 2: [81 >>] (50.0-52.0) Hz adjustable by steps of 0.1 Hz	0.1-100 s adjustable in steps of 0.1 s 0.1-5 s adjustable in steps of 0.05 s
Pos-Seq[4] UV [27D]	(20-100 %) U_n adjustable by steps of 1 % U_n	0.2-100 s adjustable in steps of 0.1 s
Neg-Seq[4] OV [47]	(1-100 %) U_n adjustable by steps of 1 % U_n	0.2-100 s adjustable in steps of 0.1 s
Zero-Seq[4] OV [59N]	(1-100 %) U_n adjustable by steps of 1 % U_n	0.2-100 s adjustable in steps of 0.1 s

[1]Protection shall comply with EN 60255-127 and evaluation of the fundamental or the rms value is allowed. [2]The calculation shall comply with 10 min aggregation of EN 61000-4-30 Class S and calculation of a new 10 min value at least every 3 s is sufficient which is then compared with threshold value. [3]The frequency protection shall function correctly for the input voltage range between 20%U_n and 120%U_n and inhibited for input voltages of less than 20%U_n. [4]Only for DER plants connected to MV networks.

damage to the DER units during the out-of-phase reclosing of the automatic recloser happening after some hundreds of milliseconds (ms). In some countries it is required that some technologies of DER units should have an appropriate immunity level against the consequences of the out-of-phase reclosing.

For the DER plants connected to the LV networks with nominal current above 16 A, the interface protection shall be provided with a dedicated device at the point of connection as defined by the DSO. For the micro-generating DERs with nominal current less than the defined threshold, the interface protection may be integrated into the DER unit. However, the integrated interface protection provision may not be possible either due to the placement of the protection system as near to the point of connection as possible for avoiding the nuisance OV tripping due to the voltage rise within the producer's network or due to the requirement of periodic field tests [23]. For the DER plants connected to the MV networks, the interface protection shall be realized only as a dedicated device and not integrated into the DER unit [22].

The interface protection relay shall act primarily on the interface switch or breaker. However, the DSO may require that the interface relay may act on another switch or breaker with a proper delay setting if the failure of interface switch happens. If the power supply of the interface protection fails, it shall trigger the interface switch without any delay. The DSO may require UPS in case of UVRT capability and delay in protection etc. [22], [23].

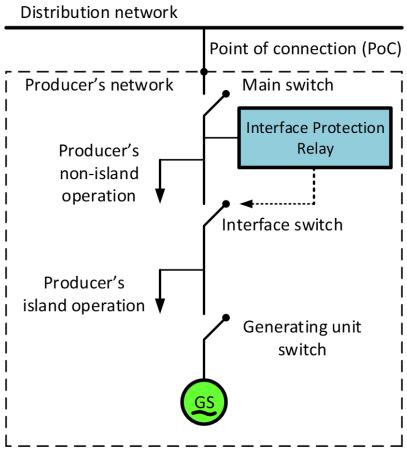

FIGURE 5. Schematic diagram of DER plant with dedicated interface protection relay and view of switches [22].

The different voltage and frequency functions for the interface protection and their settings for the DER plants connected to the LV and MV networks are summarized in Table 2.

The general requirement of the voltage protection is that all ph-ph (preferred) and ph-N voltages need to be evaluated with minimum measurement accuracy of ± 1% of U_n. The general requirement of the frequency protection is that the frequency shall be evaluated on at least one of the voltages (ph-ph or ph-N) with minimum measurement accuracy of ± 0.05 Hz. The reset time of protection is ≤ 50 ms. Fig. 5 shows the schematic diagram of the DER plant connected to the distribution network with different switches and a dedicated interface protection relay.

III. IEEE GRID CODES FOR CONVERTER-BASED DERS

The IEEE 1547-2018 standard [24] provides the technical specifications and requirements for the interconnection of DERs with electric power systems and associated interfaces at primary or secondary radial distribution systems with a nominal system frequency of 60 Hz. The IEEE 1547-2018 standard is closely related to the above reviewed European standards EN 50549-1:2019 [23] and EN 50549-2:2019 [22] for the LV and MV distribution networks with a nominal system frequency of 50 Hz. However, IEEE 1547-2018 divides the technical specifications and performance requirements of DERs into different categories based on low or high penetration levels of DERs. For example, the reactive power capability and voltage regulation requirements are divided into two categories: Category A for the low penetration levels and less frequent overall power output variations of DERs and Category B for the high penetration levels and large overall power output variations of DERs. Similarly, the abnormal operating performance of DERs depending on the stability/reliability of the bulk power system (BPS) is subdivided into three categories: category I, category II and category III operating performance. The category I abnormal operating performance requirements are related to the

essential BPS stability/reliability needs attainable by all DER technologies. The category II requirements deal with all BPS stability/reliability needs required for avoiding tripping for a wider range of disturbances coordinated with existing reliability standards. The category III requirements are recommended for both BPS stability/reliability and distribution system reliability/power quality needs coordinated with existing interconnection requirements for very high penetration level of DERs.

The IEEE 1547-2018 standard is applicable based on the name plate rating of all DER units within the local EPS. It does not define the maximum DER capacity for a specific installation interconnected to a single point of common coupling (PCC) or to a given feeder. The IEEE 1547-2018 standard allows the use of the supplement DER devices to meet the requirements of this standard. The supplement devices are not required to be co-located with the DER units but located within the Local EPS. The reference point of applicability (RPA) of this standard shall be at the PCC for all performance requirements except those otherwise stated in the standard. Only the IEEE 1547-2018 standard requirements for the high penetration levels of DERs (category III requirements) are considered and reviewed in this paper.

A. CONTINUOUS OPERATING FREQUENCY AND VOLTAGE LIMITS

The continuous operating frequency for the DERs connected at primary/MV or secondary/LV system is defined in the range of 58.8-61.2 Hz irrespective of the penetration level of DERs. The continuous operating voltage range for the DERs connected at primary or secondary distribution networks is defined as 0.88-1.10 per unit (p.u.) of nominal system voltage (RMS) at the PCC. The applicable voltages determining the performance of DERs can be measured as an individual ph-N, phase-to-ground (ph-g), or ph-ph combination and time resolution. It all depends on the location of the PCC at MV or LV system and the winding arrangements/configurations of transformers.

B. IMMUNITY AND RESPONSE TO THE ABNORMAL OPERATING CONDITIONS

The abnormal operation conditions include the short-circuit faults, open phase conditions and the unacceptable variations of voltage and frequency values. The stability of the Area EPS, the safety of the maintenance workers and general public and the avoidance of equipment damage are the main factors requiring appropriate DER response during the abnormal conditions. For short-circuit faults, the DERs are required to seize to energize and trip for all faults detected by the protection system of the Area EPS. The parameter adjustment of the DERs or the protection system may be required to ensure proper fault detection and protection coordination. The DERs shall seize to energize and trip all phases to which they are connected within 2.0 s of the open phase condition.

For the DER response to the unacceptable voltage variations, the IEEE 1547-2018 standard defines the mandatory

TABLE 3. DER response to the abnormal voltages (for abnormal operating performance category III) [24].

Shall trip-Category III				
Tripping function	Default settings		Ranges of allowable settings	
	Voltage (p.u. of nominal voltage)	Clearing time (s)	Voltage (p.u. of nominal voltage)	Clearing time (s)
OV2	1.20	0.16	Fixed at 1.20	Fixed at 0.16
OV1	1.10	13	1.10-1.20	1-13
UV1	0.88	21	0.0-0.88	21-50
UV2	0.50	2	0.0-0.50	2-21

TABLE 4. DER response to the abnormal frequencies (for abnormal operating performance category I, II And III) [24].

Tripping function	Default settings		Ranges of allowable settings	
	Frequency (Hz)	Clearing time (s)	Frequency (Hz)	Clearing time (s)
OF2	62.0	0.16	61.8-66.0	0.16-1000
OF1	61.2	300	61.0-66.0	180-1000
UF1	58.5	300	50.0-59.0	180-1000
UF2	56.5	0.16	50.0-57.0	0.16-1000

OV/UV trip settings separately for the category I, II and III abnormal performance categories. The default and the allowable settings of the two-stage OV and UV protection functions (OV1, OV2 and UV1, UV2) of the DERs and the corresponding clearing/tripping times for the performance category III are given in Table 3. For the OV and UV trip functions clearing time ranges and for the OV trip functions voltage ranges, the lower value is a limiting requirement, and the upper value is a minimum requirement. For the UV trip functions voltage ranges, the upper value is a limiting requirement, and the lower value is a minimum requirement. The limiting requirements values in Table 3 cannot be increased or decreased but the minimum requirements values can be increased and decreased, as necessary.

For the DER response to the unacceptable frequency variations, the IEEE 1547-2018 standard defines the mandatory OF/UF trip settings, the same settings for the abnormal performance categories I, II and III. The default and the allowable settings of the two-stage OF and UF protection functions (OF1, OF2 and UF1, UF2) of the DERs and the corresponding clearing/tripping times are given in Table 4.

For the OF and UF trip functions clearing time ranges and for the OF trip functions frequency ranges, the lower value is a limiting requirement, and the upper value is a minimum requirement. For the UF trip functions frequency ranges, the upper value is a limiting requirement, and the lower value is a minimum requirement. The limiting requirements values in Table 4 cannot be increased or decreased but the minimum requirements values can be increased and decreased, as necessary.

The settings outside the ranges of allowable settings in Table 3 and Table 4 shall only be allowed if necessary for the DER equipment protection, but these should not

TABLE 5. Voltage ride-through[1] requirements for DERs of abnormal operating performance category III [24].

Voltage range (p.u.)	Operating mode/response	Min ride-through time (s) (design criteria)	Max response time (s) (design criteria)
V>1.20	Cease to Energize	N/A	0.16
1.10 < V ≤ 1.20	Momentary Cessation	12	0.083
0.88 ≤ V ≤ 1.10	Continuous operation	Infinite	N/A
0.70 ≤ V < 0.88	Mandatory Operation	20	N/A
0.50 ≤ V < 0.70	Mandatory Operation	10	N/A
V < 0.50	Momentary Cessation	1	0.083

[1]HVRT in blue and LVRT in red color.

TABLE 6. Frequency ride-through* requirements for DERs of abnormal operating performance category I, II And III [24].

Frequency range (Hz)	Operating mode	Min time (s) (design criteria)
f > 62.0	No ride-through requirements apply to this range	
61.2 < f ≤ 61.8	Mandatory operation	299
58.8 ≤ f ≤ 61.2	Continuous operation	Infinite
57.0 ≤ f < 58.8	Mandatory operation	299
f < 57.0	No ride-through requirements apply to this range	

*HFRT in blue and LFRT in red color.

conflict with the disturbance voltage and frequency ride-through requirements. The voltage ride-through requirements including LVRT below the minimum continuous operating voltage and HVRT above the maximum continuous operating voltage for DERs of abnormal operating performance category III are given in Table 5. The DERs shall be designed to provide the voltage disturbance ride-through capability without exceeding DER capabilities.

Additionally, the DERs have to ride-through during multiple consecutive voltage disturbances in the ride-through operating region. The unsuccessful reclosing during the short-circuit faults, various faults during storms and dynamic voltage swings may be the causes of these consecutive temporary voltage disturbances. For the DERs of category-III, the maximum number of consecutive voltage ride-through disturbance sets is 3 with 5 s minimum time between successive disturbance sets. The time window for the new count of the disturbance sets is 20 minutes for the DERs of category-III. However, the DERs in general should ride-through as many voltage-disturbance sets as they are capable.

The frequency ride-through requirements including low-frequency ride-through (LFRT) below the minimum continuous operating frequency and the high-frequency ride-through (HFRT) above the maximum continuous operating frequency for DERs of abnormal operating performance categories I, II and III are given in Table 6. For the frequency of less than 57.0 Hz and above the 62.0 Hz, no ride-through requirements are applied. The DERs of category III shall have the capability of mandatory operation with frequency-droop (frequency-power) during the LFRT and HFRT. The IEEE 1547-2018 standard defines the ROCOF ride-through requirement for DERs of category III as 3.0 Hz/s. The ROCOF shall be the average rate of change of frequency over an averaging window of at least 0.1 s.

For both the voltage and frequency ride-through requirements, any tripping of DER or other failure to provide the specified ride-through capability, due to the DER self-protection as a direct or indirect result of voltage disturbance within the ride-through region shall constitute non-compliance with the IEEE 1547-2018 standard.

The exceptional conditions during which ride-through requirements shall not apply and the DER may cease to energize and trip without limitations include: 1) The net active power exported across the PCC into the Area EPS is maintained at a value less than the 10% of the aggregate rating of the DER connected to the Local EPS prior to any voltage disturbance. In this case, the Local EPS may intentionally disconnect from the Area EPS and form a Local EPS island, or 2) An active power demand of the Local EPS load equal to or greater than 90% of the pre-disturbance aggregate DER active power output is shed within 0.1 s of when the DER ceases to energize the Area EPS and trips.

The IEEE 1547-2018 also defines the voltage phase angle changes ride-through requirements for multi-phase DERs and single-phase DERs. According to these requirements, multi-phase DER shall ride-through for Pos-Seq phase angle changes within a sub-cycle-to-cycle period of the applicable voltage of less than or equal to 20 electrical degrees. Additionally, multi-phase DER shall remain in operation for change in the phase angle of individual phases less than 60 electrical degrees, provided that the Pos-Seq angle change does not exceeds the required criteria. Single-phase DER shall remain in operation for phase angle changes within a sub-cycle-to-cycle period of the applicable voltage of less than or equal to 60 electrical degrees [24].

C. ENTER SERVICE AND SYNCHRONIZATION PARAMETERS

The DERs shall not energize the area EPS until the applicable voltage and system frequency are within the ranges specified in Table 7 and permit service is set to ''Enabled''. The specified ranges in Table 7 do not mandate any DER to enter service and stay in operation but only permit to enter service.

The DER shall parallel with the area EPS without causing step changes in the RMS voltage at the PCC exceeding 3% of the nominal voltage at MV and 5% of the nominal voltage at LV point of connection.

The synchronization parameter limits for a synchronous connection to an EPS (or an energized Local EPS to an Area EPS) are defined in Table 8. These synchronization limits may be waived by the Area EPS operator if paralleling does not exceed the limitation of voltage fluctuations of 3-5% of the nominal voltage mentioned above.

D. THE DYNAMIC VOLTAGE SUPPORT DURING THE SHORT-CIRCUIT FAULTS

According to IEEE 1547-2018 standard, any DER may have the capability of dynamic voltage support during the LVRT

TABLE 7. Enter service criteria for DERs of category I, II, and III [24].

Enter service criteria		Default settings	Ranges of allowable settings
Permit service		Enabled	Enabled/Disabled
Applicable voltage within range	Minimum value	≥ 0.917 p.u.	0.88 p.u. to 0.95 p.u.
	Maximum value	≤ 1.05 p.u.	1.05 p.u. to 1.06 p.u.
Frequency within range	Minimum value	≥ 59.5 Hz	59.0 Hz to 59.9 Hz
	Maximum value	≤ 60.1 Hz	60.1 Hz to 61.0 Hz

TABLE 8. Synchronization parameter limits for synchronous connection to EPS [24].

Aggregate rating of DER units (kVA)	Frequency difference Δf (Hz)	Voltage difference ΔV (%)	Phase angle difference $\Delta\Phi$ (°)
0–500	0.3	10	20
> 500–1 500	0.2	5	15
> 1 500	0.1	3	10

and HVRT. The dynamic voltage support means rapid reactive power exchanges during voltage excursions to provide better voltage stability in distribution system during transient events. However, the dynamic voltage support shall not cause the DER to seize to energize in situations where the DER would not cease to energize without the dynamic voltage support. The dynamic voltage support may be utilized during the mandatory or permissive operation. The Area EPS operator may consider the impact of the dynamic voltage support from DER on the Area EPS protection. It is recommended that the dynamic voltage support implementation should have the capability of preventing the overvoltage in any phases of the applicable voltage when providing the dynamic voltage support for any types of faults (balanced or unbalanced).

E. ISLANDING

The IEEE 1547-2018 standard defines the islanding condition in distribution systems as: "Island is a condition in which a portion of an Area EPS is energized solely by one or more Local EPSs through the associated PCCs while that portion of the Area EPS is electrically separated from the rest of the Area EPS on all phases to which the DER is connected. When an island exists, the DER energizing the island may be said to be "islanding" [24].

Two types of islands are defined in IEEE 1547-2018 standard: (1) An unintentional island and (2) An intentional island. An *intentional island* is a planned island whereas an *unintentional island* is an unplanned island. An intentional island is further defined as: "A planned electrical island that is capable of being energized by one or more Local EPSs. These (1) have DERs and loads, (2) have the ability to disconnect from and to parallel with the Area EPS, (3) include one or more Local EPS(s), and (4) are intentionally planned" [24].

The intentional island may be an "intentional Area EPS island" or an "intentional Local EPS island", the latter is also called facility island. An intentional Area EPS island is

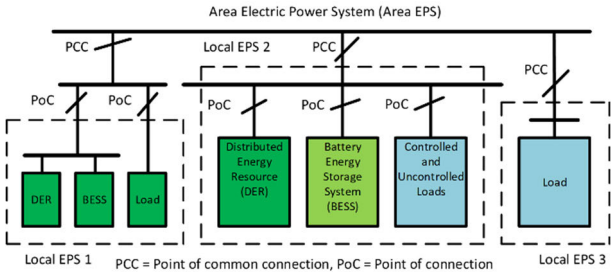

FIGURE 6. An area EPS with different local EPS categories.

an intentional island that includes portions of the Area EPS, and an intentional Local EPS island is an intentional island that is totally within the bounds of a Local EPS. Here, the Local EPS means an EPS that is contained entirely within a single premises or group of premises. The Area EPS is usually comprised of different Local EPSs that has primary access to public rights-of-way and is subject to the regulatory oversight (see Fig. 6).

1) DER CATEGORIES FOR OPERATION IN AN INTENTIONAL AREA EPS ISLAND

The IEEE 1547-2018 standard defines four categories of the participant DERs for operation in an intentional Area EPS island: *Uncategorized DERs* (not designed for intentional island), *intentional island-capable DERs*, *black start-capable DERs* and *isochronous-capable DERs* (can regulate voltage and frequency independently). These categories shall be stated by the DER operator, but the utilization shall be by mutual agreement between the DER operator and the operator of the intentional Area EPS island.

2) EXEMPTIONS FOR THE EMERGENCY SYSTEMS AND STANDBY DERS

The DER systems designated as emergency or critical operations power systems providing backup power for the hospitals, fire stations or other emergency facilities are exempt from the voltage and frequency disturbance ride-through requirements, intentional islanding requirements and interoperability, information exchange, information models and protocol requirements. The standby DERs used for infrequent testing purpose or used during load transfer to or from the Area EPS in a period of less than 300 s are also exempt from the above-mentioned requirements.

F. MICROGRID CONTROLLERS

The IEEE standard 1547.4-2011 [26] mentions different load categories and their requirements and sensitivities for the islanded mode of operation. The inrush current problems during motor starting and transformer energization need to be solved using soft-starter and series reactance respectively to avoid nuisance tripping of overcurrent (OC)/overload protection devices during cold load pickup and transition periods. An acceptable degree of load balance should be achieved by load monitoring on each phase and necessary corrective

actions should be taken like load reconfiguration and load shedding. The maximum active and reactive power requirements of the loads in the islanded mode should be known in advance and sources of active and reactive power should be available when required.

The area EPS grounding schemes/configurations (ungrounded, effectively grounded or impedance grounded) should be maintained even in the islanded mode. To do this the ground sources may require switching operations. An effectively grounded distribution system should maintain an adequate ground source at all times. Connecting multiple ground sources such as ground source transformer banks on the feeder may desensitize upstream protection devices by acting as a sink of unbalanced ground-fault currents and creating protection coordination problems during ground faults. This should be considered for the coordination of protection schemes [26].

A multifunctional communication-based microgrid management system (MMS) or microgrid control system (MCS) can be used to perform different management and control functions mentioned above for the proper operation of the microgrid in different modes of operation. The detailed functions of MMS are discussed in [30]. The physical implementation of control strategies consisting of software, hardware or a combination of software and hardware can be done in a centralized, decentralized/distributed or hybrid centralized and decentralized manner. A suitable combination of communication protocols like IEC 61850, DNP3, Modbus, IEC 60870-5 etc. can be used for this purpose. An autonomous communication-less control (droop-control) defined in [26] may be used for the basic and local control capabilities.

The IEEE standard 2030.7-2017 [27] defines the technical specifications and requirements of a generic microgrid controller or more specifically microgrid control system. The standard defines the core functions and their interactions allowing modularity and interoperability in physical implementations.

Two core functions of the MCS (Level-2 control) which supervise the lower-level functions (Level-1 control) are specified and defined in IEEE 2030.7-2017 [27]: The dispatch function and the transition function.

The dispatch function generates/calculates the dispatch order and sends it to the microgrid components as often as necessary based on the received or estimated state of microgrid and its components. It receives the dispatch mode information including the unplanned islanding (T1), planned islanding (T2), reconnect (T3), black start (T4), steady state grid-connected (SS1) and steady state islanded (SS2) modes from the transition function. The dispatch function operates on a longer timeframe compared with the transition function typically in the range of minutes.

The transition function provides the logic to switch the dispatch function between one of the relevant dispatch modes including the four transition modes (T1 to T4) and two steady state modes, SS1 and SS2. The transition function operates on a shorter timeframe compared with the dispatch function typically in the range of milliseconds.

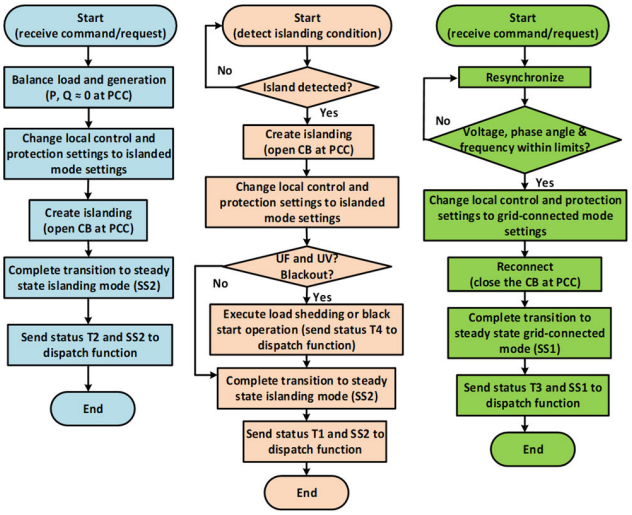

FIGURE 7. Flow charts for T2, T1 and T3 transition modes.

The process and steps of the transition function logic required for switching the dispatch function to the planned islanding mode (T2), the unplanned islanding mode (T1) and the reconnection to the main grid mode (T3) are mentioned in Fig. 7 with blue, red and green color flow charts, respectively.

IV. EVALUATION OF THE SELECTED GRID CODES FOR THE CONVERTER-BASED DERS

This section presents the evaluation of the dynamic reactive power injection capability of the converter-based DERs according to EN 50549-2-2019 grid code requirements from the perspective of AC microgrid protection in the grid-connected and the islanded modes. The standardized settings of the interface protection functions are evaluated during the unbalanced faults.

A. THE DYNAMIC REACTIVE POWER INJECTION DURING THE SHORT-CIRCUIT FAULTS

In this section the dynamic reactive power capability of a generic converter-based DER model connected to MV distribution network during unbalanced faults is evaluated using a MATLAB/Simulink model of AC microgrid (Fig. 8). The generic DER model is capable of LVRT and provides 1.2 p.u. of short-circuit current during the fault or when the voltage of any phase falls below 0.8 p.u. of the nominal voltage. The DER is also capable of operating as the grid-forming source with independent voltage and frequency control capability in the islanded mode using phase-locked loop PLL-2 (Fig. 9). The settings of the interface protection functions used in this study are done according the European standard EN 50549-2:2019 [22] and according to the ranges defined for the second-stages of the UV/OV and UF/OF protection functions (Table 2).

Two types of controls of the grid-side converter of DERs are discussed in [31]: The coupled sequence control (CSC)

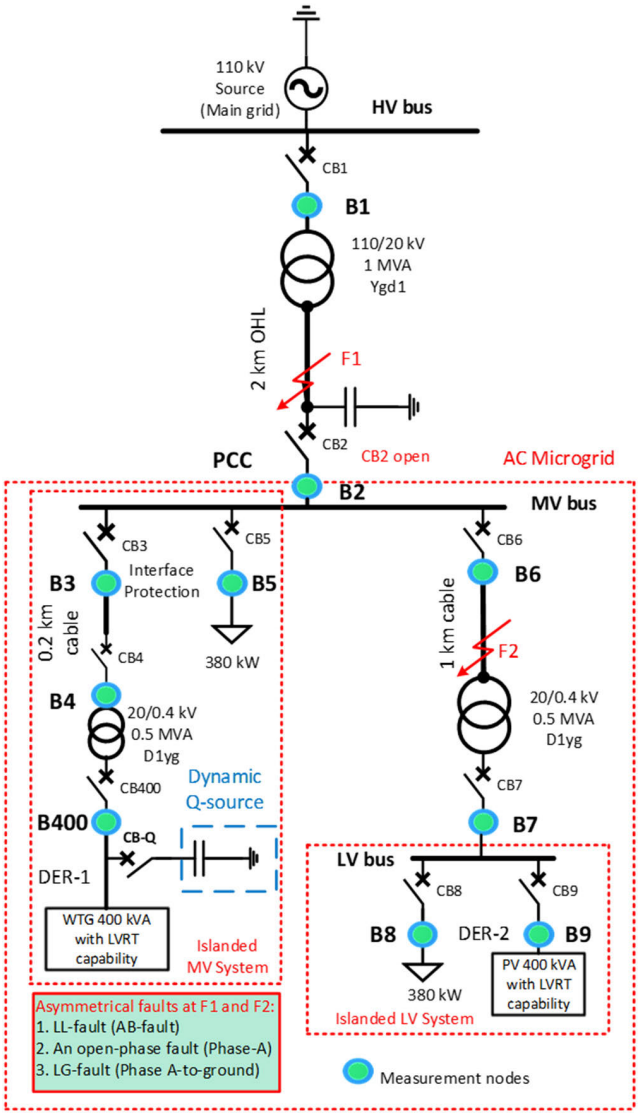

FIGURE 8. Simulink model of AC Microgrid used for the grid code evaluation of converter-based DERs.

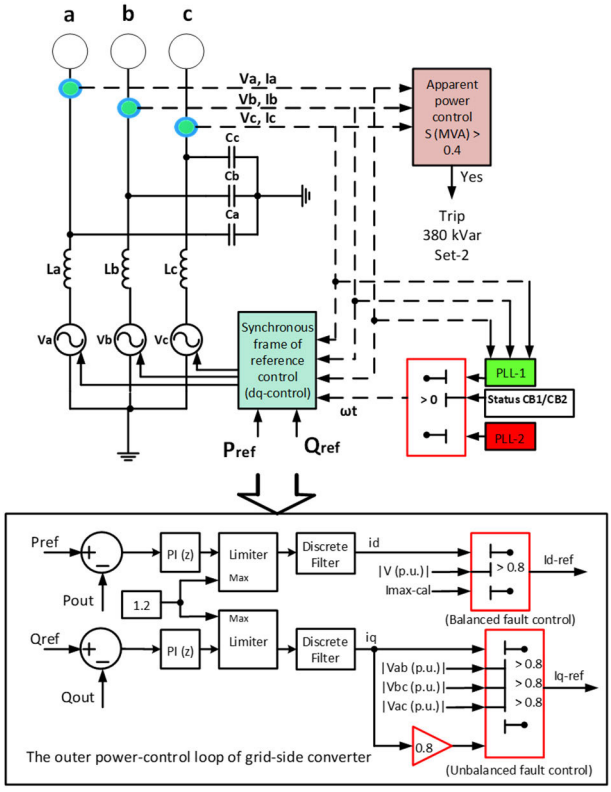

FIGURE 9. The synchronous frame of reference control (dq-control) of a generic grid-forming DER with description of the outer power-control loop during faults. The phase-locked loop PLL-1 is for the grid-connected mode and PLL-2 for the islanded mode.

and the decoupled sequence control (DSC). The CSC control method gives priority to the Pos-Seq current and provides very less amount of the Neg-Seq current. With the DSC control method, the Pos-Seq and Neg-Seq currents can be controlled independently, and enough magnitude of Neg-Seq current injection can be obtained. However, the DSC control also gives priority to the Pos-Seq current, and the remaining capacity of the converter is utilized for providing the Neg-Seq current. The output current of the most grid-side converters or inverters is primarily Pos-Seq with a small Neg-Seq current. Majority of the inverters do not produce Zero-Seq current [25]. In this paper, the dq-control in the synchronous frame of reference is used for the DERs which is a CSC control providing a limited amount of Neg-Seq current during the faults. Therefore, an additional Q-source (a thyristor-switched capacitor or equivalent) is used as an enabler to meet the grid code requirements during the faults.

An extra source of reactive power (dynamic Q-source in Fig. 8) is connected at LV terminals of the DER-1 to enable it to inject the reactive current during an external unbalanced short-circuit fault. This location of an extra Q-source connection is behind the generating unit switch in Fig. 5.

The dynamic Q-source consist of two sets of thyristor-switched capacitors of total 760 kVar capacity with each having 380 kVar capacity. The apparent power of the DER-1 is monitored during the reactive power injection so that its extent should be controlled within the rated MVA capacity of the DER-1. Normally, both sets of the dynamic Q-source are activated after the condition of reactive power injection is reached during the faults. However, if the apparent power limit of DER-1 is violated then one set of the dynamic Q-source is switched off instantly to avoid any overloading or overvoltage at the DER-1 terminals. The outer power-control loop of DER-1 and DER-2 by default reduces the q-axis current to 0.8 p.u. of the pre-fault value if the UV condition of 0.8 p.u. or less is reached during the faults (Fig. 9). The applied control of DERs is not enough to meet the grid code requirement of Neg-Seq current during faults. Hence, an additional Q-source is required to meet the stringent grid code requirements. The current during short-circuit faults is assumed as predominantly reactive current.

Table 9 shows the time delay settings of different protection functions of protection devices at different locations.

TABLE 9. The time delay settings of different protection relays and functions.

Functions	Coordinated time-delay (s)							
	CB1	CB2	CB3	CB6	CB5	CB7	CB8	CB9
OC^1	0.8	0.6	0.9	0.4	0.9	0.2	0.02	0.02
OC^{2*}	0.8	0.6	0.9	0.4	0.9	0.2	0.02	0.4
OC^0	0.8	0.6	0.9	0.4	0.9	0.2	0.02	0.4
OV^2	3.0	2.5	4.0	2.0	4.0	1.5	1.0	4.0
OV^0	3.0	2.5	4.0	2.0	4.0	1.5	1.0	4.0
UV^1/OV^1	3.5	3.0	5.0	2.5	5.0	2.0	1.5	5.0

*The ratio of I_2/I_1 during the fault is used as the main tripping criteria, the magnitude of I_2 during the fault is used as the restraining criteria, it means the tripping is allowed only if $I_2 > 0.35$ p.u. Only the coordination of the enabled protection relays in green columns is evaluated in this study. OC^1 = 51P, OC^2 = 51Q, OC^0 = 51G, $OC^{2*} = I_2/I_1$.

TABLE 10. The potential tripping thresholds of different protection functions.

Protection functions	Tripping thresholds**	
	Grid-connected mode	Islanded mode
OC^1	2.25 p.u.	1.2 p.u.
OC^{2*}	1.3	1.0-1.3
OC^0	0.45-0.5 p.u.	0.45-0.5 p.u.
OV^2	0.5 p.u.	0.5 p.u.
OV^0	0.5 p.u.	0.5 p.u.
UV^1/OV^1	0.85/1.2 p.u.	0.85/1.2 p.u.

** The maximum inrush current magnitude and the maximum load unbalance need to be evaluated for the final reliable thresholds of these protection functions. The settings of OC functions in the islanded mode are in general more sensitive than the grid-connected mode settings.

Table 10 shows the potential tripping threshold settings of different protection functions for the grid-connected and islanded modes. In addition to the Pos-Seq OC function (OC^1), a protection function based on the ratio of the Neg-Seq current (I_2) to the Pos-Seq current (I_1) or I_2/I_1 protection function (OC^{2*}) is also provided for the detection of unbalanced faults. The default tripping threshold setting of I_2/I_1 protection function is 1.3, however, it could be set well below this threshold depending on the magnitude of I_2 during different unbalanced faults. The idea behind selecting the tripping threshold of 1.3 is to trigger I_2/I_1 protection function only after the activation of the Q-injection function. The magnitude of I_2 during the fault is used as a restraining criterion, it means the tripping of I_2/I_1 protection function is only allowed if $I_2 > 0.35$-0.5 p.u.

At each relay location in Table 9, the symmetrical components of current or OC functions OC^1, OC^{2*} and OC^0 are used as the primary protections to detect the balanced and unbalanced short-circuit faults including the ground faults. The obvious symmetrical components of voltage during the faults like OV^2 and OV^0 functions are used as the first local backup protections at each relay location. The normal Pos-Seq UV^1 and OV^1 functions are used as the second local backup to all the symmetrical component-based OC and OV protection functions. All the local protection functions at each location are also coordinated with the corresponding protection functions at remote locations to cover the local malfunction of the protection relays for the maximum protection coverage.

1) UNBALANCED FAULTS IN THE GRID-CONNECTED MODE

a: CASE-1: LL-FAULT F1

The LL-fault F1 between phase A and phase B (AB-fault) with a fault resistance of 0.001 Ohm is applied at simulation time of 2 s and for a duration of 2 s from 2 s to 4 s at the end of 2 km line near the PCC of AC microgrid (Fig. 8) in the grid-connected mode. As mentioned previously, the LL-fault is an asymmetrical or unbalanced short-circuit fault which not only increases the short-circuit current in the Pos-Seq but also in the Neg-Seq component. Fig. 10 shows the instantaneous and symmetrical components of fault current observed at bus B1.

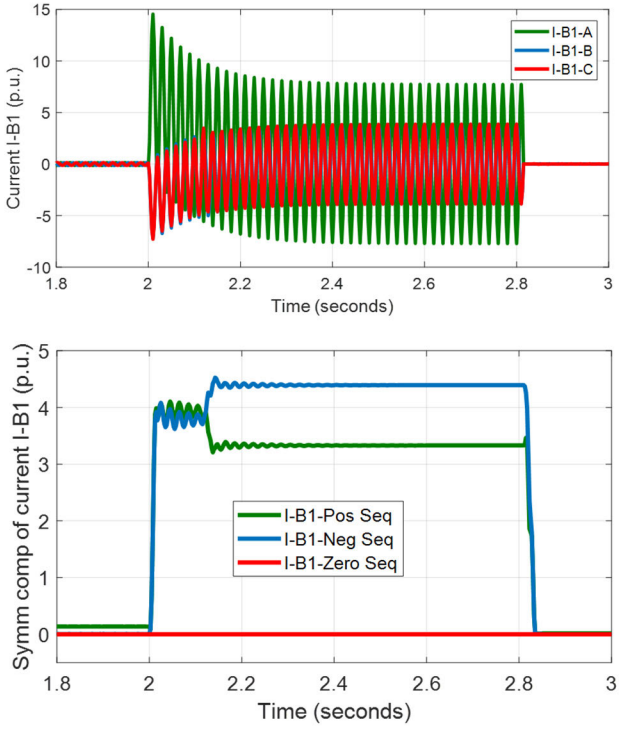

FIGURE 10. The instantaneous line current (top) and the derived symmetrical components of current (bottom) in p.u. observed at bus B1 during the LL-fault F1.

Fig. 10 (bottom) shows that the magnitudes of both the Pos-Seq and Neg-Seq components of current at B1 are increasing equally after the LL-fault F1 is triggered at 2s. However, after the injection of reactive current at 2.1 s, the magnitude of Neg-Seq current (I_2) is increased, whereas the magnitude of Pos-Seq current (I_1) is decreased at bus B1. This causes the ratio I_2/I_1 to increase from about 1.0 right after the fault to above 1.3 after the reactive power support (Fig. 11). This increased ratio of I_2/I_1 can be used as a means of detecting LL-faults downstream of bus B1. The I_2/I_1 protection function can be triggered, for example, when I_2/I_1 ratio becomes 1.3 to open CB1 after an intentional time delay of 0.8 s and to transfer trip CB2 after an additional delay of 0.02 s. However, in this study the Pos-Seq OC (OC^1) function is able to detect AB-fault F1 at 2.8 s due to enough magnitude of I_1 available from the main grid.

It should be noted that extra Q-source is activated within 0.1 s in this study after the fundamental voltage magnitude of any phase at the PCC (measured at interface protection B3) is decreased below the 0.8 p.u. according to EN 50549-2-2019 [22]. The Q-source activation function

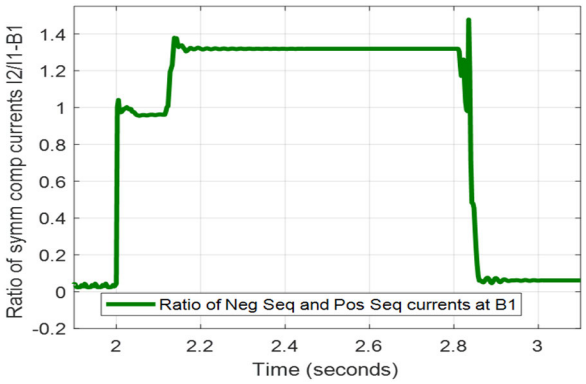

FIGURE 11. I_2/I_1 ratio at B1 after the AB-fault F1 (2-2.1 s) and after the 670 kVar Q-injection (2.1-2.8 s) during the LL-fault F1 in grid-connected mode.

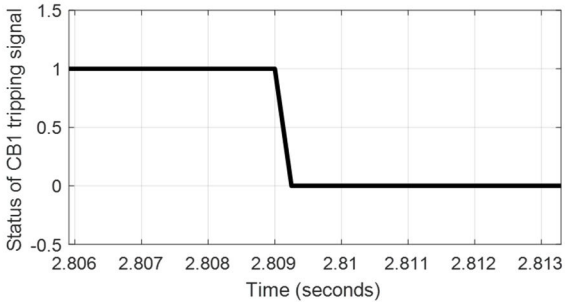

FIGURE 12. Tripping signal of the OC^1 function to trip CB1 after the LL-fault F1 in grid-connected mode.

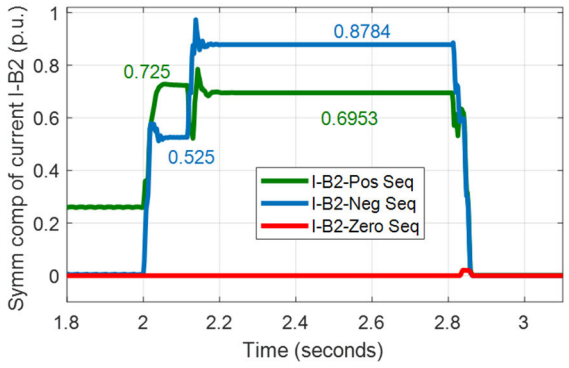

FIGURE 13. The derived symmetrical components of rms current in p.u. observed at bus B2 during the LL-fault F1 in grid-connected mode.

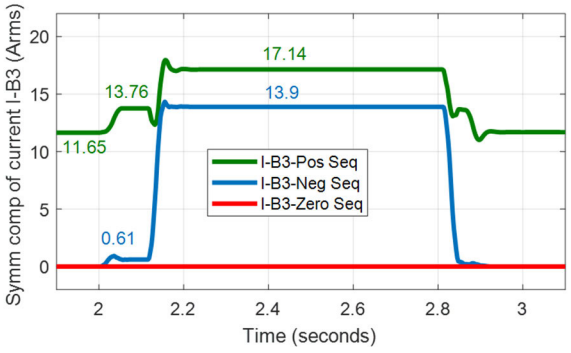

FIGURE 14. Fault current contribution from the DER-1 at PCC/MV side: The derived symmetrical components of rms current (A) observed at bus B3 during the LL-fault F1 in grid-connected mode.

also checks the connection status of CB2 and CB3 and the additional Q-source is activated only if both CB2 and CB3 are closed in the grid-connected mode. Although, the set tripping time delay of both the OC^1 and I_2/I_1 protection functions is same according to Table 9, but used switching delay of 0.1 s, that can be 40 ms in actual case, for the activation of Q-source causes OC^1 function to trip first after the threshold value of I_1 is reached at 2.8 s (Fig. 12). In this case, I_2/I_1 function will provide local backup if OC^1 function fails to detect the LL-fault due to any reason like low magnitude of I_1.

Fig 13 shows the symmetrical components of current observed at bus B2. The measurements at bus B2 are used for the protection functions acting on CB2. It should be noted that it is bus B2 which indicates the active and reactive power flow to and from the main grid or microgrid. In this case, the MV and LV loads are fully supplied by the local DERs of AC microgrid. Therefore, a low magnitude of load current flows at bus B2 before the fault. After the fault is applied, the fault current contribution comes from both the DER-1 connected at MV-bus B3 (Fig. 14) and DER-2 connected at LV-bus B9 (Fig. 16). The combined Pos-Seq fault current contribution from the DERs observed at B2 is less than the maximum normal Pos-Seq load current (about 22 A-rms) at B2 without the DERs. Therefore, the Pos-Seq overload or OC^1 function at B2 will not trip for the grid-side LL-fault F1. Only the Neg-Seq current at B2 can be used to detect this fault condition. But as the fault happens behind the relay of CB2 so some directional discrimination is required at CB2 to prevent the reverse fault tripping by the Neg-Seq OC (OC^{2*}) or I_2/I_1 protection function at B2.

If the Neg-Seq directional discrimination is not used at B2, then there is a high chance that the OC^{2*} or I_2/I_1 protection function may trip CB2 before the CB1. This is true because the time-coordination of the OC^{2*} is done just like the OC^1 starting from the LV load at CB8 towards the main grid or HV/MV transformer substation (Table 9). In this fault case, the set tripping threshold of 1.3 for the OC^{2*} or I_2/I_1 protection at B2 prevents the reverse fault tripping of CB2 before the tripping of CB1 by default without the use of 67Q directional element. Since, the DER-2 provides a low magnitude of I_2, therefore I_2/I_1 ratio of lower than 1.3 is achieved at B2.

The directional discrimination may also be required at CB6 and CB7 locations to prevent the reverse fault tripping by the Neg-Seq OC functions (OC^{2*} or I_2/I_1) at these locations during a LL-fault between CB6 and CB7 in the grid-connected mode. Particularly, if the DER-2 connected at LV-bus B9 is also required to provide the Neg-Seq current up to same extent of DER-1 during the faults. The directional element design is considered and evaluated for the selected cases in the next subsection.

Fig. 14 shows the symmetrical components of current observed at bus B3. The bus B3 is the PCC bus of the

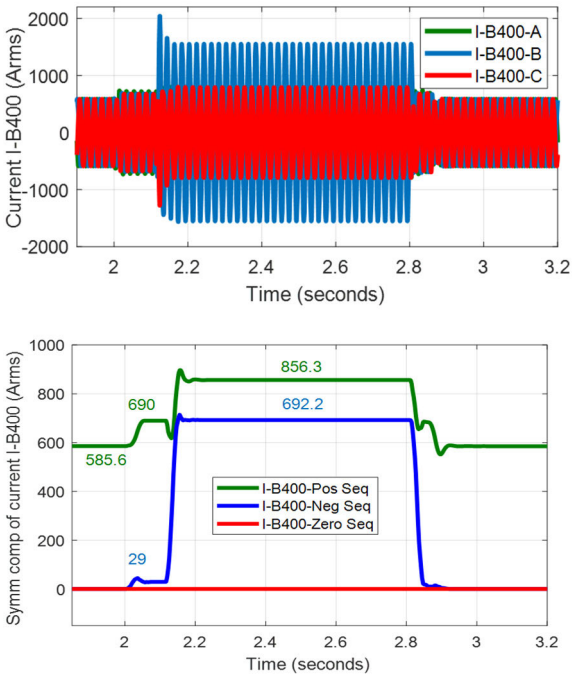

FIGURE 15. Fault current contribution from the DER-1 at LV side: The rms instantaneous line currents (top) and the derived symmetrical components of rms current (bottom) observed at bus B400 during the LL-fault F1 in grid-connected mode.

DER-1 where the interface protection is also installed with the required functions as per EN 50549-2-2019 grid code.

Fig. 14 shows that the magnitude of Neg-Seq current at B3 after the fault is quite lower compared with the Pos-Seq current during the fault from the simulation time of 2 s to 2.1 s. However, after the activation of additional Q-source at 2.1 s the magnitude of the Neg-Seq current is significantly increased to the level of Pos-Seq current after the fault. The activation of additional Q-source during the fault also increases the magnitude of the Pos-Seq current at B3 from 1.18 p.u. to 1.47 p.u. The variation of the Pos-Seq and Neg-Seq current up to the same extent is also be observed at LV side of DER-1 (Fig. 15).

A proper time-coordination and direction discrimination of OC^{2*} functions of CB3, CB2 and CB1 may be required to prevent the earlier tripping of the CB3 for the upstream grid-side faults if sensitive OC^{2*} tripping thresholds ($\leq$ 0.5 p.u.) are used. However, a higher tripping threshold of 1.3 of OC^{2*} or I_2/I_1 function and maximum time-delay at CB3 maintains the proper coordination. It can be observed from Fig. 15 (bottom) that the Q-source at DER-1 is activated with a step response of 25 ms and settling time of 50 ms which meet the EN 50549-2-2019 grid code requirements mentioned earlier in Section II part C.

Fig. 16 shows that the grid-side LL-fault F1 causes some current unbalance at DER-2, which causes some magnitude of the Neg-Seq current injected by the DER-2 during this fault. However, the magnitude of the Neg-Seq current injected by DER-2 is very much lower than the Pos-Seq load current ($\leq$ 6 % of the load current).

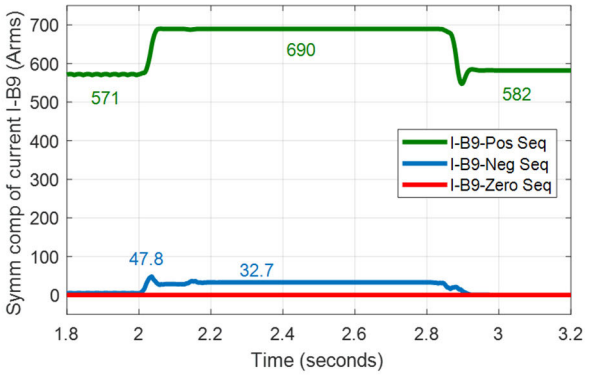

FIGURE 16. Fault current contribution from the DER-2: The derived symmetrical components of rms current (A) observed at bus B9 during the LL-fault F1 in the grid-connected mode.

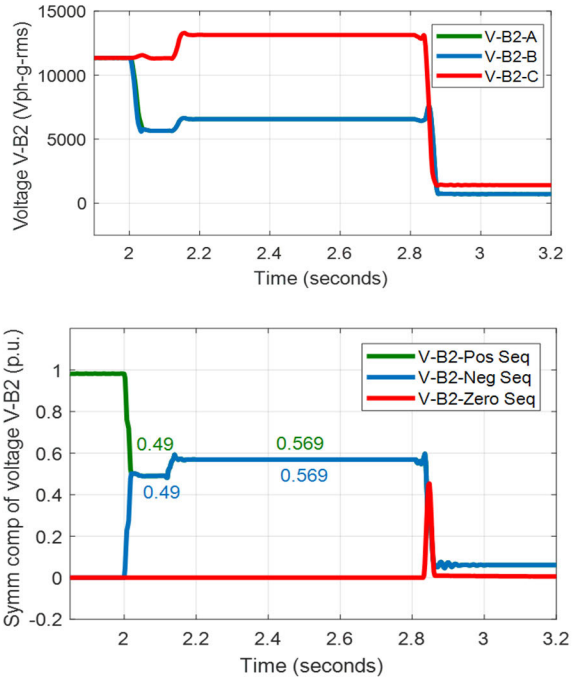

FIGURE 17. The rms phase-to-ground voltage (V) observed at bus B2 (top) and derived symmetrical components of voltage (bottom) in p.u. at bus B2 during the LL-fault F1 in grid-connected mode.

From Fig. 17 (V-B2) to Fig. 22 (V-B9) it can be seen that after the activation of Q-source during the grid-side LL-fault F1 the voltages at all buses particularly the bus B3 of PCC, bus B5 of MV-load and bus B8 of LV-load are improved. It means Q-injection during the fault provides voltage stability particularly for the single-phase loads. The only exceptions are the phase-A voltages of LV bus B400 of DER-1 (Fig. 19), LV-load bus B8 (Fig. 21) and LV bus B9 of DER-2 (Fig. 22). At these buses, the voltage of phase-A during the LL-fault F1 remains the same ($<$ 50 V) even after the Q-injection.

From Fig. 18 it can be observed that the magnitude of Neg-Seq and Pos-Seq voltage at bus B3 increases from 0.49 p.u. to about 0.57 p.u. after the Q-injection. It means according to settings of interface protection at CB3 (Table 9),

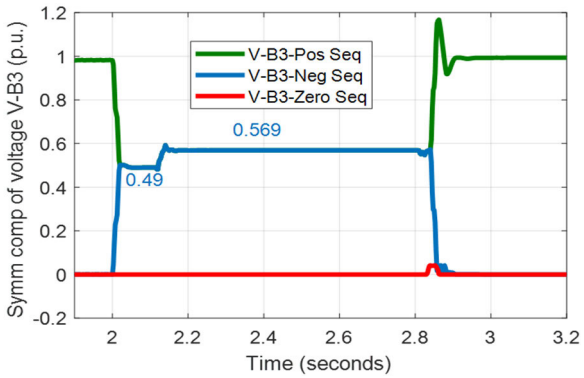

FIGURE 18. The instantaneous voltage (top) and the derived symmetrical components of voltage (bottom) in p.u. observed at bus B3 during the LL-fault F1 in grid-connected mode.

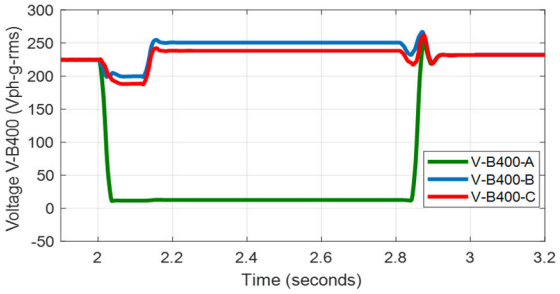

FIGURE 19. The rms phase-to-ground voltage (V) at the LV-side of DER-1 observed at bus B400 during the LL-fault F1 in grid-connected mode.

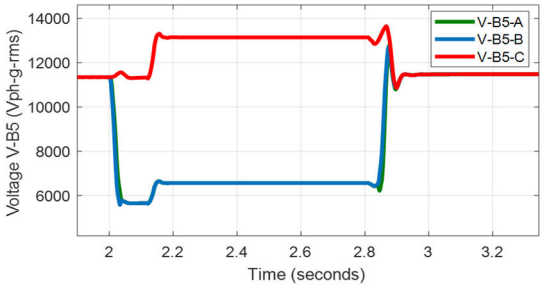

FIGURE 20. The rms phase-to-ground voltage (V) at the MV-load observed at bus B5 during the LL-fault F1 in grid-connected mode.

the Neg-Seq OV function (OV^2) will trip CB3 within 4.0 s after the Q-injection if other protection functions do not clear the grid-side LL-fault F1. From the results it can be observed that after the fault clearance at 2.82 s, the additional reactive power is deactivated, hence no Neg-Seq current (Fig. 15) or Neg-Seq voltage (Fig. 18) appear after the smooth transition of AC microgrid to the islanded mode. Fig. 23 shows the frequency of MV-load and LV-load before, during and after the LL-fault F1. Since the three-phase loads are closely balanced, therefore the frequency remains inside the continuous operating range.

b: GRID CODE COMPLIANCE CHECK FOR CASE-1:

The required minimum and maximum magnitude of Pos-Seq reactive current according to (1) and (2) based on voltage

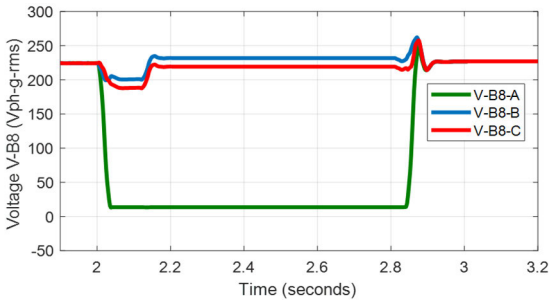

FIGURE 21. The rms phase-to-ground voltage (V) at the LV-load observed at bus B8 during the LL-fault F1 in grid-connected mode.

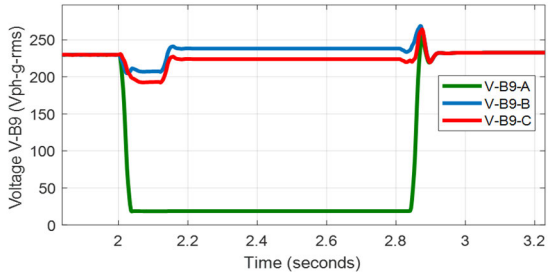

FIGURE 22. The rms phase-to-ground voltage (V) at the DER-2 observed at bus B9 during the LL-fault F1 in grid-connected mode.

measurement at the interface protection bus B3 (Fig. 18) will be as follows:

$$\Delta U_1 = (0.49 - 1)/1 = -0.51\text{p.u.}$$
$$\Delta I_{Q1} = 2\text{x}\,(-0.51\ \text{p.u.}) = -1.02\text{p.u. (MIN)} \quad (5)$$
$$= 6\text{x}\,(-0.51\ \text{p.u.}) = -3.06\ \text{p.u. (MAX)} \quad (6)$$

The required minimum and maximum magnitude of Neg-Seq reactive current according to (3) and (4) based on voltage measurement at the interface protection bus B3 (Fig. 18) will be as follows:

$$\Delta U_2 = (0.49 - 0)/1 = 0.49\ \text{p.u.}$$
$$\Delta I_{Q2} = 2\text{x}\,(0.49\ \text{p.u.}) = 0.98\text{p.u. (MIN)} \quad (7)$$
$$= 6\text{x}\,(0.49\ \text{p.u.}) = 2.94\ \text{p.u. (MAX)} \quad (8)$$

It should be noted that the negative sign of Pos-Seq voltage change (ΔU_1) indicates the voltage reduction or undervoltage, hence the negative sign of the additional Pos-Seq reactive current (ΔI_{Q1}) indicates the supply or generation of reactive power required. This is called as the overexcited operation mode of the DER (Fig. 4) used for providing voltage support to the grid. For the Neg-Seq voltage change (ΔU_2) and the additional Neg-Seq reactive current (ΔI_{Q2}), there will always be a positive sign due to the absence of Neg-Seq voltage before the fault. Hence the additional Neg-Seq current (ΔI_{Q2}) can only be provided in the underexcited mode.

Fig. 15 (bottom) shows that the normal Pos-Seq current (green color) provided by DER-1 at LV-side is 585.6 A that is purely active current. After the inception of the LL-fault F1 the current becomes 690 A that is purely reactive current.

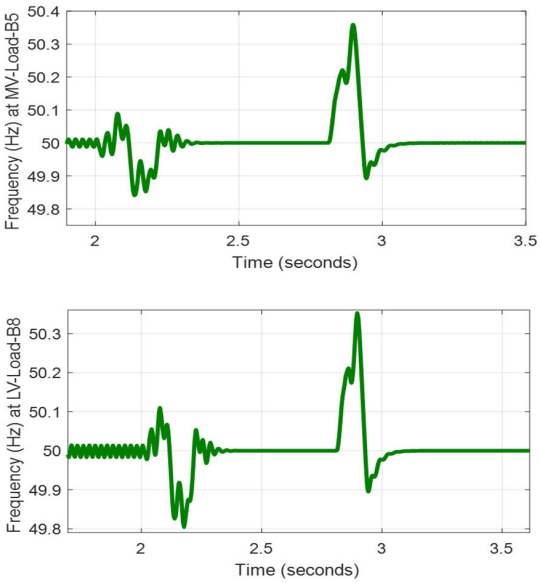

FIGURE 23. The frequency (Hz) at MV-load (top) and LV-load (bottom) during the LL-fault F1 in grid-connected mode.

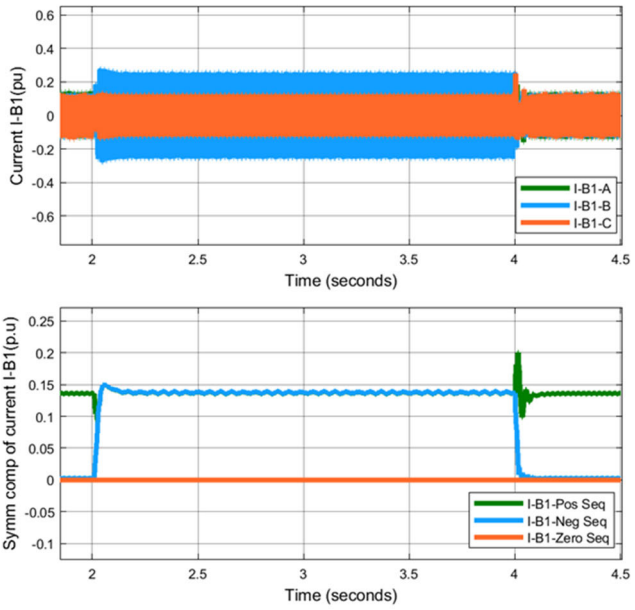

FIGURE 24. The instantaneous line current (top) and the derived symmetrical components of current (bottom) in p.u. observed at bus B1 during phase-A open fault F1 in grid-connected mode.

It means the DER-1 provides a default Pos-Seq reactive current of 1.18 p.u. during the LL-fault F1. However, after the activation of Q-source, the Pos-Seq reactive current increases to 856.3 A, which is1.46 p.u. of the normal Pos-Seq current. The Pos-Seq reactive current value of 1.46 p.u. lies in between the minimum and the maximum value as calculated in (5) and (6), respectively. With $\Delta I_{Q1} = -1.46$ p.u. and $\Delta U_1 = -0.51$, the gradient k_1 becomes equal to 2.86 (between 2 and 6) using (1). Hence, it can be said that the provision of the Pos-Seq reactive current by DER-1 during the LL-fault F1 before and after the activation of Q-source complies with the EN 50549-2-2019 grid code.

Fig. 15 (bottom) shows that the normal Neg-Seq current (blue color) provided by DER-1 at LV-side is equal to zero before the fault which becomes 29 A after the inception of the LL-fault F1. It means the DER-1 provides a default Neg-Seq reactive current of 0.049 p.u. during the LL-fault F1 which is far less than the minimum required value of 0.99 p.u. according to (7). Hence, DER-1 does not comply with EN 50549-2-2019 grid code for the Neg-Seq reactive current provision during the LL-fault F1 with the default setting/control. However, after the activation of Q-source, the Neg-Seq reactive current increases to 692.2 A which is about 1.18 p.u. of the normal Pos-Seq current. The Neg-Seq current value of 1.18 p.u. lies in between the minimum and the maximum value as calculated in (7) and (8), respectively. With $\Delta I_{Q2} = 1.18$ p.u. and $\Delta U_2 = 0.49$ p.u., the gradient k_2 becomes equal to 2.4 using (3). Hence, it can be said that the provision of the Neg-Seq reactive current by DER-1 during the LL-fault F1 complies with the EN 50549-2-2019 grid code after the activation of the dynamic Q-source.

c: CASE-2: PHASE-A OPEN FAULT F1

The phase-A open fault F1 is applied at simulation time of 2 s and for a duration of 2 s from simulation time of 2s to 4 s at the end of 2 km line near the PCC of AC microgrid (Fig. 8). The phase-A open fault is created by opening the pole-A of CB2 in the grid-connected mode.

Fig. 24 shows the instantaneous current and the derived symmetrical components of the current observed at bus B1. It can be seen from the Fig. 24 (bottom) that the Neg-Seq current at B1 increases after the creation of the phase-A open condition. Therefore, the Neg-Seq current can be used for the detection of phase-A open fault condition provided that the magnitude of the Neg-Seq current is well above the Neg-Seq current observed during the normal maximum possible unbalanced load condition. This is also true for the Neg-Seq current observed at bus B2 (Fig. 25 bottom). Otherwise, it will be difficult to detect phase-A open fault condition with only the Neg-Seq current. Fig. 26 (V-B3) shows that the voltage at the PCC remains within the static operating voltage range of 0.8-1.2 p.u., therefore Q-source is not activated. It also shows that the magnitude of the Neg-Seq voltage is also lower than the set threshold of 0.5 p.u. at the interface protection of the PCC. Hence, this fault condition is even not detected by the interface protection. The voltages and currents at all other buses remain within the normal operating ranges.

The other method to detect the phase-A open fault condition at F1 location is to observe the flow of current at phase-A/line-A of the secondary side of the HV/MV substation transformer. This will of course increase the number of measurement points and the related equipment (CTs or sensors). A negligible or lower current flow from phase-A of the secondary side of HV/MV transformer will indicate phase-A open condition.

Fig. 27 shows the RMS current at secondary side of the HV/MV transformer at bus B2. It clearly shows the current

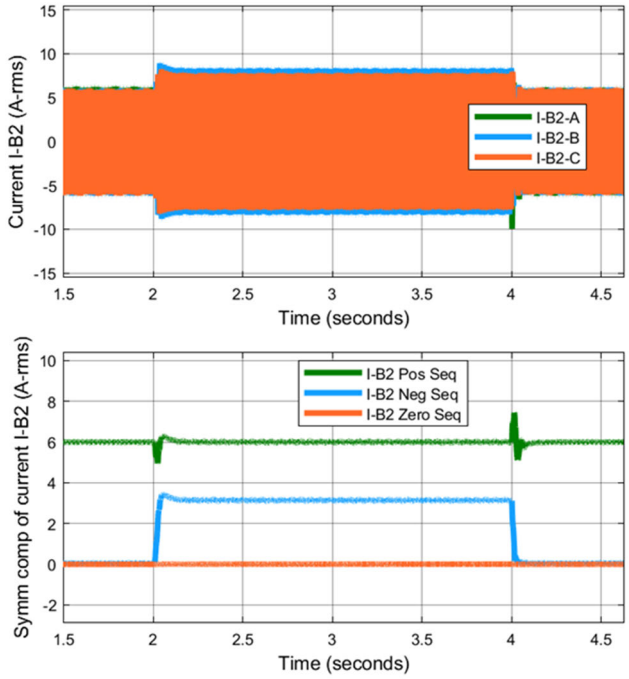

FIGURE 25. The rms instantaneous line currents (top) and the derived symmetrical components of rms current (bottom) observed at bus B2 during phase-A open fault F1 in grid-connected mode.

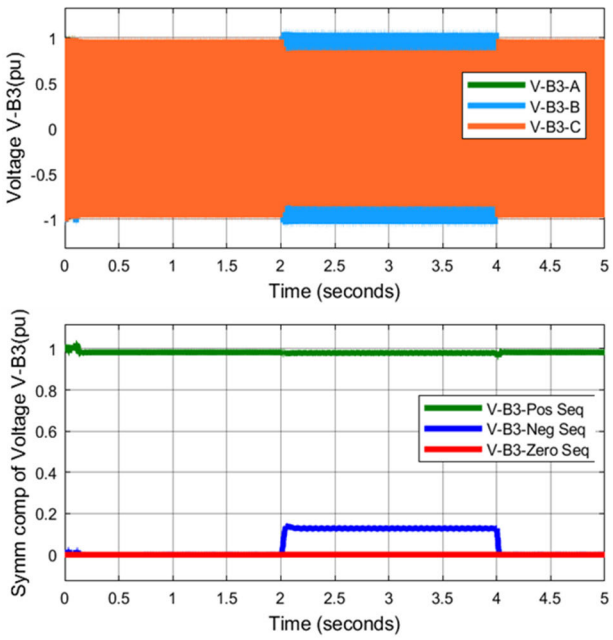

FIGURE 26. The instantaneous voltage (top) and the derived symmetrical components of voltage (bottom) in p.u. observed at bus B3 during phase-A open fault F1 in grid-connected mode.

in phase-A is less than the current in phase-B and phase-C from simulation time of 2 s to onwards. Various methods for the detection of open phase condition are discussed in [32]. Table 11 includes some of the effective and potential open phase detection schemes.

For the LL short-circuit fault and phase-A open fault at F1 in the grid-connected mode, the extent of dynamic

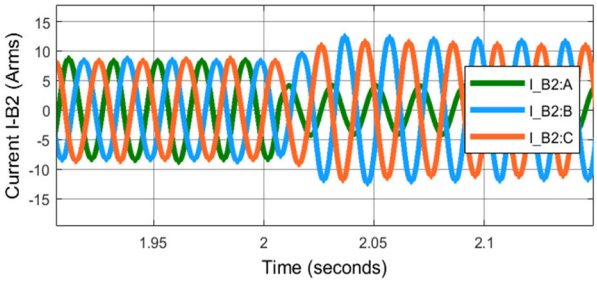

FIGURE 27. The rms instantaneous line currents observed at bus B2 during phase-A open fault F1 in grid-connected mode.

TABLE 11. The effective and potential open phase detection schemes [32].

Schemes	Description
Effective schemes	
Optical CT	Monitoring of magnetization and capacitive current. A reciprocal interferometer sensor and modulator mounted on each phase of transformer and signal processing circuit in the control room, connection via fiber optic and modulator trunk cable. IEC 61850-9-2LE process bus compliant relay.
Active neutral signal injection	Injection source, CT and controller. 100 mA, 45-90 Hz current injection. Monitoring of zero-sequence impedance and neutral OC.
Specially designed window-type CTs/sensors	Sensors installed on transformer HV bushings. Monitoring of current magnitude, phase angles, Symm Comp and waveforms. Specific relay algorithm used.
Potential schemes	
Phase current unbalance	Open phase current will be less than the healthy/closed phases. Chance of false detection during grid unbalances, therefore Symm Comp monitoring is also required.
Sequence voltage & current comparison	Magnitude and phase comparisons of Symm comp of currents and voltages.
Rogowski coils	Measurement of line currents, A/D conversion and fiber optic cable transmission.
CT open circuiting	Voltage measurement at CT secondary during intentional open circuit when measured current threshold is less than normal. No voltage at CT secondary indicates open phase at primary.
Microprocessor relays	Multiple methods: Ratio of 2nd harmonics to fundamental currents, comparison of measured current with digital filter response, zero-crossing detection, I_0/I_1 ratio, I_2/I_1 ratio.
Communication aided hybrid schemes	IEC 61850, DNP3 etc. communication protocols for information/measurement sharing between microprocessor relays and logics.

Q-injection has been found through simulation. The Q-injection of 760 kVar is required during the LL-fault F1 in order to meet the EN 50549-2-2019 grid code requirement. The extent of Q-injection during the LG-fault F1 is found to be half of that required during the LL-fault F1 in order to meet the EN 50549-2-2019 grid code requirement. The lower Q-injection during the LG-fault F1 is due to comparatively higher voltage of healthy phases during this fault.

The results for the LG-fault F1 are not included for the sake of brevity. For the effectively grounded AC microgrid, the LL-fault F1 in the grid-connected mode is correctly detected by the I_2/I_1 protection function at B1 after the Q-injection by DER-1. However, the LG-fault F1 is not detected by the I_2/I_1 protection function at B1 due to higher tripping threshold of

1.3. It means I_2/I_1 protection function at B1 requires different tripping thresholds for the LL-fault and LG-fault at the same location in the grid-connected mode. A lower ratio of I_2/I_1, for example 0.5, that is less than 1.3 can be used at B1 in order to detect both the LL-fault F1 and LG-fault F1 in the grid-connected mode. In that case, the magnitude of I_2 should be used as a restraining quantity. It means I_2/I_1 protection should only trip after reaching a threshold of 0.5 if the magnitude of I_2 is 0.35 p.u. or more. This will prevent the false tripping of I_2/I_1 protection during the times of off-peak load with some fair degree of unbalance loading.

2) UNBALANCED FAULTS IN THE ISLANDED MODE

a: CASE-3: LL-FAULT F2

The LL-fault F2 between phase A and phase B (AB-fault) is applied at simulation time of 6 s for a duration of 2 s from 6-8 s at the end of 1 km cable (Fig. 8) during the islanded mode of operation. Fig. 28 shows the instantaneous and symmetrical components of fault current observed at bus B6. Fig. 28 (bottom) shows that the magnitudes of both the Pos-Seq and Neg-Seq components of current at B6 are increasing equally after the LL-fault F2 is triggered at simulation time of 6 s. However, after the injection of reactive current at 6.1 s, the magnitude of Neg-Seq current is increased, whereas the magnitude of Pos-Seq current is decreased at bus B6. This causes the ratio I_2/I_1 to increase from about 0.95 right after the fault to above 1.3 after the Q-injection at simulation time of 6.237 s (Fig. 29). This increased ratio of I_2/I_1 has been used as a means of detecting LL-fault F2 downstream of bus B6. Therefore, I_2/I_1 protection trips CB6 at 6.637 s (Fig. 30) after the set definite time tripping delay of 0.4 s. The CB7 is transfer tripped from the CB6 after a delay of 0.02 s.

Fig. 31 shows the magnitude of the instantaneous and the symmetrical components of current observed at bus B7. Fig. 31 (bottom) shows that the magnitude of the Neg-Seq current at B7 is less than 0.35 p.u. after the inception of the LL-fault F2 at 6 s which is further decreased after the Q-injection of 760 kVar by the DER-1 at simulation time of 6.1 s. This means that I_2/I_1 protection at B7 will not trip for this upstream fault and a natural magnitude-based directional discrimination is maintained in the reverse direction due to very less Neg-Seq current infeed by the DER-2 (Fig. 32). Only the Pos-Seq UV at B6 will be able to provide the local backup to I_2/I_1 protection at B6 because Neg-Seq OV protection cannot trigger due to less than 0.5 p.u. of the Neg-Seq voltage at B6 during LL-fault F2 (Fig. 33). The reduction of the Neg-Seq voltage at B6 is mainly due to the Q-injection effect.

b: GRID CODE COMPLIANCE CHECK FOR CASE-3:

The required minimum and maximum magnitude of Pos-Seq reactive current according to (1) and (2) based on voltage measurement at the interface protection bus B3 (Fig. 34) will be as follows:

$$\Delta U_1 = (0.5669 - 0.9937)/0.9937 = -0.4295 \text{ p.u.}$$

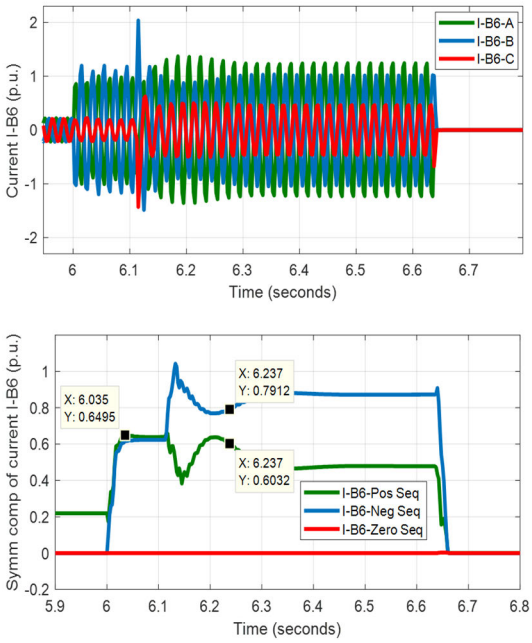

FIGURE 28. The instantaneous line currents (top) and the derived symmetrical components of current (bottom) in p.u. observed at bus B6 during LL-fault F2 in islanded mode.

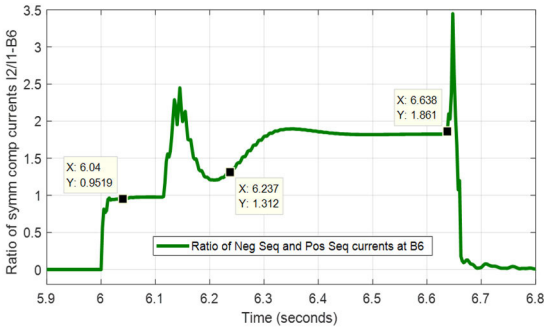

FIGURE 29. I_2/I_1 ratio at B6 after LL-fault F2 (from 6 s to 6.1 s) and after the Q-injection (from 6.1 s to 6.638 s) during LL-fault F2 in islanded mode.

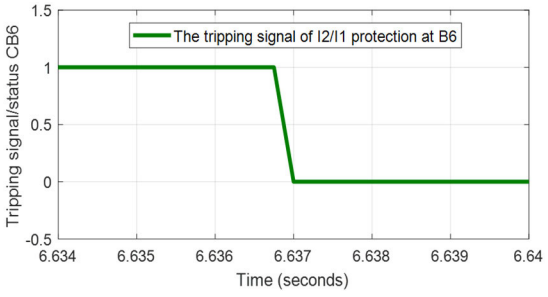

FIGURE 30. Tripping signal of the I_2/I_1 protection function at B6 to trip CB1 after the LL-fault F2 in islanded mode.

$$\Delta I_{Q1} = 2x\,(-0.4295 \text{ p.u.}) = -0.859 \text{ p.u. (MIN)} \quad (9)$$

$$= 6x\,(-0.4295 \text{ p.u.}) = -2.577 \text{ p.u. (MAX)} \quad (10)$$

The required minimum and maximum magnitude of Neg-Seq reactive current according to (3) and (4) based on voltage

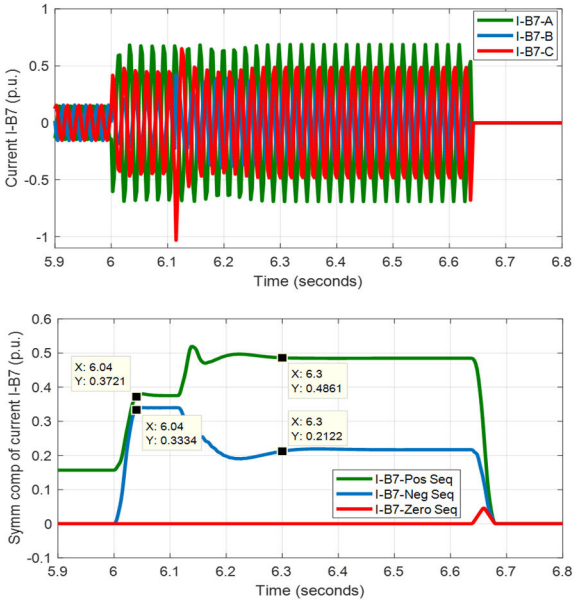

FIGURE 31. The instantaneous line currents (top) and the derived symmetrical components of current (bottom) in p.u. observed at bus B7 during LL-fault F2 in islanded mode.

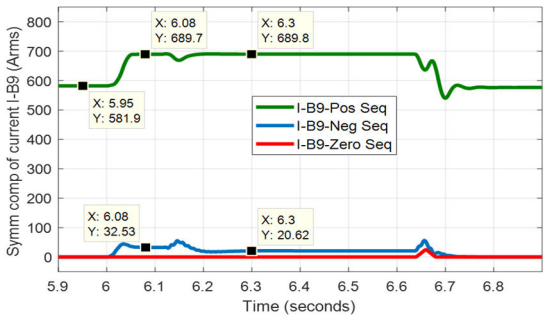

FIGURE 32. Fault current contribution from the DER-2: The derived symmetrical components of current in p.u. observed at bus B9 during LL-fault F2 in islanded mode.

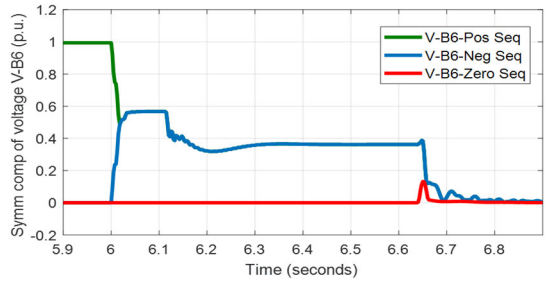

FIGURE 33. The derived symmetrical components of voltage in p.u. observed at bus B6 during LL-fault F2 in islanded mode.

measurement at the interface protection bus B3 (Fig. 34) will be as follows:

$$\Delta U_2 = (0.5669 - 0)/0.9937 = 0.57 \text{ p.u.}$$
$$\Delta I_{Q2} = 2\text{x}\,(0.57 \text{ p.u.}) = 1.14\text{p.u. (MIN)} \quad (11)$$
$$= 6\text{x}\,(0.57 \text{ p.u.}) = 3.42 \text{ p.u. (MAX)} \quad (12)$$

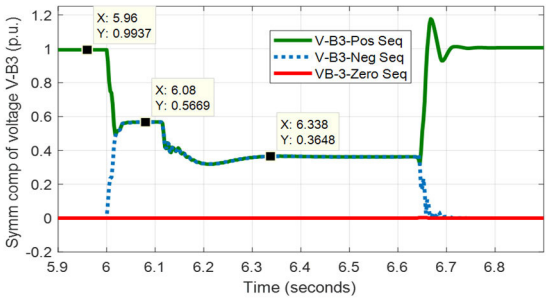

FIGURE 34. The derived symmetrical components of voltage in p.u. observed at bus B3 during LL-fault F2 in islanded mode.

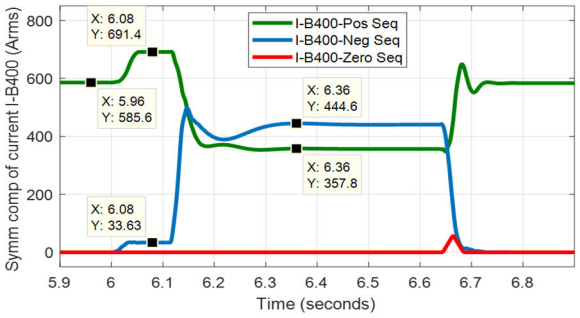

FIGURE 35. Fault current contribution from the DER-1 at LV side: The derived symmetrical components of rms current (A) observed at bus B400 during LL-fault F2 in islanded mode.

The negative sign of the Pos-Seq voltage change indicates the undervoltage situation at bus B3. Therefore, the negative sign of the additional Pos-Seq reactive current in (9)-(10) indicates that additional Pos-Seq current of 0.859-2.577 p.u. needs to be provided in overexcited operation (Fig. 4) to support the voltage at bus B3. Fig. 35 shows that the DER-1 reaches the Pos-Seq reactive current requirement of 0.61 p.u. (357.8 A) that is less than that calculated in (9). Fig. 35 also shows that DER-1 also reaches the Neg-Seq current requirement of 0.759 p.u. (444.6 A) against the minimum of 1.14 p.u. (667.6 A) of the Neg-Seq reactive current required according to (11). This means that in the islanded mode of operation more reactive power is required to meet the minimum Pos-Seq and Neg-Seq current requirements compared with the grid-connected mode requirement. Although, the minimum grid code requirements are not met by Q-injection of 760 kVar, but it is still enough capacity for the detection of the LL-fault F2 in the islanded mode of operation.

B. DIRECTIONAL ELEMENT

The indication of the direction of the fault (forward/reverse) discussed in this subsection is based on comparison of phase angle of operating (fault) current with respect to the reference or polarizing voltage. The Pos-Seq voltage (V_1) is used as the reference or polarizing quantity and the Pos-Seq current (I_1) during the fault is used as the operating quantity for the design of the Pos-Seq directional OC element 67P. Similarly, the Neg-Seq voltage (V_2) is used as the reference or polarizing quantity and the Neg-Seq current (I_2) during the fault is

TABLE 12. The Pos-Seq and Neg-Seq voltages and currents during LL-Faults.

Quantity	Before Q-injection	After Q-injection
LL-fault F1 in the grid-connected mode		
V_1 at B1	1.0∠0° p.u.	1.0∠0° p.u.
I_1 at B1	3.9∠-87° p.u.	3.33∠-87.6° p.u.
V_2 at B1 is zero	0∠93° p.u.	0∠91.5° p.u.
I_2 at B1	3.8∠-88° p.u.	4.4∠-88.5° p.u.
V_1 at B2	0.49∠-29° p.u.	0.569∠-30.35° p.u.
I_1 at B2	0.725∠176° p.u.	0.6953∠-123.2° p.u.
V_2 at B2	0.49∠-149° p.u.	0.569∠-150.35° p.u.
I_2 at B2	0.525∠-146.7° p.u.	0.8784∠-106.3° p.u.
LL-fault F2 in the islanded mode		
V_1 at B6	0.58 ∠-9.89° p.u	0.38 ∠-90.66° p.u
I_1 at B6	0.6495 ∠-28.45° p.u	0.6 ∠-5.519° p.u
V_2 at B6	0.567∠-129.9° p.u.	0.364∠149.3° p.u.
I_2 at B6	0.6234∠52.32° p.u.	0.88∠30.56° p.u.
V_1 at B7	0.58∠22.58° p.u.	0.38∠-55.14° p.u.
I_1 at B7	0.372∠-134.8° p.u.	0.486∠139.3° p.u.
V_2 at B7	0.54∠-162.3° p.u.	0.3653∠117.4° p.u.
I_2 at B7	0.3334∠-160.9° p.u.	0.2122∠116.9° p.u.

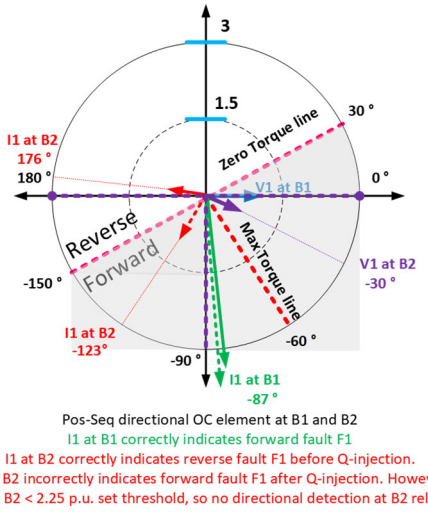

FIGURE 36. The 67P directional element operation at B1 and B2 during the LL-fault F1 in the grid-connected mode with RCA of 60° lagging with respect to V1 at B1 and B2.

used as the operating quantity for the design of the Neg-Seq directional OC element 67Q. The Pos-Seq and the Neg-Seq voltages and currents during the LL-fault F1 in the grid-connected mode and LL-fault F2 in the islanded mode are presented in Table 12.

a: 67P ELEMENT DESIGN PRINCIPLE

The maximum torque line is assumed to be at a relay characteristic angle (RCA) of 60° or 30° lagging from the measured angle of the reference voltage (V_1) and the zero torque line is assumed at ±90° from the RCA. If the measured phase angle of Pos-Seq current I_1 during the fault lies in between RCA ± 90°, the fault is classified as the forward fault by the 67P element. Otherwise, the fault is classified as the reverse fault. The third approach is to use RCA of 0 degrees with respect to the polarizing voltage (V_1) and assuming zero torque line at RCA ± 90°. This means the fault is considered in the forward direction if the Pos-Seq current I_1 during the fault is lagging or leading the reference voltage V_1 by 90°. These directional principles are adopted from [33] but with different polarizing and operating quantities. The forward/reverse fault is declared only if the magnitude of I_1 during the fault is 2.25 p.u. or greater in the grid-connected mode and 1.2 p.u. or greater in the islanded mode.

b: 67Q ELEMENT DESIGN PRINCIPLE

The same principles as discussed for the 67P element design are also considered for the 67Q element design but the Neg-Seq voltage V_2 is used as the polarizing quantity and the Neg-Seq current I_2 is used as the operating quantity. Additionally, the forward direction is considered in the opposite direction of the considered RCA. This means if the measured phase angle of Neg-Seq current I_2 during the fault lies in between RCA ± 90°, the fault is classified as the reverse fault by the 67Q element. Otherwise, it is classified as the forward fault. The forward/reverse fault is declared only if the ratio of I_2/I_1 during the fault is 1.3 or greater in both the grid-connected and the islanded modes. Moreover, the magnitude of $I_2 \geq 0.5$ p.u. is used as the restraining quantity to avoid the false operation of 67Q element during the load unbalance.

The above mentioned design principles of 67P and 67Q elements are applied for the forward/reverse fault directional discrimination during LL-fault F1 in the grid-connected mode and LL-fault F2 in the islanded mode. For the demonstration purpose, the operation of 67P directional element with RCA of 60° lagging is shown in Fig 36. Similarly, the operation of 67P directional element with RCA of 30° lagging is shown in Fig 37. The shaded area on the 360° planes of Fig 36 and Fig. 37 indicates the forward direction of the fault whereas the unshaded area indicates the reverse direction of the fault. The zero torque line is the boundary or threshold line for angles of the Pos-Seq fault current between the forward and the reverse direction regions. It means if the angle of the Pos-Seq fault current I_1 lies in the shaded area, the fault is considered in the forward direction otherwise it is considered in the reverse direction. The variable lengths of radius along the 360° plane marked with blue lines indicate the thresholds of the magnitudes of voltages and currents. The current threshold should be 2.25 p.u. or greater for the grid-connected mode and 1.2 p.u. or greater for the islanded mode.

The results (Table 12) show that only the 67P element could be reliable for LL-fault F1 in the grid-connected mode. This is clearly evident from the Fig. 36 and Fig. 37 that I_1 at B1 correctly indicate the fault to be in forward direction with its angle located in the shaded area and its magnitude greater than 2.25 p.u. set threshold. Fig. 36 and Fig. 37 also reveal that I_1 at B2 correctly indicate the reverse fault direction before Q-injection as its angle lies in the unshaded area. However, I_1 at B2 incorrectly indicate forward direction after Q-injection as its angle lies in the shaded area instead of unshaded area. The characteristic of 67P element at B2 with V_1 at B2 used as the polarizing quantity is drawn with purple lines

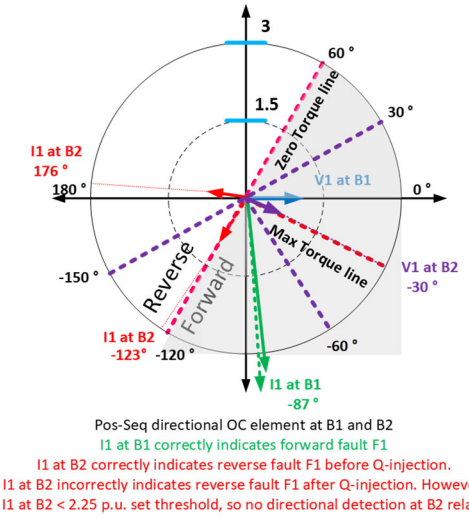

FIGURE 37. The 67P directional element operation at B1 and B2 during the LL-fault F1 in the grid connected mode with RCA of 30° lagging with respect to V1 at B1 and B2.

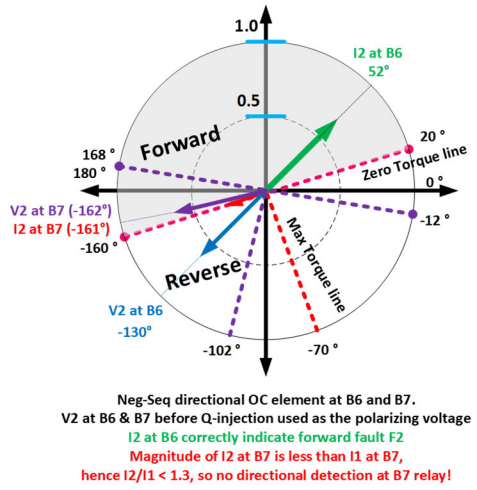

FIGURE 38. The 67Q directional element operation at B6 and B7 during the LL-fault F2 in the islanded mode before Q-injection with RCA of 60° lagging with respect to V2 at B6 and B7.

(see Fig. 36 and Fig. 37). The magnitude of I_1 at B2 is less than set threshold of 2.25 p.u., therefore the AND logic of 67P element at B2 will not indicate the presence of the reverse fault even if the angle indicates the fault to be in the forward or reverse direction. The 67P element would not be reliable during the LL-fault F2 in the islanded mode due to less than 1.2 p.u. magnitude of Pos-Seq current I_1 in both the forward direction (bus B6) and the reverse direction (bus B7).

The results (Table 12) reveal that the 67Q element would not work during the LL-fault F1 in the grid-connected mode due to nearly zero magnitude of Neg-Seq voltage V_2 in the forward direction (bus B1) and the ratio I_2/I_1 of less than 1.3 in both the forward direction (bus B1) and the reverse direction (bus B2) before Q-injection. Although the ratio I_2/I_1 of greater than 1.3 is obtained in the forward direction (bus B1) after Q-injection but the persistent zero magnitude

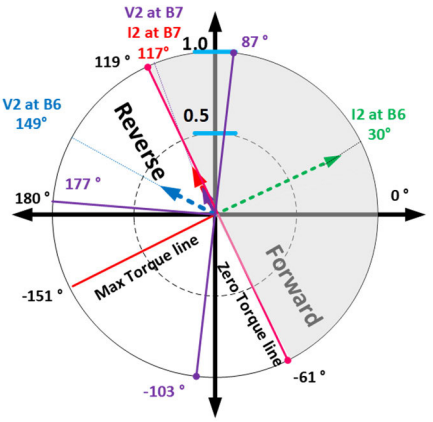

FIGURE 39. The 67Q directional element operation at B6 and B7 during the LL-fault F2 in the islanded mode after Q-injection with RCA of 60° lagging with respect to V2 at B6 and B7.

of V_2 even after Q-injection makes it inapplicable for the 67Q element operation. The 67Q element could be reliable during the LL-fault F2 in the islanded mode particularly in the forward direction (bus B6) after the activation of Q-injection function which results in the ratio I_2/I_1 of greater than 1.3.

The operation of 67Q directional element during the LL-fault F2 in the islanded mode with RCA of 60° lagging before and after Q-injection is shown in Fig. 38 and Fig. 39, respectively. It can be seen in Fig. 38 and Fig. 39 that I_2 at B6 correctly indicate the fault to be in forward direction with its angle located in the shaded area (green line), its magnitude greater than 0.5 p.u. and the ratio of I_2/I_1 during the fault is greater than the set threshold of 1.3. Fig. 38 and Fig. 39 also reveal that I_2 at B7 will correctly indicate the reverse fault direction before and after Q-injection as its angle lies in the unshaded area (red line). However, the magnitude of I_2 at B7 is less than set threshold of 0.5 p.u. and the ratio of I_2/I_1 is also less than 1.3 due to limited Q-injection by DER-2, therefore the AND logic of 67Q element at B7 will not indicate the presence of the reverse fault. The characteristic of 67Q element at B7 with V_2 at B7 used as the polarizing quantity is drawn with purple lines (see Fig. 38 and Fig. 39).

Similar results will be obtained for the 67Q element with the RCA of 0° and 30°. The RCA of 0° in particular would make the directional detection straightforward in the forward or the reverse direction for both 67P and 67Q directional elements even after Q-injection. The three directional characteristics with RCA of 0°, 30° and 60° can be used simultaneously with OR logic to cover the wide range of angle variations of the symmetrical component quantities. Fig. 40 shows the OR logic inputs/outputs of 67P and 67Q elements. Fig. 41 shows the standardized protection logic for the unbalanced faults used at the interface protection bus B3 and other buses (B1, B2, B6, B7). Fig. 40 explains the details of 67P (ANG) and 67Q (ANG) of Fig. 41.

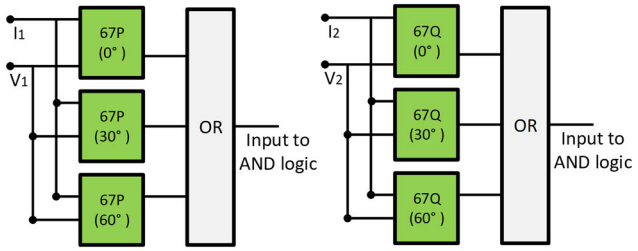

FIGURE 40. The OR logic of 67P and 67Q directional elements with RCA of 0°, 30° and 60°.

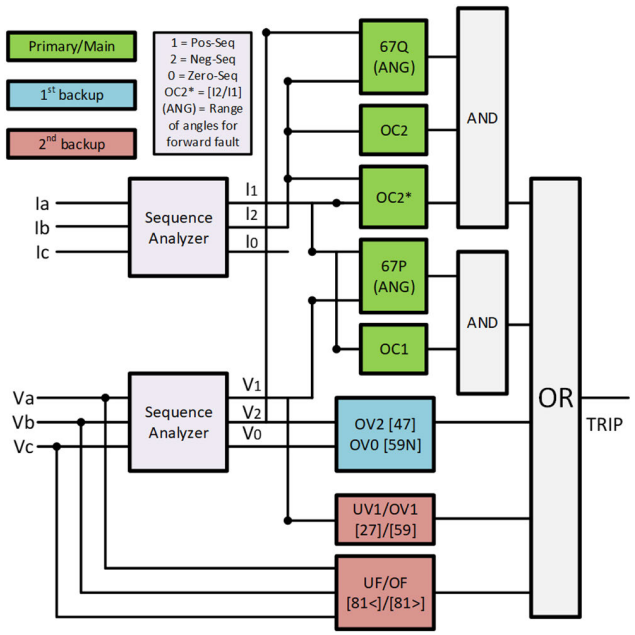

FIGURE 41. Standardized protection logic for the unbalanced faults used at the interface protection bus B3 and other buses (B1, B2, B6, B7).

C. GRID CODES PROPOSAL FOR ISLANDED MODE

From the review of European and IEEE grid codes for the DERs in MV/LV networks it is found that the grid codes for islanded mode of operation are still lacking. Although IEEE grid codes cover the transition and synchronization rules between the grid-connected and islanded modes during the intentional islanded mode in addition to few changes in OV, OF, UF ride-through and adaptive settings. However, particular UVRT, OVRT, LFRT and HFRT requirements for the islanded mode are still not mentioned. In our previous paper [34], we proposed a new UVRT curve for the islanded mode operation of AC microgrids. In this paper, we propose a new five-cycle OVRT curve for the islanded mode operation of AC microgrids (Fig. 42). The new OVRT curve is developed on the basis of overvoltage observed during the transition of AC microgrid to the islanded mode operation in our previous paper [35]. After the initial five cycles of the fundamental frequency during the transition mode, the normal OVRT curve (Fig. 3) will be applied. It means the new OVRT curve is similar to the OVRT curve for the grid-connected mode after the initial five cycles of the fundamental frequency during the transition to the islanded mode.

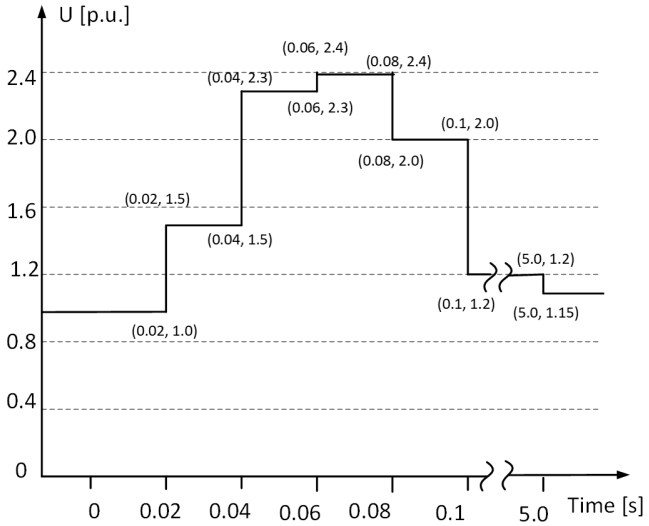

FIGURE 42. The new proposed five-cycle HVRT curve for smooth transition to the islanded mode operation.

TABLE 13. The Comparison of EN 50549 and IEEE 1547 grid codes of DERs.

EN Grid codes [22] [23]	IEEE Grid codes [24] [26] [27]
Applicable for only the grid-connected mode.	Applicable for both grid-connected and islanded modes. However, islanding mode requirements are defined generally and not specifically.
Limits of capacities of DERs specified (type-A & B)	Limits of capacities of DERs not specified
Requirements are applicable irrespective of penetration levels of DERs.	Requirements depend on penetration levels of DERs (categories I, II, III)
Applicable for 50 Hz distribution systems	Applicable for 60 Hz distribution systems
ROCOF immunity of 2 Hz/s	ROCOF immunity of 3 Hz/s
Specific limits for short-circuit current or reactive current by DERs during faults are defined.	Specific limits are not defined but DERs are required to have capability of exchanging reactive power during short-circuit faults for dynamic voltage stability during LVRT and HVRT events.
DERs have to ride-through only one voltage disturbance according to the defined LVRT curve.	DERs have to ride-through multiple voltage disturbances with specified short-time interval between two consecutive voltage disturbances.
No exemptions to UVRT, OVRT and frequency disturbance requirements for DERs.	Exemption to UVRT, OVRT and frequency disturbance requirements for emergency systems and standby DERs.
No voltage phase angle changes ride-through requirements for DERs are specified.	Voltage phase angle changes ride-through requirements for DERs are specified.
Interface protection settings of DERs overrule the technical capabilities and the ride-through requirements.	Any tripping of DERs for the self-protection and failure to provide ride-through requirements is considered as the non-compliance of the grid code.

The suggested five-cycle OVRT curve (Fig. 42) means that the DERs need to either ride-through during this time or a voltage regulation should be provided to avoid the DER tripping during the transition period by the OV protection.

V. DISCUSSION

The most relevant European and IEEE grid codes for the connection of the converter-based DERs to MV/LV networks have been reviewed and the selected grid code requirements have been evaluated. Table 13 presents a comparison between EN and IEEE grid codes of DERs.

One important requirement of the grid codes is the provision of the reactive current by the converter-based DERs during the voltage changes at the PCC. The certain amount of reactive current up to the rated current limit of individual DER has to be provided by the DERs both in the Pos-Seq and Neg-Seq components. The control of the converter-based DERs is usually designed to provide the Pos-Seq current during the voltage steps or faults and the Neg-Seq current is usually limited. Even if the DERs are controlled to provide the Neg-Seq reactive current as the priority, its magnitude may not be enough to meet the stringent grid code requirements. Therefore, extra Q-sources have to be installed in MV/LV networks to meet the new/revised grid code requirements.

In this study, the extent of Q-injection during the unbalanced faults has been found according to the minimum grid code requirements. Moreover, the effect of Q-injection on the unbalanced short-circuit faults detection, and protection coordination using different symmetrical components-based protection functions has been observed. It is found that Q-injection at LV terminals of DER equal to twice the MVA rating of the individual DER is enough to meet the minimum grid code requirements of EN 50549-2-2019 [22] during the unbalanced faults in the grid-connected mode. The extent of Q-injection higher than twice the MVA rating of individual DER is required during the unbalanced faults in the islanded mode. However, Q-injection of twice the MVA rating of the individual DER is also effective for the detection of the unbalanced short-circuit faults in the islanded mode.

It should be noted that the reactive current requirement mentioned in subsection C of section II is generally applicable for 3Ph balanced and unbalanced faults. It means the Pos-Seq current requirement during the LLL-faults and the Neg-Seq current requirement during the LLLG-faults and other unbalanced faults. For other types of unbalanced faults, the Q-injection requirement of EN 50549-2-2019 is open for future developments. In [36], a distinction is made between the fault types for the requirement of Q-injection. It states that a WTG unit must be able to provide a reactive current of at least 100% of the rated current during the 3-pole faults and at least 40% of the rated current during 1-pole and 2-pole faults. Moreover, the relevant reactive current requirements only consider voltage and reactive current changes ascertained from Pos-Seq system components of the basic harmonic component. However, maximum possible reactive current is allowed during the 1-pole and 2-pole faults with simultaneous flow of Neg-Seq current as permitted by WTG size. With the mentioned limits of reactive current during faults in [36], the selected capacity of Q-injection meets the grid code requirement. It is further clarified that the main purpose of an additional Q-injection in this study is the enhancement of short-circuit current level during the unbalanced faults particularly the Neg-Seq current. This has been achieved in quite successful manner. The proposed Q-injection method is also valid for the average WTG model.

It is recommended that the outer control of DERs (Fig. 9) should discriminate between the balanced and unbalanced short-circuit faults and give priority to Pos-Seq current during the balanced faults and Neg-Seq current during the unbalanced fault. From the context of DER control presented in this paper, this means that the Pos-Seq current should not be reduced during the balanced LLL-fault. The AND logic can be used for the detection of simultaneous voltage magnitude drop of three-phases to prioritize Pos-Seq current during the balanced LLL-fault. The protection of AC microgrids during the balanced LLL-fault is discussed in detail in our previous papers [34], [35]. In this study, only the symmetrical Q-injection has been used in order to maintain the asymmetry of voltage and current during the unbalanced faults. According to the previous study [37], an asymmetrical Q-injection may provide better performance in terms of voltage support at PCC. However, it may require separate control for each phase. Moreover, asymmetrical Q-injection may raise the voltage of individual phases to the extent of OV protection tripping threshold causing nuisance tripping.

The natural magnitude-based directional coordination is available due to extremely limited amount of the Neg-Seq current provision by the DER-2. Therefore, the AC microgrid can be protected against unbalanced short-circuit faults even without the 67P or 67Q directional elements. However, directional elements will be required if DER-2 also injects the Neg-Seq current up to the same extent of DER-1. This is a typical case for DERs in the ring networks which will be covered in future publications. Nevertheless, the 67Q directional element is also designed and evaluated for the discrimination of forward/reverse fault direction during the selected unbalanced LL-fault in the islanded mode. The Pos-Seq directional element 67P and Neg-Seq directional element 67Q can correctly indicate the forward AB-fault during the grid-connected and the islanded mode, respectively. The directional elements also detect the reverse faults reliably with few exceptions. During these exceptions, though the reverse fault is falsely detected by the directional elements, but its operation is restrained by the threshold settings. In this way a desired operational performance is achieved. During inrush conditions, the blocking of the 67Q directional element is recommended [7]. The protection coordination between the primary/main and backup protections of Fig. 41 at various locations (buses 1, 2, 3, 6 and 7) was also observed according to the settings of Table 9 during the considered faults with and without Q-injection and it was found quite satisfactory.

VI. CONCLUSION

The latest grid codes of DERs connected to the MV/LV networks have been reviewed and the evaluation of selected grid codes applicable for AC microgrid protection is presented. The extent of Q-injection during the unbalanced faults in the grid-connected and islanded modes is determined through simulations. The determined amount of Q-injection meets the minimum grid code requirements and helps detect the unbalanced faults in both the grid-connected and islanded

modes. A new five-cycle OVRT curve is also suggested for smooth transition to the islanded mode operation. The standardized protection settings maintain the proper protection coordination. In future, this work will be further extended for the AC microgrids with the ring-network topology. This means the 67P and 67Q directional elements will be used to distinguish between the forward and reverse faults due to Q-injection of the same extent from both sides of the fault point.

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