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RESEARCH ARTICLE

High-Performance Buck-Boost Partial Power Quasi-Z-Source Series Resonance Converter

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ABSTRACT The converter efficiency defines the overall efficiency of a renewable energy system. In a full power converter, its components process the whole input power, even if it is not mandatory. Partial power processing (PPP) is an exciting concept for improving overall system efficiency and reducing system cost and size. In PPP, the converter processes the amount of power needed to be processed. This work proposes a PPP based on the high-performance Quasi-Z-Source Series Resonance converter (QZSSRC). The proposed partial power converter has a series-input parallel-output (SIPO) architecture. Previous publications in this area mainly consider converters with step-down voltage regulation, like the phase-shifted full-bridge converter. They underperform in this application due to operating at the maximum power when bucking the voltage the most. This paper studies two other types of dc-dc converters, buck-boost and boost, in SIPO partial power converters. Theoretical operation principles are corroborated with full experimental results given and analyzed. A 300 W prototype of the QZSSRC is used to convert the power of up to 2 kW in a PPP system with overall system efficiency over 99%.

INDEX TERMS Power converters, partial power processing (PPP), quasi Z-source series resonance converter (QZSSRC), step up, step down, efficiency.

I. INTRODUCTION

The significant developments in semiconductor devices, like replacing Si with SiC and GaN, led to considerable advances in power electronics circuits and systems architectures [1], [2], [3], [4]. Power electronic converter efficiency is an essential parameter influencing the suitability of a particular converter to a given application. Nowadays, many power converters have shown very high efficiency. The best-in-class examples reach 99% in some applications [5].

The new concept of partial power processing (PPP) has provided this very high efficiency [6], [7], [8], [9], [10], [11], [12], [13]. This concept is built based on the fact that the PPP converter processes a fraction of the system power required for load regulation or other functions based on system requirements [14], [15], [16], [17]. Distinct features of PPP, like high efficiency and reduced power rating of components, make it attractive in many applications such as photovoltaic systems, electric vehicle (EV) charging, electrolyzer cell (EC) and fuel cell (FC) chargers, battery storage systems, LED drivers, and wind power systems [18], [19], [20], [21], [22], [23], [24]. The first appearance of the PPP concept was in aerospace applications, where a PV array was used to charge the space system battery. PPP solutions increase the efficiency and power density of the system, plus adding redundancy [25].

Another application of the PPP concept was reported in [26], where the converter was charging a flying capacitor

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in both polarities. This enables the converter to provide different voltage levels at the input and output flexibly. The fast charging stations are another promising applications for the PPP concept, where the system could be rated at more than 350 kW [27]. PPP would decrease installation and maintenance costs.

The difference between the power flow in full power processing (FPP) and PPP converters is illustrated in Figure.1. As can be seen from Figure.1(a), the FPP requires a dc-dc converter to carry the full power of the system. Hence, the converter components are dimensioned to handle 100% of the system power, which causes power loss and high system costs. On the other hand, as seen in Figure.1(b), the PPP configuration required a dc-dc converter that processes only a fraction of the power flowing from the source to the load. This way, the losses generated by the power converter and its size are reduced. Furthermore, by maintaining the same efficiency for the power converter, the global efficiency of the system increases [29].

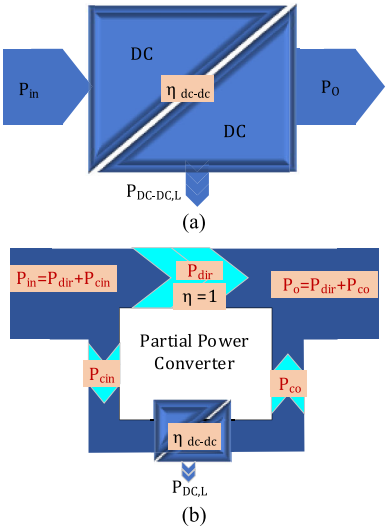

FIGURE 1. Different power converter configurations: (a) full power configuration and (b) partial power configuration.

Equations (1) and (2) describe how the efficiency of a dc-dc converter cell affects the system efficiency differently, depending on whether it is based on FPP or PPP.

$$\eta_{FPC} = \frac{P_O}{P_{in}} = \eta_{dc-dc} \tag{1}$$

$$\eta_{PPC} = \frac{P_O}{P_{in}} = 1 - K_{Pr}\,(1 - \eta_{dc-dc}) \tag{2}$$

where, η_{FPC}, η_{dc-dc}, η_{PPC}, P_O, P_{in}, and Kpr are the full power converter efficiency, dc-dc converter efficiency in a partial power converter (PPC), PPC efficiency, output power, input power, and processed power ratio (partiality coefficient), respectively.

Different configurations have been reported in the literature for the PPP. However, in general, it can be classified into parallel current regulators (PCRs) and series voltage regulators (SVRs), series connected partial power converters (S-PPCs) [30]. S-PPC is a series regulator that regulates the voltage difference between input and output voltages [31], [32].

S-PPC is defined according to input and output connection into the series input parallel output (SIPO), which is more suitable for voltage step-down applications, and the parallel input series output (PISO), which is more convenient for voltage step-up applications, as shown in Figure.2.

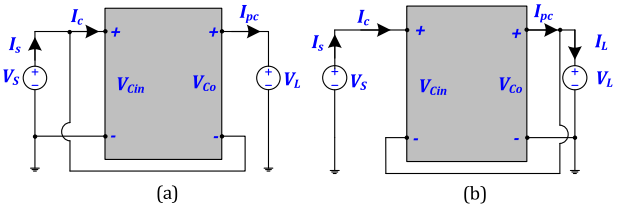

FIGURE 2. Series partial power converter S-PPC architectures (a) PISO, (b) SIPO.

Partial power converters based on PISO configuration have been extensively researched in recent years. They show high performance in voltage step-up applications, while SIPO PPCs have not shown comparable performance in voltage step-down applications [33]. One of the root causes of the observed relatively low performance of the SIPO PPCs is the application of inherent voltage backing topologies like phase-shifted full-bridge converters. These topologies are complicated to design for this application, as their transformer should have a high turns ratio to match the minimum requirement for series voltage between the input and output. At the same time, they should handle the highest power (highest K_{pr}) at the lower dc gain, i.,e., when bucking the input voltage the most.

This work aims to consider alternative implementations of the SIPO PPCs that are expected to provide better performance, namely, using buck-boost and boost dc-dc topologies. The high-performance buck-boost quasi-Z-source series resonant (QZSSR) converter was selected for this study as it can be implemented as buck-boost or as a boost dc-dc converter, depending on the transformer turns ratio while keeping all the other converter components unchanged. The second section presents the basic requirements and operation principles of PPCs. The third section describes the operation principle of the case study converter, while tis design is covered in the fourth section. The experimental results are provided in the fifth section. The conclusions are drawn in the sixth section.

II. BASIC PRINCIPLES AND LIMITATIONS OF PARTIAL POWER CONVERTER

A. REQUIREMENT OF GALVANIC ISOLATION

Isolation is a critical requirement for dc-dc topologies used in partial power converters. PPP comprises numerous non-isolated architectures, requiring galvanic isolation inside to deliver power between parallel and series ports of a dc-dc cell.

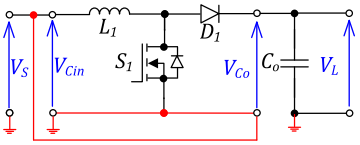

FIGURE 3. Short circuit occurrence in non-isolated PPCs.

Figure.3 is an example of using a non-isolated boost converter to implement a PPP, where a potential short-circuit is taking place. Nevertheless, some non-isolated PPP configurations were presented, as shown in Figure.4. Figure.4(a) and (b) are PPP configurations using a flipped buck converter and a regular buck-boost converter, respectively. However, later research showed they are equivalent to a full power boost converter in terms of stress of the main components and thus cannot be considered true PPCs [34]. Hence, dc-dc topology used in a PPC must have some kind of galvanic isolation, either by a transformer or using a flying energy storage component (capacitor or inductor) [33], [35], [36].

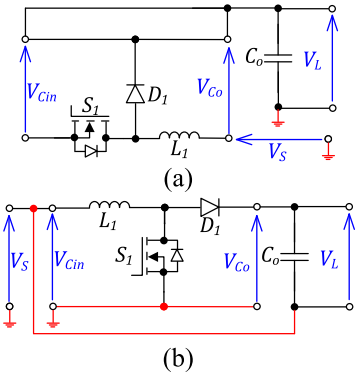

FIGURE 4. Non-isolated converters mistakenly considered PPCs: realized by (a) a flipped buck converter and (b) a boost converter [8], both suffer from full stress on the components.

B. LIMITATIONS OF VOLTAGE REGULATION CAPABILITIES

The limitation of the transformation ratio is a trade-off in partial power converters. Figure.5 illustrates the relationship between the transformation ratio $M = V_L/V_S$, and the converter power rating normalized by the total input power for the voltage step-up conversion ($V_S < V_L$). There is a critical voltage conversion ratio $M_{crit1} = 2$ for SIPO partial power converters. If the conversion ratio is higher than M_{crit1}, the SIPO partial power converter will handle more power than the full power converter and lose its advantages due to the opposite power flow [32]. The voltage gain of the converter decides the percent of power processed by the converter, as can be appreciated from Figure.6.

C. SERIES INPUT PARALLEL OUTPUT PARTIAL POWER CONVERSION

In the case of SIPO PPC configuration, the relation between input and output voltage and currents are as follows:

$$V_L = V_{Co} = V_S + V_{Cin} \tag{3}$$

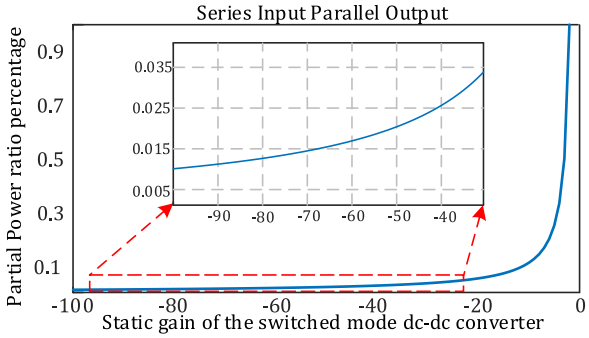

FIGURE 5. Power processing factor in SIPO.

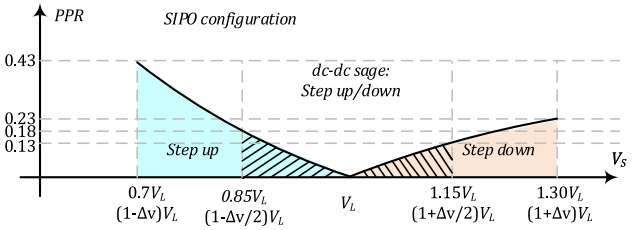

FIGURE 6. Active power processing ratio (PPR) against the relative input voltage in SIPO PPCs.

$$I_S = I_C \tag{4}$$

$$I_L = I_S + I_{pc} \tag{5}$$

$$M = \frac{V_L}{V_S} = \frac{1}{1 - {}^{v_{cin}}/_{V_L}} = \frac{1}{1 - M_C} \tag{6}$$

where $V_L, V_{Co}, V_s, I_S, I_L, I_C, M, M_C$ are the load voltage, dc-dc converter output voltage, source voltage, source current, load current, dc-dc converter input current, static dc voltage gain of the system, and the static dc voltage gain of the dc-dc converter.

The active power processed by the PPP system components is derived by multiplying equation (1) by the load current

$$V_L * I_L = V_L * I_S + V_L * I_{PC} P_t = P_D + P_P \tag{7}$$

The total power of the system is denoted as P_t, P_D is the amount of power transferred to the load without any processing and P_P is devoted to the power processed by the switched mode dc-dc converter.

And the power processed ratio (PPR) for this configuration is defined as

$$PPR = \frac{P_P}{P_t} = \left| \frac{1/M_C}{1 + 1/M_C} \right| \tag{8}$$

Different topologies based on SIPO configuration have been reported in the literature [6], [9], [32], [37], [38]. In [6], a SIPO PPC is presented based on the flyback converter. The PPP system was designed for PV applications. The system demonstrated an efficiency of around 96% with a partiality ratio of 20%. The presented efficiency is not high compared to the full power converter, and due to the usage of the flyback converter, there is a restriction in the duty cycle range. SIPO

PPC presented in [32] is like the system described in [31]. However, due to the high partiality ratio considered, around 50%, the PPP system efficiency is low and less than 93%.

In [37], a SIPO PPC based on the dual active bridge topology has been presented. The dc-dc cell is working in bucking mode all the time. The converter operates with soft switching most of the time even with high partiality ratio reaching 50%. The converter demonstrated an efficiency of around 96.4%.

A two-stage step-down SIPO PPC based on the full-bridge isolated dc-dc converter is presented in [9]. This PPP system is designed for string PV integration and demonstrated experimentally. Due to bucking at the extreme limit, the converter efficiency is around 98.7%, even though the partiality ratio is around 10%, as was predicted above.

Though the SIPO configuration is suitable for step-down applications, the topology developed in [38] is based on a boost converter. The dc-dc converter is boosting the fraction of voltage across its terminal. The reported efficiency of around 99% shows that SIPO implementation with other than bucking dc-dc topologies could be beneficial.

III. PARTIAL POWER BUCK-BOOST QUASI Z-SOURCE SERIES RESONANT PARTIAL POWER CONVERTER

The proposed QZSSR partial power converter schematic is illustrated in Figure.7. The schematic is based on SIPO configuration. The Proposed PPP is stepping down; the input voltage is always higher than the output voltage. However, the QZSSR converter itself may operate in boosting or bucking mode based on the voltage applied to its input terminals and the used transformer ratio.

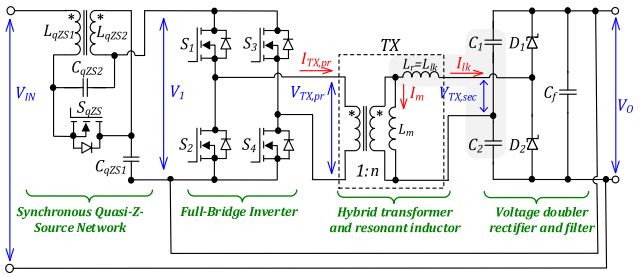

FIGURE 7. Power circuit topology of the partial power QZSSR buck-boost converter.

The high-performance QZSSR converter studied in this work was originally proposed and validated in [39], [40], and [41]. The converter operates in shot-through mode when the voltage at its input terminals is less than $V_o/2n$, normal mode at $V_o/2n$, and bucking mode when the voltage is higher than $V_o/2_n$.

The leakage inductance of the isolation transformer L_{lk} could be used as a resonant inductor. During the active states, its current resonates with the voltage of the parallel combination of the voltage doubler (VDR) capacitors C_1 and C_2. As the switching frequency is close to the resonant frequency, the inverter switches and VDR diodes operate under zero current switching conditions.

Idealized waveforms of the QZSSR PPP converter for the bucking and boosting modes are shown in Fig.8.

A. OPERATION IN THE BOOST MODE

In the boost operating region, the converter is controlled by the shoot-through PWM with symmetric overall poof active states (ST-PWM) at the resonant frequency, as shown in Figure 8 (b). The converter operates in the boosting mode if the input voltage is below $V_o/2n$. The DC voltage gain is regulated by the variation of the shoot-through duty cycle:

$$G_{boost} = \frac{V_o}{n \cdot \Delta v} = \frac{1}{1 - 2D_{ST}}, \tag{9}$$

where V_o, n, Δv, and D_{ST} are load voltage, voltage applied to the input of the dc-dc converter (difference between source and load voltage), cumulative duty cycle of the shoot-through states over the switching period T_{SW} ($D_{ST} = T_{ST}/T_{SW}$). The shoot-through states are generated by the cross-conduction of all switches of the inverter bridge, which occurs twice per switching period. Equivalent circuits describing the converter operation in the boost mode are illustrated in Figure 9.

B. OPERATION IN THE BUCK MODE

In the buck mode, the converter is controlled by the Phase Shift Modulation (PSM) at the resonant frequency, see Figure 8 (a). The converter operates in the buck mode if the input voltage is above $V_o/2n$. Equivalent circuits describing the converter operation in the buck mode are illustrated in Figure 10. The switch S_{qZS} is always conducting, thus configuring the *qZS* network as a passive filter at the input of the dc-dc converter. The output voltage is controlled by the variation of the phase shift angle φ between the leading (S_1 and S_2) and lagging (S_3 and S_4) legs of the inverter bridge. As the resonant current is discontinuous, the control characteristic of the QZSSR in the buck mode depends strictly on the quality factor Q of the resonant tank:

$$G_{buck} = \frac{V_o}{n\Delta V} = 0.5\left[A\left(\frac{2}{\pi Q} - 1\right) + \sqrt{\left(\frac{2}{\pi Q} - 1\right)^2 A^2 + A\frac{8}{\pi Q}}\right], \tag{10}$$

where

$$A = 0.5 - 0.5\cos\left[\pi\left(1 - \frac{\varphi}{180}\right)\right], \text{ and}$$
$$Q = \frac{8\pi f_{SW} L_{lk}}{R_L}, \tag{11}$$

where R_L is the load resistance.

IV. CONVERTER DESIGN GUIDELINES

Converter parameters are designed to cover the worst scenarios of operation. The system design is divided into two parts as follows:

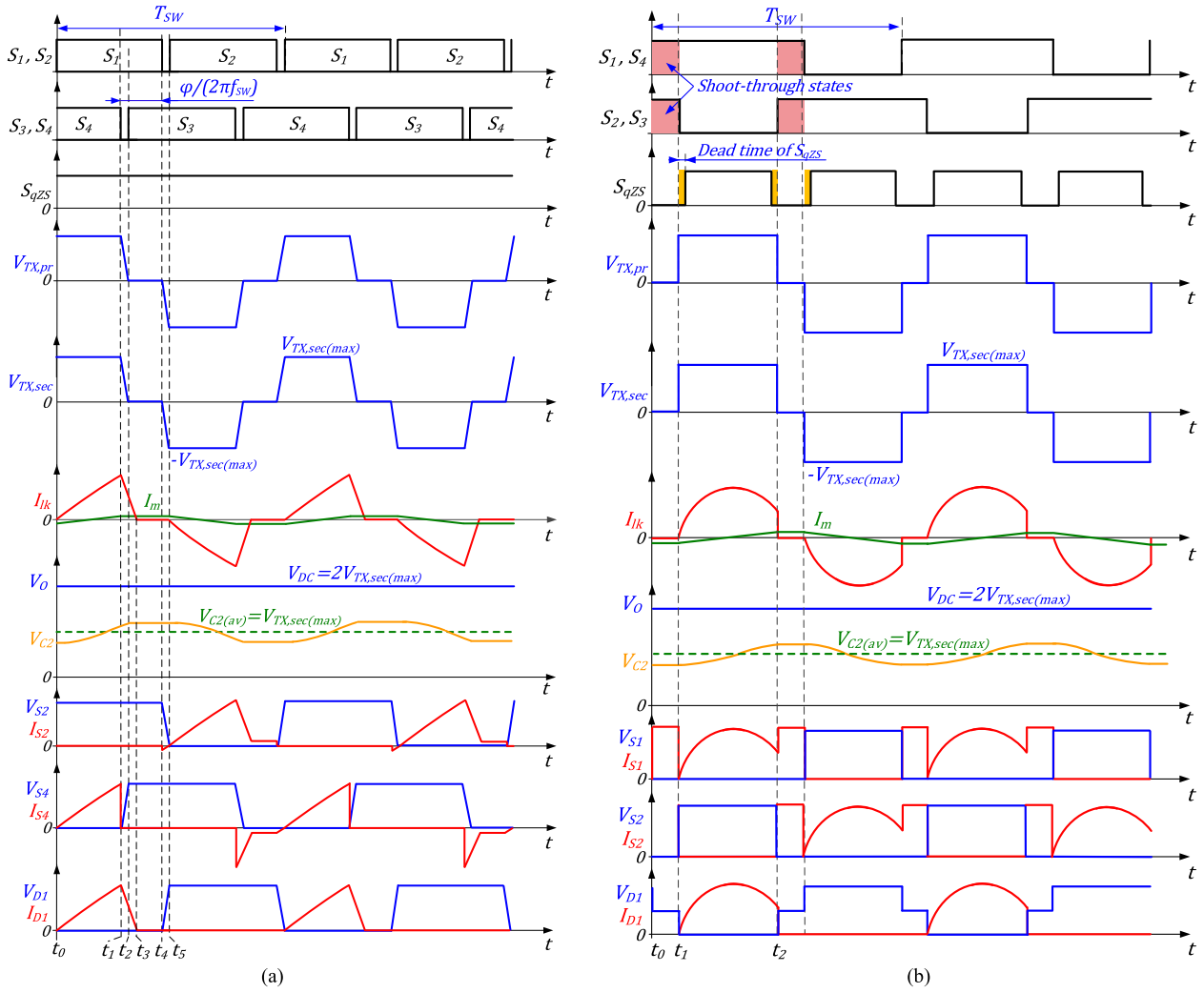

FIGURE 8. Operating waveforms of the qZS BBC (a) bucking mode and (b) boosting mode.

A. MAGNETICALLY INTEGRATED QZS NETWORK

The design of the coupled inductor relies on the current ripple passing through it, and the maximum ripple occurs in the boost mode at minimum input voltage and shoot-through duty cycle at its maximum level.

Assuming that the qZS network is symmetrical, see the equivalent circuit of the synchronous magnetically integrated shown in Fig. 11. Hence the leakage inductances are not considered in the design guidelines.

Due to high operation under high switching frequency, the parasitic inductance of interconnection wires between the input source and the converter (L_W) may affect the winding leakage inductance L_{lk1}, which affects the current ripples of the windings currents I_1 and I_2.

In order to avoid that difference in ripple, L_W has been considered in the design equations as follows [40]:

$$\Delta I_1 = \frac{V_{ST(min)}.L_{lk1}.D_{ST(max)}\left(1-D_{ST(max)}\right)}{f_{SW}\left(L_{lk1*}.L_{lk2}+L_{Mi}\left(L_{lk1*}+L_{lk1}\right)\right)\left(1-2.D_{ST(max)}\right)}, \tag{12}$$

$$\Delta I_2 = \frac{\Delta V_{(min)}.L_{lk2}.D_{ST(max)}\left(1-D_{ST(max)}\right)}{f_{SW}\left(L_{lk1*}.L_{lk2}+L_{Mi}\left(L_{lk1*}+L_{lk2}\right)\right)\left(1-2.D_{ST(max)}\right)}, \tag{13}$$

where L_{lk1*} is the effective leakage inductance of the input winging of the coupled inductor ($L_{lk1*} = L_{lk1}+L_W$), $\Delta V_{(min)}$ is the minimum input voltage value of the converter, and $D_{ST(max)}$ is the corresponding maximum shoot-through duty cycle.

Magnetizing inductance is much larger than the leakage inductances, even though taking into account the parasitic inductance for the interconnection wires. Therefore, the simplified equation for the magnetizing inductance can be indicated as [40]:

$$I_{LMi(max)} = \frac{2.P}{\Delta V_{(min)}} + \frac{\Delta V_{(min)}.D_{ST(max)}\left(1-D_{ST(max)}\right)}{2.L_{Mi}.f_{SW}\left(1-2.D_{ST(max)}\right)}. \tag{14}$$

The qZS capacitors are designed at the condition where the ripple of the (ΔV_{CqZS}) is at its highest value – in the boost

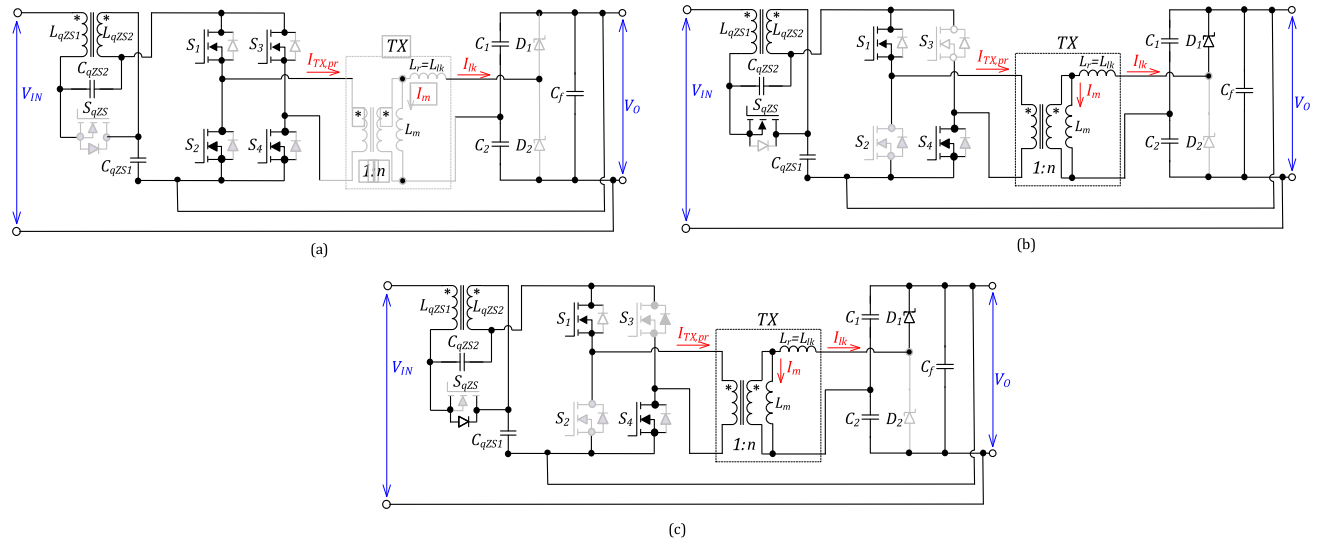

FIGURE 9. Generalized equivalent circuits of the QZSSR converter operating in the boost mode: (a) $t_0 < t < t_1$, (b) $t_1 < t < t_2$ and (c) during the dead-time of S_{qZS}.

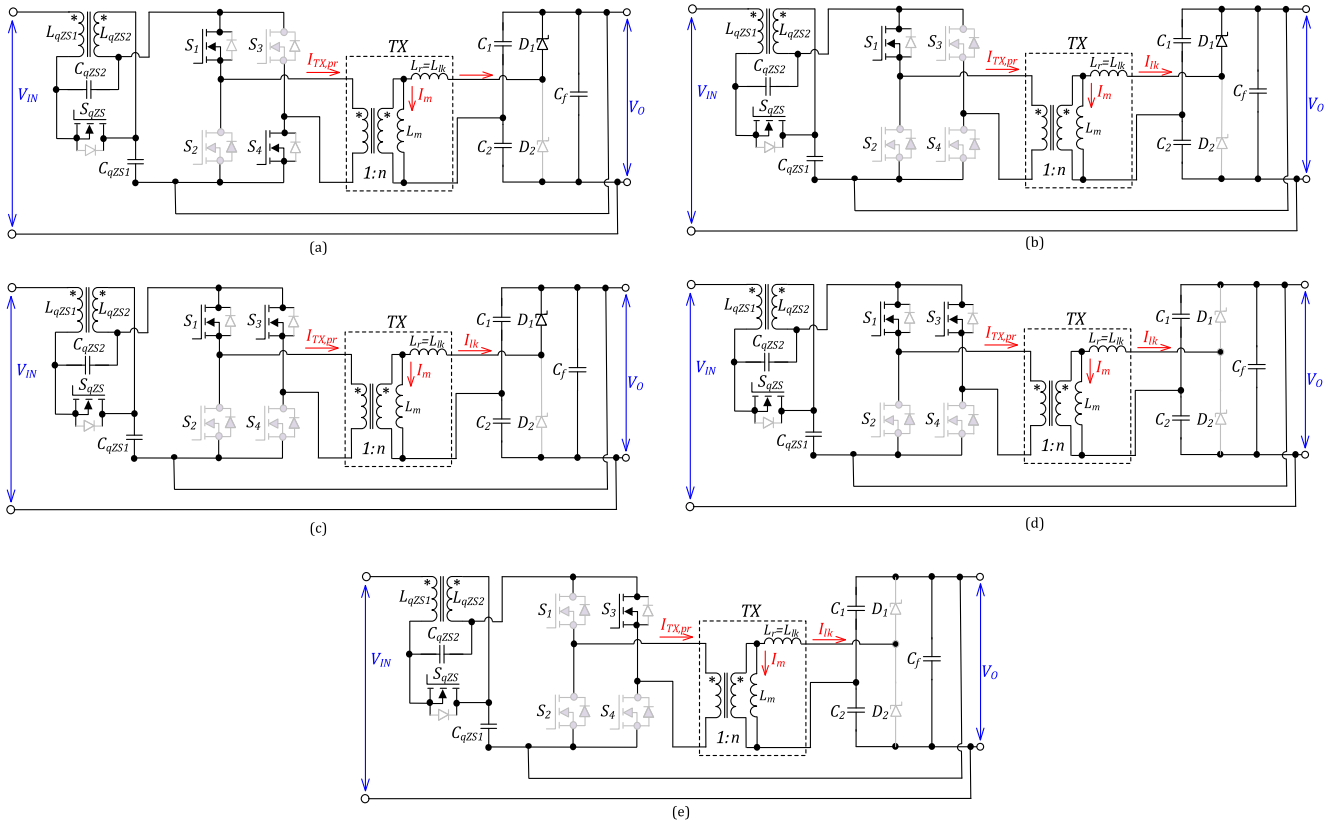

FIGURE 10. Generalized equivalent circuits of the QZSSR converter operating in the buck mode: (a) $t_0 < t < t_1$, (b) $t_1 < t < t_2$, (c) $t_2 < t < t_3$, (d) $t_3 < t < t_4$, and (e) $t_4 < t < t_5$.

mode at the minimum input voltage:

$$\Delta V_{CqZS} = \Delta V_{CqZS1} = \Delta V_{CqZS2} \approx \frac{P.D_{ST(max)}}{C_{qZS}.f_{SW}.\Delta V_{(min)}}, \tag{15}$$

where C_{qZS} is the capacitance of the qZS capacitors.

B. INTEGRATED SERIES RESONANT TANK

The integrated series resonant tank of the converter is composed of the parallel combinations of the VDR capacitors $(C_1 + C_2)$, and the isolation transformer leakage inductance referred to the secondary winding (L_{lk}). The inverter switches and VDR are operating at Zero Current Switching (ZCS),

due to the discontinuity of the current through the resonant network. Therefore, the critical value of the L_{lk} when the converter still maintains DCM could be given as:

$$L_{lk(cr,DCM)} < \frac{V_o^2}{8.\pi.P.f_{SW}} \tag{16}$$

Special attention should be given to the design of the leakage inductance L_{lk}, as the smaller values of L_{lk} will lead to higher currents through the isolation transformer, which results in increased current stresses of the semiconductors.

To maintain the resonance, the values of VDR capacitors could be selected by

$$C_1 = C_2 = \frac{1}{8.\pi^2.f_{sw}^2.L_{lk}} \tag{17}$$

C. TRANSFORMER DESIGN

The QZSSRC could operate in both voltage buck and boost modes. However, their utilization directly depends on the transformer turns ratio n. This paper utilizes two ways to design the given converter to provide to compare the performance of boost and buck-boost dc-dc converter topologies in the SIPO PPCs.

First, the transformer turns ratio could be selected to ensure that the proposed SIPO PPC operates in the boost mode from the minimum (Δv_{min}) to the maximum (Δv_{max}) series voltage values for a fixed load voltage V_L:

$$n_{boost} = \frac{V_o}{2\Delta v_{max}} \tag{18}$$

The other alternative would be to design the given converter to cover one-half of the voltage regulation range with the boost mode and the other half with the buck mode. Assuming $\Delta v_{min} \leq \Delta v_{max}/10$, the turns ratio could be selected as:

$$n_{buck-boost} = \frac{V_o}{4\Delta v_{max}} \tag{19}$$

The unique feature of the selected QZSSRC topology is that the same prototype could be used with two different transformers. This approach would provide a fair comparison between the performance of the boost and buck-boost dc-dc topologies in the SIPO PPCs.

V. EXPERIMENTAL RESULTS AND DISCUSSION

The proposed system has been tested in the laboratory to verify its operation and measured efficiency until 2 kW. A 300 W prototype, which is depicted in Figure 12, has been built based on parameters shown in Table 1.

This prototype was wired between two high voltage ports to form a SIPO configuration discussed in the previous sections. The load side voltage is stabilized at 350 V, while the input voltage of the PPP system varies to cover all the operating points of the converter.

The operating voltage range for the dc-dc converter is set to ensure $\Delta v_{max} = 60$ V. Therefore, two transformers were built on the RM14 core of 3C95 material: with turns ratios of $n = 3$ and $n = 5.6$. Both designs aimed to achieve the same maximum flux density in the transformer core.

For the transformer with $n = 5.6$, the dc-dc converter operates in the boost mode when the voltage applied to its input terminal varies from $\Delta v_{min} = 5$ V to 31V, normal mode

TABLE 1. Specifications of the Quasi Z-Source SIPO PPC.

Operating parameters		
Parameter	*Symbol*	*Range/Value*
Operating power range	P	0…300 W
Switching frequency	f_{SW}	100 kHz
Load voltage	V_L	350 V
Dc-dc input voltage range	Δv	5...60 V
Transformer turns ratio	$n_{buck\text{-}boost}$	5.6
	n_{boost}	3
Semiconductor components		
Component		*Part number*
$S_1 \ldots S_4$ and S_{qZS}		Fairchild FDMS86180
Rectifier diodes D_1 and D_2		Cree C3D02060E

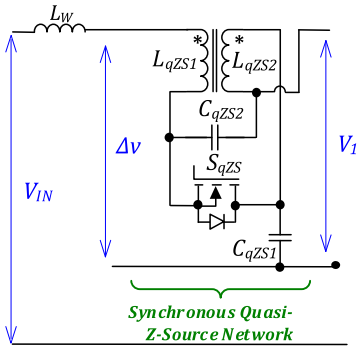

FIGURE 11. Equivalent circuit of the magnetically integrated qZS network.

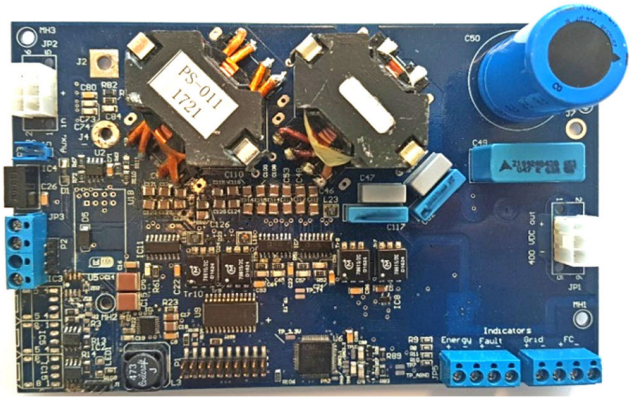

FIGURE 12. Hardware prototype for the SIPO Quasi Z-Source PPC.

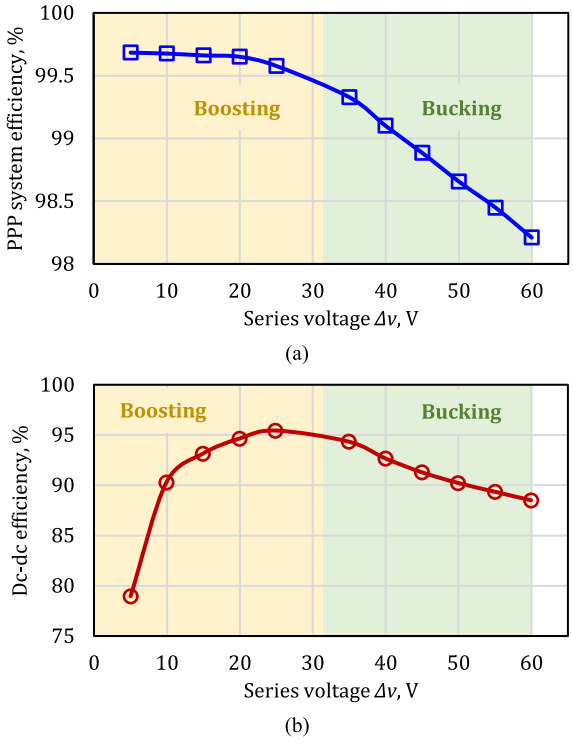

FIGURE 13. Efficiency of (a) PPP system and (b) buck-boost dc-dc converter at 1 A input current and fixed dc load voltage of 350 V.

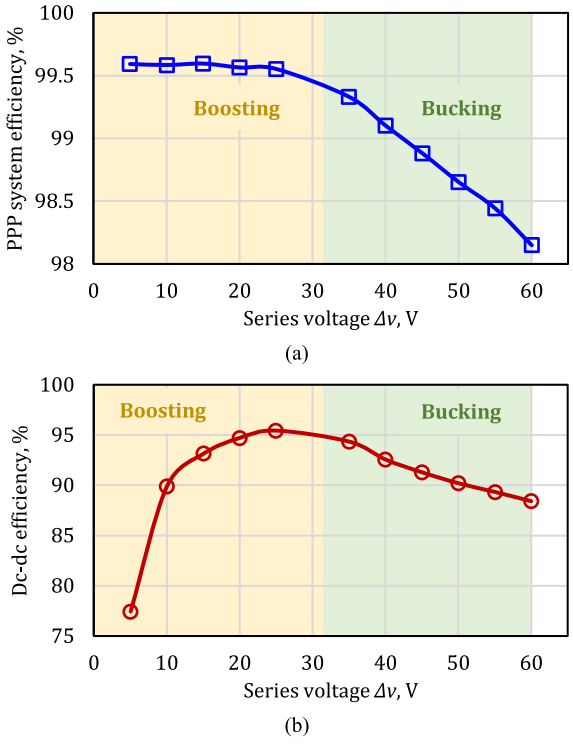

FIGURE 14. Efficiency of (a) PPP system and (b) buck-boost dc-dc converter at 2 A input current and fixed dc load voltage of 350 V.

at 31 V, and buck mode from 31 to 62 V. At each operating voltage the current is varied from 0 to 5 A. The load voltage is fixed at 350V for all operating points. The experimental efficiency was measured using a Yokogawa WT1800 power analyzer.

Figure. 13 represents a case study where the input current is fixed to 1A, and the input voltage of the PPP system is swept from 355V to 410 V. In the case of 355V at the input, the converter input terminal voltage is $\Delta v_{min} = 5$ V due to SIPO connection. With a transformer turns ratio of 5.6, the converter operates in the boost mode until the voltage across its terminal is lower than 31 V, and higher than this value the converter is operating in bucking mode. Figure. 13(a) is the overall PPP system efficiency, while Figure. 13(b) represents the dc-dc converter efficiency. Despite the relatively low efficiency of the converter, the overall system efficiency is higher than 99%. By having higher voltage across the dc-dc converter input, the converter will process higher power, which is an apparent reason for the reduction of overall system efficiency.

Different case studies with the input current of 2 A, 3 A, 4 A, and 5 A are shown in Figures 14 – 17, respectively. By increasing the input current, the overall efficiency is slightly decreased at the same partiality ratio; meanwhile, the dc-dc converter efficiency is improving slightly. For all case studies, the buck mode is used at partiality ratios above 8%, which could explain the relatively low efficiency of the dc-dc converter in the buck mode. In the buck mode, when the input voltage of the PPP system increases up to 410 V, i. e., the series voltage Δv reaches 60 V. Hence, the converter has to process higher powers at lower efficiency values, which results in the PPC minimum efficiency achieved at the maximum partiality, as could be expected. It varies from 98.1% at the current of 1 A to 97.9% at the current of 5 A, which shows small variations across the load power. The efficiency drop is caused by the relatively low dc-dc converter efficiency dropping from 89% to 86%.

These relatively low dc-dc converter efficiency values could be explained by the very pragmatic design of the dc-dc converter aiming at a low cost and use generic off-the-shelf components. As could be expected, the dc-dc converter achieves its maximum efficiency at around 30 V at the input. For all the load currents, the PPC efficiency stays over 99.5% for $\Delta < 30$ V owing to the good performance of the dc-dc converter at light loads in the boost mode as the normalized gain is limited to six by design.

In order to extend the boosting range of the converter, the used transformer has been replaced by another one with a turns ratio of $n = 2.9$. The primary purpose of this modification in turns ratio is to study the system performance when the dc-dc converter operates solely in the boost mode. As a result, the dc-dc converter operates at the minimum dc gain, i.e., minimum voltage boosting efforts and high efficiency, at higher K_{pr} values when it handles the maximum power. On the other hand, it has to operate at the normalized dc gain of over tenfold at $\Delta v_{min} = 5$ V.

It is worth mentioning that the PPP system based on the buck-boost converter shows almost no variations in the

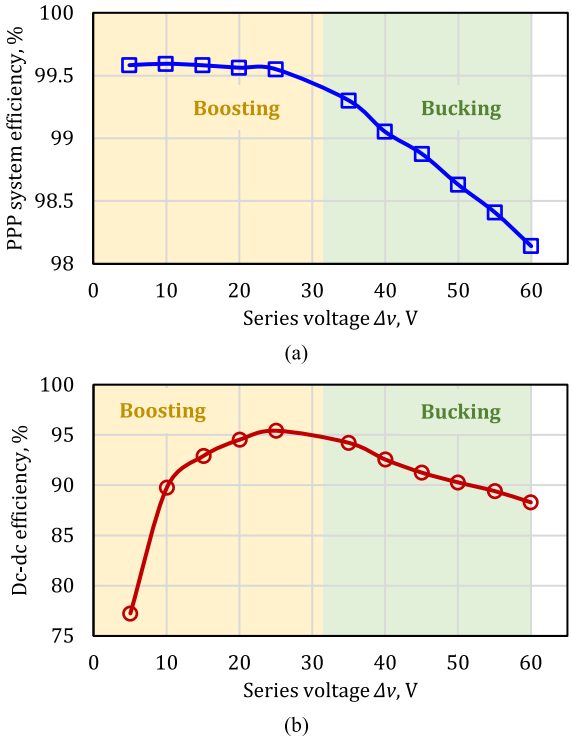

FIGURE 15. Efficiency of (a) PPP system and (b) buck-boost dc-dc converter at 3 A input current and fixed dc load voltage of 350 V.

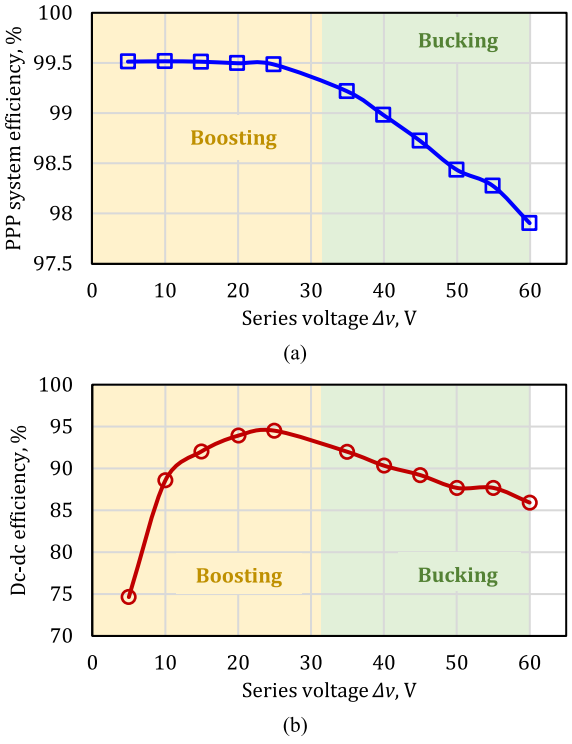

FIGURE 17. Efficiency of (a) PPP system and (b) buck-boost dc-dc converter at 5 A input current and fixed dc load voltage of 350 V.

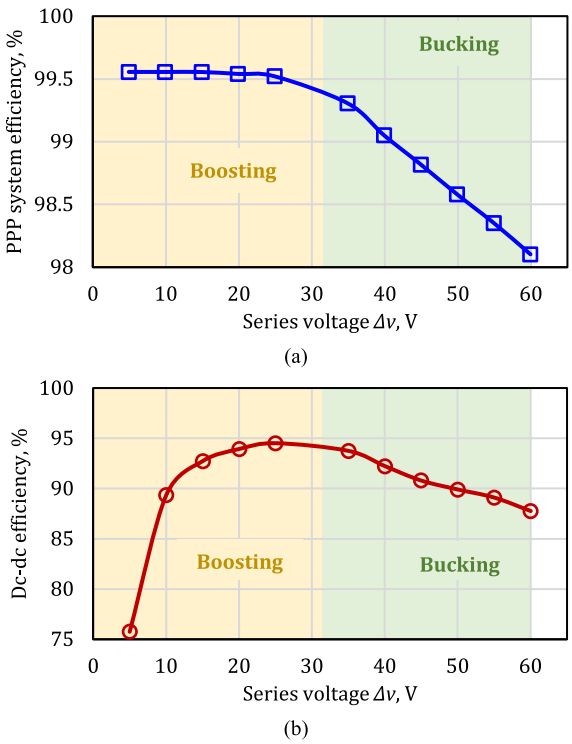

FIGURE 16. Efficiency of (a) PPP system and (b) buck-boost dc-dc converter at 4 A input current and fixed dc load voltage of 350 V.

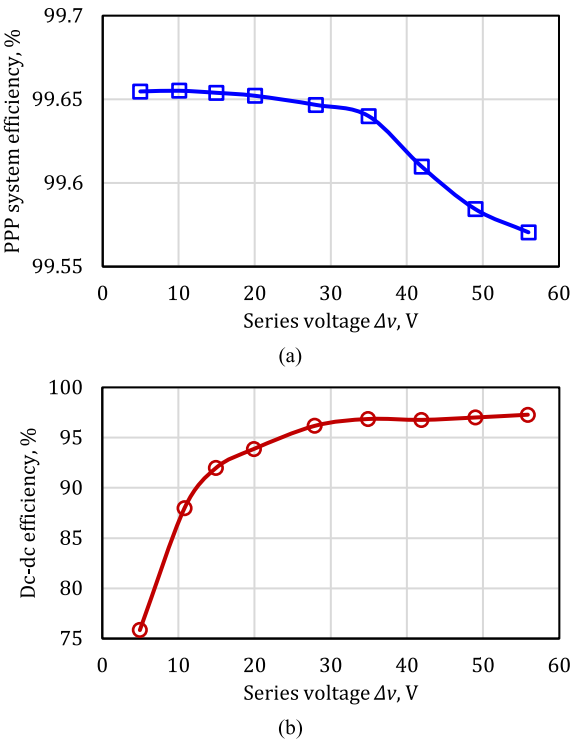

FIGURE 18. Efficiency of (a) PPP system and (b) boost dc-dc converter at 1 A input current and fixed dc load voltage of 350 V.

efficiency at series voltage value below 30 V, i.e., in the boost more of the dc-dc converter. This is caused by the dc-dc converter efficiency increasing with the power processed by the PPC.

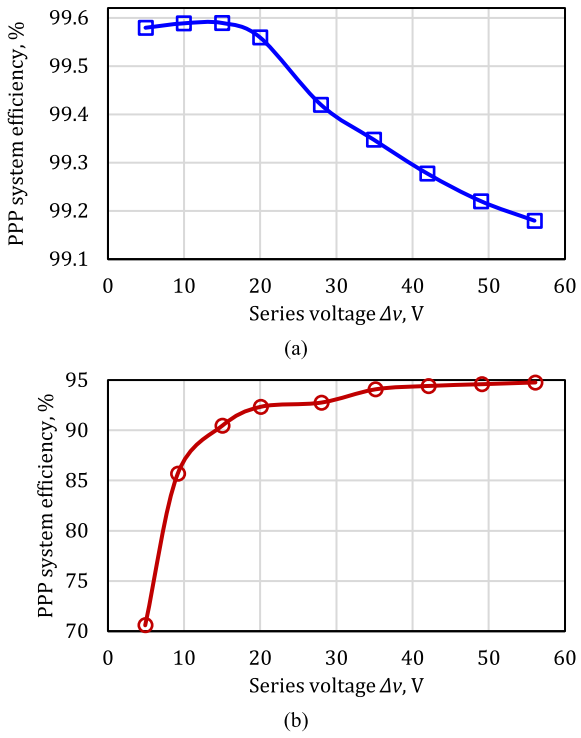

FIGURE 19. Efficiency of (a) PPP system and (b) boost dc-dc converter at 2 A input current and fixed dc load voltage of 350 V.

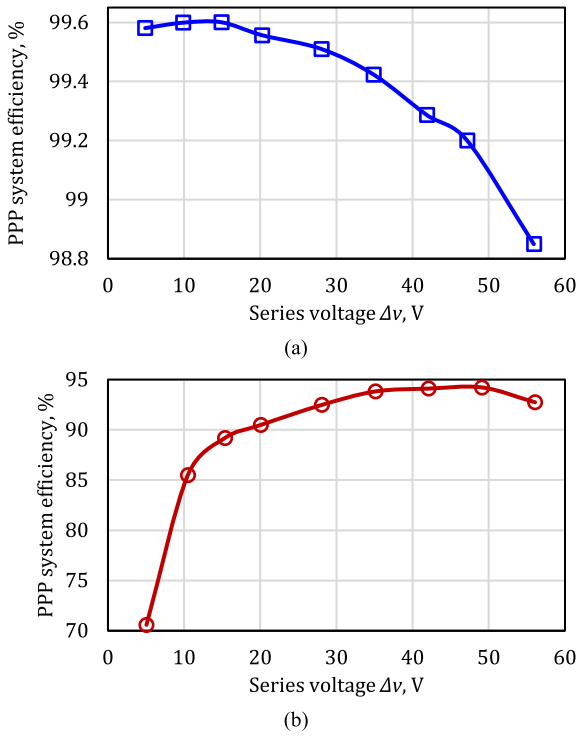

FIGURE 20. Efficiency of (a) PPP system and (b) boost dc-dc converter at 3 A input current and fixed dc load voltage of 350 V.

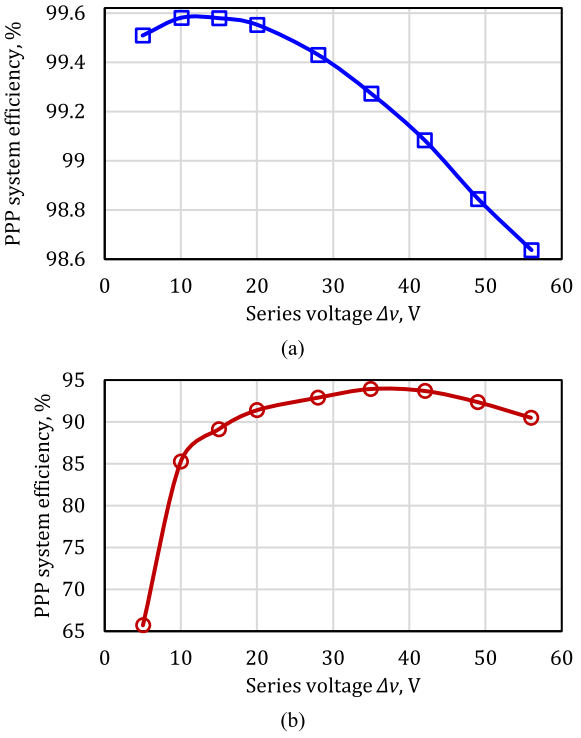

FIGURE 21. Efficiency of (a) PPP system and (b) boost dc-dc converter at 4 A input current and fixed dc load voltage of 350 V.

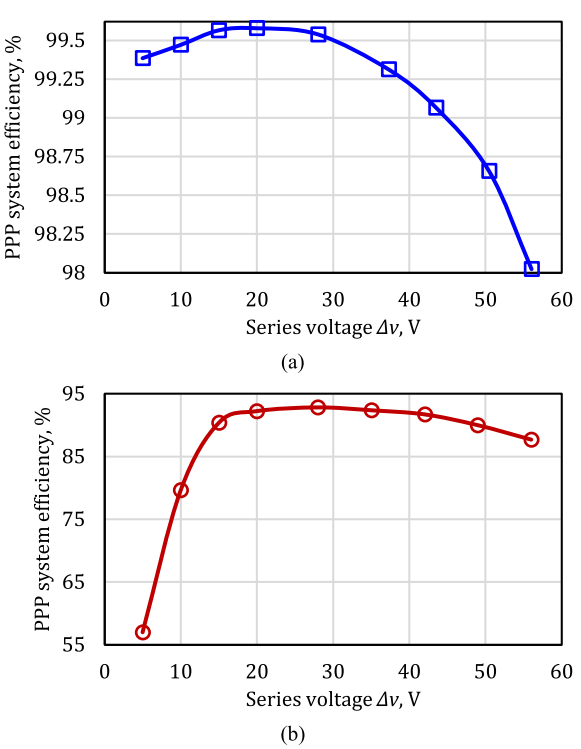

FIGURE 22. Efficiency of (a) PPP system and (b) boost dc-dc converter at 5 A input current and fixed dc load voltage of 350 V.

After replacing the transformer, the dc-dc converter is able to operate in the boost mode until 400 V at the input side of the PPP system. Similar to the buck-boost implementation, PPC with the boost dc-dc converter was studied for the input

currents of 1, 2, 3, 4, and 5 A, as shown in Figures 18-22, correspondingly. As could be expected, the boost implementation of the dc-dc converter results in its best performance achieved at the partiality ratios over 7%, i.e., series voltage $\Delta v > 25$ V. As it was predicted, the dc-dc converter performance at lower partialities is poor, resulting in efficiency as low as 57% due to the dc-dc converter operating at a normalized dc gain of over tenfold. However, those low efficiency values are achieved at very low power levels, resulting in the PPP system efficiency of over 99.4%. Compared to the buck-boost implementation of the dc-dc converter, the PPP system efficiency is reduced at $\Delta v < 30$ V. However, it is improved at higher partiality ratios. For example, at $\Delta v = 50$ V, the PPP system efficiency is improved by 0.2% at the maximum current of 5 A.

VI. CONCLUSION

Despite numerous research activities in the field of partial power processing, the series input parallel output partial power converters were underrepresented in literature. This could be associated with the relatively poor performance of the first demonstrated examples. However, this poor performance is mainly caused by the use of voltage-bucking galvanically isolated dc-dc topologies. As a result, the design of such a SIPO PPC becomes unpractical as it requires a very high transformer turns ratio to realize the required regulation range. In addition, it features low efficiency due to the very high voltage step-down requirements when operating at the maximum power, i.e., the maximum series voltage between a voltage source and a dc load.

This work compares two other possible dc-dc converter implementations – boost and buck-boost. By selecting the quasi-Z-source series resonant converter topology, it was possible to provide a fair comparison between the boost and buck-boost implementations as they differ only in transformer design and use the same other components in the experimental prototype.

The following conclusions could be drawn based on the existing literature and the obtained results. First, SIPO PPCs are beneficial in voltage step-down applications, where they can provide full efficiency of over 99%. Second, galvanically isolated buck dc-dc converter topologies are not recommended for implementation in SIPO PPCs. Third, galvanically isolated buck-boost dc-dc converter topologies provide good performance in SIPO PPCs in applications where a PPC operates mainly at low partiality ratios (below 10%). Fourth, galvanically isolated boost dc-dc converter topologies provide balanced performance in the entire regulations range as their efficiency increases with the power processed by a SIPO PPC. Hence, they could be recommended for implementation in SIPO PPCs in applications where PPC will operate mainly at partiality ratios above 10% or where its operation is equally probable in the entire regulation range.

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