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RESEARCH ARTICLE

Control Design and Fault Handling Performance of MMC for MMC-Based DC Distribution System

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ABSTRACT Modular multilevel converters (MMCs) have emerged as a viable choice in future DC grid architectures due to their scalability to meet voltage level requirements. However, MMC-based DC distribution systems are at risk of short-term outages during the faults in either the DC or AC networks feeding the MMC, so it remains a challenge to accomplish AC and DC fault ride-through (FRT) capability in such applications. To ensure stable operations of the DC terminals, FRT strategies are required for the faults on both the AC and DC sides of the converter. This paper proposes a FRT strategy for the AC and DC side of the converter to ensure stable and economically viable operation of the DC distribution network. The asymmetrical faults in the upstream AC grids are managed by using the integrated energy of the MMC. Whereas, the DC FRT capability of the MMC is accomplished by changing the redundant submodules of the MMC to full-bridge submodules (FBSMs), thus allowing a DC FRT to be achieved by using DC circuit breakers that are low cost and reduced in size. Applying the proposed DC FRT strategy, which makes possible the use of low-cost and reduced in size DC circuit breakers in DC distribution, results in a reduction in the overall initial investments.

INDEX TERMS Modular multilevel converter, DC FRT, asymmetrical fault in AC grid, DC faults.

I. INTRODUCTION

There are many advantages of DC power distribution networks over AC power distribution networks, especially in terms of power supply capacity, reliability, controllability, and power quality [1]. DC distribution networks have the advantage of reducing line losses and do not require additional reactive power compensation. Voltage source converters (VSC) are among the best candidates for building DC distribution grids, owing to their ability to control the characteristic parameters of the grid, i.e. phase-angle and frequency of the AC voltage. VSCs controlled with pulse

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width modulation can decrease harmonic content and offer faster response times [2], [3], [4]. Due to high change in current and absence of zero DC current during the DC fault, fault control and regulation of the DC distribution systems becomes a serious problem using VSCs in distribution grids [5]. DC faults and their safe handling have remained one of the most challenging aspects of the VSC-based DC distribution system [6], [7]. A solution is urgently needed if DC grids are to be implemented. Many of these shortcomings of conventional VSC topologies have been addressed by modular multilevel converters (MMCs). MMCs are first introduced in [8] as a well-established technology. Implementing this technology in HVDC system includes several benefits i.e. voltage modularity, enhanced reliability, low switching

losses, reconfigurable design and better efficiency [9], [10], [11], [12]. It produces a lower level of harmonics, thus it needs smaller AC grid filters. MMCs can be designed for several hundred different voltage levels for industrial motors, electric railways and high voltage DC transmission systems [13], [14]. MMC converters have some of the basic issues including circulating current, semiconductor power losses, and current harmonics but different efficient controllers have been designed to overcome these issues efficiently. Several types of MMC topologies have been designed to enhance the efficiency of the converter. Academic and industrial studies have been conducted on MMCs, and several solutions have been proposed regarding their control scheme and operation characteristics [15]. Half-bridge MMC plays a dominant role in MMC-based DC distribution systems currently due to its low cost and low power loss. In the event of a DC fault, however, half-bridge MMC cannot clear the fault current due to the free-wheeling diodes.

It blocks all its IGBTs when there is a DC fault to protect MMC from any damage, but the DC fault current still flows through its anti-parallel free-wheeling diodes. The fault current that flows through it is similar to a 3-phase short circuit fault in the upstream AC grid. The fault current could be large enough to harm the MMC or shut down the entire DC distribution system. In order to handle DC faults, three possible strategies can be employed as follows:

- When DC circuit breakers aren't available, the DC fault can be isolated by opening AC circuit breakers placed on the AC grid side of the MMC. If the DC fault position is located, the associated AC circuit breakers open located on the AC grid side of the MMC and then selectively open the DC dis-connectors to isolate the faulty area and restore the rest of the DC distribution system [17]. It is a simple, economic, and reliable method, but the AC circuit breakers have slow operation characteristics. During the operation period of the AC circuit breakers, fault currents flow through the semiconductor devices of the converter due to the slow operating characteristics of AC circuit breakers (ACCBs), which require high ratings of the semiconductor devices for converters. Consequently, there will be a shut down of the system for a long period.
- In recent years, several designs have been proposed for fault-tolerant converters that suppress DC fault current. The design of the fault-tolerant device has needed more semiconductor devices than that of an HB-MMC, therefore, power losses and capital expenses are higher [18], [19]. The FBSM-MMC has the potential to generate the negative or reverse voltage during the fault when all of its IGBTs are blocked and can produce bipolar DC voltage regardless of the arm current direction, but this device has twice as many power semiconductors and suffers from twice as much power loss as a conventional HB-MMC [20]. A fault-tolerant hybrid MMC combining HBSMs and FBSMs which enables DC fault-ride through capability while reducing capital costs is also

proposed in the literature. The DC fault-ride through capability of the hybrid MMCs is mainly achieved by using effective controllability of the full-bridge submodule, but it might shut down the DC systems for a short period during the fault condition. In a hybrid MMC topology, each lower arm contains only a single full bridge submodule (FBSM), as in [21] proposed a solution for handling complete converter fault currents. The fault current is isolated with a fault-tolerant converter without using DC circuit breakers, but the system is shut down for a short period.

- DC circuit breaker plays a significant role to isolate selectively and abruptly the faulty areas from the rest of the healthy DC distribution system [22]. However, it faces great challenges since there is no natural zero-crossing current. The low impedance of DC distribution lines contributes to a rapid increase in DC fault currents during DC bipolar faults. Therefore, DC circuit breakers can be evaluated based on speed, maximum interruption capacity and investment made [23]. The recovery process of the DC circuit breakers is lengthy which is not favorable for the distribution system. It is noteworthy that the use of hybrid DC circuit breakers may be an effective way to handle DC fault currents, but the investment is still quite high.

In the event of DC short circuit faults on an MMC-based DC distribution system, the above-mentioned strategies have shortcomings i.e. the traditional AC circuit breakers are slow in response, and during its operation, the free-wheeling diodes of MMC need to be rated for full prospective short circuit current [24]. Moreover, it requires a long time to recover the system, and no active and reactive power is exchanged [25]. Although DC circuit breakers including mechanical, solid-state, and hybrid CBs might be used to mitigate the aforementioned issues, they present the following drawbacks. The mechanical DC circuit breakers are slow in response and their inrush current may damage the semiconductor devices [26]. Solid-state DC circuit breakers are fast to respond to the DC faults, but they might significantly increase the on-state power losses of their semiconductors. The hybrid DC circuit breakers are operating with the minimum power loss under normal operation but for large transmission systems, they would importantly increase the footprint and overall cost of the application [27]. Furthermore, hybrid DC circuit breakers have complex control and coordination with MMC. A recent research focus has been given to fault-tolerant MMC deriving from modifying its submodules to handle DC fault currents [28], [29]. Another potential solution is to use fault-tolerant (hybrid) MMCs which employ both the HBSM and FBSM submodules with the potential to generate reverse voltage using the FBSMs type to overcome the DC fault current rapidly. Different fault tolerant MMC control the AC current while riding through DC faults working as wave-shaping circuits. Fault-tolerant FB-MMC uses FBSMs to generate the reverse voltages to clear the DC faults but

TABLE 1. Pros and cons of different fault tolerant MMCs [16].

MMC Configuration	Half bridge MMC	Hybrid design I MMC	Hybrid design II MMC	Hybrid design III MMC	Hybrid design IV MMC	Hybrid design V MMC
Submodule circuit	HBSM	HBSM+FBSM	HBSM+CDSM	HBSM+UFBSM	HBSM+3LCCSM	HBSM+5LCCSM
Fault handling capability	No	Yes	Yes	Yes	Yes	Yes
Semiconductors required	Less	More	More	More	More	More
Cost	Low cost	Expensive	Expensive	Expensive	Expensive	Expensive
Estimated power loss	0.69%	0.798%	0.798%	0.798%	0.798%	0.798%

the power losses and cost of the FB-MMC are higher than those of HB-MMC due to the higher number of components which compromises its overall efficiency. It is needed that an MMC could be designed to have low cost, minimum power losses, and provide both DC and AC fault handling capabilities. Recently researchers have designed different types of fault-tolerant MMC topologies. The estimated power loss of different hybrid designed fault tolerant converters including (HBSM+FBSM), (HBSM+CDSM), (HBSM+UFBSM), (HBSM+5LCCSM), and (HBSM+3LCCSM) are 0.798% while the estimated power loss of half-bridge MMC is about 0.69 % [16], [30]. Thus, it is necessary to design the MMC in order to achieve the best combination of fault handling capability, efficiency, cost and to offer both AC and DC fault handling capabilities. In this paper HBSMs-based MMC is designed in conjunction with the DC circuit breaker to accomplish economically viable operation and respond quickly to the system during the pole-to-pole and pole-to-ground DC faults. MMCs are designed with redundant submodules to avoid unnecessary shut down upon the failure of its submodules. Redundant SMs act as an idle component during normal operation but it participates when a fault occurs at an operating submodule. Our proposed MMC has 50 half-bridge submodules in each arm and the redundancy ratio is kept at 10%, in which the redundant submodules are based on full-bridge structures in order to allow the MMC to handle the DC fault current during DC faults. 10% redundancy means 10% of 50 half-bridge submodules of each arm that is 5 submodules which are kept redundant because keeping more than five submodule redundant can increase the cost and footprint of MMC while less than five redundant submodule can increase the risk factor in case of failure of more than one submodule simultaneously. The minimum redundancy for proposed MMC can be one submodule or 2% redundancy, which means 2% of 50 half-bridge submodules is one redundant submodule. In normal operation, the redundant SMs are bypassed and only the HB is working, but in fault scenarios when fault current is detected, the control system inserts all the redundant FBMSs to generate the reverse voltage to overcome the DC fault current. Once the fault is cleared FBSMs are bypassed again. Therefore, the power loss of the converter during the normal operation is comparable to MMC using only HBSM.

A. CONTRIBUTIONS

The contribution of this paper is as follows:

- The proposed optimal design of a fault-tolerant MMC achieves the best combination of fault handling capability, low cost, low power losses similar to HB-MMC, and effectively handling DC and AC faults.
- We implemented the DC FRT control strategy and validated it for both pole-to-pole and pole-to-ground DC faults, analyzing not only the fault current limiting capability but also the performance of the converter during fault conditions.

B. ORGANIZATION

This article continues as follows: Detailed system of the designed modular multilevel converter is explained in Section II of the paper. Mathematical modeling of the detail control system including circulating current suppression controller (CCSC), operational characteristics of MMC including DC fault analysis of the MMC before blocking state, after blocking state, AC, and DC voltage controllers are described in section III. Section IV explains the DC fault management of the HB-MMC, the operating principle of the redundant full-bridge submodules, and the DC FRT strategy of the designed MMC. Section V compares the simulation results for interruption performance of the designed and conventional MMC during a fault on a DC terminal and also analyzes AC grid voltage transient and its impacts during the re-closing period in detail. The AC FRT analysis of the designed MMC is also explained with validated simulation results. The conclusion of the research article is presented in Section VI.

II. SYSTEM DESCRIPTION

An MMC is interfaced between upstream 132 kV AC grid system and downstream DC distribution network to convert power and ensure efficient power supply to DC distribution network is illustrated in Figure 1. The MMC topology employed in this paper consists of 50 half-bridge submodules (HBSMs) in each upper and lower arm. The HBSMs have lower semi-conductors power losses and better operational performance but they are not able to block the fault current. In case of a DC fault, however, half-bridge MMC cannot clear the fault current due to the free-wheeling diodes. It blocks all its IGBTs when there is a DC fault to protect MMC from

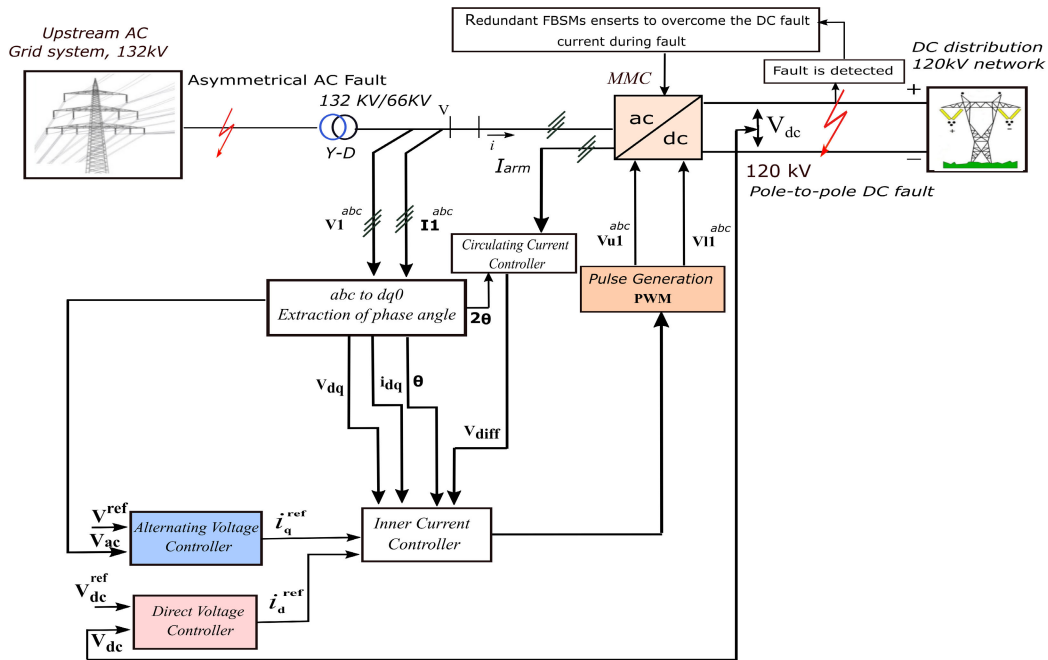


FIGURE 1. Control system model of the designed MMC for DC distribution networks.

any damage, but the DC fault current still flows through its anti-parallel free-wheeling diodes. so the MMC topology is employed to handle fault current efficiently. The redundancy ratio of the converter is 10%, and all the 10% redundant submodules are changed into full-bridge submodules. DC FRT strategy is implemented to limit the fault current by inserting the redundant FBSMs in series with the HBSMs to generate the reverse or the negative voltages. This limits the fault current and reduces the stress on DC circuit breakers while interrupting the fault current economically and efficiently. The simulation studies prove the feasibility and efficiency of the designed MMC and the FRT strategy mapped out to handle the DC fault current. Characteristic parameters of the modular multilevel converter. i.e. arm inductance of MMC, the number of submodules per arm, dimensioning, and sizing of the submodule’s capacitance are illustrated in table 2. The equivalent circuit of MMC is depicted in Figure 2. The architecture of the hybrid MMC topology has three-phase legs and each phase leg has 50 submodules in each the upper and lower arm. A power transformer, core type (Y-D), having a voltage ratio of 132 kV/66 kV is linked between the overlaying 132 kV AC grid and MMC. Y-D transformer is capable to limits the zero sequence current during AC faults. The main purpose of designing MMC and its control is to limit the fault current economically in either case. i.e. pole to pole or pole to ground DC faults.

Moreover, an aggregate model of the MMC is used for analytical reasons, accuracy, and efficiency to increase the performance of the analysis and reproduce the dynamic behavior of the converter. Figure 2 shows the equivalent model of the MMC for mathematical modeling of

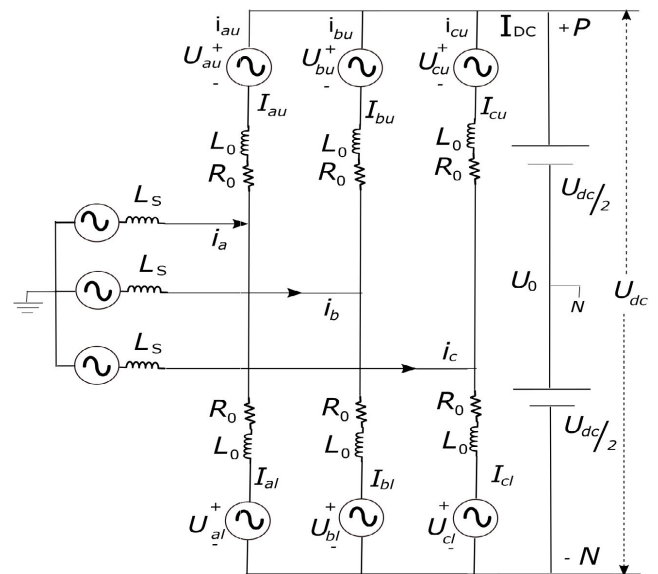


FIGURE 2. Equivalent circuit of 3-phase MMC.

system-level. The equivalent circuit of MMC illustrates that; I_{au}, I_{bu}, I_{cu} and I_{al}, I_{bl}, I_{cl} are the upper and lower arm currents whereas U_{au}, U_{bu} and U_{cu} and U_{al}, U_{bl}, U_{cl} are upper and lower arm voltages of MMC. The phase currents of the MMC

$$[I_a \ I_b \ I_c]^T = [I_{au} \ I_{bu} \ I_{cu}]^T + [I_{al} \ I_{bl} \ I_{cl}]^T \quad (1)$$

$I_{a,diff}, I_{b,diff}$ and $I_{c,diff}$ are the differential arm currents of each phase given by

$$[I_{a,diff} \ I_{b,diff} \ I_{c,diff}]^T = \frac{[I_{au} \ I_{bu} \ I_{cu}]^T - [I_{al} \ I_{bl} \ I_{cl}]^T}{2} \quad (2)$$

the following equations illustrate the difference between the upper arm and lower arm currents in the phase leg of MMC

$$[I_{au} \ I_{bu} \ I_{cu}]^T = \frac{1}{2}[I_a \ I_b \ I_c]^T + [I_{a,diff} \ I_{b,diff} \ I_{c,diff}]^T \quad (3)$$

$$[I_{al} \ I_{bl} \ I_{cl}]^T = \frac{1}{2}[I_a \ I_b \ I_c]^T - [i_{a,diff} \ i_{b,diff} \ i_{c,diff}]^T \quad (4)$$

the phase voltages U_a , U_b and U_c of the MMC are illustrated in the following equations

$$\begin{bmatrix} u_a \\ u_b \\ u_c \end{bmatrix} - \begin{bmatrix} u_0 + \frac{u_{dc}}{2} - u_{au} \\ u_0 + \frac{u_{dc}}{2} - u_{bu} \\ u_0 + \frac{u_{dc}}{2} - u_{cu} \end{bmatrix} = 2L \frac{d}{dt} \begin{bmatrix} i_{au} \\ i_{bu} \\ i_{cu} \end{bmatrix} + 2R \begin{bmatrix} i_{au} \\ i_{bu} \\ i_{cu} \end{bmatrix} \quad (5)$$

$$\begin{bmatrix} u_a \\ u_b \\ u_c \end{bmatrix} - \begin{bmatrix} u_0 - \frac{u_{dc}}{2} + u_{al} \\ u_0 - \frac{u_{dc}}{2} + u_{bl} \\ u_0 - \frac{u_{dc}}{2} + u_{cl} \end{bmatrix} = 2L \frac{d}{dt} \begin{bmatrix} i_{al} \\ i_{bl} \\ i_{cl} \end{bmatrix} + 2R \begin{bmatrix} i_{al} \\ i_{bl} \\ i_{cl} \end{bmatrix} \quad (6)$$

where the DC voltage i.e. u_{dc} is between the two DC poles and voltage u_0 is actually between the ground and two neutral points. Adding equations (5) to (6) gives

$$\begin{bmatrix} u_a \\ u_b \\ u_c \end{bmatrix} - \begin{bmatrix} u_0 + \frac{u_{an} - u_{au}}{2} \\ u_0 + \frac{u_{bn} - u_{bu}}{2} \\ u_0 + \frac{u_{cn} - u_{cu}}{2} \end{bmatrix} = L \frac{d}{dt} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} + R \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \quad (7)$$

Let

$$\begin{bmatrix} u'_a \\ u'_b \\ u'_c \end{bmatrix} = \begin{bmatrix} \frac{u_{an} - u_{au}}{2} \\ \frac{u_{bn} - u_{bu}}{2} \\ \frac{u_{cn} - u_{cu}}{2} \end{bmatrix}$$

$$\begin{bmatrix} u_a \\ u_b \\ u_c \end{bmatrix} - \begin{bmatrix} u_0 + u'_a \\ u_0 + u'_b \\ u_0 + u'_c \end{bmatrix} = L \frac{d}{dt} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} + R \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \quad (8)$$

Equation (8) mathematically illustrates the AC side of the converter. In the following sections, we design controllers based on this model.

III. CONTROL DESCRIPTION AND MODELLING

A control system has been designed to accomplish the objective and respond quickly to the system during a fault in the DC distribution system. DSRF is used to control the inner and outer current control loops designed for MMC. Outer

control loops have been designed for a converter that contains DC voltage and AC voltage control loops. Differential currents due to the floating nature of SMs's capacitors and load dis-balance among three-phase legs of MMC cause an increase in the arm current and system losses. A circulating current suppression controller is mapped out for MMC to suppress the differential currents. In addition, this section describes the control loops including the inner current control loop (ICCL) and outer voltage control loops (OVCLs) of the converter in detail.

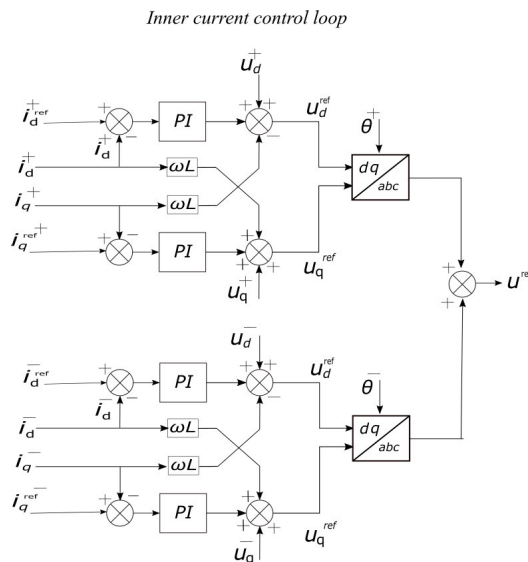


FIGURE 3. The inner current control loop (ICCL) of a modular multilevel converter.

A. INNER CURRENT CONTROLLER MMC

The inner current control loop plays a significant role in the main control process of the MMC. The inner current control loop operates with the previous loops that are the d-axis and q-axis current. It also accepts external references from the outer loops i.e. the control for suppressing circulating currents is illustrated in Figure 6. The AC grid during an asymmetrical fault, shown in Figure 1, becomes unbalanced. Under the unbalanced conditions circulating current consists of +ve, -ve, and zero sequence components can be controlled independently. They can be separated into three independent systems according to equation (8)

$$u_{ABC}^+(t) - u_{ABC}^+(t) = L \frac{d}{dt} i_{ABC}^+ + R i_{ABC}^+ \quad (9)$$

$$u_{ABC}^-(t) - u_{ABC}^-(t) = L \frac{d}{dt} i_{ABC}^- + R i_{ABC}^- \quad (10)$$

$$u^0(t) - (u^0(t) + v_0(t)) = L \frac{d}{dt} i_{ABC}^0 + R i_{ABC}^0 \quad (11)$$

In a dq^+ and dq^- frame, Equations 9 and 10 become

$$\frac{d}{dt} \begin{bmatrix} i_d^+ \\ i_q^+ \end{bmatrix} = \begin{bmatrix} -\frac{R}{L} & w \\ -w & -\frac{R}{L} \end{bmatrix} \begin{bmatrix} i_d^+ \\ i_q^+ \end{bmatrix} - \frac{1}{L} \begin{bmatrix} u_d^+ \\ u_q^+ \end{bmatrix} + \frac{1}{L} \begin{bmatrix} u_d^+ \\ u_q^+ \end{bmatrix} \quad (12)$$

$$\frac{d}{dt} \begin{bmatrix} i_d^- \\ i_q^- \end{bmatrix} = \begin{bmatrix} -\frac{R}{L} & -w \\ w & -\frac{R}{L} \end{bmatrix} \begin{bmatrix} i_d^- \\ i_q^- \end{bmatrix} - \frac{1}{L} \begin{bmatrix} u_d^- \\ u_q^- \end{bmatrix} + \frac{1}{L} \begin{bmatrix} u_d^- \\ u_q^- \end{bmatrix} \quad (13)$$

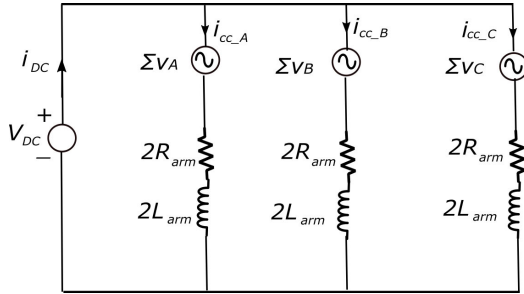


FIGURE 4. Equivalent circuit of 3-phase MMC.

B. CIRCULATING CURRENT CONTROL OF MODULAR MULTILEVEL CONVERTER

The MMC has a specific structure made up of two arms, each of them containing several number of submodules. The converter’s submodule has a floating capacitor due to its charging and discharging processes, which result in low-frequency fluctuations in its voltage. In the end, these low-frequency fluctuation appears as prevalent second harmonic voltages in the arm voltage $\sum v$ of the converter [23]. Circulating current increases the arm current which causes to increase in the power loss. The equivalent circuit of MMC is illustrated in Figure 4. The following equations can be used to describe the dynamics of circulating current in MMC

$$V_{dc} = \sum v + 2i_{cc} \cdot R_{arm} + 2L_{arm} \frac{di_{cc}}{dt} \quad (14)$$

$$V_{dc} = v_{upper} + v_{lower} + 2i_{cc} \cdot R_{arm} + 2L_{arm} \frac{di_{cc}}{dt} \quad (15)$$

The main variable that controls the circulating current of the MMC is $(v_{upper} + v_{lower})$. By splitting the term $\sum V$ into circulating current driving term V_{cc} and DC-link voltage

$$V_{dc} = 2V_{cc} + v_{upper} + v_{lower} \quad (16)$$

$$V_{dc} - 2V_{cc} = v_{upper} + v_{lower} \quad (17)$$

$$V_{dc} = V_{dc} - 2V_{cc} + 2R_{arm} \cdot i_{cc} + 2L_{arm} \frac{di_{cc}}{dt} \quad (18)$$

$$V_{cc} = i_{cc} \cdot R_{arm} + L_{arm} \frac{di_{cc}}{dt} \quad (19)$$

The time-domain dynamics of the modular multilevel converter is

$$V_{cc_a} = i_{cc_a} \cdot R_{arm} + L_{arm} \frac{di_{cc_a}}{dt} \quad (20)$$

$$V_{cc_b} = i_{cc_b} \cdot R_{arm} + L_{arm} \frac{di_{cc_b}}{dt} \quad (21)$$

$$V_{cc_c} = i_{cc_c} \cdot R_{arm} + L_{arm} \frac{di_{cc_c}}{dt} \quad (22)$$

Second harmonics control in the circulating current (CS) can be formalized in the following equations

$$i_{cc_a} = \frac{1}{3}I_{dc} + I_{cc} \cos(2\omega t + \theta) \quad (23)$$

$$i_{cc_b} = \frac{1}{3}I_{dc} + I_{cc} \cos(2\omega t + \theta - \frac{2\pi}{3}) \quad (24)$$

$$i_{cc_c} = \frac{1}{3}I_{dc} + I_{cc} \cos(2\omega t + \theta - \frac{4\pi}{3}) \quad (25)$$

$$i_{cc_a} + i_{cc_b} + i_{cc_c} = 0 \quad (26)$$

In an analysis of the circulating current, CCS control, the DC terms are ignored.

$$\vec{I}_{cc} = I_{cc} e^{j(-2\omega t + \theta)} \quad (27)$$

A vector control method is applied to control the second harmonics of the circulating current. The second harmonic is a negative sequence component therefore current is controlled with -2ω in the dq rotating frame. The equations for V_{cc_a} , V_{cc_b} and V_{cc_c} are transformed using rotating vectors into $\alpha\beta$ -frame

$$\vec{V}_{cc} = I_{cc} R_{arm} e^{j(-2\omega t + \theta)} + L_{arm} \frac{d(I_{cc} e^{j(-2\omega t + \theta)})}{dt} \quad (28)$$

Upon converting $\alpha\beta$ -frames into dq-frames

$$e^{-j\theta} \cdot \vec{V}_{cc} = e^{-j\theta} \cdot I_{cc} R_{arm} e^{j(-2\omega t + \theta)} + e^{-j\theta} \cdot L_{arm} \frac{d(I_{cc} e^{j(-2\omega t + \theta)})}{dt} \quad (29)$$

$$\vec{V}_{cc,dq} = I_{cc} R_{arm} \cdot e^{j\theta} + L_{arm} \frac{d(I_{cc} \cdot e^{j\theta})}{dt} - 2j\omega L_{arm} \cdot e^{j\theta} \quad (30)$$

$$\begin{bmatrix} V_{cc-d} \\ V_{cc-q} \end{bmatrix} = R_{arm} \begin{bmatrix} I_{cc-d} \\ I_{cc-q} \end{bmatrix} + L_{arm} \frac{d}{dt} \begin{bmatrix} I_{cc-d} \\ I_{cc-q} \end{bmatrix} + \begin{bmatrix} 2L_{arm}\omega i_{cc-q} \\ -2L_{arm}\omega i_{cc-p} \end{bmatrix} \quad (31)$$

Using equation 31, the circulating current controller has been constructed for MMC illustrated in Figure 5. The current is controlled with zero control voltages when the references are set to zero during steady-state operation. This controller reduces the submodule voltage ripples, improves arm current quality with lower harmonics, and limits the peak value of the arm current reducing the stress on submodule components such as IGBT, transistor, diodes, and reducing the power loss in semiconductors of the MMC.

C. OUTER CURRENT CONTROLLERS FOR MMC

This section focuses on the design of the AC and DC network voltages controllers. When the overlaying AC grid is under an unbalanced condition the AC voltage controller will support the AC grid by injecting reactive power and the MMC consumes negative reactive power. Essentially, this implies that the MMC consumes reactive power when it receives a command from the control system. Figure 6 illustrates that the outer loop of DC voltage control is designed to control the DC output voltage of the modular multilevel converter. It is accomplished by comparing the reference DC voltage to

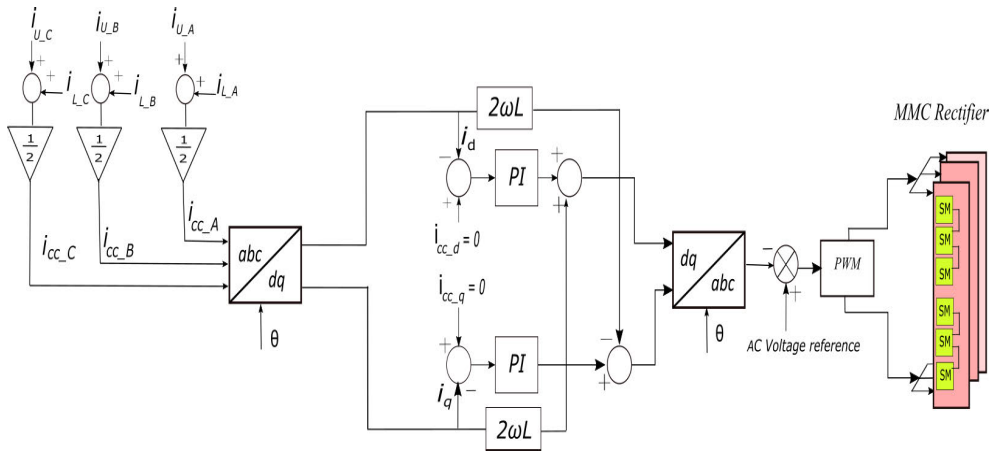


FIGURE 5. Circulating current controller for modular multilevel converter.

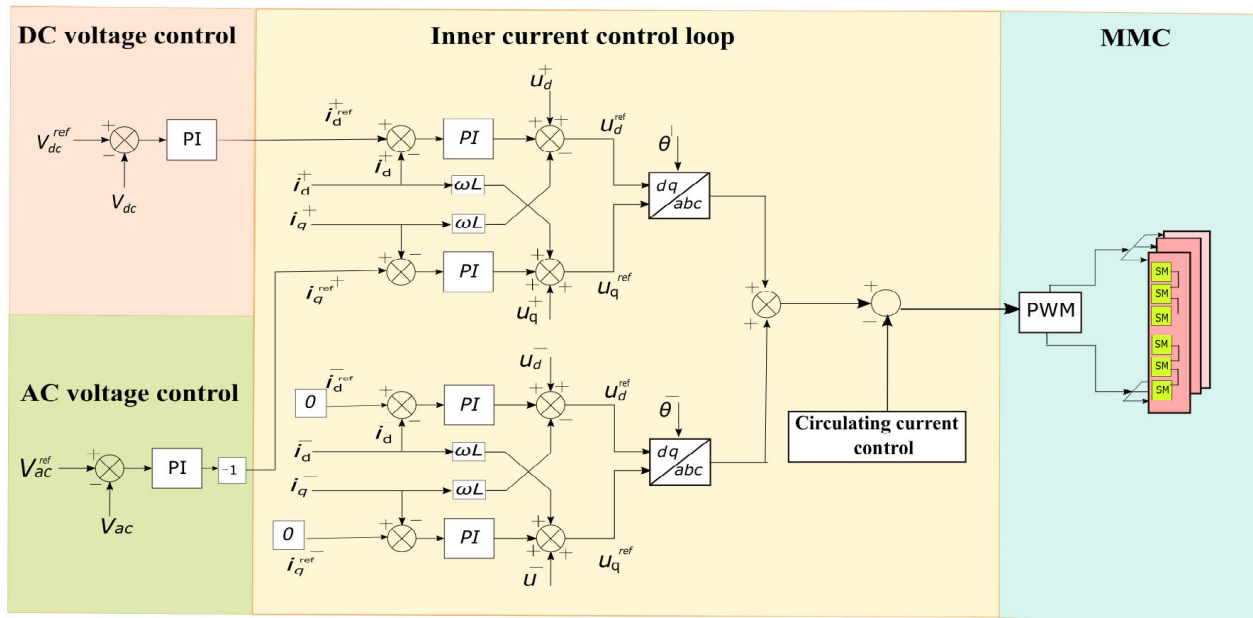


FIGURE 6. Inner & outer current control loop of designed MMC.

the measured DC voltage of the MMC and feeding I_d , error signal, to the proportional-integral controller which further creates a reference current I_d^{+ref} of the d-axis for the inner current loop of MMC. Equation (32) presents the outer control loop for DC voltage control and the DC controller is shown in Figure 6.

$$I_d^{+ref} = (V_{DC}^{ref} - V_{DC}) \cdot (K_p - \frac{K_i}{s}) \quad (32)$$

The outer loop AC voltage controller of the converter is shown in Figure 6. The primary aim of this control is to shape the AC voltage of the upstream AC grid. It is accomplished by comparing the reference AC voltage to the measured AC voltage of the overlaying AC grid and feeding I_q , error signal, to the proportional-integral controller which further creates a reference current I_q^{+ref} of the q-axis for the inner current

loop of MMC. Equation (33) shows the outer control loop of the MMC for AC voltage control. AC voltage controller is illustrated in Figure 6.

$$I_q^{+ref} = (V_{ac}^{ref} - V_{ac}) \cdot (K_p - \frac{K_i}{s}) \quad (33)$$

The AC component of the differential currents in the arm of MMC is effectively suppressed by the circulating current controller. The PI controller gains values set for the AC voltage controller are shown in table 1. Figure 5 illustrates the outer loop controller designed for the modular multilevel converter to suppress circulating differential currents in the arms of the converter. The circulating current controller is enabled at $t = 0.8$ seconds and the immediate effect can be seen in the CCSC simulation. It reduces the submodule voltage ripples, improves arm current quality with lower harmonics,

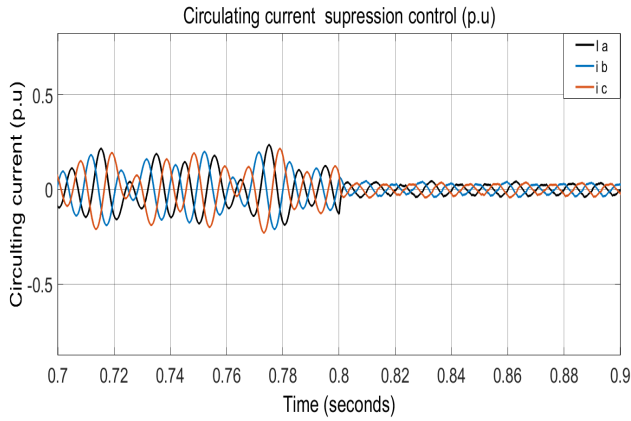


FIGURE 7. Circulating current control of MMC.

limits the peak value of the arm current reduces the stress on submodule components such as IGBT, transistor, diodes, and reduces the power loss in semiconductors of the MMC. Figure 7 illustrates the simulation results of the circulating current suppression controller.

TABLE 2. PI controller gain values.

Parameter	K_p	K_i
DC voltage PI controller gains	$K_{pdc}=7$	$K_{idc}=148$
AC voltage PI controller gains	$K_{pac}=2.2$	$K_{iac}=258$
Inner current PI controller gains	$K_{pii}=2$	$K_{iic}=100$
Circulating current PI controller gains	$K_{pcc}=1$	$K_{icc}=5$

D. ANALYSIS OF DC FAULT CURRENT WHEN MMC IS NOT BLOCKED

The MMC topology with the HBSMs and FBSMs configurations is illustrated in Figure 8. The converter is not in blocking mode because the threshold of the fault current detection has not yet been reached. Applying KVL to the upper loop, we have

$$V_a = L_a \frac{di_{ag}}{dt} + i_{ag}R_i + L_{arm}i_{au} - u_{au} + L_{sc} \frac{di_{az}}{dt} + i_zR_{sc} + V_{nN} \quad (34)$$

$$V_b = L_b \frac{di_{bg}}{dt} + i_{bg}R_i + L_{arm}i_{bu} - u_{bu} + L_{sc} \frac{di_{bz}}{dt} + i_zR_{sc} + V_{nN} \quad (35)$$

$$V_c = L_c \frac{di_{cg}}{dt} + i_{cg}R_i + L_{arm}i_{cu} - u_{cu} + L_{sc} \frac{di_{cz}}{dt} + i_zR_{sc} + V_{nN} \quad (36)$$

The mathematical expressions for the lower loop can be written as:

$$V_a = L_a \frac{di_{ag}}{dt} + i_{ag}R_i - L_{arm} \frac{di_{al}}{dt} - i_{al}R_{arm} + V_{nN} \quad (37)$$

$$V_b = L_b \frac{di_{bg}}{dt} + i_{bg}R_i - L_{arm} \frac{di_{bl}}{dt} - i_{bl}R_{arm} + V_{nN} \quad (38)$$

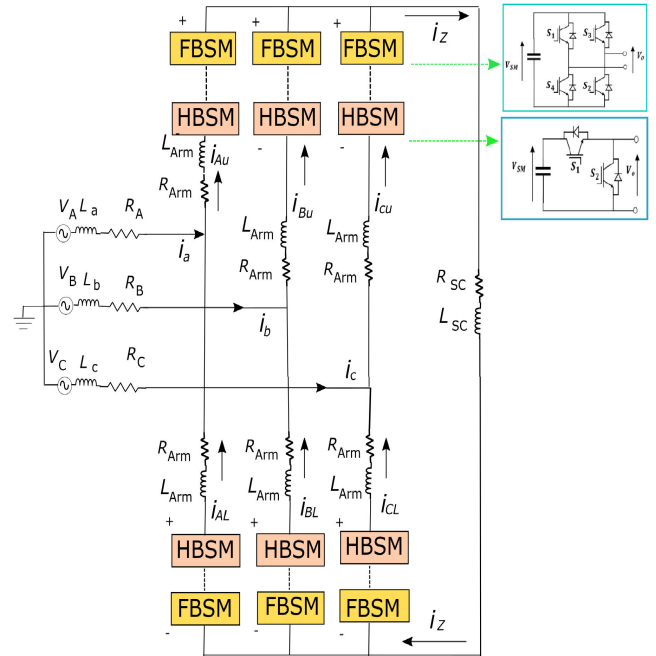


FIGURE 8. Modular multilevel converter topology.

$$V_c = L_c \frac{di_{cg}}{dt} + i_{ag}R_i - L_{arm} \frac{di_{cl}}{dt} - i_{cl}R_{arm} + V_{nN} \quad (39)$$

Applying KCL, in each node we get:

$$i_a = i_{au} - i_{al} \quad (40)$$

$$i_b = i_{bu} - i_{bl} \quad (41)$$

$$i_c = i_{cu} - i_{cl} \quad (42)$$

The value of i_z for the upper and lower arm is

$$i_z = i_{au} + i_{bu} + i_{cu} \quad (43)$$

$$i_z = i_{al} + i_{bl} + i_{cl} \quad (44)$$

Subtracting Equations (37),(38), and (39) from (34),(35), and (36) that yields:

$$(V_{au} + V_{al}) = L_a \frac{d(i_{au} + i_{al})}{dt} + (i_{au} + i_{al})R_i + L_{sc} \frac{di_z}{dt} + i_zR_{sc} \quad (45)$$

$$(V_{bu} + V_{bl}) = L_b \frac{d(i_{bu} + i_{bl})}{dt} + (i_{bu} + i_{bl})R_i + L_{sc} \frac{di_z}{dt} + i_zR_{sc} \quad (46)$$

$$(V_{cu} + V_{cl}) = L_c \frac{d(i_{cu} + i_{cl})}{dt} + (i_{cu} + i_{cl})R_i + L_{sc} \frac{di_z}{dt} + i_zR_{sc} \quad (47)$$

In general equations (45),(46) and (47) becomes

$$(V_{(abc)u} + V_{(abc)l}) = L_{(abc)} \frac{d(i_{(abc)u} + i_{(abc)l})}{dt} + (i_{(abc)u} + i_{(abc)l})R_i + L_{sc} \frac{di_z}{dt} + i_zR_{sc} \quad (48)$$

Equation (48) is valid for all three phases. Adding equation (48) for each phase, we obtain:

$$\sum_{n=a,b,c} (u_{nu} + u_{nl}) = (2L_z + 3L_{sc}) \frac{di_z}{dt} + (2R_z + 3R_{sc}) i_z \quad (49)$$

The number of submodules (SM) per arm of MMC is 'N'. Therefore, it can be written as follows:

$$u_{nu} + u_{nl} = NV_{sm} \quad (50)$$

As per [16], all capacitors are parallel at this point, so we can express the DC current as

$$i_z = \frac{2C_{sm}}{N} \sum_{n=a,b,c} (u_{nu} + u_{nl}) \quad (51)$$

C_{sm} is the capacitance of the capacitor of a submodule. Substituting equation (51) into equation (49) gives

$$(2L_z + 3L_{sc}) \frac{d^2 i_z}{dt^2} + (2R_z + 3R_{sc}) \frac{di_z}{dt} + \frac{Ni_z}{2C_{sm}} = 0 \quad (52)$$

(52) gives us the equation of the DC current i_z . As long as i_z reach the limit [31], this equation holds.

IV. OPERATING CHARACTERISTICS OF MODULAR MULTILEVEL CONVERTER SYSTEM

Detailed analysis and discussion of DC fault current management of the conventional and designed MMC is presented in this section.

A. ANALYSIS OF DC FAULT CURRENT WHEN CONVENTIONAL MMC IS BLOCKED

Half-bridge (HB) sub-module of MMC consists of two IGBTs with anti-parallel diodes (APDs) and a capacitor. The capacitor can either be connected or bypassed through the switching of the IGBTs. As a result, each half-bridge module can be viewed as an independent two-level two-quadrant voltage converter that is capable of generating either V_{sm} or 0 but also supporting the current I_{SM} to flow in both directions. The possible conditions of the arm current I_{arm} can be either I_{upper} or I_{lower} . The direction and signals of the gate of the submodule are summarized in Figure 9. Half-bridge cells support two cell states. The terminal voltage V_{cell} can either be zero or the positive capacitor voltage $+V_c$.

1) DC FAULT MANAGEMENT USING CONVENTIONAL MMC

During the DC fault, conventional MMC automatically blocks its IGBTs soon after a fault is detected, but its anti-parallel free-wheeling diodes (FWDs) continue a conductive path for AC current to reach the DC terminals so that the fault continues to feed. Half-bridge cells cannot provide a reverse blocking voltage in the event of a DC fault [32]. The DC circuit breaker is therefore essential to stop the fault current. DC circuit breaker with a current limiting reactor, to reduce stress on DC breakers, is required for interrupting the DC fault currents, illustrated in Figure 10. A high voltage

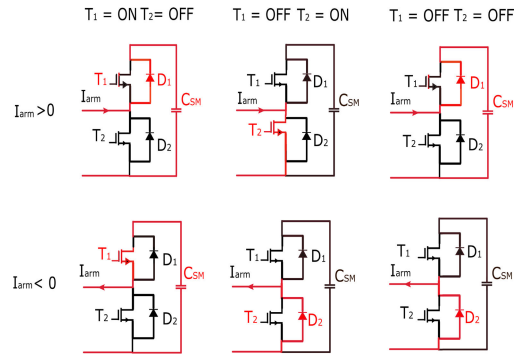


FIGURE 9. Half bridge submodule (HBSM) states and paths.

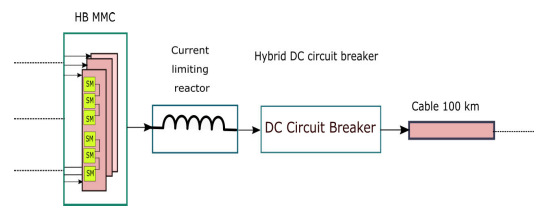


FIGURE 10. FRT strategy for conventional MMC.

DC network's circuit breakers must create a current zero and dissipate the energy trapped within the DC network. The limiting reactor used in series with DC circuit breakers makes the arrangement exorbitant. The industry and academia have recently researched DC circuit breakers extensively to overcome various limitations [33]. However, hybrid DC circuit breakers are prohibitively expensive and large in volume, limiting their application and development in high voltage DC distribution systems [34], [35].

B. ANALYSIS OF DC FAULT CURRENT USING PROPOSED MMC

In this paper HBSMs-based, MMC is designed in conjunction with the DC circuit breakers to accomplish economically viable operation and respond quickly to the system during the pole to pole and pole to ground DC faults. 10% redundant HBSMs are changed into full-bridge submodules making them capable to handle DC fault current in the event of DC faults. In normal operation 10%, redundant FBSMs are bypassed only HBSMs are working, but in a fault scenario, all 10% redundant FBSMs are inserted from bypass state to working state only when there is a fault to generate the reverse voltage to overcome the DC fault current. The model type used for the redundant full bridge submodule of FB-MMC is the switching model. As the fault vanishes the inserted 10% redundant FBSMs back reinstates to bypass state.

1) OPERATING PRINCIPLE OF REDUNDANT FULL BRIDGE SUBMODULE

The possible operating modes of the full-bridge submodule are bypass state, working state, and blocking state, illustrated in Figure 12. When the switches, IGBTs, of the full-bridge

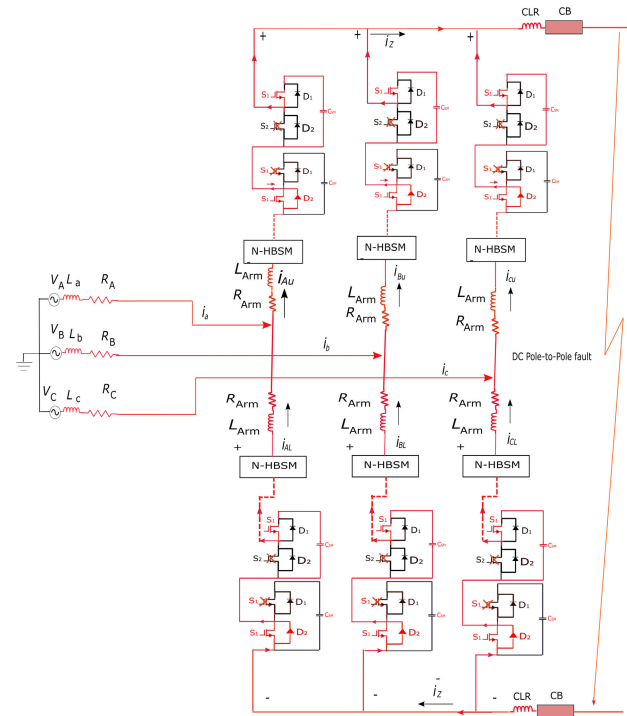


FIGURE 11. DC fault current through MMC.

submodule i.e. switch S_2 and switch S_3 are turned OFF while, switch S_1 and switch S_4 are turned ON, the capacitor of the submodule gets charging or discharging based on the current direction, this mode of full-bridge submodule indicates that it is in working state. If switches of the IGBTs i.e. S_1 and S_2 are only turned ON while S_3 and S_4 are OFF, or if S_3 and S_4 are only turned ON and S_1 and S_2 are OFF and the parallel capacitor is bypassed, this indicates that FBSM of MMC is the bypass state. On the other hand when S_1, S_2, S_3 and S_4 are turned OFF and the capacitor can only be charged regardless of what direction the current is flowing, this shows that FBSM of MMC is the blocking mode. In the blocking mode of MMC, the voltage of the FBSMs is reversed.

2) DC FAULT MANAGEMENT USING PROPOSED DC FRT STRATEGY

A DC FRT strategy is implemented to limit the fault current and give the circuit breakers enough time to interrupt the fault current. The redundancy ratio of the converter is kept at ten percent, in which the redundant submodules are based on full-bridge structures in order to allow the MMC to handle the DC fault current during DC faults. In normal operation, the redundant SMs are bypassed and only the HB one is working, but in a fault scenario when a fault current is detected, the control system inserts all the redundant FBMSs to generate the reverse voltage to overcome the DC fault current. The working principle of FBSMs from bypass state to working state is explained in Figure 12. When the fault vanishes the inserted 10% redundant FBSMs back reinstates to the bypass state. Therefore, the power losses of the converter

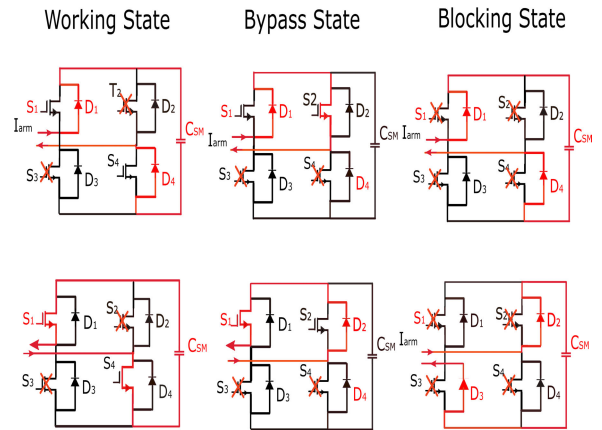


FIGURE 12. Different state conditions of full bridge submodule (FBSM).

are low, as the HBSM uses fewer semiconductors compared to FBSMs while the MMC is working in normal operation. In the normal operation of the DC distribution system, all

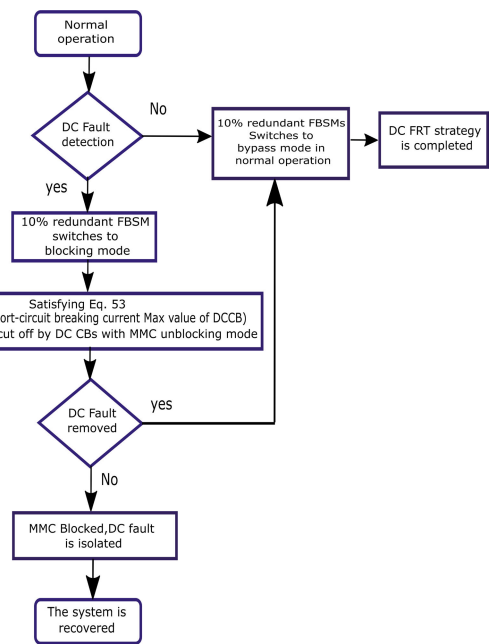


FIGURE 13. DC FRT strategy implemented for MMC.

the FBSM are kept bypassed. When pole to pole DC fault occurs on the distribution side, the fault current quickly rises and triggers its over-current threshold set to be equal to 1.1 (p.u), and the full-bridge submodules switch from bypass state to blocking state (see figure 12). Consequently, the full-bridge submodules will generate the reverse or negative voltage required to reduce the magnitude of the fault current; thus providing sufficient time for circuit breakers to interrupt the DC fault current. Blocking state characteristics of the redundant full-bridge submodule play a significant role in limiting the fault current during fault scenario. Before that the arm bridge current trigger MMC in a blocking state, DCCB

cut off DC fault currents. DC fault current must meet the following requirements to achieve this

$$I_{DC}(t_p) \leq I_p \quad (53)$$

where I_{DC} is the current which flows through a DC circuit breaker during fault conditions, where t_p is the breaking current peak time after the fault occurs and I_p is the short-circuit breaking current peak value of the DC circuit breaker. When the DC fault current meets (53), the MMC redundant submodules (RSMs) will be switched to bypass mode and the DC fault current can be interrupted before blocking the MMC. If not, the system will be temporarily shut down and MMC will be blocked.

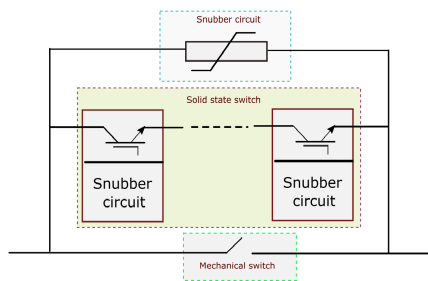


FIGURE 14. DC circuit breaker topology.

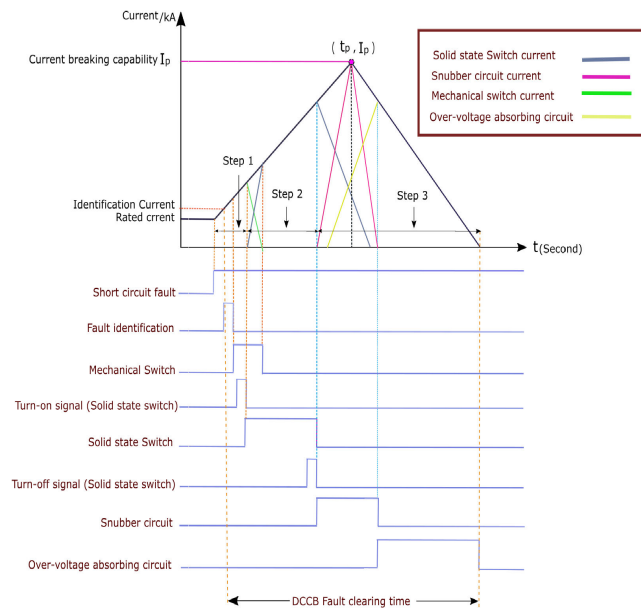


FIGURE 15. Characteristics of the operation of DCCB.

3) DC CIRCUIT BREAKER OPERATION

The topology of the DCCB is shown in Figure 14. It consists of the following three parts

- Mechanical switch.
- Solid-state switch.
- Snubber circuit.

There are three steps involved in the operation of the DC circuit breaker.

a: STEP 1

During the DC short circuit faults on the DC line, the current will increase sharply, leading the DCCB's mechanical switch to be turned off. As a result, electric arcs may appear when the mechanical switch branch is turned off, resulting in a forward voltage drop that activates the solid state switch, which in turn initiates current commutation. The first step operation of DCCB is shown in Figure 15.

b: STEP 2

When the current commutation process starts, the current in the mechanical switch decreases and rises in the solid state switch of the DCCB as shown in Figure 15.

c: STEP 3

The third step of the DCCB operation starts with a solid state switch turning off to break the DC fault current. The snubber circuit starts to conduct and clamp the voltage due to the inductance of the line and finishing the operation of the DCCB. An over voltage absorbing circuit determines the time duration of its operation. The operation characteristics of the DCCB are shown in Figure 15.

V. RESULTS OF THE SIMULATION AND DISCUSSION

MATLAB-based Simulink system is used for simulation of the designed MMC and DC fault current ride-through method. MMC parameters and simulation environment are shown in table 3. Figure 16 illustrates the steady-state oper-

TABLE 3. Characteristic parameters of the designed MMC & DC distribution system.

S.No	Characteristic parameter	Values
1	AC grid voltage	132 kV
2	Power transformer voltage ratio	132/66 kV (Core type)
3	Transformer power rating	220 MVA
4	No of HB SMs in MMC	50
5	No of FB redundant SMs in MMC	5
6	MMC's arm inductance L_{arm}	0.0164 (p.u)
7	MMC's arm resistance R_{arm}	0.0300 (p.u)
8	Sub module capacitance	13.34 mF
9	DC grid voltage	120 kV
10	Resistance of the DC cable	0.133 Ohms/km
11	Inductance of the DC cable	0.0008373 H/km
12	Capacitance of the DC cable	0.139e-9F/km
13	Length of the DC distribution line	100 Km
14	Sampling time	20 μ s

ation of the designed modular multilevel converter with submodule voltage, arm current, and capacitors voltages. The submodule's voltage is calculated per unit where 2.25 kV is set as a base voltage. Arm current, illustrated in Figure (b), in one phase of the modular multilevel converter and the base current, is 1.924 kA. The MMC has a voltage ripple of about 11%. Capacitors of SMs can bear this voltage effectively. IGBT module with a rating of 4.5kV and 1800A used as a

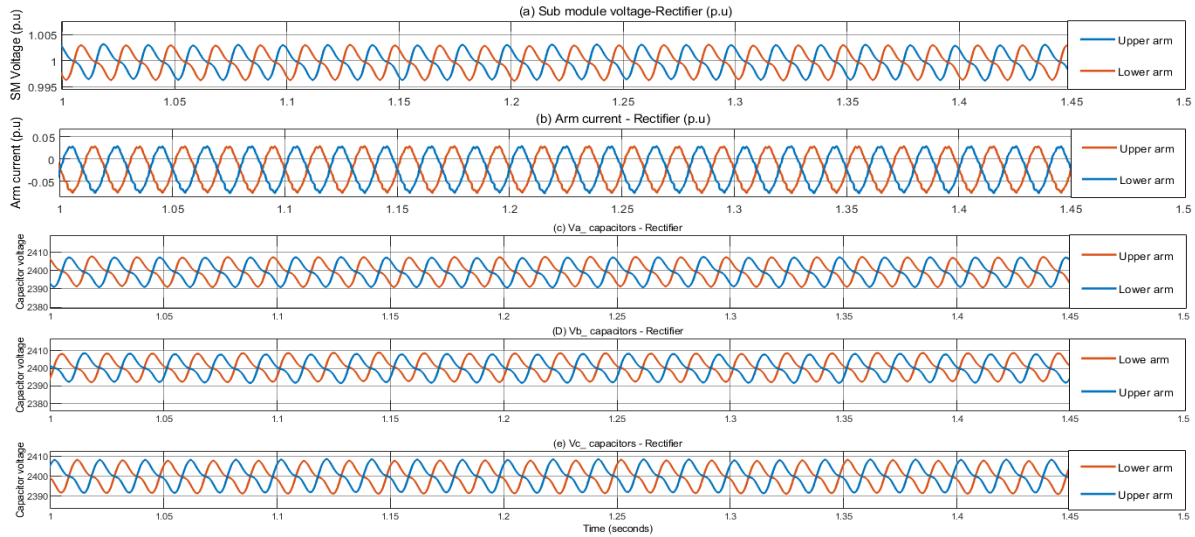


FIGURE 16. Steady state operation of the designed MMC.

semiconductor switch of submodule having approximately 11% voltage ripples.

A. FAULT INTERRUPTION PERFORMANCE OF THE CONVENTIONAL VERSUS DESIGNED MMC

To evaluate the fault current blocking ability and economic viability of the designed MMC, it is important to analyze and compare it with other conventional MMC for different types of DC faults i.e. pole to pole and pole to ground faults.

B. BLOCKING OF FAULT CURRENTS DURING POLE TO POLE FAULTS

A pole to pole DC fault occurs at $t = 0.7$ seconds at a distance of 100 km from the MMC. Once the pole to pole DC fault happens, the fault current rises abruptly and reaches the over-current threshold. IGBT module with a rating of 4.5kV and 1800A used as a semiconductor switch of submodule. During pole to pole fault on the DC distribution network, the fault current in the arm of MMC does not exceed the current rating of the semiconductor switch of the submodule and does not violate the thermal limits of the IGBT switch. The arm current of the MMC is shown in Figure 17.

The conventional modular multilevel converter is not capable to limit or cut-off the fault current itself without using DC circuit breakers. Therefore, a DC circuit breaker is mandatory to isolate selectively and abruptly the faulty areas from the rest of the healthy power system. Figure 18 shows that when a fault occurs at $t = 0.7$ seconds, the peak value of the fault current abruptly reaches 15.2 p.u in 40 milliseconds. The fault current is interrupted by a DC circuit breaker at $t = 0.74$ seconds and the system is restored at $t = 0.78$ seconds by re-closing the circuit breakers of the DC terminals.

In the case of the designed MMC, when a fault is detected at $t = 0.7$ seconds all the redundant submodules of the MMC are inserted and switched from bypass mode to blocking

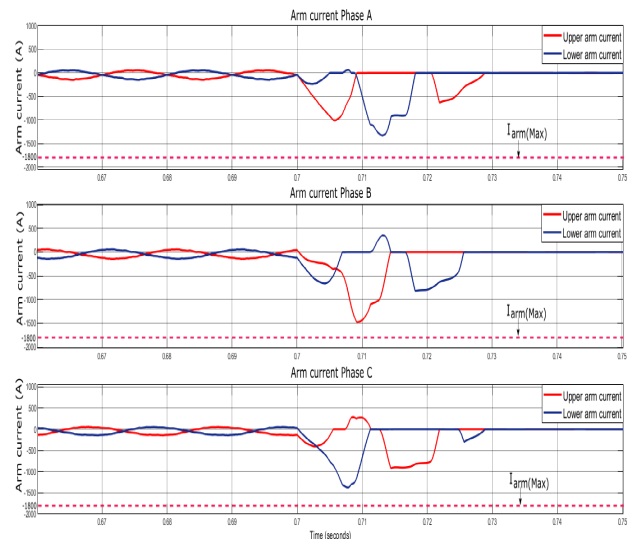


FIGURE 17. Arm current of MMC during fault condition.

mode. The inserted full-bridge submodules have generated the reverse voltage and kept limiting the peak value of the fault current up to 6.4 p.u. The magnitude of the peak value of the fault current is reduced because of the reverse or negative voltage generated by inserted redundant FBSMs and the fault current is suppressed. This will provide sufficient time for DC circuit breakers to terminate the fault current. If the fault persists, the DC fault current is cut-off by DC circuit breakers and MMC is turned unblocked before the arm current of the converter triggers MMC in a blocking state. In this case, the magnitude of the fault current is low so we need DC circuit breakers having a low rating of short-circuit breaking current as compared to the case of conventional MMC. The pole to pole fault on the DC distribution side has vanished

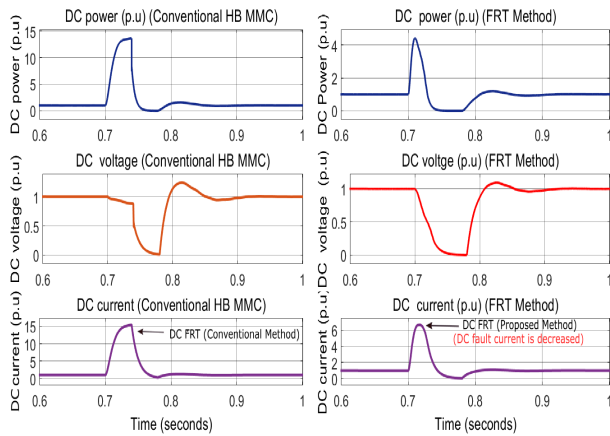


FIGURE 18. Interruption performance of the conventional MMC and designed MMC during pole to pole fault.

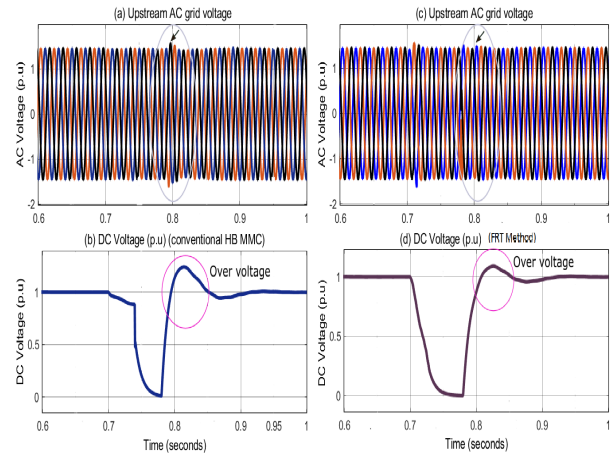


FIGURE 20. Upstream AC grid and DC grid voltages during pole to pole fault in case of the conventional and designed MMC.

exceed their steady-state value for 50 milliseconds. A voltage transient of 1.58 p.u occurs during the re-closing time, which can be seen in Figure 20 (a). After the re-closing period, the magnitude of DC terminal voltage is 1.24 p.u, which is greater than that of the maximum limit of 1.1 p.u, as shown in Figure 20 (b). The stress on the insulation is relatively high in this case.

In the case of the DC FRT strategy for the designed MMC; when a fault is detected at $t = 0.7$ seconds all the redundant submodules of the MMC are switched from bypass mode to blocking mode. The inserted full-bridge submodules have generated the reverse voltage and suppressed the fault current. In $t = 40$ milliseconds the fault has been removed and the DC circuit breakers have re-closed at $t = 0.78$ seconds. The AC grid voltages can be seen in Figure 20 (c). Figure 20 (c) shows that there is a very low transient in AC grid voltages during the re-closing period because the designed MMC has consumed the negative reactive power and injected the reactive power into the AC grid system. After re-closing the magnitude of DC voltage is 1.09 p.u which is not greater than that of the maximum limit of 1.1 p.u as shown in Figure 20 (d). The stress on the insulation is low in this case.

C. BLOCKING OF FAULT CURRENTS DURING POLE TO GROUND FAULTS

A pole to ground DC fault occurs at $t = 0.7$ seconds at a distance of 100 km from the conventional modular multilevel converter. Once the pole to pole DC fault happens, the fault current rises abruptly and reaches the over-current threshold. The conventional modular multilevel converter is not capable to limit or cut-off the fault current itself without using DC circuit breakers. Therefore, a DC circuit breaker is mandatory to isolate selectively and abruptly the faulty areas from the rest of the healthy power system. Figure 21 shows that when a fault occurs at $t = 0.7$ seconds, the peak value of the fault current abruptly reaches 2.166 p.u in 40 milliseconds. The fault current is interrupted by a DC circuit breaker at

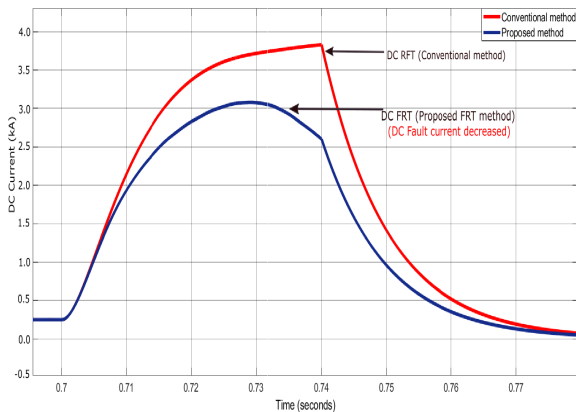


FIGURE 19. Comparison of simulation results of proposed DC FRT and conventional FRT method.

at $t = 0.78$ seconds, MMC is turned unblocked and all the redundant submodules have switched to a bypass mode and the system's operation is normal and DC FRT strategy is completed.

The main advantage of the FRT strategy of the designed MMC over the conventional MMC fault interruption method is its economic viability. The proposed DC FRT strategy requires a low rating of short-circuit breaking current of DC circuit breakers which reduces the requirement and investments. therefore, the levelized cost of the system is reduced.

1) AC AND DC GRID'S TRANSIENT VOLTAGES DURING POLE TO POLE FAULT

Figure 20 (a) illustrates the upstream AC grid's voltage during the pole to pole DC fault when conventional MMC is interfaced between AC and DC grids. The fault current rises abruptly upon an occurrence of DC fault at $t = 0.7$ seconds. The DC circuit breaker has tripped at $t = 0.74$ seconds, after 40 milliseconds the fault has been removed and DC circuit breakers have re-closed at $t = 0.78$ seconds. During the re-closing time of the DC breakers, the AC grid voltages

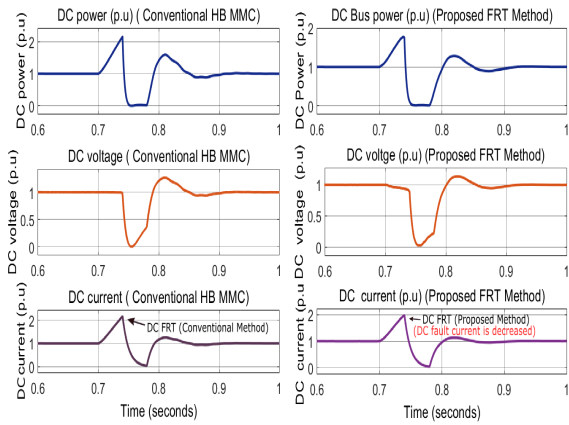


FIGURE 21. Interruption Performance of the conventional MMC and designed MMC during pole to ground fault.

$t = 0.74$ seconds and the system is restored at $t = 0.78$ seconds by re-closing the circuit breakers of the DC terminals.

In the case of the designed MMC, when a fault is detected at $t = 0.7$ seconds all the redundant submodules of the MMC are inserted and switched from bypass mode to blocking mode. The inserted full-bridge submodules have generated the reverse voltage and suppressed the peak value of the fault current up to 1.9 p.u. The magnitude of the peak value of the fault current is reduced because of the reverse or negative voltage generated by inserted redundant FBSMs and the fault current is suppressed. This will provide sufficient time for DC circuit breakers to terminate the fault current. If the fault persists, the DC fault current is cut-off by DC circuit breakers and MMC is turned unblocked before the arm current of the converter triggers MMC in a blocking state. In this case, the magnitude of the fault current is low so we need DC circuit breakers having a low rating of short-circuit breaking current as compared to the case of conventional MMC. The pole to pole fault on the DC distribution side has vanished at $t = 0.78$ seconds, MMC is turned unblocked and all the redundant submodules have switched to a bypass mode and the system's operation is normal and DC FRT strategy is completed.

The main advantage of the FRT strategy of the designed MMC over the conventional MMC fault interruption method is its economic viability. The proposed DC FRT strategy requires a low rating of short-circuit breaking current of DC circuit breakers which reduces the requirement and investments. Therefore, the leveled cost of the system is reduced.

1) AC AND DC GRID'S TRANSIENT VOLTAGES DURING POLE TO GROUND FAULT

Figure 22 (a) illustrates the upstream AC grid's voltage during the pole to pole DC fault when conventional MMC is interfaced between AC and DC grids. The fault current rises abruptly upon an occurrence of DC fault at $t = 1.2$ seconds. The DC circuit breaker has tripped at $t = 0.74$ seconds, after 40 milliseconds the fault has been removed and DC

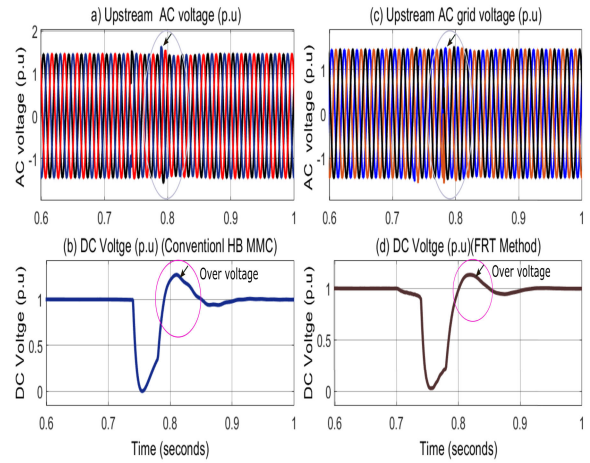


FIGURE 22. Upstream AC grid and DC grid voltages during pole to ground fault in case of the conventional and designed MMC.

circuit breakers have re-closed at $t = 0.78$ seconds. During the re-closing time of the DC breakers, the AC grid voltages exceed their steady-state value for 50 milliseconds. A voltage transient of 1.63 p.u. occurs during the re-closing time, which can be seen in Figure 22 (a). After the re-closing period, the magnitude of DC terminal voltage is 1.5 p.u, which is greater than that of the maximum limit of 1.1 p.u, as shown in Figure 22 (b). The stress on the insulation is relatively high in this case.

In the case of the DC FRT strategy for the designed MMC; when a fault is detected at $t = 0.7$ seconds all the redundant submodules of the MMC are switched from bypass mode to blocking mode. The inserted full-bridge submodules have generated the reverse voltage and suppressed the fault current. In $t = 40$ milliseconds the fault has been removed and the DC circuit breakers have re-closed at $t = 0.78$ seconds. The AC grid voltages can be seen in Figure 22 (c). Figure 22 (c) shows that there is a very low transient in AC grid voltages during the re-closing period because the designed MMC has consumed the negative reactive power and injected the reactive power into the AC grid system. After re-closing the magnitude of DC voltage is 1.04 p.u which is not greater than that of the maximum limit of 1.1 p.u as shown in Figure 22 (d). The stress on the insulation is low in this case.

D. AC FRT MANAGEMENT OF THE DESIGNED MMC

The objective of this study is to evaluate the ability of the designed modular multilevel converter to manage its output power under fault conditions. The asymmetrical fault of 40% voltage dip is modeled through a 132 kV source on the upstream AC side. The simulation model is subjected to an asymmetrical fault where 40 percent of the voltage dip occurs as illustrated in Figure 23. Fault on the upstream AC grid side occurs on 1.2 seconds and it remains for 75 milliseconds. The objective of this study is to evaluate the ability of the designed modular multilevel converter to manage its output power under fault conditions.

TABLE 4. Comparison of the fault handling capabilities of the conventional and designed modular multilevel converter.

S.NO	Characteristic parameter	Simulation Condition	Conventional MMC	Designed MMC
1	MMC structure	-	HB-MMC -(Redundant SMs type is HBSM) -DCCB required (High current rating).	HB-MMC -(Redundant SMs type is FBSM) -DCCB required (Low current rating)
2	DC fault current (Max) during fault (During Pole to pole fault)	100 km from MMC	15.2 (p.u)	6.4 (p.u)
3	DC fault current (Max) during fault (During Pole to ground fault)	100 km from MMC	2.166 (p.u)	1.9 (p.u)
4	Current limiting reactor	-	Required	Not required
5	AC grid voltage transient in re-closing period (Pole to pole fault)	-	1.584 (p.u)	1.5 (p.u)
6	AC grid voltage transient in re-closing period (Pole to ground fault)	-	1.63 (p.u)	1.5 (p.u)
7	DC over voltage in re-closing period (During Pole to pole fault)	-	1.24 (p.u)	1.09 (p.u)
8	DC over voltage in re-closing period (During Pole to ground fault)	-	1.5 (p.u)	1.04 (p.u)
9	Stress on insulation	-	Relatively high	Low
10	AC& DC FRT capability	Asymmetrical fault& DC pole to pole and pole to ground fault	NO	Yes
11	Cost	-	Expensive	Low cost

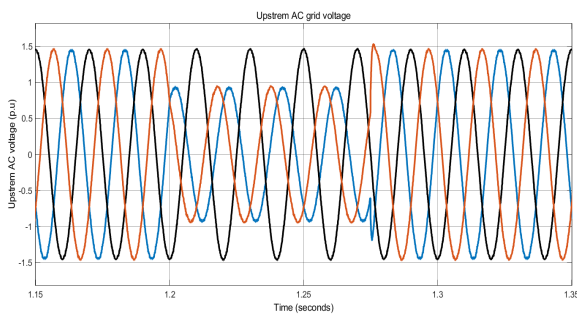


FIGURE 23. Asymmetrical fault on upstream AC grid.

1) ENERGY STORED IN DESIGNED MMC

Capacitors of the submodules of the designed MMC act as energy buffers. When the asymmetrical fault occurs on the AC grid side, MMC provides the energy stored in the SMs of the converter to offset the loss of energy due to voltage dips in AC voltage. According to equation 54, the submodule voltage is 2.4 kV and the capacitor’s capacitance is 13.24 mF, so the energy stored in SMs is 38.1312 kJ.

$$E_c = \frac{1}{2} CV_c^2 \tag{54}$$

The total energy stored in the arm of MMC is 1.90 megajoule and one phase leg has the energy of about 3.812 MJ respectively. The total energy stored in the modular multilevel

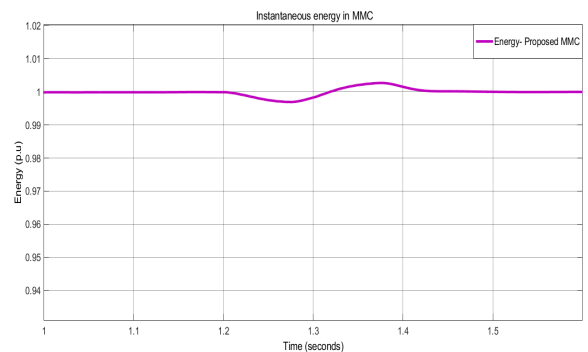


FIGURE 24. Instantaneous energy (p.u) of the designed modular multilevel converter.

converter is 11.43 MJ. Accordingly, the modulation index, which defines the threshold of capacitor-discharge, is 0.8 for a modular multilevel converter in steady-state operation. Therefore, the converter can operate efficiently when the voltage dip is from 1.0 p.u to 0.8 p.u.

When a fault occurs, the energy stored in MMC should have supplied 0.3% of its installed energy, as in our case its energy discharged to about 0.997 p.u as shown in Figure 24. The designed MMC has a maximum installed energy of 11.43 MJ, since only 0.3% of the energy installed in MMC, which is 0.342 MJ, is discharging to manage the effect of

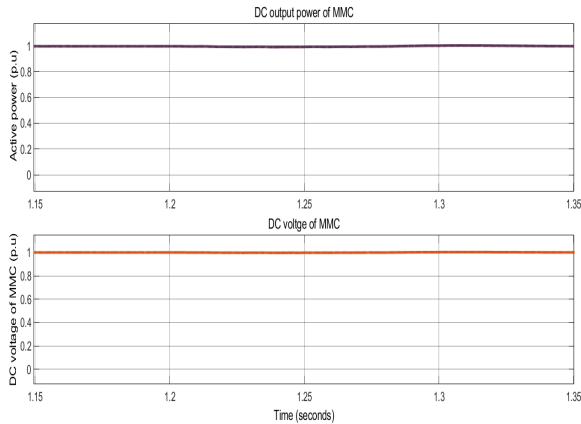


FIGURE 25. Output power and DC voltage of the designed MMC.

an asymmetrical fault on the upstream AC grid side without interfering with MMC operation. The active power and DC voltage of the MMC is shown in Figure 25. This indicates that the effect of the fault on the upstream AC grid has been effectively managed by the integrated energy stored in the converter.

VI. CONCLUSION

In this research article, we primarily focus to engineer the AC and DC FRT strategies for a modular multilevel converter. The AC and DC FRT strategies are accomplished by using the integrated energy of the SMs of the designed MMC for the AC grid's asymmetrical faults and changing the redundant submodules of the designed MMC to FBSMs for DC faults respectively. The effectiveness of the FRT strategies for DC pole to pole and pole to ground faults and AC grid asymmetrical fault are proven through simulation results. The FRT strategies are compared with the conventional strategies used for MMC. The results conclude that the designed MMC with AC and DC FRT capability is economically viable and efficient for future AC and DC grid architecture. The designed DC FRT strategy requires a low rating of short-circuit breaking current of DC circuit breakers which reduces the requirement and investments. Therefore, it reduces the overall cost of the initial investments.

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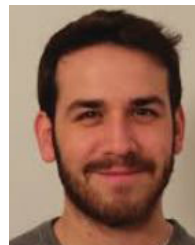
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