IEEE Access
Multidisciplinary ⋮ Rapid Review ⋮ Open Access Journal

Received 25 October 2022, accepted 15 November 2022, date of publication 21 November 2022,
date of current version 30 November 2022.

Digital Object Identifier 10.1109/ACCESS.2022.3224008

RESEARCH ARTICLE

Reliability Characterization of Solder Joints in Electronic Systems Through a Neural Network Aided Approach

REZA REIHANISARANSARI[1], FARSHAD SAMADIFAM[2], ANAS A. SALAMEH[3], FARZAM MOHAMMADIAZAR[4], NAFISEH AMIRI[1], AND SITTIPORN CHANNUMSIN[5]

[1]Department of Electrical and Computer Engineering, University of Houston, Houston, TX 77004, USA
[2]Department of Biomedical Engineering, Medical College of Wisconsin, Milwaukee, WI 53226, USA
[3]Department of Management Information Systems, College of Business Administration, Prince Sattam bin Abdulaziz University, Al-Kharj 11942, Saudi Arabia
[4]Department of Electrical and Computer Engineering, University of Tabriz, Tabriz 15731, Iran
[5]Space Technology Research Center, Geo-Informatics and Space Technology Development Agency (GISTDA), Chonburi 20230, Thailand

Corresponding author: Sittiporn Channumsin (sittiporn@gistda.or.th)

This work was supported by the Geo-Informatics and Space Technology Development Agency (Public Organization) (GISTDA).

ABSTRACT Rapid and precise reliability evaluation of electronic circuits plays a key role in the design stage of the electronic systems. The task becomes even more difficult when several major parameters contribute into the reliability evaluation. This paper proposes a neural network aided approach as a prediction tool for estimating the useful lifetime of the ball shaped solder joint as the most resistless part under accidental drops in the electronic devices. Several contributory factors including ball grid array (BGA) chip location, printed circuit board (PCB) thickness, solder alloy composition and solder ball volume are considered in our proposed rapid prediction model and their effects are investigated. 480 finite element simulations as well as 20 experimental tests are performed to obtain an enriched database for our neural network based prediction model. The accuracy of the proposed model is calculated as 97.55% in comparison with the finite element and the experimental results. Ability of considering multi contributory factors in the reliability evaluation of the BGA chip makes our proposed approach be a suitable candidate in design for reliability of the electronic systems.

INDEX TERMS Solder joint, drop test, lifetime estimation, machine learning.

I. INTRODUCTION

Designing a reliable and robust system performs a decisive role in today's manufacturing processes [1], [2], [3]. By ever-increasing technological enhancement in electronic components leading to smaller sizes and lighter weight, handheld electronic devices from cell phones to industrial portable equipment have received significant attention [4], [5]. Although the portable devices are easily carried, the damage probability of the devices is growing due to the possibility of the accidental drop [6], [7], [8]. Since 2003, a board-level drop-test standard has been introduced by Joint Electronic Device Engineering Council (JEDEC) called JESD22-B111 for investigating the strength of the electronic devices against drop impacts [9]. Numerous studies have been employed the procedure of JESD22-B111 to survey the failure process of the solder joint under accidental drop [10], [11], [12]. It has been reported that the pulling stress originated by different mechanical properties (the stiffness and the elastic moduli) of the components from the printed circuit board (PCB) is the deeply-rooted cause of the failure in the electronic devices under mechanical shocks such as vibration loading and drops impact [13], [14]. In addition, several studies have been undertaken to investigate the drop impacts on the electronic devices considering diverse conditions including PCB materials, solder alloys, PCB arrangement, solder joint geometry, and type [15], [16], [17], [18]. Wu and Lan [19] investigated the behavior of two different lead-free solder alloys

The associate editor coordinating the review of this manuscript and approving it for publication was Xiao-Sheng Si.

This work is licensed under a Creative Commons Attribution-NonCommercial-NoDerivatives 4.0 License.
For more information, see https://creativecommons.org/licenses/by-nc-nd/4.0/

including Sn-1.0Ag-0.5Cu and Sn-1.2Ag-0.5Cu with nickel in the electronic devices under drop impacts and established a simulation-based low-cycle fatigue predictive model for them using the JEDEC Condition B drop test. The stress-induced in the solder joint was used in the proposed predictive model. Although the model was established to predict the low-cycle fatigue lifetime of the solder joint in two different alloys, it is not generalized enough to be employed in the design stage investigation of reliability. Niu et al. studied the effects of low-G and High-G drop impacts on the ball-shaped solder joints using the time-domain reflectometry (TDR) approach [20]. The paper's main focus was dedicated to the location of the electronic devices on the PCB. It was found that the farther the electronic device is from the center of mass; the more accelerated damage of solder joint is probable. This fact was also validated by the research conducted in [21] in which three different printed circuit boards (PCBs) were experimentally tested as the board-level testing. In these tests, only Sn-3.0Ag-0.5Cu was considered and other contributory factors were missing in the drop-impact lifetime prediction model. The effects of high-G and low-G drop impacts on the ball solder joint were investigated in [22] using finite element simulations. Two drop test conditions (1000g and 300g for 1ms and 2ms respectively) were designed and the failure probability of the solder joint as the most vulnerable part was discussed. Although the location of the maximum tension and the failure mode sequence was detected through this study, PCB materials, solder joint materials, and the location of the BGA device were not considered. Different types of drop failure of the lead-free solder joints in the presence and the absence of electro-migration were considered in [23] and [24]. Some prediction models were proposed to estimate the useful lifetime of the solder joint under the drop impacts using both simulations and experimental tests [25], [26], [27], [28].

These prediction models are not generalized and not capable to be used in the design stage of the electronic systems. Inconsideration of the contributory factors in the mechanical reliability assessment in these prediction models makes them suitable for a unique case study not a multi-aspect solder joint lifetime estimation study. In this study, machine learning-based drop impact reliability has been used for a global consideration of solder joint dimension, chip location, solder joint chemical composition, and PCB thickness. Since this approach is capable of taking into account different values and states for the contributory factors, a stage of design for reliability can be included in the design of electronic systems. The approach estimates the solder joint lifetime very fast and can be updated by adding a new data library either from simulations or experimental tests. The paper is organized as follows. While the simulating and experimental procedure is described in section II, section III deals with the proposed neural network for lifetime estimation of the solder joint. Section IV presents the experimental, simulating, analytical results for the solder joint lifetime estimation. Finally, a conclusion is drawn in section V.

II. DROP EXPERIMENTAL AND FINITE ELEMENT ANALYSIS

The importance of the lifetime estimation of the solder joint lies in the experimental investigation of the drop impacts on the electronic package and a descriptive finite element (FE) model to capture the effects of the accidental drops on the electronic devices. In this section, the procedure of FE simulations and the experimental drop tests will be discussed and their results will be compared and validated.

A. FINITE ELEMENT SIMULATIONS

To extract the induced strain and stress in the ball solder joints of the electronic device under the drop events, ABAQUS finite element software was used in the dynamic-explicit model. 480 FE simulations were performed in the different conditions focusing on four major factors including the location of the electronic package on the printed circuit board (PCB), solder joint geometry, solder joint chemical composition, the PCB thickness. **Figure 1a** demonstrates one of the considered circuit configurations in FE simulation. The PCB material is FR4 with a thickness of 1.6mm as the default value for the FE simulations. However, a range of [0.8mm 2.4mm] was considered as the PCB thicknesses in different FE simulations in order to create diverse conditions for evaluating the effects of the PCB thickness on the useful lifetime of the solder joint under drop impacts. As shown, a BGA electronic device is located in the center of the PCB. This BGA electronic device, then, is assumed to be remounted in the twenty different locations on the PCB to investigate the effects of the BGA device location on the reliability of the solder joint under drop impacts. **Figure 1b** shows the barrel-type solder joint used in the BGA electronic device. The solder joint volume which is proportional to its mid-, top-radius, and height is considered as a parameter in the reliability assessment of the solder joint in the BGA components as reported in [21], [29], and [30]. eleven different solder joint volumes, namely from 3.3mm^3 to 6.0mm^3 ({3.3, 3.6, 3.9, 4.2, 4.5, 4.8, 5.1, 5.4, 5.7, 6.0}), were considered for FE

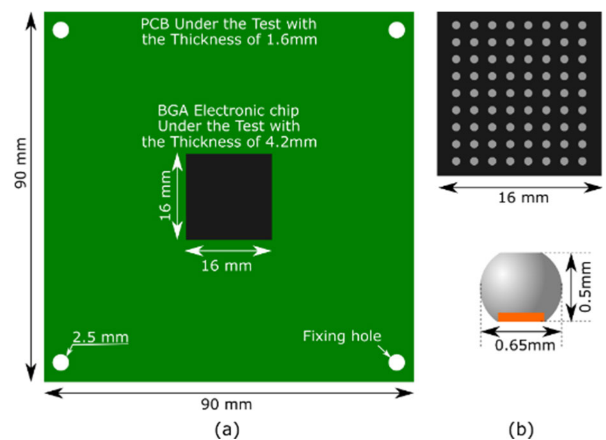

FIGURE 1. Geometric of the PCB and the BGA electronic chip under the drop test. a) PCB schematic, b) BGA chip and solder joint structure.

TABLE 1. Material properties of the different parts in FE simulations [22], [19].

Components	Materials	Coefficient of thermal Expansion (10^{-6}/ºC)	Young's Module (GPa)	Poisson Ratio	Density (*10^{-6}kg/mm^3)
Solder Pad	Cu	17	132	0.34	8.69
Chip	Si	3.5	130	0.22	2.33
Solder ball	SAC105	23.4	35.7	0.30	7.37
Solder ball	SAC1205N	23.8	39.8	0.30	7.53
PCB	FR4	14	26	0.40	2.752

simulations. In addition, two solder alloys including SAC105 (Sn-1.0Ag-0.5Cu) and SAC1205N (Sn-1.2Ag-0.5Cu with nickel) were taken into account in FE simulations. Accordingly, 480 FE simulations were performed with the combination of the above-mentioned conditions. The simulations were performed in ABAQUS dynamic-explicit step analysis with the element type of C3D10M (a 10-node modified quadratic tetrahedron). The meshed model has 46236 elements and 78324 nodes. High-G input acceleration with an amplitude of 1000g and impulse period of 1ms as shown in **Figure 2** was applied to all FE simulations [22]. The material properties of the different parts in the simulations are listed in Table 1.

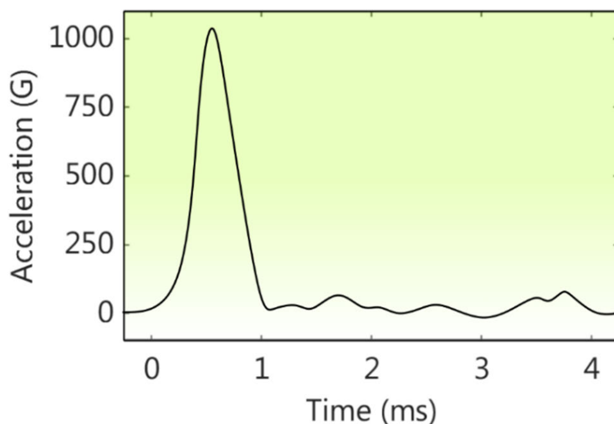

FIGURE 2. Acceleration curve with the amplitude of 1000g.

B. EXPERIMENTAL DROP TEST PROCEDURE

The experimental drop tests were designed in compliance with the conditions considered in FE simulations. In this regard, several different conditions were applied to the BGA device drop test to validate the FE simulations performed with the ABAQUS environment. **Figure 3** demonstrates the graphical structure of the experimental drop tests. As shown, the PCB was mounted on the drop table through the base plate. The drop table hit the rigid base through the guide rods by freefall from the top. One of the major parameters and factors in the quality of solder interconnection is the reflow soldering process implementing in the reflow oven. The BGA chip has been connected to the one layer printed circuit board through the reflow soldering process [31]. It has been extensively reported that improper reflow process may

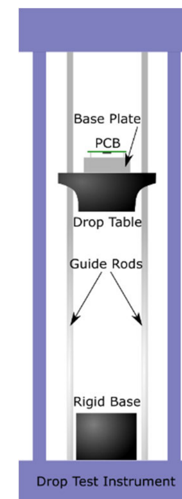

FIGURE 3. Schematic of the instrument for free fall drop tests. The PCB mounted on the Baseplate and hit the rigid base via guide rods.

lead to some defects including bridges, cracks and delamination [32]. Accordingly, a process with the following conditions was employed in order to minimize any interconnection defects. The preheating process started from 130°C to 170°C and continued for 90s to 120s. The maximum temperature ranges at the reflow zone were 220°C to 250°C and last for 20s to 30s. By reaching the peak temperature (250°C), air cooling process started until reaching ambient temperature. A solder joints loop was implemented using a daisy-chain design. To determine the failure and monitor the damage level, the resistance of the solder joint loop was considered as the failure criteria [19], [33]. A 10% increase of the electrical resistance was considered as the failure criteria provided that five consecutive tests confirm the results [34]. In this regard, the results of the drop experimental test can validate the FE simulation results as the main data supplier in the neural network. The experimental tests were adapted to the well-known standard JESD22-B111. One can find the drop height and the acceleration curve as follows based on the calculation in [9]:

$$A(t) = A_0 sin(\frac{\pi t}{t_w})$$
$$\sqrt{2gh} = \frac{2A_0}{C}\frac{t_w}{\pi} \tag{1}$$

where A(t) represents the time-dependent acceleration of the moving part (A_0 is the maximum acceleration), h and g are the

drop height and gravity force, respectively. C is the rebound coefficient and t_w is the dropping duration. All the parameters are in SI units.

C. FATIGUE LIFETIME MODEL

Since the mechanical properties such as bending stiffness of the PCB, solder interconnections and BGA chip is different from each other, peel/push and shear stresses at the interconnection interface is induced [19]. However, the amount of created shear stress is lower than the peeling stress. The shear stress is originated from the lateral displacement of The BGA chip and the PCB which has less significant in the drop test [35]. The peeling stress is originated from the bending impacts of the PCB and the BGA chip. Accordingly, the bending effect is known as the root cause of inducing stress in the solder interconnection. In this regard, the maximum peeling stress has to be included in the lifetime modeling of the solder joint. An exponential fatigue lifetime equation is able to characterize the behavior of the solder joints under drop impacts provided that the curve-fitting coefficients are well estimated. In this regard, it was widely reported that the peeling stress can be considered as an index in evaluating the lifetime of the solder joints in the electronic devices [21], [19], [36]. Accordingly [19],

$$N_{10\%} = \alpha \sigma_z^{\beta} \tag{2}$$

where $N_{10\%}$ is the number of drops to failure for 10% failure rate, σ_z represents the average of the maximum peeling stress in the solder joint in MPa, and α, β are the constant coefficient of the fatigue model. The constant values of the fatigue lifetime equation are listed in Table 2. The maximum peeling stress is directly extracted from FE simulations. Thus, one can find the solder joint lifetime from equation (2).

TABLE 2. Constants for SAC 105 and SAC 1205N fatigue lifetime model of equation (2) [19].

Material	α	β
SAC105	1350000	-2.345
SAC1205N	12153	-1.035

III. III PROPOSED NEURAL NETWORK FOR LOW-CYCLE FATIGUE SOLDER JOINT LIFETIME ESTIMATION

Artificial intelligence has been widely used as a prediction model in many applications [37], [38], [39]. However, it has been recently become popular in the reliability assessment of power electronic components [40], [41]. In this study, we established our proposed method based on the fully connected deep neural network. Four consecutive steps constitute the main machine learning process, which is illustrated in **Figure 4a**. The first step is to collect an adequate amount of data. The raw data for training the neural network is one of the most important parts of a machine learning algorithm. The more the data collected, the more reliable the outputs of the neural network are. In this study, four main data categories, namely location of the electronic package on the PCB, solder joint geometry, solder joint chemical composition, and PCB thickness, are considered as the most effective input data. As it was previously mentioned, there exist 480 FE simulations with different conditions so that the wide range of data can improve the training process and help the global lifetime model to be more accurate in real applications. In the second step, the input data is sorted and applied to the fatigue life model to calculate the number of cycles to failure in each dataset. This process may purify the contributory input and target data for network training. In the next step, the data (either the input or target) are normalized to maximize the performance of the trained neural network [40], [41], [42]. In this regard, the following min-max range scaling is used to normalize the data into a predefined range of [a, b]:

$$x_{new} = a + \frac{(b-a)(x - min(x))}{max(x) - min(x)} \tag{3}$$

where *min(.)* and *max(.)* are the functions to extract the minimum and the maximum values of a vector, respectively, and x_{new} is the rescaled value of the associated x data. As reported in [40], the scaling maximum value (b) of lower than 1 would lead to the best training results. To obtain the best range for scaling the input data, several training processes were performed with different scaling ranges. In this regard, the ranges were considered as [α (1-α)] where the α, scaling parameter, varied from 0 to 0.4 by steps of 0.05. For each of the defined range, a training process was performed and its determination factor (r) and root mean square error (RMSE) were calculated. **Figure 4b** demonstrates the results of this training processes. As shown, the RMSE minimized and r maximized in the scaling parameter of $\alpha = 0.2$. Accordingly, the range [a, b] is considered as [0.2, 0.8] for the training process. In the last step, a fully-connected neural network (FCNN) has been used for lifetime estimation of the solder joint under the drop impacts. The structure of the FCNN is depicted in **Figure 4c**. As shown in this figure, four input features including solder joint chemical composition, solder joint volume, radial displacement of the BGA device from the PCB center, and the PCB thickness are inserted into the FCNN with three hidden layers. Each layer has its own specific number of neurons which are biased by the previous layer outputs and a set of weight factors (ω_1- ω_3). The output parameter (solder joint useful lifetime) is extracted from the last hidden layer through the output weights (ω_o). There exist several machine learning-based algorithms in mapping input data to the target such as linear, nonlinear, and ensemble methods [40], [43]. Neuron and the layer numbers in the FCNN play vital roles in the performance and accuracy of the trained neural network. In this study, several numbers of neurons and layers and their combination thereof were considered and the best fitted one in terms of computational time and accuracy was selected as the FCNN architecture. Accordingly, three hidden layers with the number of neurons of [23], [30], [34] were employed for designing of machine

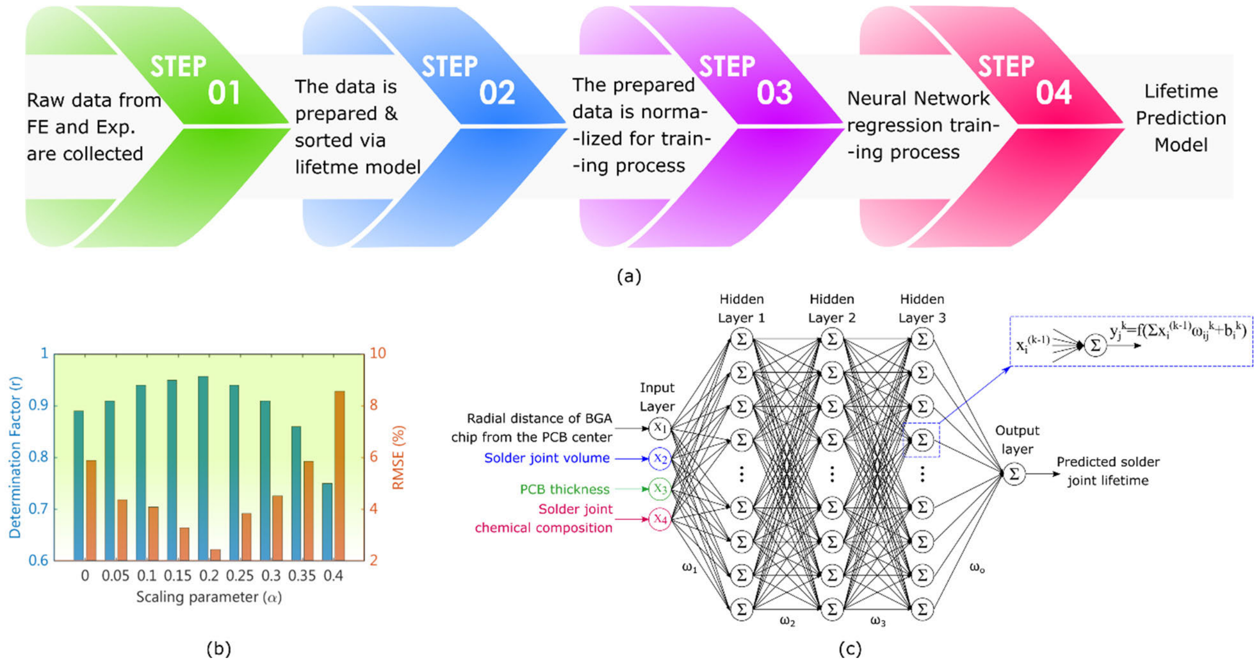

FIGURE 4. Descriptive procedure of lifetime estimation of the solder joint under drop tests using neural network, a) the schematic indication of the main steps in extraction of the lifetime prediction model for BGA electronic devices and b) performance of training process with the variation of the scaling parameter and c) fully connected neural network.

learning-based lifetime estimator. The input layer has four neurons since we have four contributory factors including solder joint chemical composition, solder joint volume, radial displacement of the BGA device from the PCB center, and the PCB thickness. The output layer consists of one neuron since the target is the solder joint useful lifetime. As shown in **Figure 4a**, the normalized processed input data are inserted into the FCNN through three hidden layers to minimize the solder joint lifetime estimation and the target. The information of each hidden layer comes from the previously processed data from the previously hidden layer which can be formulated as follows:

$$\gamma_i^{\ell} = f\left(\sum_{j=1}^{N_{\ell-1}} \omega_{ij}^{l}\, \gamma_i^{\ell-1} + b_i\right) \quad i = 1, \ldots, N_\ell \tag{4}$$

where γ_i^l is the output of the ith neuron in the lth layer. ω_{ij}^l and b_i are the weight and bias matrices that are in charge of mapping input data to the target data with the minimum error during the training process and will be tuned during FCNN training. N_l is the number of the lth layer. f is the Sigmoid activation function. During the back-propagation training process, two major indices including determination factor (r) and root mean square error (RMSE) was employed to optimize the FCNN performance. They are formulated as follows [40]:

$$r = \sqrt{\sum_{i=1}^{n} \left(\hat{y}_i - \bar{y}\right)^2 \Big/ \sum_{i=1}^{n} \left(y_i - \bar{y}\right)^2}$$

$$RMSE = \sqrt{\sum_{i=1}^{n} \frac{1}{n} \left(\hat{y}_i - y_i\right)^2} \tag{5}$$

where $\hat{y}_i$, y_i and $\bar{y}$ are predicted, actual, and the mean value of the actual output, respectively. r=1 represents the perfect regression while r=0 represents the most deviated regression modeling.

IV. RESULTS AND DISCUSSION

In this section, the results of the experimental tests and FE simulations will be discussed. It will be shown that the experimental and FE simulation results are in compliance with each other and therefore it is reasonable to utilize FE simulation results in neural network training of the solder joint lifetime estimation. Experimentally, the number of cycles to failure of the BGA chip was directly obtained from the experimental tests based on the well-known standard JESD22-B111 in different conditions. In this study, twenty experimental drop tests were performed in different conditions and their numbers of cycles to failure were extracted based on the previous mentioned failure criterion. The number of cycles to failure was also estimated from eq. (2) based on the calculated maximum peeling stress in the solder joint base on the FE simulations. The FE and the experimental results are shown in **Figure 5**for the similar conditions. The RMSE of the results between FE and experimental data sets are calculated as 6.8%. Therefore, one can obtain that FE results are in a good agreement with the experimental results.

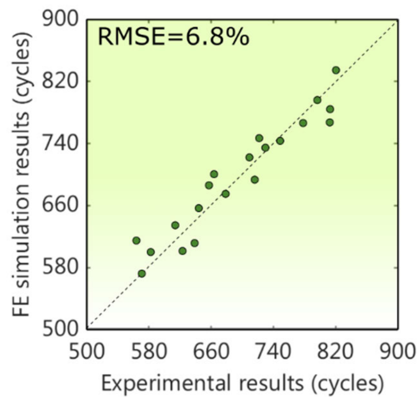

FIGURE 5. Experimental results versus FE simulation results for the similar conditions. The root mean square error of the results showed a good compliance between these two sets of results.

The FE simulations fell into two main categories, global FE exploitation, and detailed simulation. In the first category, Since the dimensions of the FE model were too large and it was too time-consuming for performing the FE simulations, a set of FE simulations with a low number of meshes was designed to primarily exploit the vulnerable parts of the electronic devices in the lower time consumption. It allowed us to create a FE model with the coarse meshes in the uncritical zones while finer meshes were used in the vulnerable and critical zones. The critical parts with the highest equivalent plastic strains in the electronic device were related to the corners of the BGA electronic component in the outermost row especially those near the center of the PCB as also reported in the previous studies [12], [23], [29]. In the second category with the optimized mesh size in the critical zones, 480 FE simulations with the different initial conditions were performed. As an example, **Figure 6a** and **Figure 6b** demonstrate the distributions of the creep strain and the maximum peeling stress in the most critical solder joint under high G-drop impacts for both solder joint compositions, respectively. It reveals that the most critical site is the boundary between the PCB/package and the solder joint. The maximum creep strain is located on the above-mentioned critical site (failure site). The creep strain dramatically decreases going through the central body of the solder joint. This strain concentration on the surface of the solder joint interconnection is said to be the primarily driven force in the crack initiation and propagation through the solder joint and the PCB [13], [44], [22]. The solder joints were exposed to the bending force induced by different materials and physical properties of diverse parts in the electronic circuit. The creep strain domination in the solder joint interface was originated from the fact that the bending stiffness and the physical properties of the materials in FE simulation are different from each other. The more difference is evident in these parameters; the more accumulated inelastic strain is induced in the solder joint.

The FE results for the different conditions are illustrated in **Figures 6c** to **6e**. As it was mentioned, four contributory factors are considered in this study, namely solder joint chemical composition, solder joint volume, BGA electronic device displacement, and PCB thickness from the center of the PCB. **Figure 6c** demonstrates the effects of the solder joint volume on the induced plastic strain in the most critical solder joint. It can be clearly seen that the trend of the plastic strain significantly decreases by the solder joint volume increase in both solder joint chemical compositions. The solder joint experienced its maximum induced plastic strain, $6.0{*}10^{-3}$ and $5.2{*}10^{-3}$ for SAC105 and SAC1205N respectively, in the minimum considered solder joint volume. The trend has been slightly decreased by more decrease in the solder joint volume. It means that by the volume decrease, the decreasing slope has become slow and saturated. The trend of decreasing for both solder joint chemical compositions is roughly the same with a slight change in the rate of decrease of the induced plastic strain in $5.2{*}10^{-3}$ for SAC105 and SAC1205N, respectively. It originates from the fact that the inelastic strain energy density in the solder joint depends on the solder joint volume provided that the applied loading keeps constant during all FE simulations which is the case. Accordingly, by decreasing the solder joint volume the strain energy density significantly climbed which is leading to more deformation of the solder ball, especially in its interconnections. The induced plastic strain in the solder joint under different radial displacements of the BGA component from the PCB center is illustrated in **Figure 6d**. In the same case, the plastic strain was reduced from its maximum value to its minimum value by displacement rise in the FE simulations. However, above the 50% of rated displacement, the trend is leveled out for both solder joint chemical compositions. The strains have a similar trend manner in both solder joint chemical compositions with just a decreasing drift in the SAC105. The trends experience a more rapid decrease in the case of displacement decrease rather than that of solder joint volume under their 50% rated values. In other words, the effects of BGA chip displacement from the PCB center on the induced plastic strain are more than that of the solder joint volume. The dependence of the induced plastic strained in the different displacement is originated from the fact that the induced stress in the BGA chip increases when it exposes to the maximum bending at the center of the PCB. By going farther from the PCB center, the normal bending force on the BGA chip decreases leading to more decrease in the solder joint plastic strain. The effects of the PCB thickness on the induced plastic strain in the most critical solder joint is depicted in **Figure 6e**. By increasing the PCB thickness, the plastic stain in the solder ball first increased and after a certain PCB thickness with the maximum induced strain, the trend experience a decreasing slope in both solder joint compositions (the solder joint volume is 3.3mm^3 and the displacement is 0mm). The maximum induced plastic strain is $6.2{*}10^{-3}$ and $5.9{*}10^{-3}$ for SAC105 and SAC1205N, respectively at PCB thickness of 1.4mm. The lowest and highest value of the induced plastic strain

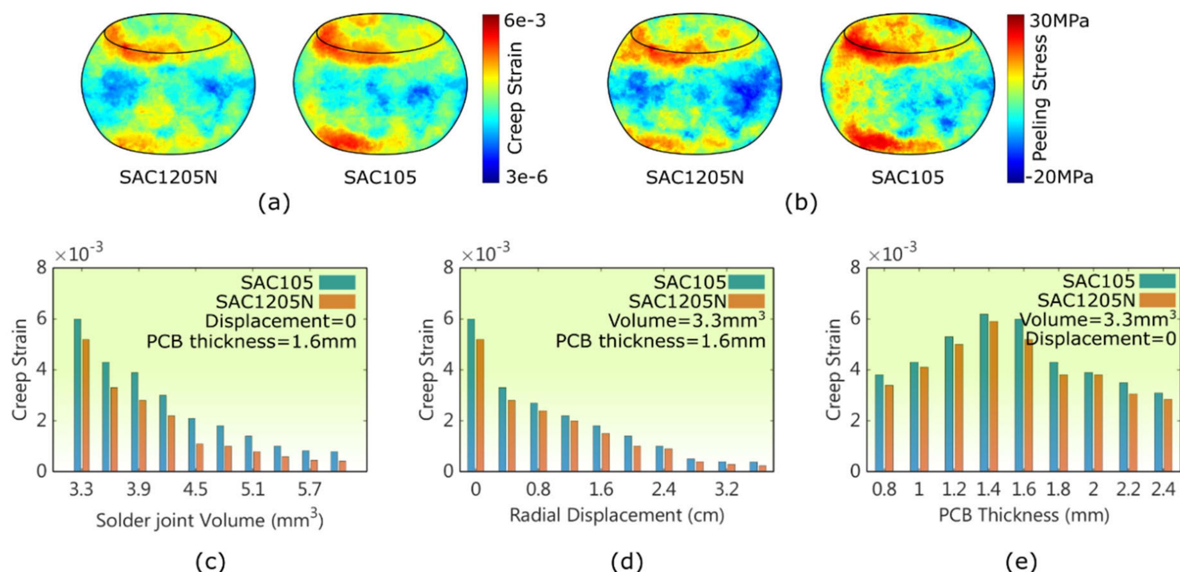

FIGURE 6. FE simulation results regarding various parameters' variations. a) creep strain in the most vulnerable solder ball in the BGA chip (the ball on the corner of the BGA chip), b) maximum peeling stress in the most vulnerable solder ball in the BGA chip (the ball on the corner of the BGA chip), c) creep strain variation versus variation of the solder joint volume while the BGA chip is mounted at the PCB center, and the PCB thickness is 1.6mm, d) creep strain variation versus variation of the chip radial displacement while the solder joint volume is fixed and equals to 3.3mm^3, and the PCB thickness is 1.6mm and e) creep strain variation versus variation of the PCB thickness while the BGA chip is mounted at the PCB center and the solder joint volume is fixed and equals to 3.3mm^3.

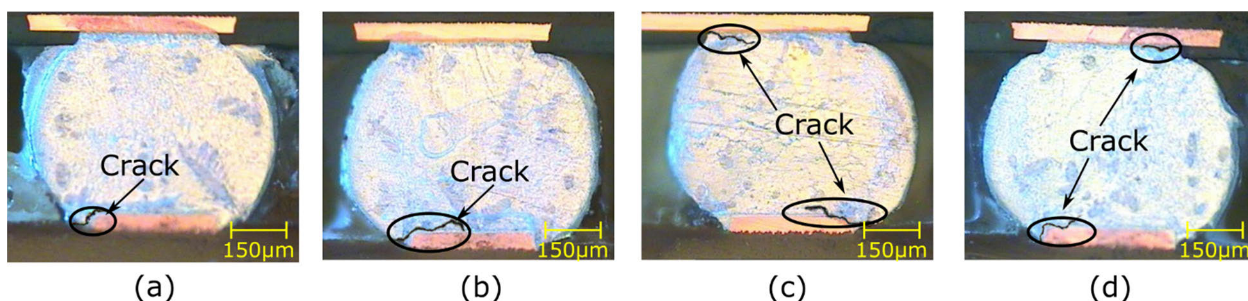

FIGURE 7. Optical images of the most vulnerable solder ball in the BGA chip (PCB thickness is 1.6mm), a) SAC1205N solder joint with the solder joint volume of 6mm^3 and radial displacement of 3.6 cm, b) SAC105 solder joint with solder joint volume of 6mm^3 the radial displacement of 3.6 cm, c) SAC105 solder joint with the radial displacement of 0 cm and solder joint volume of 3.3mm^3 and d) SAC1205N with the solder joint volume of 3.3mm^3 and radial displacement of 0cm.

is limited to $3.1*10^{-3}$-$6.2*10^{-3}$ and $2.85*10^{-3}$-$5.9*10^{-3}$ for SAC105 and SAC1205N, respectively. Regarding these ranges, the effects of the PCB thickness on the plastic strain of the solder joint is lower than the other contributory factors, namely displacement of the BGA chip from the center and solder joint volume. As stated in the previous studies, the root cause of the interconnect failure is PCB bending in the drop impacts. In the low stiffness PCB (lower PCB thickness), the PCB compromise and kink locally where at the interconnection zone. In fact, the thinner PCB can become in the shape of the BGA chip [45]. Accordingly, less stress would be applied to the solder joint. By PCB stiffness increase and reaching a certain PCB thickness, the maximum stress would be induced in the interconnection. By increasing the PCB thickness more than this certain thickness, however, lower relative motion would be occurred between the PCB and the BGA chip. Thus, the interconnection would experience less stress [46].

The experimental results of the drop tests are shown in **Figure 7** for different conditions for the most vulnerable solder joint. The drop tests were stopped whenever a 10% resistance increase was measured in the solder joint daisy chain via applying a DC voltage and measuring the induced current ($R=V_{DC}/I_{meas}$). As shown in this figure, the crack initiations and propagations are evident in the interface of the solder joint and the PCB surface. The location of the failure in the solder joint (crack initiation at the interface) complies with the maximum creep strain in the FE simulations. The crack propagation is more penetrated the solder ball in the case of using SAC105 rather than SAC1205N leading

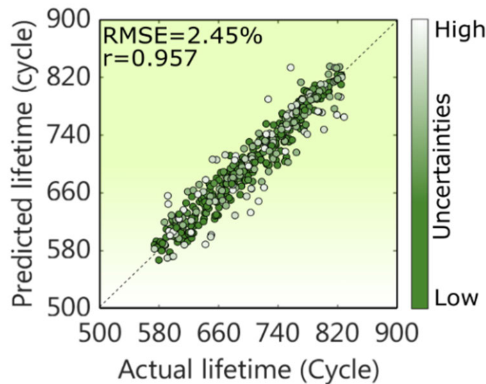

FIGURE 8. Performance of the proposed machine learning based prediction model for the solder joint lifetime estimation in the BGA chips under drop tests.

to the more accelerated fatigue damage of the solder joint. It was reported that inhomogeneous elemental distribution in the solder joint as well as intermetallic growth at the interface would be created under the drop tests [30]. This heterogeneity and intermetallic growth were lower in SAC1205N in comparison with the SAC105. In addition, the bonding behavior in the case of using SAC1205N was better which improves the tolerance of the solder joint under the drop test. The inherent physical properties of the SAC 1205N listed in Table 1 also confirmed the strength of the SAC1205N against the bending effect under the drop test. As shown in **Figure 7**, the solder joint volume and the location of the BGA chip both affected the tolerance of the solder joint under the drop test. The results can be compared with the extracted results from FE simulations. Accordingly, one can observe that the crack propagations were deeper in the case in which the solder joint volume is lower and the BGA chip displacement is closer to the PCB center. The results were proved with FE simulation results as shown in **Figures 6c** and **6d**. The performance of the proposed neural network predictive model is the primary task to be performed to investigate whether the model has acceptable results. **Figure 8** demonstrates the predicted versus the measured and simulated (actual) solder joint lifetimes. As it was mentioned three hidden layers with the neuron numbers of [23], [30] and [34] constituted the architecture of the neural network. This architecture was chosen as a trade-off between training time and the accuracy of the prediction. As shown in **Figure 8**, the RMSE of the prediction model was limited to 2.45%, and the determination coefficient r is 0.957 which shows a good integration among the predicted values. Generally, it can be easily seen that the proposed prediction model represents a sound performance in the solder joint lifetime estimation under the drop impacts. The training time for 420 data (extracted from experimental tests and FE simulations) was limited to 368s. In real applications, the quantitative contributory parameters may experience some uncertainties. Accordingly, a deviation of 10% was considered for three of our contributory parameters including solder joint volume, radial displacement of the BGA chip from the PCB center and the PCB thickness to capture the effects of uncertainties. The effects of uncertainties' degrees are illustrated with the color palette on the right side of **Figure 8**. The more deviated from the considered value, the lightest the color map is. As shown, one can find that the parameters with more uncertainty have led to more deviated results from the determination line shown with a dashed line. It should be noted that by enriching training data, a more accurate performance might be attained even considering the parameters' uncertainties.

In this part, the effects of the solder joint volume on the lifetime estimation of the electronic devices will be discussed. **Figure 9** depicts the predicted lifetime of the solder joint versus solder joint volume for two considered solder joint compositions. The **Figure 9a** shows the predicted results while the considered solder joints were SAC1205N and the **Figure 9b** indicates the predicted results in which the SAC105 solder joints were considered. For each solder joint volume, ten displacements of the BGA chip from the PCB center and nine PCB thicknesses were randomly selected and shown in the figure. The solder joint lifetime estimation shows an increasing trend while the solder joint volume increases. More obviously, the increasing trend in the solder joint lifetime is much more in the SAC1205N. Generally, the predicted results elucidate that SAC1205N solder joints were more resistant against the drop impacts. The inherent physical properties of the SAC1205N in comparison with SAC105 confirm the strength of the SAC1205N against the bending effect under the drop test. Additionally, the elemental distribution heterogeneity and intermetallic growth were lower in SAC1205N in comparison with the SAC105 [19]. As mentioned, the effects of the solder joint volume stick to the fact that the strain energy density becomes higher by decreasing the solder joint volume. The strain energy density, then, directly leads to more deformation in the solder joint which may either initiate or propagate cracks in the solder ball.

The fatigue behavior of the solder joint as a function of radial displacement of the BGA device from the PCB center will be discussed. **Figures 10a** and **10b** illustrate the predicted fatigue lifetime of the solder joints in the different locations of the PCB for SAC1205N and SAC105, respectively. For each radial displacement of the BGA chip, ten random solder joint volumes and nine PCB thicknesses were considered and their average value is depicted in **Figure 10**. In the first look, it is seen that the fatigue lifetime of the solder joint strongly depends on the solder alloy composition and the displacement of the solder joint from the PCB center. Moving from the PCB edge to the PCB center, one can find that solder joint lifetime decreases. This decrease is much more while moving from the PCB corners to the PCB center. This phenomenon is because the BGA device exposed to more bending force in the PCB center. The induced peeling stress as the main cause of damage in the BGA chip was maximized because of the bending effects of PCB and BGA chip. It is

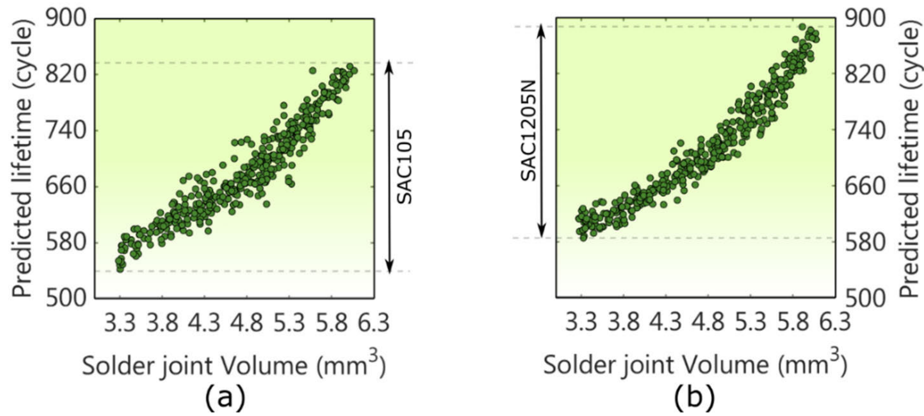

FIGURE 9. BGA chip lifetime estimation versus solder joint volume in different random radial displacement and PCB thickness for a) SAC105 and b) SAC1205N.

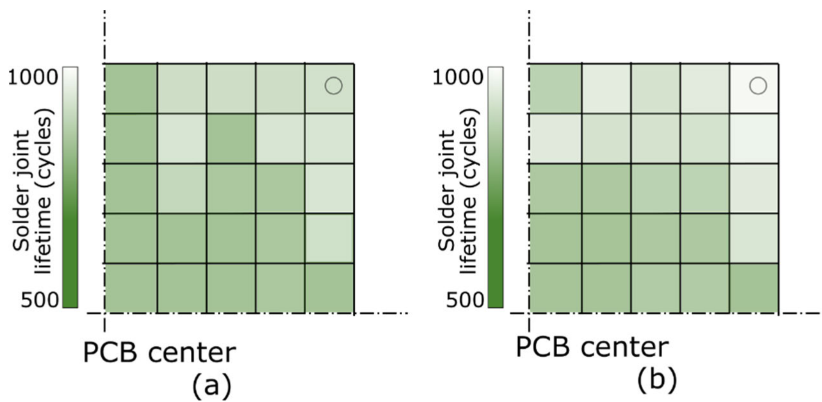

FIGURE 10. BGA chip lifetime estimation versus its radial displacement from the PCB center with the random solder joint volume consideration for a) SAC105 and b) SAC1205N.

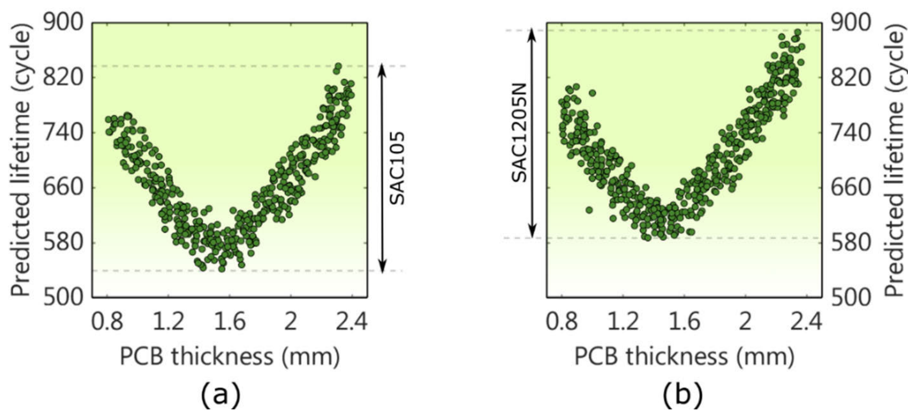

FIGURE 11. BGA chip lifetime estimation versus PCB thickness in different random radial displacement and solder joint volume for a) SAC105 and b) SAC1205N.

noted that the disparity of the neighboring results in **Figure 10** originates from the fact that the solder joint volume and the PCB thickness were randomly selected for each prediction.

The impacts of the PCB thickness on the lifetime estimation of the electronic devices will be discussed. **Figure 11** illustrates the predicted lifetime of the PCB thickness for two considered solder joint compositions. The **Figure 11a** demonstrates the predicted results while the considered solder joints were SAC1205N and the **Figure 11b** shows the predicted results in which the SAC105 solder joints were

considered. For each solder joint volume, ten displacements of the BGA chip from the PCB center and ten solder joint volumes were randomly selected and shown in the figure. Generally, the results reveal that SAC1205N has better performance in comparison with SAC105 solder interconnection in all PCB thicknesses owing to its better inherent physical properties. As it was predicted, the solder joint lifetime may not follow a monotonically trend. By increasing the PCB thickness, the solder joint lifetime decreases and after a certain PCB thickness it starts going up. The fact of this turning point in the lifetime of the solder joint was expressed in **Figure 6e**.

The maximum solder joint lifetime was estimated at 886 cycles which are occurred in the maximum solder joint volume and maximum displacement at the corner of the PCB. It is while that the minimum of the solder joint lifetime was estimated 543 cycles in which the BGA device was located at the PCB center, solder joint volume was at its maximum value and the SAC1205N solder joint was used. From the revealed results, one can obtain the importance of the contributory factors on the global solder joint lifetime using a machine learning-based lifetime estimation algorithm. Additionally, different combinations of the major factors on the reliability of the BGA chip is investigated and achieved by using the proposed approach thanks to the neural network capability. The proposed approach is limited to the four dominant contributory factors, namely the location of the electronic package on the printed circuit board (PCB), solder joint geometry, solder joint chemical composition, the PCB thickness. The current approach can be further developed by enriching the data base including other important parameters such as solder joint type (barrel- or hourglass-type), PCB material, other solder alloy compositions and loading conditions.

V. CONCLUSION

Evaluation of the BGA chip useful lifetime was investigated considering various contributory factors in the study. From the outcome of our investigation it is possible to conclude that the solder joint chemical composition, the BGA chip radial displacement from the PCB center, and the solder joint volume all play vital roles in the performance of the electronic circuits from a reliability point of view. This paper has clearly shown that the SAC1205N joint has better performance in comparison with the SAC105 joint. It is also revealed that the solder joint lifetime has been enhanced while its volume increases and the BGA chip is far from the PCB center. The proposed method can be readily used in the designing stage of the electronic circuits owing to its capability of simultaneous consideration of several contributory parameters.

REFERENCES

[1] Y. Bai, D. C. Nardi, X. Zhou, R. A. Picón, and J. Flórez-López, "A new comprehensive model of damage for flexural subassemblies prone to fatigue," *Comput. Struct.*, vol. 256, Nov. 2021, Art. no. 106639, doi: 10.1016/j.compstruc.2021.106639.

[2] X. Zhou, Y. Bai, D. C. Nardi, Y. Wang, Y. Wang, Z. Liu, R. A. Picón, and J. Flórez-López, "Damage evolution modeling for steel structures subjected to combined high cycle fatigue and high-intensity dynamic loadings," *Int. J. Struct. Stability Dyn.*, vol. 22, nos. 3–4, Mar. 2022, Art. no. 2240012.

[3] L. Liang, M. Xu, Y. Chen, T. Zhang, W. Tong, H. Liu, H. Wang, and H. Li, "Effect of welding thermal treatment on the microstructure and mechanical properties of nickel-based superalloy fabricated by selective laser melting," *Mater. Sci. Eng., A*, vol. 819, Jul. 2021, Art. no. 141507.

[4] J. Yan, H. Jiao, W. Pu, C. Shi, J. Dai, and H. Liu, "Radar sensor network resource allocation for fused target tracking: A brief review," *Inf. Fusion*, vols. 86–87, pp. 104–115, Oct. 2022.

[5] A. Li, D. Spano, J. Krivochiza, S. Domouchtsidis, C. G. Tsinos, C. Masouros, S. Chatzinotas, Y. Li, B. Vucetic, and B. Ottersten, "A tutorial on interference exploitation via symbol-level precoding: Overview, state-of-the-art and future directions," *IEEE Commun. Surveys Tuts.*, vol. 22, no. 2, pp. 796–839, 2nd Quart., 2020.

[6] J. Gu, J. Lin, Y. Lei, and H. Fu, "Experimental analysis of Sn-3.0Ag-0.5Cu solder joint board-level drop/vibration impact failure models after thermal/isothermal cycling," *Microelectron. Rel.*, vol. 80, pp. 29–36, Jan. 2018, doi: 10.1016/J.MICROREL.2017.10.014.

[7] A. L. Teoh, M. A. A. M. Salleh, D. S. C. Halin, K. L. Foo, N. R. A. Razak, H. Yasuda, and K. Nogita, "Microstructure, thermal behavior and joint strength of Sn-0.7Cu-1.5Bi/electroless nickel immersion gold (ENIG)," *J. Mater. Res. Technol.*, vol. 12, pp. 1700–1714, May 2021, doi: 10.1016/j.jmrt.2021.03.068.

[8] S. H. Ali, M. Heydarzadeh, S. Dusmez, X. Li, A. S. Kamath, and B. Akin, "Lifetime estimation of discrete IGBT devices based on Gaussian process," *IEEE Trans. Ind. Appl.*, vol. 54, no. 1, pp. 395–403, Jan. 2018, doi: 10.1109/TIA.2017.2753722.

[9] *Board Level Drop Test Method of Components for Handheld Electronic Products*, Standard JESD22-B111, JEDEC, Jul. 2003. [Online]. Available: http://scholar.google.com/scholar?hl=en&btnG=Search&q=intitle:Board+Level+Drop+Test+Method+of+Components+for+Handheld+Electronic#1

[10] F. Liu, G. Meng, and M. Zhao, "Experimental investigation on the failure of lead-free solder joints under drop impact," *Soldering Surf. Mount Technol.*, vol. 22, no. 3, pp. 36–41, Jun. 2010, doi: 10.1108/09540911011054172.

[11] J.-M. Kim, S.-W. Woo, Y.-S. Chang, Y.-J. Kim, J.-B. Choi, and K.-Y. Ji, "Impact reliability estimation of lead free solder joint with IMC layer," *Thin Solid Films*, vol. 517, no. 14, pp. 4255–4259, May 2009.

[12] A. Pearl, M. Osterman, and M. Pecht, "Evaluation of ENEPIG and immersion silver surface finishes under drop loading," *J. Electron. Mater.*, vol. 45, no. 1, pp. 391–402, Jan. 2016, doi: 10.1007/s11664-015-4104-y.

[13] V. Samavatian, A. Masoumian, M. Mafi, M. Lakzaei, and D. Ghaderi, "Influence of directional random vibration on the fatigue life of solder joints in a power module," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 9, no. 2, pp. 262–268, Feb. 2018, doi: 10.1109/TCPMT.2018.2838148.

[14] Y. H. Ko, S. Yoo, and C. W. Lee, "Evaluation of lead-free solder reliability under vibration at elevated temperature," *Int. J. Mater. Struct. Integr.*, vol. 8, no. 1/2/3, p. 53, 2014, doi: 10.1504/IJMSI.2014.064773.

[15] S.-J. Jeon, J.-W. Kim, B. Lee, H.-J. Lee, S.-B. Jung, S. Hyun, and H.-J. Lee, "Evaluation of drop reliability of Sn–37Pb solder/Cu joints using a high speed lap-shear test," *Microelectron. Eng.*, vol. 91, pp. 147–153, Mar. 2012, doi: 10.1016/j.mee.2011.09.006.

[16] A. Surendar, W. A. Siswanto, M. Alijani, K. Alhaifi, and M. Salmani, "High-G drop effect on the creep-fatigue failure of SAC solder joints in BGA packages," *Microsyst. Technol.*, vol. 25, no. 10, pp. 4027–4034, Oct. 2019, doi: 10.1007/s00542-019-04435-x.

[17] J. Tang and Z.-G. Yang, "Root causes analysis on malfunction of PCBA in smartphone," in *Proc. Int. Conf. Quality, Rel., Risk, Maintenance, Saf. Eng. (QR2MSE)*, Aug. 2019, pp. 1–6, doi: 10.1109/QR2MSE46217.2019.9021188.

[18] M.-L. Wu and J.-S. Lan, "Prediction of fatigue resistance in lead-free Ni-doped SAC 1205 solder alloys using a rate-dependent material model and subjected to drop tests," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 8, no. 10, pp. 1777–1787, Oct. 2018, doi: 10.1109/TCPMT.2018.2869248.

[19] M.-L. Wu and J.-S. Lan, "Reliability and failure analysis of SAC 105 and SAC 1205N lead-free solder alloys during drop test events," *Microelectron. Rel.*, vol. 80, pp. 213–222, Jan. 2018, doi: 10.1016/J.MICROREL.2017.12.013.

[20] X.-Y. Niu, W. Li, G.-X. Wang, and X.-F. Shu, "Effects of temperature and strain rate on mechanical behavior of low-silver lead-free solder under drop impact," *J. Mater. Sci., Mater. Electron.*, vol. 26, no. 1, pp. 601–607, Jan. 2015, doi: 10.1007/s10854-014-2441-x.

[21] S. Chung and J. B. Kwak, "Comparative study on reliability and advanced numerical analysis of BGA subjected to product-level drop impact test for portable electronics," *Electronics*, vol. 9, no. 9, p. 1515, Sep. 2020.

[22] J. Gu, Y. Lei, J. Lin, H. Fu, and Z. Wu, "The failure models of lead free Sn-3.0Ag-0.5Cu solder joint reliability under low-G and high-G drop impact," *J. Electron. Mater.*, vol. 46, no. 2, pp. 1396–1404, Feb. 2017, doi: 10.1007/s11664-016-5027-y.

[23] M. L. Huang and N. Zhao, "Effect of electromigration on the type of drop failure of Sn–3.0Ag–0.5Cu solder joints in PBGA packages," *J. Electron. Mater.*, vol. 44, no. 10, pp. 3927–3933, Oct. 2015, doi: 10.1007/s11664-015-3856-8.

[24] P. Zhang, S. Xue, and J. Wang, "New challenges of miniaturization of electronic devices: Electromigration and thermomigration in lead-free solder joints," *Mater. Des.*, vol. 192, Jul. 2020, Art. no. 108726, doi: 10.1016/j.matdes.2020.108726.

[25] T. Y. Tee, H. S. Ng, C. T. Lim, E. Pek, and Z. Zhong, "Impact life prediction modeling of TFBGA packages under board level drop test," *Microelectron. Rel.*, vol. 44, no. 7, pp. 1131–1142, Jul. 2004, doi: 10.1016/j.microrel.2004.03.005.

[26] K. Xia, Z. Zhu, H. Zhang, and Z. Xu, "Modeling simplification for thermal mechanical stress analysis of TSV interposer stack," *Microelectron. Rel.*, vol. 96, pp. 46–50, May 2019, doi: 10.1016/j.microrel.2019.03.008.

[27] H. Jiaxing, J. Bo, S. Zengjin, L. Fang, C. Yaojun, and Z. Yulin, "Failure and failure characterization of QFP package interconnect structure under random vibration condition," *Microelectron. Rel.*, vol. 91, pp. 120–127, Dec. 2018, doi: 10.1016/j.microrel.2018.08.011.

[28] O. Mülkoğlu, M. A. Güler, E. Acar, and H. Demirbağ, "Drop test simulation and surrogate-based optimization of a dishwasher mechanical structure and its packaging module," *Struct. Multidisciplinary Optim.*, vol. 55, no. 4, pp. 1517–1534, Apr. 2017, doi: 10.1007/s00158-016-1585-0.

[29] B. Singh, G. Menezes, S. McCann, V. Jayaram, U. Ray, V. Sundaram, R. Pulugurtha, V. Smet, and R. Tummala, "Board-level thermal cycling and drop-test reliability of large, ultrathin glass BGA packages for smart mobile applications," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 7, no. 5, pp. 726–733, May 2017, doi: 10.1109/TCPMT.2017.2684464.

[30] A. Surendar, K. H. Kishore, M. Kavitha, A. Z. Ibatova, and V. Samavatian, "Effects of thermo-mechanical fatigue and low cycle fatigue interaction on performance of solder joints," *IEEE Trans. Device Mater. Rel.*, vol. 18, no. 4, pp. 606–612, Dec. 2018, doi: 10.1109/TDMR.2018.2879123.

[31] S. Jing, M. Li, X. Li, and P. Yin, "Optimization of reflow soldering temperature curve based on genetic algorithm," *Energy Rep.*, vol. 7, pp. 772–782, Nov. 2021, doi: 10.1016/j.egyr.2021.09.195.

[32] S. Huang, J. Zeng, H. Zhou, Z. Liu, and Y. Zhou, "A near-field magnet peak values detecting method to locate short circuit points on PCB," *Int. J. Embedded Syst.*, vol. 9, no. 3, pp. 262–274, 2017.

[33] J. Wen, H. Yao, B. Wu, Z. Ji, L. Wen, M. Xu, Y. Jin, and X. Yan, "Dynamic analysis and structure optimization on trapezoidal wave generator for eliminating the over deviation of the residual wave in shock test measurement," *Measurement*, vol. 182, Sep. 2021, Art. no. 109665, doi: 10.1016/j.measurement.2021.109665.

[34] V. Samavatian, H. Iman-Eini, Y. Avenas, and M. Samavatian, "Effects of creep failure mechanisms on thermomechanical reliability of solder joints in power semiconductors," *IEEE Trans. Power Electron.*, vol. 35, no. 9, pp. 8956–8964, Sep. 2020.

[35] P. F. Fuchs, G. Pinter, and Z. Major, "PCB drop test lifetime assessment based on simulations and cyclic bend tests," *Microelectron. Rel.*, vol. 53, no. 5, pp. 774–781, May 2013.

[36] N. Jiang, L. Zhang, Z.-Q. Liu, L. Sun, W.-M. Long, P. He, M.-Y. Xiong, and M. Zhao, "Reliability issues of lead-free solder joints in electronic devices," *Sci. Technol. Adv. Mater.*, vol. 20, no. 1, pp. 876–901, Dec. 2019, doi: 10.1080/14686996.2019.1640072.

[37] G. Luo, Q. Yuan, J. Li, S. Wang, and F. Yang, "Artificial intelligence powered mobile networks: From cognition to decision," *IEEE Netw.*, vol. 36, no. 3, pp. 136–144, May 2022.

[38] G. Luo, H. Zhang, Q. Yuan, J. Li, and F.-Y. Wang, "ESTNet: Embedded spatial–temporal network for modeling traffic flow dynamics," *IEEE Trans. Intell. Transp. Syst.*, vol. 23, no. 10, pp. 19201–19212, Oct. 2022.

[39] D. Javaheri, S. Gorgin, J.-A. Lee, and M. Masdari, "An improved discrete Harris hawk optimization algorithm for efficient workflow scheduling in multi-fog computing," *Sustain. Comput., Informat. Syst.*, vol. 36, Dec. 2022, Art. no. 100787, doi: 10.1016/j.suscom.2022.100787.

[40] V. Samavatian, M. Fotuhi-Firuzabad, M. Samavatian, P. Dehghanian, and F. Blaabjerg, "Correlation-driven machine learning for accelerated reliability assessment of solder joints in electronics," *Sci. Rep.*, vol. 10, no. 1, p. 14821, Dec. 2020, doi: 10.1038/s41598-020-71926-7.

[41] V. Samavatian, M. Fotuhi-Firuzabad, M. Samavatian, P. Dehghanian, and F. Blaabjerg, "Iterative machine learning-aided framework bridges between fatigue and creep damages in solder interconnections," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 12, no. 2, pp. 349–358, Feb. 2022, doi: 10.1109/TCPMT.2021.3136751.

[42] J. Xiong, S.-Q. Shi, and T.-Y. Zhang, "A machine-learning approach to predicting and understanding the properties of amorphous metallic alloys," *Mater. Des.*, vol. 187, Feb. 2020, Art. no. 108378, doi: 10.1016/j.matdes.2019.108378.

[43] S. Sun, R. Ouyang, B. Zhang, and T.-Y. Zhang, "Data-driven discovery of formulas by symbolic regression," *MRS Bull.*, vol. 44, no. 7, pp. 559–564, 2019, doi: 10.1557/mrs.2019.156.

[44] T. T. Mattila and J. K. Kivilahti, "Reliability of lead-free interconnections under consecutive thermal and mechanical loadings," *J. Electron. Mater.*, vol. 35, no. 2, pp. 250–256, Feb. 2006, doi: 10.1007/BF02692443.

[45] E. H. Wong, K. M. Lim, N. Lee, S. Seah, C. Hoe, and J. Wang, "Drop impact test—Mechanics & physics of failure," in *Proc. 4th Electron. Packag. Technol. Conf.*, 2002, pp. 327–333, doi: 10.1109/EPTC.2002.1185692.

[46] A. Agrawal, T. Levo, J. Pitarresi, and B. Roggeman, "Board level energy correlation and interconnect reliability modeling under drop impact," in *Proc. 59th Electron. Compon. Technol. Conf.*, May 2009, pp. 1694–1702, doi: 10.1109/ECTC.2009.5074243.

REZA REIHANISARANSARI received the B.Sc. degree in electrical engineering from Shahid Beheshti University and the M.Sc. degree in photonics engineering from the Amirkabir University of Technology (Tehran Polytechnic). He is currently pursuing the Ph.D. degree in cancer diagnosis with the University of Houston. His research interests include optics, image processing, spectroscopy, and machine learning.

FARSHAD SAMADIFAM received the M.S. degree in mechanical engineering from the Isfahan University of Technology, Isfahan, Iran, in 2020. He is currently pursuing the Ph.D. degree in biomedical engineering with the Joint Department of Biomedical Engineering, Marquette University, and the Medical College of Wisconsin, USA. His research interests include improving/creating diagnostics using machine learning and deep learning.

ANAS A. SALAMEH has been an Associate Professor with the Department of Management Information Systems, College of Business Administration, Prince Sattam bin Abdulaziz University, since 2016, where he is currently the Deputy Director of the Students' Activities Committee as well as a member of the Exams Scheduling Committee. His research interests include e-commerce (m-commerce), e-business, e-marketing, technology acceptance/adoption, e-learning, e-CRM, and service quality, and he evaluated service quality in many areas related to e-services aspects.

FARZAM MOHAMMADIAZAR received the B.Sc. degree in electrical engineering from the University of Bonab, Iran, in 2019, and the M.Sc. degree in electrical engineering from the University of Tabriz, Iran, in 2022. His research interests include analog and RF integrated circuits design, power electronics, dc–dc boost converters, and micro-electromechanical systems.

NAFISEH AMIRI received the M.S. degree in electrical engineering from Tarbiat Modares University, Iran, in 2016. She is currently pursuing the Ph.D. degree in electrical and computer engineering with the University of Houston, Houston, TX, USA. Her research interests include plasmonic nanostructures and development of machine learning algorithms that can be used for nanoparticle detection and classification.

SITTIPORN CHANNUMSIN received the bachelor's degree in electronics engineering from the King Mongkut's Institute of Technology Ladkrabang (KMITL), Thailand, in 2006, the Master of Science degree in space technology and planetary exploration from the University of Surrey, in 2011, and the Ph.D. degree in aerospace engineering from the University of Glasgow, U.K., in 2016. He is currently the Director of the Space Technology Research Center, Geo-Informatics and Space Technology Development Agency (GISTDA). His research interests include spaceflight dynamics, space debris mitigation, machine learning, energy, and attitude and orbit control optimization. He serves as a co-editor and a technical reviewer.