IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received 23 October 2022, accepted 6 November 2022, date of publication 14 November 2022,
date of current version 6 December 2022.

Digital Object Identifier 10.1109/ACCESS.2022.3222331

RESEARCH ARTICLE

A 10-Bit, 600 MS/s Multi-Mode Direct-Sampling DAC-Based Transmitter

NAM-SEOG KIM, (Member, IEEE)
School of Information and Communication Engineering, Chungbuk National University, Cheongju 28644, Republic of Korea
e-mail: namseog.kim@cbnu.ac.kr

This work was supported by the National Research Foundation of Korea (NRF) grant funded by the Ministry of Science and Information and Communications Technology (MSIT) of South Korea Government under Grant number 2022M3F3A2A01044952. The EDA tool was supported by the Integrated Circuit Design Education Center (IDEC), South Korea.

ABSTRACT This paper presents a 10-bit, 600 MS/s direct-sampling sub-Nyquist rate DAC-based frequency-agile wideband transmitter for IEEE 802.22 cognitive radio applications in the VHF/UHF TV band (54 – 862 MHz). Multi-mode reconstruction using Gilbert cells, including non-return-to-zero, return-to-complement, and return-to-complement with reset, allows the DAC to utilize the image spectrum in the higher Nyquist zones for wideband direct synthesis. A two-dimensional decoder of the dynamic element matching is applied to reduce the correlated noise to the input signals. A multi-mode control signal generator uses a slack borrowing strategy to provide the transmitter's zero frequency hopping time without interference between the three modes to improve the quality of service of the cognitive radio system. A low-power supply-regulated PLL and a divided-by-2 circuit generates quadrature DAC sampling clock signals of 600 MHz to ensure a SDR of > 70dB. The proposed transmitter is fabricated in 65 nm CMOS within an active area of 0.3 mm^2, and it achieves a DNL of 0.12 LSB, an INL of 0.25 LSB, an SFDR of > 57 dBc, and IM3 of < −62 dBc in the TV band while consuming 19 mW.

INDEX TERMS Cognitive radio, complementary metal-oxide-semiconductor, current-steering, differential non-linearity, digital-to-analog converter, dynamic element matching, frequency hopping, IEEE 802.22, integral non-linearity, inter-modulation distortion, non-return-to-zero, phase-locked loop, return-to-complement, return-to-complement with reset, slack borrowing, spurious-free dynamic range.

I. INTRODUCTION

As wireless systems reach a point where they can better use their allocated spectrum to achieve the next largest capacity gain, increasing flexibility and efficiency in spectrum utilization becomes important. According to the spectrum utilization measurement from 30 MHz to 3 GHz in 24 hours [1], the spectrum usage experiences vast temporal and geographic variations ranging from 15 % to 85 %, which shows the evidence of low utilization in most of the spectrum and overcrowded situations in certain frequency bands as shown in Figure 1(a).

Cognitive Radio (CR) technology has been proposed to overcome the spectrum scarcity over a wide frequency range and exploits the spectrum occupancy information to provide wireless links [2]. The CR technology allows secondary users (SUs) to use unused licensed spectrum temporarily under the constraint of returning the band to primary users (PUs) when the PUs reuse the band, as shown in Figure 1(b). IEEE802.22 is a standard for wireless regional area networks (WRANs) that use the CR technology to operate on a license-exempt and non-interference basis in the spectrum allocated to TV broadcast bands (54-862MHz) [3]. It aims to provide alternative wideband wireless Internet access without causing harmful interference to licensed TV broadcasts. Although the CR system borrows the spectrum band of the PUs, it needs to assure the quality of service (QoS) satisfaction of SUs and reliable spectrum sensing to protect PUs. However, in non-hopping mode operation, communications are periodically interrupted for spectrum sensing, and the spectrum sensing time ranges from tens of milliseconds up to more than 0.1 seconds, so these interruptions degrade the QoS severely, especially for real-time or streaming applications.

The associate editor coordinating the review of this manuscript and approving it for publication was Francesco Benedetto.

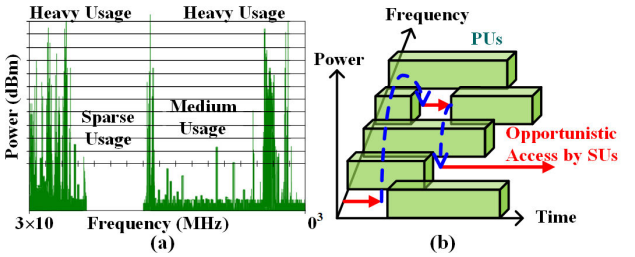


FIGURE 1. (a) Spectrum utilization between 30 MHz and 3 GHz in the US. Spectrum usage is concentrated on certain frequency bands and (b) a dynamic spectrum access concept in spectrum hole [1].

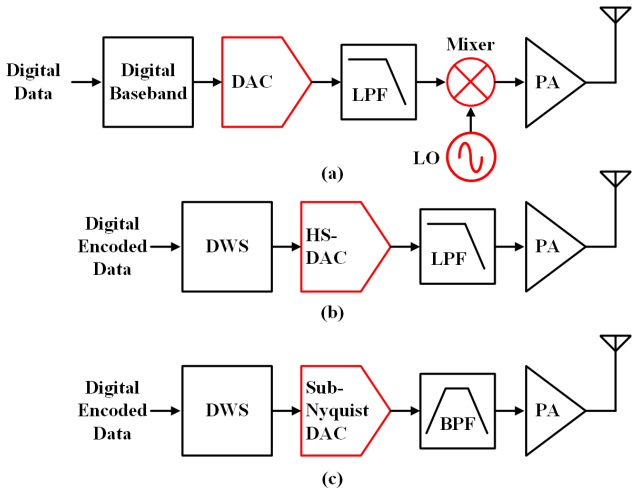


FIGURE 2. (a) Conventional transmitter and SWDR-type transmitter architecture with (b) a Nyquist rate high-speed DAC and (c) a sub-Nyquist rate DAC.

Dynamic frequency hopping (DFH) is proposed to improve the QoS in non-hopping mode. The spectrum sensing is performed in parallel on the next intended working channel while the CR device hops over a set of channels in the DFH [4]. Therefore, DFH can solve the problem of communication interruption in the non-hopping mode due to spectrum sensing time.

A conventional direct conversion transmitter block diagram is shown in Figure 2(a). The digital bitstreams are converted to analog signals by a digital-to-analog converter (DAC) in the baseband, and a mixer and a frequency synthesizer up-convert the analog baseband signals to RF frequency signals. The disadvantage of this transmitter architecture is that analog/RF front-end circuit up-conversion mixers and frequency synthesizers require wide tuning ranges and fast frequency hopping to the available spectrum in the TV band, which leads to complex analog/RF circuits and high-power consumption. Moreover, due to the long re-locking time of the frequency synthesizer as shown in Figure 3(a), it is difficult to provide seamless communication connectivity to assure QoS satisfaction while hopping channels for adapting to time-varying spectral environments.

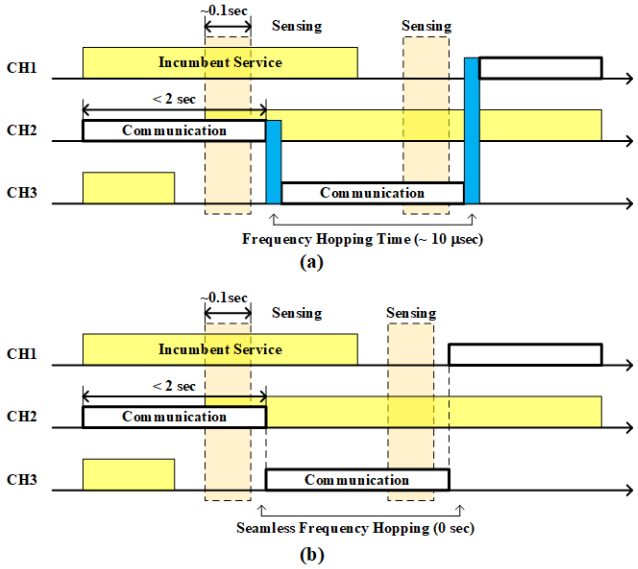


FIGURE 3. (a) The conventional and (b) the seamless dynamic frequency hopping mode with spectrum sensing and data transmission in IEEE 802.22.

Unlike the conventional analog/RF front-end architecture, the alternative approach adopts most digital implementations by placing digital circuits as close as possible to the antenna, a software-defined radio (SWDR) transmitter architecture for cognitive wireless applications, as shown in Figure 2(b). In the SWDR transmitter architecture, digital waveform synthesis (DWS) directly composites wideband RF waveforms without analog up-conversion blocks [5]. Thus, it achieves the best dynamic adaptation to the desired available spectrum. With advanced CMOS technology that fully controls waveforms in the digital domain, the transmitter can quickly switch to various modulation schemes and transmitter parameters while ensuring seamless connectivity with agile reconfiguration. The synthesized discrete waveform samples are directly converted into continuous-time analog waveforms at the sampling rate of f_{DAC} by a high-speed digital-to-analog converter (HS-DAC). However, the main challenge of this architecture is the drastic increase in the difficulty of the DAC for wideband applications. A low pass filter (LPF) is added for an anti-aliasing filter that follows the Nyquist rate DAC. The f_{DAC} should be at least twice the highest frequency component in the target synthesized signal frequency to meet the Nyquist rate requirement. The SWDR transmitter having a sub-Nyquist rate DAC can overcome the disadvantages of the Nyquist rate DAC. the DAC exploits the image spectrum with lower power consumption compared to the Nyquist rate DAC since the f_{DAC} is lower than the Nyquist rate [6]. A tunable band-pass filter (BPF) extracts a high-order image spectrum that can be used as synthetic RF waveforms from the sub-Nyquist rate DAC as shown in Figure 2(c).

In this paper, a 10-bit, 600 MS/s direct-sampling current steering DAC-based frequency-agile wideband transmitter

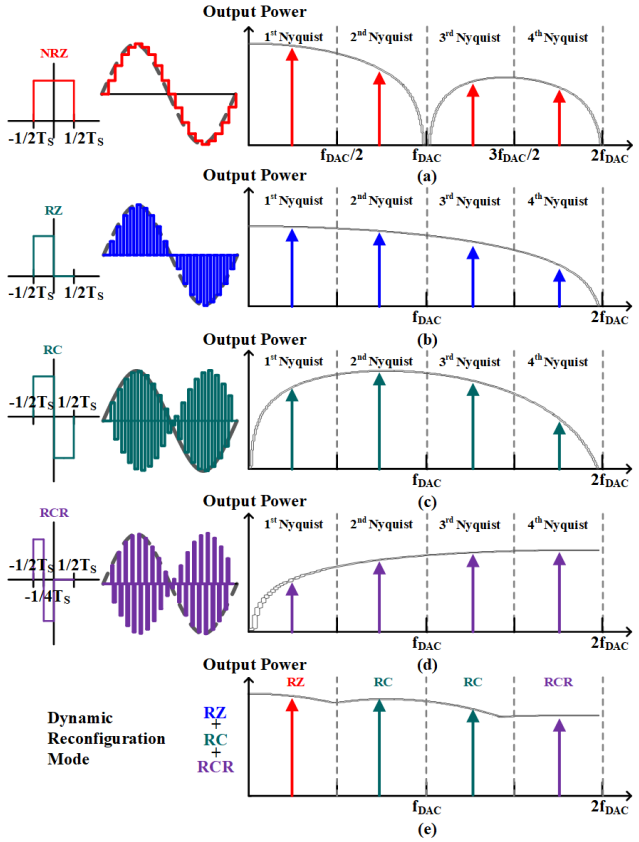


FIGURE 4. Multi-mode sub-Nyquist rate DAC operations of (a) NRZ, (b) RZ, (c) RC, (d) RCR, and (e) dynamic reconfiguration mode.

is presented to support zero dynamic frequency hopping time for IEEE 802.22 cognitive radio applications in the VHF/UHF TV band (54 – 862 MHz), as shown in Figure 3(b). Multi-mode reconstruction allows the DAC to utilize the image spectrum in the higher Nyquist zones for wideband direct synthesis. The multi-mode control signal generator uses a slack borrowing strategy to provide zero frequency hopping time to the transmitter without interference between multi-modes for QoS satisfaction. A low-power frequency synthesizer that is insensitive to supply noise generates a low jitter f_{DAC} of 600 MHz. The remainder of this article is organized as follows. Section II discusses the transmitter architecture design in terms of multi-mode DAC architecture, resolution, sampling frequency, and jitter performance. Section III describes a circuit design focusing on a high-linearity DAC array, a multi-mode current switch cell, a seamless DAC mode controller, and a low-jitter sampling clock generator for the TV band transmitter. Section IV delineates measurement results and comparisons, and Section V concludes this paper.

II. TRANSMITTER ARCHITECTURE

A. DAC ARCHITECTURES

A conventional DAC type is non-return-to-zero (NRZ) mode. The NRZ DAC with an inherent SINC amplitude roll-off attenuates the image spectrum in the higher Nyquist zone and creates a dead zone near the null frequency of multiples of the f_{DAC}. Thus, direct wideband synthesis across all Nyquist zones is not possible with the NRZ DAC only, as shown in Figure 4(a). The frequency response of NRZ DAC can be expressed as equation (1) [7].

$$|H_{NRZ}| = SINC(f_{OUT}/f_{DAC}) \tag{1}$$

Therefore, wideband Nyquist rate synthesis requires the f_{DAC} above GHz, which leads to huge power consumption. Moreover, high-speed DACs require the stringent jitter performance of f_{DAC}. The power dissipated in the wideband front-end stage as well as sensitivity and gain requirements for these blocks are also important. Finally, the area and power consumption burden incurred by the digital signal processing and demodulation blocks must also be considered.

Return-to-zero (RZ) DACs can be used in the SWDR transmitter architectures to provide sufficiently large signal power in the higher Nyquist zone than NRZ DAC transmitters as shown in Figure 2(b). The RZ DAC evaluates the output signal with input encoded data for a one-half cycle of the evaluation period, and the output goes to zero status for the remaining half cycle of the reset period. Then, the null frequency of the SINC attenuation shifts by twice that of the NRZ DAC and the flatter envelope of the RZ DAC results in less droop distortion in the higher Nyquist zone, as shown in Figure 4(b). The frequency response of the RZ DAC can be expressed as equation (2) [8].

$$|H_{RZ}| = 0.5 \cdot SINC(f_{OUT}/2 \cdot f_{DAC}) \tag{2}$$

The output power of the RZ DAC at the image frequency is higher than that of the NRZ DAC, followed by a tunable bandpass filter to select the image frequency component. It also eliminates the need for SINC amplitude roll-off compensation with filters or equalizers in conventional SWDR transmitters. Therefore, the RZ DAC transmitter allows lower power consumption than the NRZ DAC transmitter. The magnitude of the fundamental spectrum and its images is reduced compared to the NRZ DAC transmitter since the shorter holding pulse contributes less signal energy at the first Nyquist zone but delivers more power at the second and third Nyquist zones.

Return-to-complement (RC) DACs can boost the magnitudes of the images in the second and third Nyquist zones compared to the RZ DAC at the expense of underlying fundamental tone magnitude. The image spectral magnitude is enhanced due to the inverted output, especially around the f_{DAC}. RC DAC has the same evaluation period as the RZ DAC but sets the inverted output during the reset period of the RZ DAC as shown in Figure 4(c). The frequency response of the RC DAC can be expressed as equation (3) [9].

$$|H_{RC}| = SINC(f_{OUT}/2f_{DAC}) \cdot sin(\pi f_{OUT}/2f_{DAC}) \tag{3}$$

Return-to-complement with reset (RCR) DACs reduce the bipolar pulse duration of the RC DAC in half and utilize a

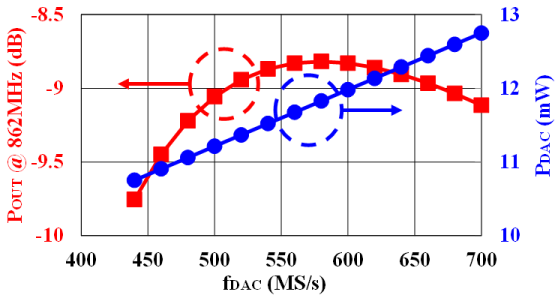


FIGURE 5. Spectral magnitude of the RCR DAC at 862 MHz.

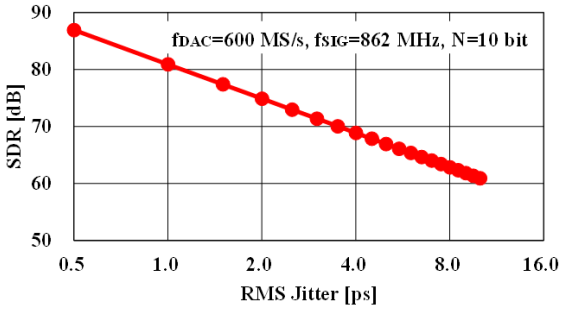


FIGURE 6. SDR of the 600 MS/s 10-bit DAC with RMS jitter.

reset period for the other half cycle. This allows the RCR DAC to flatten the frequency response across of the third and fourth Nyquist zones and to provide the highest output magnitude in the fourth Nyquist zone of the four DAC modes as shown in Figure 4(d). The frequency response of the RC DAC can be expressed as equation (4) [9].

$$|H_{RCR}| = 0.5SINC(f_{OUT}/4f_{DAC}) \cdot sin(\pi f_{OUT}/4f_{DAC}) \quad (4)$$

Therefore, dynamic reconfiguration of the NRZ mode in the first Nyquist zone, the RC mode in the second and third Nyquist zones, and the RCR mode in the fourth Nyquist zone can achieve a wide frequency response in the TV broadcast band (54-862MHz) with low-power consumption as shown in Figure 4(e).

B. DAC RESOLUTION AND SAMPLING FREQUENCY

Each country defines a channel bandwidth of 6, 7, or 8 MHz according to its own IEEE 802.22 standard. The emission spectrum of a CR device on an adjacent channel of the operating frequency must be at least 55 dB below the highest average power of that band [10]. This indicates that the adjacent channel power ratio (ACPR) requirement for adjacent channels is −55 dBr, and the DAC should have a resolution of at least 10 bits to support the IEEE 802.22 standard modulation scheme such as QPSK, 16-QAM, and 64-QAM.

The DAC sampling frequency of the f_{DAC} is defined in consideration of the spectrum magnitude (P_{OUT}) at the maximum frequency of the TV band (862 MHz) and the power consumption of the multi-mode sub-Nyquist DAC. The f_{DAC} should be > 430 MHz to support the 862 MHz image spectrum at the fourth Nyquist zone. The power consumption (P_{DAC}) of the N-bit current-steering DAC consists of analog blocks in the N-bit DAC, switch transistors of the current steering DAC, and digital blocks for the clock and timing circuitry. The P_{DAC} is expressed as equation (5) when operating at the Nyquist rate with a switching activity factor of 0.5.

$$P_{DAC} = (2^N - 1)[(V_{AVDD} \cdot I_{UNIT}) + C_T \cdot V_{DVDD}^2 \cdot f_{DAC}] \quad (5)$$

where V_{AVDD} is the analog supply voltage, I_{UNIT} is the DAC unit current, C_T is the total capacitance of the switching and clocking paths, and V_{DVDD} is the digital supply voltage. P_{DAC} increases linearly with f_{DAC} due to the mixed-signal and digital parts. Therefore, it is possible to reduce the P_{DAC} by using the lowest acceptable f_{DAC} of the sub-Nyquist DAC. Figure 5 shows the spectral magnitude of the RCR DAC at 862 MHz with equation (4). The spectral magnitude peaks at around 600 MS/s, so an f_{DAC} of 600 MS/s provides the best spectral envelope over the entire TV band, taking power consumption into account.

C. TIME DOMAIN ERRORS

A DAC performance is also limited by the uncertainty of the f_{DAC} in the time domain, jitter. Signal-to-distortion ratio (SDR) is commonly used to measure the effect of timing jitter on a DAC and can be expressed as equation (6) [11].

$$SDR = 3.01(N-1) - 10\log_{10}(\sigma^2 \cdot f_{SIG} \cdot f_{DAC} - 9.03[dB] \quad (6)$$

where N is the resolution of the DAC, σ is the RMS jitter, and f_{SIG} is the signal frequency. The SDR decreases by 20 dB/dec as RMS jitter increases. For a 600 MS/s 10-bit DAC, an SDR of > 70 dB is required not to degrade the DAC SNR, which leads to an RMS jitter of < 3.5 ps at an f_{SIG} of 862 MHz, as shown in Figure 6.

III. TRANSMITTER CIRCUITS

Figure 7 shows a block diagram of the proposed low-power 10-bit, 600 MS/s, multi-mode SWDR type transmitter. It consists of a 10-bit sub-Nyquist rate current steering DAC, a DAC mode controller (DMC), and a clock generator (CKGEN).

A. 600MS/S 10-BIT DAC ARRAY

A segmented current-steering DAC architecture that is a hybrid between binary weighted and thermometer coded DACs is applied at the 10-bit resolution. The segmentation is determined by considering glitches between MSB and LSB parts, area, timing precision requirements, switching noise in digital logic, and speed and power consumption tradeoffs,

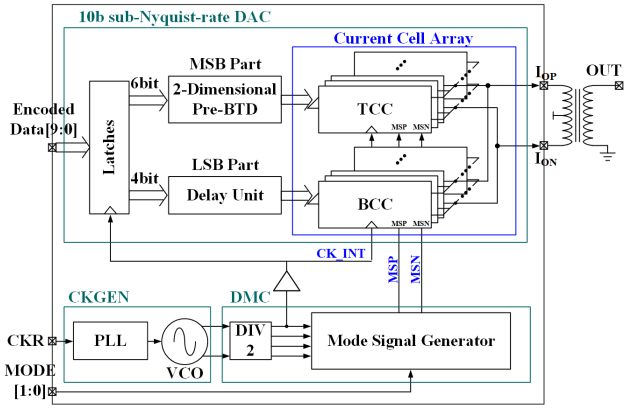


FIGURE 7. Block diagram of the proposed low-power 10-bit, 600 MS/s, multi-mode SWDR type transmitter.

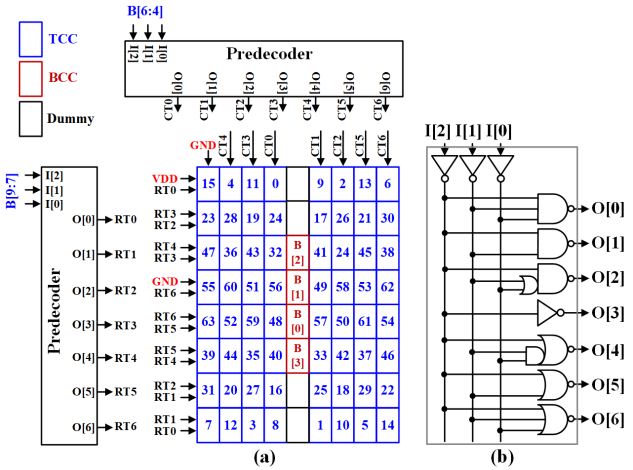


FIGURE 8. (a) Scrambled mapping of DAC array with two-dimensional DEM pre-decoder and (b) 3-to-7 bit binary to thermometer pre-decoder.

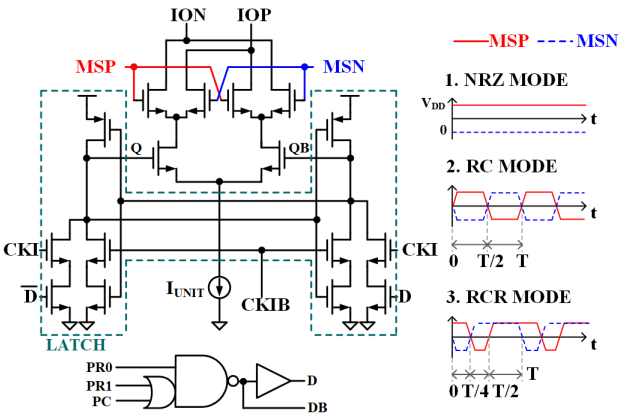


FIGURE 9. Differential Gilbert cell for multi-mode sub-Nyquist rate DAC.

leading to a 6-bit thermometer-coded MSB array and a 4-bit binary-weighted LSB array.

The output currents of the MSB and LSB arrays are interconnected to produce differential output currents, I_{OP} and I_{ON}. The MSB array has 63 identical thermometer current cells (TCC) consisting of a final binary-to-thermometer decoder (BTD), a differential latch, differential current switches, and a 16 × I_{UNIT} current source where I_{UNIT} is the DAC unit current. The LSB array has four binary current cells (BCC) consisting of a differential latch, differential current switches, and a 1 × I_{UNIT}, a 2 × I_{UNIT}, a 4 × I_{UNIT}, or an 8 × I_{UNIT} depending on binary weight. The I_{UNIT} is 10 μA, and the DAC differential output currents of I_{OP} and I_{ON} drive a 50 Ω impedance of a transformer and generate a 1.0 V differential signal swing between V_{OP} and V_{ON}. A transformer converts a differential output into a single-ended signal.

High-resolution DACs require high spectral purity that can be degraded due to unit element mismatch to maintain linearity performance. The mismatch is exacerbated by using small transistors at the current sources to achieve small parasitic capacitance and wide signal bandwidth. Spurious free dynamic range (SFDR) is a DAC dynamic range that can be used before spurious tones interfere with or distort the fundamental tone. SFDR is the measure of the amplitude difference between the fundamental tone and the largest harmonically or non-harmonically related spurious tone within Nyquist bandwidth. For high SFDR, common centroid layout technique and dynamic element matching (DEM) [11] are employed to reduce the static DAC noise and the correlated noise to the input signals, respectively. The two-dimensional DEM pre-decoder scrambles the mapping of the TCC. The output of row and column 3-to-7-bit binary to thermometer pre-decoders are scrambled so that the mapping of TCCs is randomized as shown in Figure 8. Although the DEMs are performed in the row and column pre-decoders independently, signal routing at the decoder output is regular in the switch cell array, simplifying signal routing from pre-decoders to TCC array compared to fully scrambled DEMs. The Reduction of input signal routing parasitics of DAC array helps to implement HS DACs.

B. CURRENT SWITCH CELL

Multi-mode operation is performed on the DAC array by using differential Gilbert cells with current switch control signals of MSP and MSN as shown in Figure 9.

In NRZ mode, the CS-DAC differential output current of IOP and ION is controlled by the input data of Q and QB while MSP switch is on and MSN switch is off. In RC mode, the CS-DAC differential output currents of IOP and ION are controlled by the input data of Q and QB for the evaluation half-cycle period (positive phase) when MSP switch is on and MSN switch is off. The differential output is inverted for the remaining half-cycle period (negative phase) when the MSP switch is off and MSN switch is on. In RCR mode, CS-DAC performs the evaluation operation of RC mode for the first quarter cycle period and inversion operation of RC mode for the second quarter cycle period. IOP and ION are short-circuited for the reset operation for the remaining half-cycle

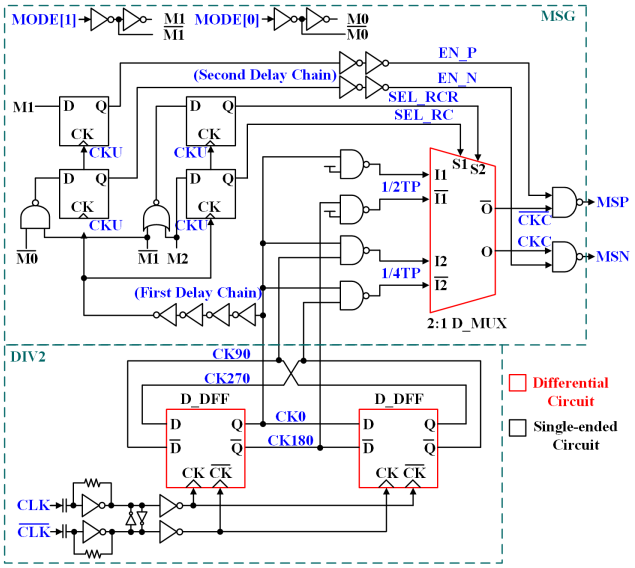


FIGURE 10. Block diagram of dynamic reconfigurable DAC mode controller.

period when the MSP and MSN switches are turned on at the same time.

The TCC cell also contains the final decoder and latch. The decoding logic is equivalent to an AND–OR gate function that takes one signal at the column decoder output and two signals at the row decoder output. Latching is essential for timing synchronization as all the current cells should be switched at the same time. In addition, the differential signals of Q and QB for driving the switch cells are optimized to have a high crossing point to reduce the glitches at the common source node of the switch cells during the CS-DAC switching transients. BCC cells do not require decoding, so they contain only latches.

C. DAC MODE CONTROLLER

The reconfigurable DAC mode controller (DMC) generates current switch control signals for the MSP and MSN with 2-bit mode signals (MODE[1:0]) for the differential current switches, allowing seamless and glitch-free DAC mode change between NRZ, RC, and RCR modes. Figure 10 illustrates a block diagram of the DMC configured with a mode signal generator (MSG) and a divided-by-2 (DIV2). DIV2 uses two differential DFFs (D_DFF) to generate 600 MHz quadrature-phase clocks for CK0, CK90, CK180, and CK270 from the 1.2 GHz differential clocks of the frequency synthesizer.

NRZ mode requires static DC control signals with a high MSP and low MSN as shown in Figure 9. The disabled EN_P signal sets the NAND output MSP to a high state. An enabled EN_N and a high static CKC signal bring MSN to a low state due to a NAND operation. Deselecting SEL_RC and SEL_RCR of the 2:1 D_MUX generates the high static CKC signal.

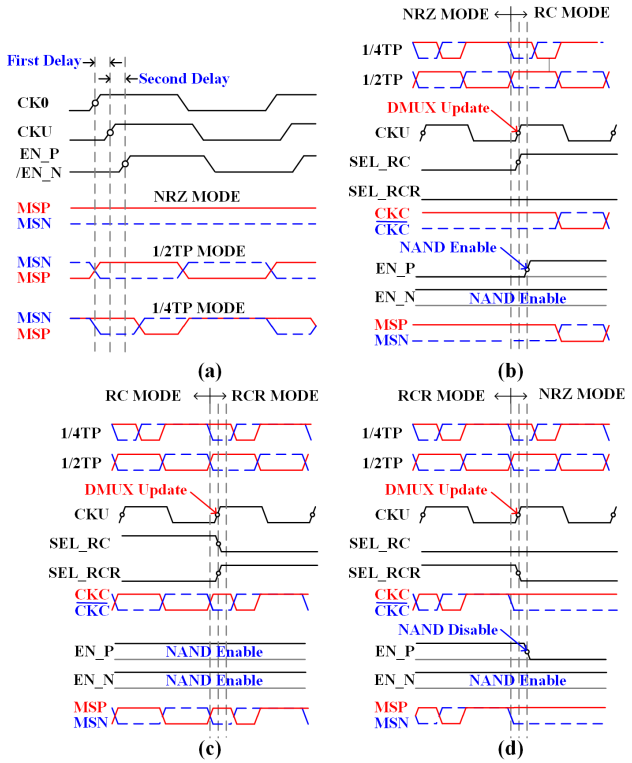


FIGURE 11. Timing diagrams of (a) 2:1 D_MUX inputs relative to MUX selection and NAND gating signals and seamless mode conversion examples (b) from NRZ to RC, (c) from RC to RCR, and (d) from RCR to NRZ modes.

RC mode needs an evaluation and inversion period for each half-cycle. EN_P and EN_N are enabled throughout the entire cycle of RC mode. The MSP and MSN are controlled by 50% duty cycle differential clocks (1/2TP) that can be provided by CK0 and CK180 from the DIV2. Thus, MSP and MSN are high and low states for the half-cycle evaluation period, and MSP and MSN are low and high states for the half-cycle inversion period as shown in Figure 9. The 1/2TP signal is connected to the 2:1 D_MUX output by selecting SEL_RC and deselecting SEL_RCR. RCR mode uses a 25% duty cycle quadrature signal (1/4TP) generated by two NAND operations between CK0 and CK90 and between CK180 and CK270, respectively. The 1/2TP signal for RC mode also pass through the same NAND gates to obtain the same delay as the 1/4TP signal. EN_P and EN_N are also activated during the first half-cycle of the RCR mode, and the 1/4TP signal is connected to the 2:1 D_MUX output by selecting SEL_RCR and deselecting SEL_RC. EN_P and EN_N are deactivated during the other half-cycle of the RCR mode, leading to MSP and MSN high states during the reset period as shown in Figure 9.

The mode update should be well controlled so that the dynamic frequency hopping time becomes zero. As shown in Figure 11(a), all three modes have a common period of high MSP and low MSN during the first quarter cycle time of each mode. Thus, the mode update is performed using this common time. The 2:1 D_MUX selection signal

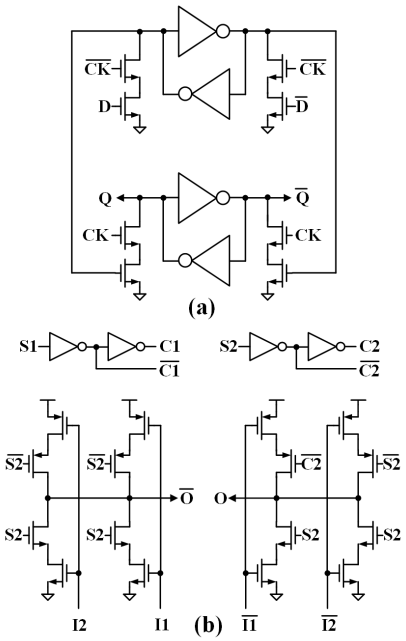


FIGURE 12. Pseudo-differential (a) cross-coupled latch (D_DFF) and (b) 2:1 multiplexer (D_MUX).

is synchronized with the delayed CKU from CK0 using DFFs. The first delay chain causes the CKU rising edges to lag slightly behind the 1/4TP and 1/2TP rising edges, even considering PVT variations. The 2:1 D_MUX selects either 1/4TP or 1/2TP depending on the selection signal with the CKU rising edges as shown in Figure 10. The first delay helps the selection signal avoid transient time of 1/4TP and 1/2TP, and the D_MUX differential outputs are changed seamlessly with the selection signal.

An additional NAND gate step is required to support the seamless multi-mode frequency hopping. EN_P and EN_N signals are delayed through a second delay chain after the 2:1 D_MUX selection signal (SEL_RC or SEL_RCR) to avoid interference with D_MUX output transient time. The sum of the first delay time and the second delay time should be less than a quarter cycle since the minimum steady-state time of the RCR mode is less than a quarter cycle, as shown in Figure 11(a). Figure 11(b), (c), and (d) show three examples of seamless mode transformation from NRZ to RC, from RC to RCR, and from RCR to NRZ, respectively. D_MUX updates occur after transients of 1/4TP and 1/2TP signals with the first delay chain, and the NAND operation is performed after the D_MUX updates, which is a slack borrowing strategy. This strategy is applied to ensure that there is no signal interference during the mode conversion time if the first and second delay amounts are less than a quarter cycle, even if there are PVT variations.

Figure 12(a) shows a pseudo-differential cross-coupled D flip-flop (D_DFF). An SR latch in the D_DFF consists of a pair of cross-coupled inverters and four additional NMOSs

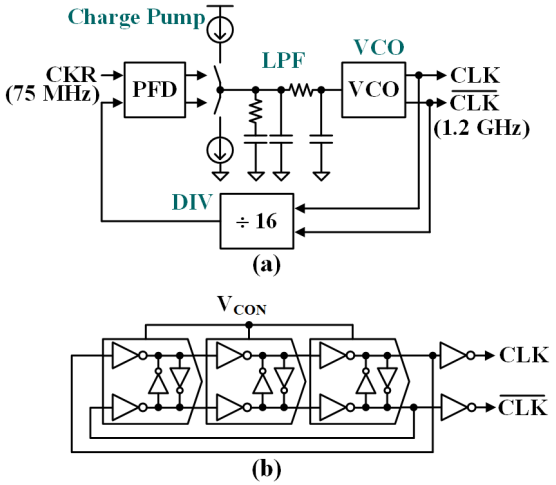


FIGURE 13. (a) Type-II third order phase-locked loop (PLL) for CKGEN and (b) pseudo-differential ring-VCO.

that drive from one latch to another and provide clocked operation. The cascoded NMOS driver is sized to pull down the output below the switching threshold of the cross-coupled inverter. Thus, the D_DFF does not consume any static power since one inverter resides in a high state while the other one is in a low state. Figure 12(b) shows a pseudo-differential multiplexer (D_MUX) consisting of two CMOS single-ended multiplexers for the complementary inputs. MSP and MSN are not differential signals during the reset period of the RCR mode, so there is no cross-coupled inverter on the two outputs.

D. CLOCK GENERATOR

The clock generator (CKGEN) provides differential clock signals of 1.2 GHz, twice the f_{DAC}. Implemented with a type-II third order phase-locked loop (PLL), it consists of a phase frequency detector (PFD), a low pass filter (LPF), a voltage-controlled oscillator (VCO), and a divided-by-16 (DIV16), as shown in Figure 13(a). The PLL achieves fast settling times with a 1 MHz of PLL bandwidth (PLLBW) and a 50° of phase margin by adjusting the zero frequency of the LPF and other residual pole frequencies. Moreover, the VCO and DIV16's pre-scaler run at 1.2 GHz, while the other blocks run at 75 MHz reference clock (CKR), which leads to low power consumption.

The VCO has a huge impact on the overall performance of the PLL. LC VCOs outperform ring-VCOs (RVCOs) in jitter performance due to their high quality (Q) factor. However, RVCOs have the advantage of a much smaller area and lower power consumption. A pseudo-differential RVCO is employed in the CKGEN as shown in Figure 13(b) because it provides a differential clock signal with common-mode rejection while maintaining a large output swing. The cross-coupled inverters also correct the duty cycle of the output clock by 50% [12].

The RVCO frequency can be controlled by adjusting the supply voltage, but the ring-VCOs also have a wide frequency

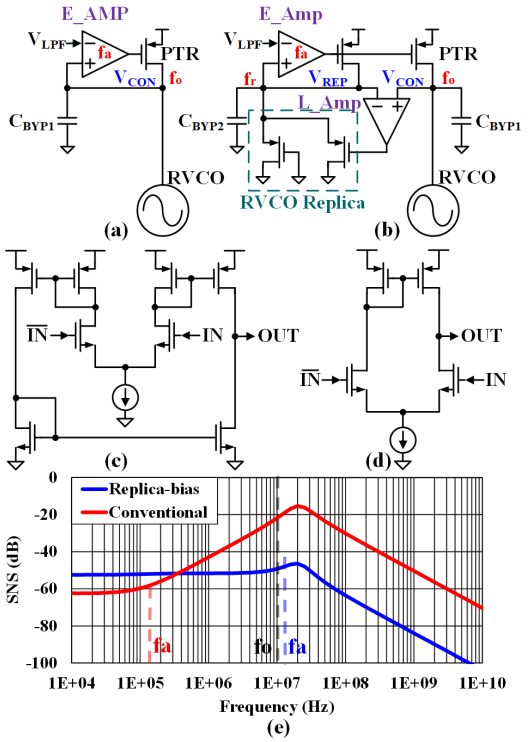


FIGURE 14. (a) Conventional SR-VCO, (b) replica-biased SR-VCO, (c) error amplifier (E_AMP), (d) local feedback amplifier (L_AMP), and (e) SNSs of conventional SR-VCO and replica-biased SR-VCO.

tuning range with large VCO gains, which increases supply noise sensitivity. Therefore, one of the most common PLL architectures is a supply-regulated PLL (SR-PLL) [13]. The regulator output pole (f_o) is the residual pole frequency of the PLL that affects the PLL stability, and the f_o must be kept well above 1 MHz of PLL_{BW}.

Figure 14(a) shows a conventional low dropout regulator (LDO) that drives the VCO directly. It consists of an error amplifier (E_AMP) and a PMOS pass transistor (PTR) for low supply voltage operation. The −3dB bandwidth (fa) of E_AMP must be much larger or much smaller than f_o to maintain LDO stability. For $f_a > f_o$, the E_AMP has 3-5 times higher power dissipation than the VCO due to the wide bandwidth of E_AMP, making the entire LDO high power dissipation. [14] Therefore, the case of $f_a < f_o$ is suitable for low-power designs even with a high gain of E_AMP. However, the LDO suffers from supply noise sensitivity (SNS) peak issues [15] as shown in Figure 14(e).

The replica biased regulated VCO allows the LDO to have degrees of freedom in f_a of the E_AMP to avoid the SNS peak issue with low-power consumption [16] as shown in Figure 14(b) since the small parasitic capacitance of the replica enables f_a of the E_AMP can be extended to f_o of 10 MHz at 1.2 GHz RVCO output frequency without the LDO loop stability issue anymore. Figure 14(c) shows the E_AMP with a gain of 40 dB. For a f_o of 10 MHz, a 100 pF

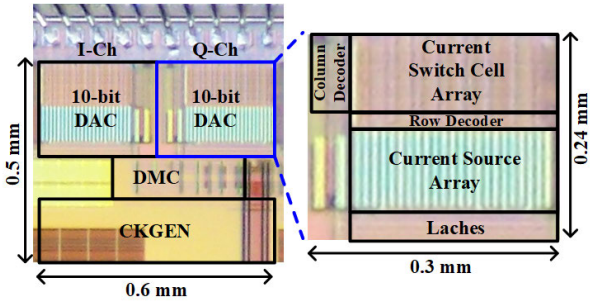


FIGURE 15. Chip microphotograph.

bypass capacitor (C_{BYP1}) is connected to the LDO output to reduce high-frequency power supply noise.

The replica VCO is implemented as a parallel combination of an appropriately sized diode-connected PMOS and a source-follower PMOS. The impedance mismatch between the VCO and the replica is trimmed by adjusting the gate voltage of the source-follower PMOS with local feedback through a local feedback amplifier (L_AMP) having a low-frequency gain of 30 dB and 3dB bandwidth of 100 kHz in order not to interfere with the main LDO loop stability. Figure 14(d) shows the L_AMP. The small signal resistance ($r_{REP}=1/g_{m,REP}$) is set to 1/5 of the RVCO ($r_{VCO}=1/g_{m,VCO}$) where gm is transconductance. The rvco is smaller than the PTR output resistance (r_{PTR}). The impedance mismatch between the VCO and the replica is trimmed by adjusting the gate voltage of the source-follower PMOS that is parallel to the diode connected PMOS with local feedback through a local feedback amplifier (L_AMP) having a low-frequency gain of 30 dB and 3dB bandwidth of 100 kHz in order not to interfere with the main LDO loop stability. The SNS of a replica-biased VCO is shown in Figure 14(e) at a VCO output frequency of 1.2 GHz, resulting in SNS peak level reduction by 28 dB.

IV. MEASUREMENT RESULTS AND COMPARISON

Figure 15 shows the 10-bit, 600 MS/s, multi-mode SWDR type transmitter fabricated in a 65 nm CMOS process. The core consists of two 10-bit DACs for I and Q channels, a DAC mode controller, and a clock generator. The measurements of the transmitter output were performed by connecting the output of the DAC to an off-chip transformer to get single-ended output. The 10-bit DAC contains latches for storing 10-bit encoded data, a row/column decoder, a current source array, and a current switch cell array. The transmitter core area is 0.3 mm^2, and the DAC core area is 0.072 mm^2. The 10-bit DAC, the DMC, and the CKGEN consume 12 mW, 3 mW, and 4 mW respectively. For static performance characterization, integral non-linearity (INL) and differential non-linearity (DNL) figures are used. The measured DNL value is 0.12 LSB, and the measured INL value is 0.25 LSB as shown in Figure 16. This clearly shows the advantage of the two-dimensional decoder of the DEM.

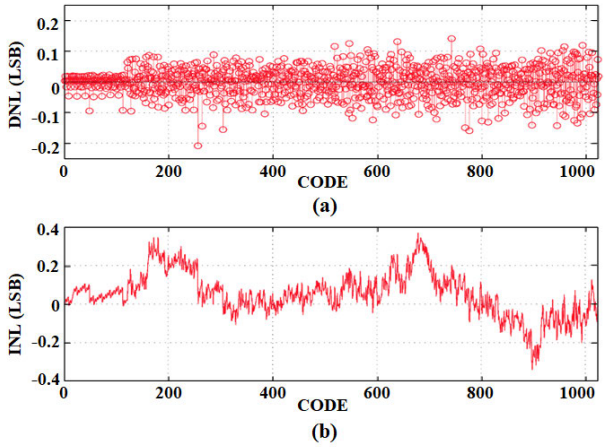


FIGURE 16. Measured (a) DNL and (b) INL of proposed direct-sampling DAC.

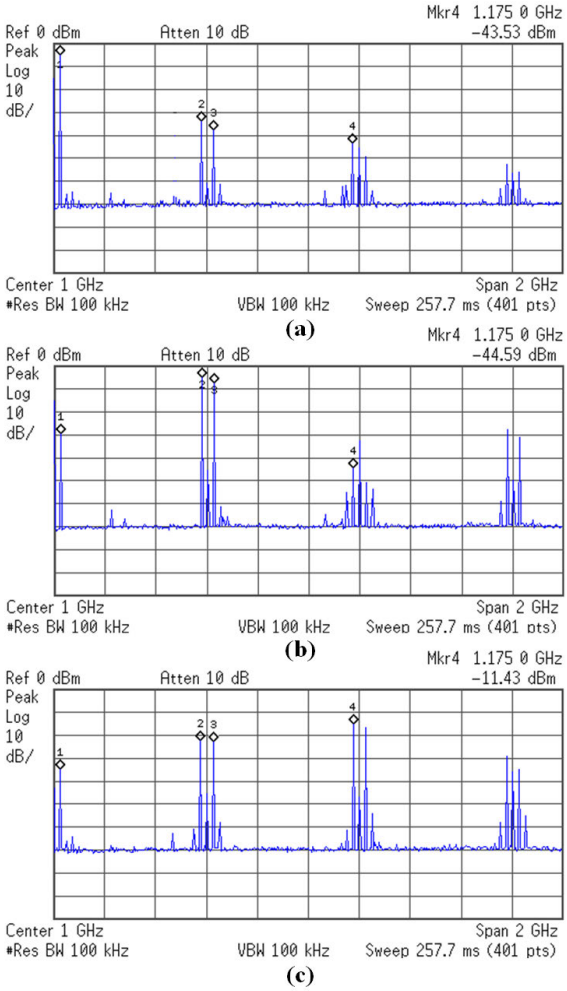


FIGURE 17. Measured spectrums of the proposed transmitter output with (a) NRZ, (b) RC, and (c) RCR modes.

The spectrum of the output signals sampled at 600 MS/s of the proposed transmitter is measured over multiple Nyquist zones by using a 25 MHz fundamental output signal in the NRZ, RC, and RCR modes. In NRZ mode, the fundamental

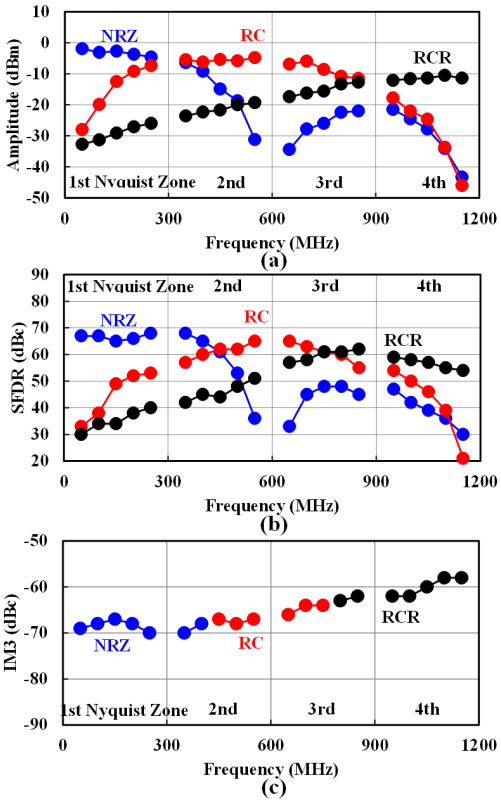


FIGURE 18. Measured (a) spectral magnitude envelopes, (b) SFDR curves, and (c) IM3 of the proposed transmitter with NRZ, RC, and RCR modes.

tone output power at 25 MHz (the first Nyquist zone) is -5.4 dBm, and the first image at 575 MHz (the second Nyquist zone) is attenuated by 29 dB due to the SINC roll-off as shown in Figure 17(a). Thus, the transmitter can use NRZ mode in the first Nyquist zone of up to 300 MHz. The transmitter reconfigures the output switch to RC mode to utilize the second and part of the third Nyquist zones. The output powers of the second and third images increased by 30dB compared to the NRZ mode as shown in Figure 17(b). Moreover, the RCR mode boosts the output powers of the part of the third and fourth Nyquist zones. The output power at 1175 MHz in the RCR mode is higher than the NRZ and RC modes by about 33 dB as shown in Figure 17(c). Thus, the proposed transmitter can operate over a wideband range with low sampling frequency because of the flexibility to adapt the DAC into different reconstruction modes.

The output power magnitude responses are measured to reveal the spectral envelopes of the NRZ, RC, and RCR modes by sweeping a test single-tone frequency at a 600 MS/s sampling rate. The multi-mode operations shape the spectrum envelope and shift the energy from fundamental frequency in the first Nyquist zone to the image frequency at higher Nyquist zones with RC and RCR modes as shown in Figure 18(a). A spurious-free dynamic range (SFDR) measurement identifies any spurs as a function of the input signal frequency in the NRZ, RC, and RCR modes

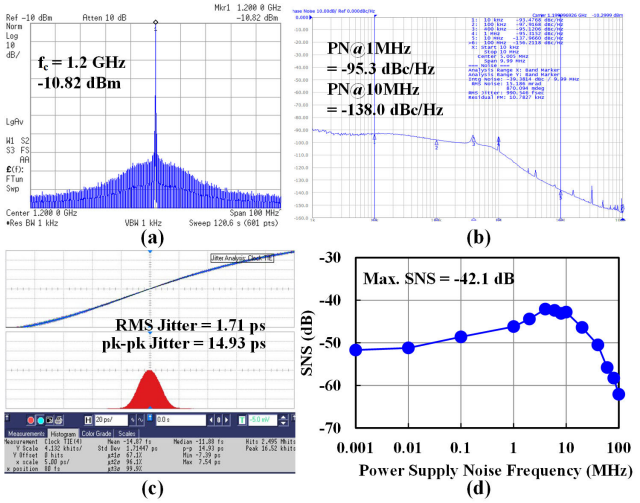


FIGURE 19. Measured (a) power spectrum, (b) phase noise, (c) jitter histogram, and (d) supply noise sensitivity of the SR-PLL at 1.2 GHz.

at 600 MS/s sampling frequency within their corresponding Nyquist zones as shown in Figure 18(b). The NRZ mode provides the largest SFDR of > 65 dBc in the range of approximately DC to 400 MHz, which is the first and part of the second Nyquist zones. The RC mode achieves the largest SFDR of > 61 dBc from 400 to 750 MHz, part of the second and third Nyquist zones. Moreover, the RCR mode gives the largest SFDR of > 54 dBc between 750 to 1200 MHz, part of the third and fourth Nyquist zones. Thus, the proposed transmitter can achieve the SFDR of > 60 dB with the multi-mode sub-Nyquist DAC for TV band cognitive radio applications (54-862 MHz). Figure 18(c) shows the measured IM3 versus signal frequency in the NRZ, RC, and RCR modes within the corresponding Nyquist zone. It shows an IM3 of < -67 dBc, < -64 dBc, and < -58 dBc, respectively, in each Nyquist zone at 600 MS/s sampling frequency. The IM3 measurement result shows a wider bandwidth than the SFDR result since IM3 measurements deal with close-in third-order components while SFDR deals with all the tones within the Nyquist zone.

Figure 19(a) shows the measured spectrum of the PLL that shows a 1.2 GHz center frequency. There is no spurious tone within a channel bandwidth of 6, 7, or 8 MHz since the PLL uses 75 MHz of the reference clock. Figure 19(b) shows the measured phase noises (PN) at 1 MHz and 10 MHz are -95.3 dBc/Hz and -138.0 dBc/Hz respectively. Figure 19(c) shows the measured jitter histograms of the 1.2 GHz PLL output signal. The measured RMS jitter is 1.71 ps, and the peak-to-peak jitter is 14.93 ps. The supply noise sensitivity (SNS) of the PLL is tested by modulating the regulator supply voltage with a sinusoidal tone. The SNS metric is used as the quantitative measure of the amount of phase noise that is caused by supply noise, and it is defined as equation (7) [17].

$$SNS[dB] = 20\log\frac{\Delta T_j/T}{\Delta V_{DD}/V_{DD}} \tag{7}$$

TABLE 1. Performance summary and comparison with prior works.

	This Work	[18] JSSC17	[19] JSSC18	[20] JSSC21	[21] TCASII22
Technology (nm)	65 CMOS	130 SiGe	65 CMOS	28 CMOS	40 CMOS
Voltage (V)	1, 1.2	1.5, 4	1.1, 2	1.1	1, 2.5
Architecture	DAC + PLL	DAC	DAC + DDS	DAC	DAC + PLL
DAC Resolution	10 (6T+4B)	10 (4T+6B)	16 (6T+3B)	14 (9T+5B)	14 (4T+10B)
DAC MODE	NRZ, RC, RCS	RZ, MRZ	RZ + DSM	NRZ, MDAC	NRZ (RDQS)
Min. SFDR in Band (dBc)	57	54	52	50.1	63
BW (GHz) @ 6(N-1) dBc	1	20	0.3	0.8	0.2
BW (GHz) @ > 50 dBc	1.1	20	6	10	1.4
IMD in Band (dBc)	56	46	44	56	N/A
Max. f_{DAC} (GS/s)	0.6	3.35	12	10	3
DNL (LSB)	0.12	N/A	N/A	N/A	N/A
INL (LSB)	0.25 1.4*	N/A 2.0*	N/A 164.6*	N/A 51.2*	N/A 11.6*
Clock Source	PLL	External	DDS	External	PLL
CK_{IN} (GHz)	0.075	3.350, 20.1	12	10	N/A
Clock Jitter (ps)	1.71	N/A	N/A	N/A	N/A
P_{TOT} (mW)	19	N/A	1760	N/A	N/A
P_{DAC} (mW)	12	1910	250	210	190
DAC Area (mm^2)	0.072	0.21	0.1	0.1	0.9
FoM_1 (MS/s/mW)	50	2	48	48	16
FoM_2 (GHz/mW)	85	11	79	62	17

$INL^* = \frac{2^N}{10^{(SFDR/20)}}$ [22]; $FoM_1 = \frac{\text{Sampling Rate}}{P_{DAC}}$, $FoM_2 = \frac{2^N \cdot BW_{6(N-1)\,dB}}{P_{DAC}}$ [23]

where T is the period of the output clock and ΔT_j is jitter variation due to the peak-to-peak supply-noise amplitude of ΔV_{DD}. Figure 19(d) shows the measured SNS as the frequency of the sinusoidal tone modulating the supply voltage from 1k to 100 MHz. The replica-biased SR-VCO alleviates the SNS peak issue of the conventional SR-VCO. Moreover, the maximum RMS jitter is 3.06 ps on a 4 MHz sinusoidal tone, which translates to the SNS of -42.1 dB and guarantees an SDR of > 70 dB.

Table1 summarizes the performance of the proposed transmitter using a multi-mode sub-Nyquist rate DAC and compares it with the state-of-the-art 10-bit or more wideband DACs [18], [19], [20], [21]. The transmitter integrates a 10-bit DAC and a PLL providing a sampling frequency of 600 MS/s with a 75 MHz low-frequency clock. The minimum SFDR in the TV band is 57 dBc, the bandwidth (BW) for SFDR > 54 dBc (=6(N-1)) is 1 GHz, and the BW for SFDR > 50 dBc is 1.1 GHz. For static performance comparison, the relationship between INL and SFDR at low frequencies [22] is applied since DNL and INL are not available in the state-of-the-arts. However, parasitic capacitance seriously affects the current cell output impedance, so the relationship is less accurate at high-frequency SFDR. A simple first-order figure of merit (FoM_1) defines the sampling rate per 1 mW of DAC power consumption. Another FoM_2 defines BW where the SFDR

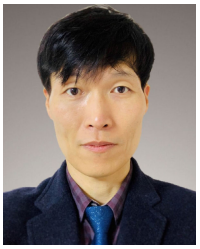
drops by 6 dB (1bit) per 1 mW [23]. The proposed DAC outperforms others in INL and FoM_2 and is comparable to other state-of-the-arts in FoM_1.

V. CONCLUSION

A 10-bit, 600 MS/s direct-sampling DAC-based transmitter integrated circuit that provides a frequency-agile operation is implemented in 65nm CMOS within an active area of 0.3 mm^2. A multi-mode sub-Nyquist DAC with the NRZ, RC, and RCR modes shapes a spectral envelope for the wide range of from 54 to 862 MHz even at sampling rates of 600 MS/s. The mode signal generator selects the DAC mode with 600 MHz quadrature signals from a divided-by-2 circuit and adds appropriate delay circuits to ensure a seamless transition between the three modes. A low-power supply-regulated PLL generates a 1.2 GHz differential clock signal from a 75 MHz reference clock, and the RMS jitter is 3.06 ps at the worst-case supply noise sensitivity, which can guarantee a SDR of > 70 dB. The transmitter achieves a DNL of 0.12 LSB, an INL of 0.25 LSB, an SFDR of > 57 dBc, and IM3 of < −62 dBc in the TV band while consuming 19 mW, demonstrating the acceptable performances of the transmitter with low-power consumption for the IEEE 802.22 cognitive radio applications in the VHF/UHF TV band.

REFERENCES

[1] S. Haykin, "Cognitive radio: Brain-empowered wireless communications," *IEEE J. Sel. Areas Commun.*, vol. 23, no. 2, pp. 201–220, Sep. 2005, doi: 10.1109/JSAC.2004.839380.
[2] K. G. Shin, H. Kim, A. W. Min, and A. Kumar, "Cognitive radios for dynamic spectrum access: From concept to reality," *IEEE Wireless Commun.*, vol. 17, no. 6, pp. 64–74, Dec. 2010, doi: 10.1109/MWC.2010.5675780.
[3] *Draft Standard for Wireless Regional Area Networks—Part 22: Cognitive Wireless RAN Medium Access Control (MAC) and Physical Layer (PHY) Specifications: Policies and Procedures for Operation in the TV Bands*, Standard IEEE P802.22/D1.0, Apr. 2008.
[4] W. Hu, D. Willkomm, M. Abusubaih, J. Gross, G. Vlantis, M. Gerla, and A. Wolisz, "Dynamic frequency hopping communities for efficient IEEE 802.22 operation," *IEEE Commun. Mag.*, vol. 45, no. 5, pp. 80–87, May 2007, doi: 10.1109/MCOM.2007.358853.
[5] L. Van der, "Architectures and circuits for software-defined radios: Scaling and scalability for low cost and low energy," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2007, pp. 568–569, doi: 10.1109/ISSCC.2007.373547.
[6] S.-Y-S. Chen, N.-S. Kim, and J. Rabaey, "A 10b 600 MS/s multi-mode CMOS DAC for multiple Nyquist zone operation," in *Proc. IEEE Symp. VLSI Circuits (VLSIC)*, Jun. 2011, pp. 66–67.
[7] T. Lin and H. Samulei, "A 200-MHz CMOS x/sin(x) digital filter for compensating D/A converter frequency response distortion," *IEEE J. Solid-State Circuits*, vol. 26, no. 9, pp. 1278–1285, Sep. 1991, doi: 10.1109/4.84945.
[8] M.-J. Choe, K.-H. Baek, and M. Teshome, "A 1.6-GS/s 12-bit return-to-zero GaAs RF DAC for multiple Nyquist operation," *IEEE J. Solid-State Circuits*, vol. 40, no. 12, pp. 2456–2468, Dec. 2005, doi: 10.1109/JSSC.2005.856276.
[9] S. Yuan-Shih Chen, N.-S. Kim, and J. M. Rabaey, "Multi-mode sub-Nyquist rate digital-to-analog conversion for direct waveform synthesis," in *Proc. IEEE Workshop Signal Process. Syst.*, Oct. 2008, pp. 112–117, doi: 10.1109/SIPS.2008.4671747.
[10] S. J. Shellhammer, A. K. Sadek, and W. Zhang, "Technical challenges for cognitive radio in the TV white space spectrum," in *Proc. Inf. Theory Appl. Workshop*, Feb. 2009, pp. 323–333, doi: 10.1109/ITA.2009.5044964.
[11] W.-T. Lin, H.-Y. Huang, and T.-H. Kuo, "A 12-bit 40 nm DAC achieving SFDR > 70 dB at 1.6 GS/s and IMD < –61dB at 2.8 GS/s with DEMDRZ technique," in *IEEE J. Solid-State Circuits*, vol. 49, no. 3, pp. 708–717, Mar. 2014, doi: 10.1109/JSSC.2014.2301769.
[12] A. Emami-Neyestanak, A. Varzaghani, J. F. Bulzacchelli, A. Rylyakov, C.-K. K. Yang, and D. J. Friedman, "A 6.0-mw 10.0-Gb/s receiver with switched-capacitor summation DFE," *IEEE J. Solid-State Circuits*, vol. 42, no. 4, pp. 889–896, Apr. 2007, doi: 10.1109/JSSC.2007.892156.
[13] V. V. Kaenel, D. Aebischer, C. Piguet, and E. Dijkstra, "A 320 MHz, 1.5 mW@1.35 V CMOS PLL for microprocessor clock generation," *IEEE J. Solid-State Circuits*, vol. 31, no. 11, pp. 1715–1722, Nov. 1996, doi: 10.1109/JSSC.1996.542316.
[14] S. Sidiropoulos, D. Liu, J. Kim, G. Wei, and M. Horowitz, "Adaptive bandwidth DLLs and PLLs using regulated supply CMOS buffers," in *Symp. VLSI Circuits. Dig. Tech. Papers*, Jun. 2000, pp. 124–127, doi: 10.1109/VLSIC.2000.852868.
[15] E. Alon, J. Kim, S. Pamarti, K. Chang, and M. Horowitz, "Replica compensated linear regulators for supply-regulated phase-locked loops," *IEEE J. Solid-State Circuits*, vol. 41, no. 2, pp. 413–424, Feb. 2006, doi: 10.1109/JSSC.2005.862347.
[16] G. W. den Besten and B. Nauta, "Embedded 5 V-to-3.3 V voltage regulator for supplying digital IC's in 3.3 V CMOS technology," *IEEE J. Solid-State Circuits*, vol. 33, no. 7, pp. 956–962, Jul. 1998, doi: 10.1109/4.701230.
[17] A. Arakali, S. Gondi, and P. K. Hanumolu, "Low-power supply-regulation techniques for ring oscillators in phase-locked loops using a split-tuned architecture," *IEEE J. Solid-State Circuits*, vol. 44, no. 8, pp. 2169–2181, Aug. 2009, doi: 10.1109/JSSC.2009.2022916.
[18] L. Duncan, "A 10-bit DC-20-GHz multiple-return-to-zero DAC with >48-dB SFDR," *IEEE J. Solid-State Circuits*, vol. 52, no. 12, pp. 3262–3275, Dec. 2017, doi: 10.1109/JSSC.2017.2749441.
[19] S. Su and M. S.-W. Chen, "A 16-bit 12-GS/s single-/dual-rate DAC with a successive bandpass delta-sigma modulator achieving <-67-dBc IM3 within DC to 6-GHz tunable passbands," *IEEE J. Solid-State Circuits*, vol. 53, no. 12, pp. 3517–3527, Dec. 2018, doi: 10.1109/JSSC.2018.2871143.
[20] H.-Y. Huang, X.-Y. Chen, and T.-H. Kuo, "A 10-GS/s NRZ/Mixing DAC with switching-glitch compensation achieving SFDR >64/50 dBc over the first/second Nyquist zone," *IEEE J. Solid-State Circuits*, vol. 56, no. 10, pp. 3145–3156, Oct. 2021, doi: 10.1109/JSSC.2021.3079111.
[21] F. Wang, Z. Wang, J. Liu, and F. Yu, "A 14-bit 3-GS/s DAC achieving SFDR >63dB up to 1.4GHz with random differential-quad switching technique," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 69, no. 3, pp. 879–883, Mar. 2022, doi: 10.1109/TCSII.2021.3123251.
[22] X. Wu, P. Palmers, and M. S. J. Steyaert, "A 130 nm CMOS 6-bit full Nyquist 3 GS/s DAC," *IEEE J. Solid-State Circuits*, vol. 43, no. 11, pp. 2396–2403, Nov. 2008, doi: 10.1109/JSSC.2008.2004527.
[23] W.-T. Lin, H.-Y. Huang, and T.-H. Kuo, "A 12-bit 40 nm DAC achieving SFDR > 70 dB at 1.6 GS/s and IMD < –61dB at 2.8 GS/s with DEMDRZ technique," *IEEE J. Solid-State Circuits*, vol. 49, no. 3, pp. 708–717, Mar. 2014, doi: 10.1109/JSSC.2014.2301769.



NAM-SEOG KIM (Member, IEEE) received the B.S. degree in electronics engineering from Korea University, South Korea, in 1997, the M.S. degree in electrical engineering from Seoul National University, South Korea, in 1999, and the Ph.D. degree in electrical engineering and computer science from the University of California at Berkeley, CA, USA, in 2014.

He is currently an Associate Professor with the School of Information and Communication Engineering, Chungbuk National University, South Korea. From 1999 to 2007, he was with Samsung Electronics, South Korea, where he was involved in developing analog/mixed-signal circuits for the SRAMs/DRAMs high-speed links. From 2014 to 2019, he was with Qualcomm Inc., San Diego, USA, and Samsung Electronics, Hwasung, South Korea, where he worked on designing RF ICs and analog ICs for wireless communications and the IoTs. He worked as a Senior Researcher with Agency for Defense Development (ADD), Daejeon, South Korea, while focusing on small-sized RADAR sensors. His research interests include RF ICs, analog/mixed-signal ICs, and digital ICs for artificial intelligence systems, biosensors, RADAR sensors, and energy-efficient systems.