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RESEARCH ARTICLE

Design Method of Vertical Lattice Loop Structure for Parasitic Inductance Reduction in a GaN HEMTs-Based Converter

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ABSTRACT Among the wide-bandgap devices, gallium nitride high electron mobility transistors (GaN HEMTs) are contributing to the high power density technology of power conversion systems due to their excellent physical properties. In contrast, the driving voltage and threshold voltage are relatively low compared to conventional power semiconductor devices, so a reliable circuit design is required. In this paper, a parasitic inductance reduction design method for the stable driving of GaN HEMTs is proposed. To reduce parasitic inductance, we propose a vertical lattice loop structure having multiple loops, and this method can be applied regardless of the package type and shape of GaN HEMT. For the design of the proposed vertical lattice loop structure, the reference loop is defined to minimize leakage inductance and the identical loop is vertically stacked. The proposed structure is applied 6-layer PCB design example and verified by experimental results. Furthermore, the proposed design method is applied at the buck converter, and improved efficiency is verified from 600 kHz to 1MHz switching frequency.

INDEX TERMS Flux cancellation, gallium nitride high electron mobility transistors, parasitic inductance, PCB layout, vertical lattice loop.

I. INTRODUCTION

In modern industry, power semiconductor devices such as MOSFETs and IGBTs are widely used in power conversion systems. There has been a continuous demand for enhanced power density and higher efficiency of power conversion systems that are designed based on power semiconductor devices. Although the performance of the conventional Si-based power semiconductor has improved, it has reached its technical and inherent physical limits [1]. Therefore, research on wide-bandgap (WBG) devices, which have superior physical properties more than Si, has been conducted, and as a result, new power semiconductor devices are being developed and mass-produced. Recently, gallium nitride high electron mobility transistors (GaN HEMTs) and silicon carbide (SiC) MOSFETs have emerged as WBG devices, enabling the revolutionary development of power conversion systems with higher efficiency and power density [2], [3], [4], [5], [6]. Especially, GaN HEMTs have faster switching speed and lower conduction loss than SiC MOSFET owing to the high electron density forming a two-dimensional electron gas (2DEG) layer [7].

GaN HEMT has better characteristics and performance compared to conventional devices, but there are essential considerations for stable operation [8], [9], [10], [11], [12], [13]. The first consideration is fast *di/dt* and *dv/dt*. Because of the fast *di/dt* and *dv/dt*, voltage spikes and ringing of the gate-source voltage occur even when very small parasitic components are present in the circuit. These, in turn, can result in increased losses or even device failure. The second

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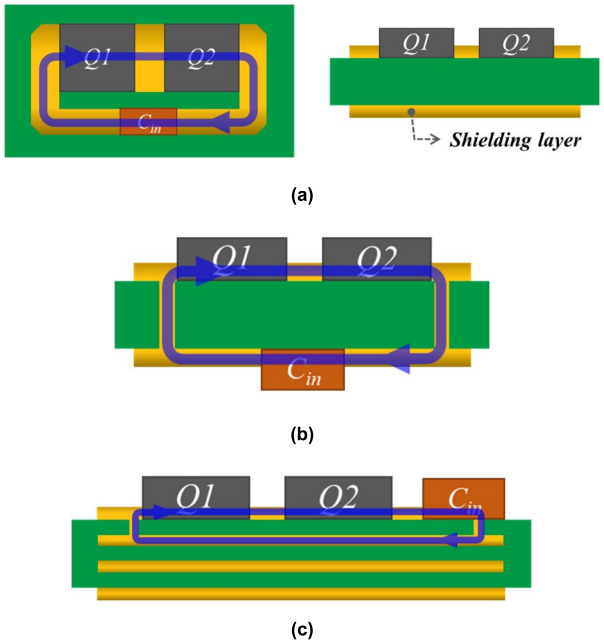


FIGURE 1. Conventional method (blue line: current loop): (a) top and cross-sectional view of lateral structure, (b) cross-sectional view of vertical structure 1, (c) cross-sectional view of vertical structure 2.

consideration is the driving voltage range of the device. The driving voltage and threshold voltage of GaN devices are extremely small than conventional devices. The driving voltage of the Si device is −20 to 20 V range, whereas that of the GaN device is −10 to 7 V range. Also, the Si device has a threshold voltage about 3 to 4 V, whereas the GaN device has a low threshold voltage of about 1.5 V. Thus, the GaN devices is more likely to be a false turn-on and turn-off. The main causes of the aforementioned phenomena are the ringing and overshoot caused by the resonance of parasitic capacitors and parasitic inductances in the devices and hardware circuits. Therefore, research is being carried out to reduce the effect of parasitic components. In particular, research to reduce the effect of parasitic inductance is being actively conducted [14], [15], [16], [17], [18], [19], [20].

In a prior study [14], the effects of parasitic inductance could be reduced through *RC* snubber circuits or ferrite beads; however, there were trade-offs such as increased loss in the circuit and increased inductance during low frequency operation. Skibinski and Divan [15] reduced the parasitic inductance by increasing the width and height of the PCB trace. However, they did not consider the length of the current loop, which could reduce parasitic inductance. Subsequent studies [16], [17], [18] minimized the distance between the switches and capacitors. Thus, parasitic inductance can be reduced. However, there is a limitation on the reduction in parasitic inductance because the effect of the magnetic flux generated by the current was not considered. Reusch and Strydom [19] minimized power loop inductance using the PCB layout. There are two structures that reduce power loop inductance, namely horizontal and vertical structures.

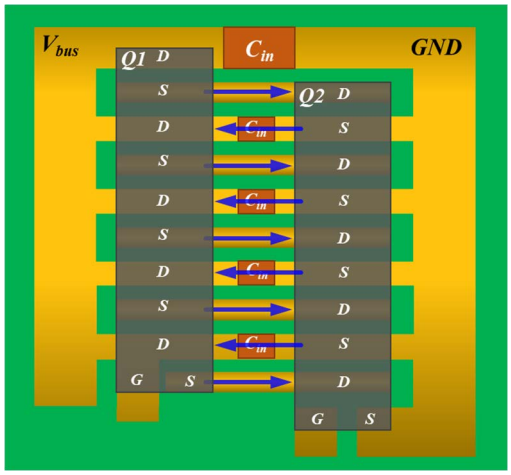


FIGURE 2. Top view of multiple loop method (blue line: current loop).

Figure 1 shows the already studied method of reducing parasitic inductance through magnetic flux cancellation. The yellow layer is copper, the green color represents FR-4 of PCB, $Q1$ is the high-side switch, $Q2$ is the low-side switch, and C_{in} is the decoupling capacitor in the half-bridge circuit. Figure 1(a) shows the horizontal structure when a power loop is formed on the top layer. In this structure, the magnetic flux caused by the current induces an eddy current in the shielding layer. In addition, since the eddy current induces the magnetic flux in the opposite direction to the magnetic flux generated in the top layer, magnetic flux cancellation occurs. This reduces the power loop inductance. The vertical structure is shown in Figure 1(b) and (c). In Figure 1(b), the switches and capacitor are mounted on the top and bottom layers, respectively. A power loop is formed through the PCB vertically. In this structure, because the current direction between the loops facing the power loop is reversed, magnetic flux cancellation occurs. This, in turn, reduces the power loop inductance. In Figure 1(c), both switch and capacitor are in the top layer. However, the power loop is formed through the via and inner layers vertically. Also, magnetic flux cancellation occurs due to the same current relationship with Figure 1(b). This, in turn, reduces the power loop inductance. However, there is a limitation on the reduction in parasitic inductance by magnetic flux cancellation because the current loop is single. Wang et al. [20] presents the multiple loop structure shown in Figure 2. The parasitic inductance is reduced further by the magnetic flux cancellation with multiple loops. However, this structure can only be acceptable to a specific GaN HEMT package. Furthermore, there is a limitation on the reduction in parasitic inductance because the gate loop inductance cannot form multiple loops.

In this paper, a vertical lattice loop structure is proposed to overcome the aforementioned limitations. It can apply multiple loops to both power and gate loops and is not affected by the package type and shape of the GaN HEMT. The single loop is defined as the reference loop for the design of the proposed vertical lattice loop structure. Furthermore, the

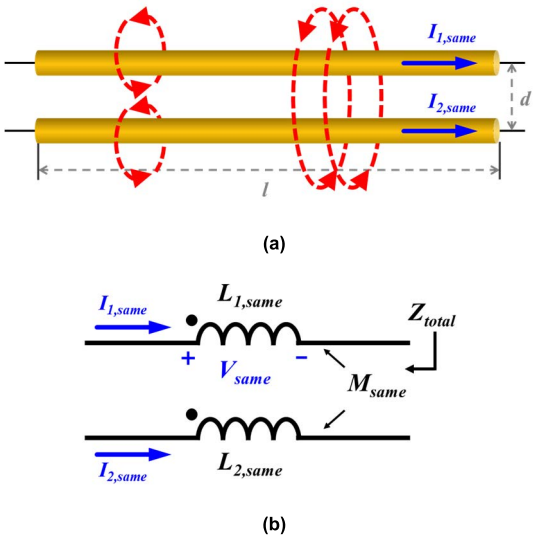


FIGURE 3. Two conductors with same direction of current. (a) current and magnetic flow, (b) equivalent circuit.

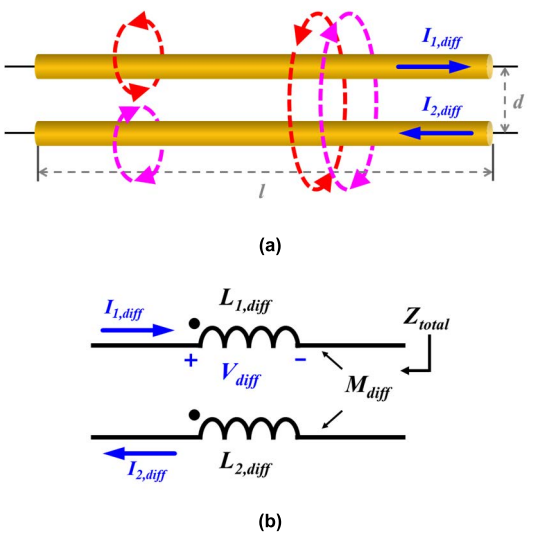


FIGURE 4. Two conductors with opposite directions of current. (a) current and magnetic flow, (b) equivalent circuit.

proposed structure is designed by layering the reference loop. With the proposed vertical lattice loop structure, power loop inductance and gate loop inductance are reduced together. Finally, improved switching performances, such as overshoot and ringing voltage, and switching losses, are experimentally verified to demonstrate the validity of the proposed vertical lattice loop structure.

II. PROPOSED STRUCTURE FOR REDUCING PARASITIC INDUCTANCE

A. THEORETICAL ANALYSIS OF PARASITIC INDUCTANCE

Figure 3(a) shows current flows in the same direction through two parallel conductors. $I_{1,same}$ and $I_{2,same}$, represent the current flowing through the conductors. The dotted line indicates the direction of the magnetic flux; d is the distance between the conductors, and l is the length of each conductor. The magnetic fluxes are in opposite directions on the inside area of conductors and the equal direction on the outside area. Figure 3(b) shows the electrical equivalent circuit of the configuration shown in Figure 3(a). Here, $L_{1,same}$ and $L_{2,same}$ are the self-inductances of the upper and lower conductors, respectively, and M_{same} is the mutual inductance between the conductors.

The voltage induced by $I_{1,same}$ and $I_{2,same}$ can be expressed as shown in (1) and (2) by applying Faraday's law to each conductor:

$$V_{1,\text{same}} = L_{1,\text{same}}\frac{dI_{1,\text{same}}}{dt} + M_{\text{same}}\frac{dI_{2,\text{same}}}{dt} \tag{1}$$

$$V_{2,\text{same}} = L_{2,\text{same}}\frac{dI_{1,\text{same}}}{dt} + M_{\text{same}}\frac{dI_{1,\text{same}}}{dt} \tag{2}$$

If both the conductors have identical material, length, and diameter, and current flow, the current and self-inductance can be represented as below:

$$L_{\text{same}} = L_{1,\text{same}} = L_{2,\text{same}} \tag{3}$$

$$I_{\text{same}} = I_{1,\text{same}} = I_{2,\text{same}} \tag{4}$$

Equation (5) is obtained by substituting (3) and (4) into (1) and (2) and applying the Laplace transform. Thus, I_{same} can be expressed as in (6). Finally, the sum of the currents flowing through the two conductors, I_{total}, is expressed as shown in (7), based on the relationship between (4) and (6). The total impedance, Z_{total}, can be expressed as shown in (8).

$$V_{\text{same}} = V_{1,\text{ same}} = V_{2,\text{ same}} = sI_{\text{same}}\ (L_{\text{same}} + M_{\text{same}}) \tag{5}$$

$$I_{\text{same}} = \frac{1}{s}\frac{V_{\text{same}}}{L_{\text{same}} + M_{\text{same}}} \tag{6}$$

$$I_{\text{total}} = I_{1,\text{ same}} + I_{2,\text{ same}} = 2I_{\text{same}} = \frac{2}{s}\frac{V_{\text{same}}}{L_{\text{same}} + M_{\text{same}}} \tag{7}$$

$$Z_{\text{total}} = \frac{V_{\text{same}}}{I_{\text{total}}} = s\frac{L_{\text{same}} + M_{\text{same}}}{2} \tag{8}$$

If the parasitic capacitance and parasitic resistance are assumed to be negligible, the total impedance is equal to the total inductance, $L_{total,same}$, of the equivalent circuit as shown in (9). According to (8) and (9), $L_{total,same}$ can be represented as (10). Therefore, when the current direction of the conductors is the same, M_{same} must be reduced in order to reduce $L_{total,same}$. Assuming that d is sufficiently smaller than l in Figure 3(a), M_{same} can be simplified as shown in (11). Here, μ_0 represents the permeability of the vacuum [21]. Therefore, d must be increased to reduce M_{same} and $L_{total,same}$.

$$Z_{\text{total}} \simeq sL_{\text{total,same}} \tag{9}$$

$$L_{\text{total,same}} \simeq \frac{L_{\text{same}} + M_{\text{same}}}{2} \tag{10}$$

$$M_{\text{same}} \simeq \frac{\mu_0}{2\pi} l\left(\ln\frac{2l}{d} - 1\right) \tag{11}$$

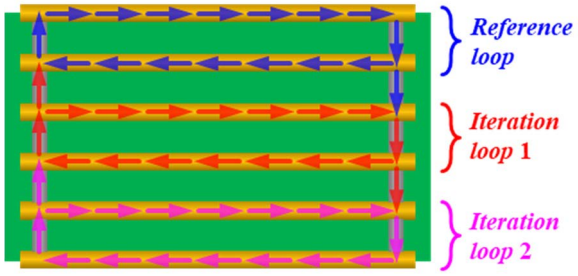


FIGURE 5. Conceptual configuration of proposed vertical lattice loop structure.

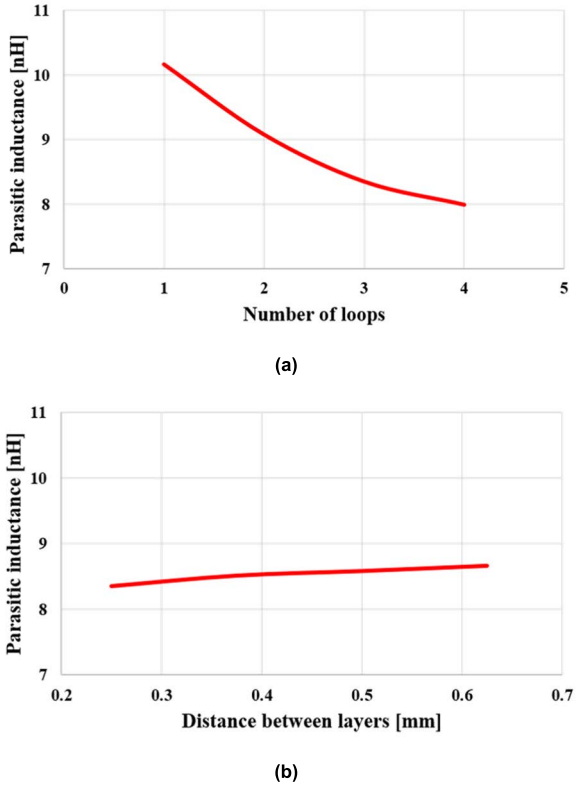


FIGURE 6. Factors that affect parasitic inductance. (a) effect of number of loops (b) effect of distance between layers.

Figure 4 shows current flows in the opposite direction through two parallel conductors. $I_{1,diff}$ and $I_{2,diff}$ represent the current flowing through the conductors. In this case, the magnetic fluxes are in same directions on the inside area of conductors and the opposite direction on the outside area. In Figure 4(b), $L_{1,diff}$ and $L_{2,diff}$ represent the magnetic inductance of the upper and lower conductors, respectively. M_{diff} represents the mutual inductance between the conductors. If the analysis procedure is applied in the same manner, the total inductance $L_{total,diff}$ of Figure 4 can be expressed as in (12).

$$L_{\text{total,diff}} = \frac{L_{\text{diff}} - M_{\text{diff}}}{2} \tag{12}$$

Therefore, M_{diff} must be increased to reduce $L_{\text{total,diff}}$. Also, M_{diff} has the same relationship as shown in (11), d should be decreased to increase M_{diff}. Overall, if the current direction of the conductors is the opposite, the distance between the conductors should be minimized to reduce $L_{\text{total,diff}}$.

B. PROPOSED VERTICAL LATTICE LOOP STRUCTURE

Figure 5 illustrates the concept of the proposed vertical lattice loop structure. Here, the yellow square is the copper layer, the green square is FR-4, black arrow lines depict current flow, and the gray square is the via of the PCB. The proposed vertical lattice loop structure consists of the reference loop and the iteration loop. *The reference loop* is a path designed to have the shortest distance between conductors through which currents flow opposite. *The iterative loop* is a path designed as a vertically stacked loop identical to a reference loop.

This configuration makes a vertical lattice loop structure in which conductors with different current directions exist between conductors with identical current directions. Therefore, the distance between conductors with the same current directions becomes larger, and at the same time, the distance between conductors with different current directions becomes small. From this relationship, effective cancellation of magnetic flux can be achieved.

Figure 6 is the analysis results of the value of parasitic inductance according to the number of loops and the distance between layers based on Ansys Q3D simulation. Figure 6(a) is the result of analyzing the trend of parasitic inductance when the number of iteration loops increases in the proposed structure. It shows that the parasitic inductance decreases when the number of loops increases. This implies that a larger number of loops induces more magnetic flux cancellation. Figure 6(b) shows the tendency of parasitic inductance according to the distance between layers with the number of iteration loops fixed to two. It shows that the parasitic inductance decreases when the distance between layers is reduced. Therefore, to reduce parasitic inductance, PCB should be designed to use more layers and use a shorter distance between layers.

Figure 7 and Table 1 show a comparison of parasitic inductance according to the proposed vertical lattice loop structure applied to six copper layers. The distance between layers is 0.25 mm. The parasitic inductance analysis is performed by the finite element method based simulation tool (Ansys Q3D). In Figure 7(b), the reference loop consists of layers 1 and 2, and iteration loops consist of layers 3 and 4, and layers 5 and 6. As shown in Table 1, the parasitic inductance is reduced by 40% when the vertical lattice loop structure is applied.

Figure 8 shows the example of current flow based on six layers with the half-bridge circuit. Here, $Q1$ is the upper switch, $Q2$ is the lower switch, and C is the input capacitor. If the vertical lattice loop structure is not applied as shown in Figure 8(a), the parasitic inductance increases according to the single current direction. However, when the vertical lattice

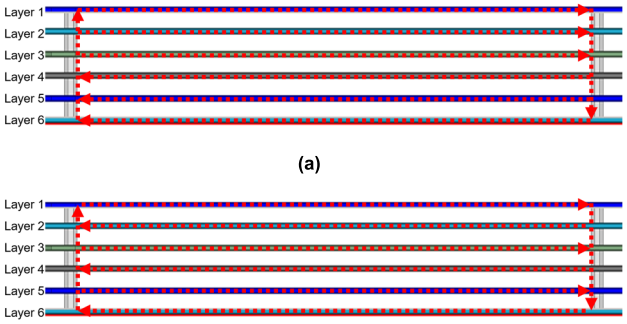


FIGURE 7. Comparison of a PCB with 6 copper layers. (a) without vertical lattice loop structure, (b) with vertical lattice loop structure.

TABLE 1. Comparison of parasitic inductance.

Condition	Value [nH]
Without Vertical Lattice Loop Structure	14.05
With Vertical Lattice Loop Structure	8.35

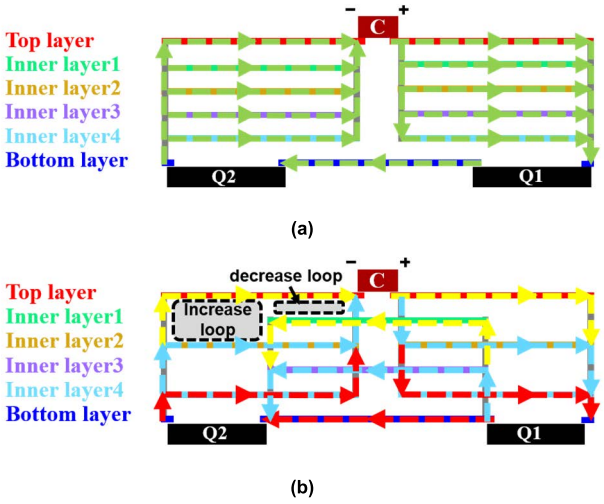


FIGURE 8. Example of PCB cross-section with half-bridge circuit. (a) without vertical lattice loop structure, (b) with vertical lattice loop structure.

loop is applied as shown in Figure 8(b), a long-distance loop is formed if the current direction is the same, and a short-distance loop is formed if the current direction is opposite. Accordingly, the parasitic inductance value can be effectively reduced, and as a result, a stable gate voltage can be supplied. The detailed procedure for configuring the vertical lattice loop is as follows.

1) Design the reference loop; As analyzed in Chapter 2-A, the farther the current paths in the same direction and the closer the current paths in the opposite direction, the greater the effect of flux cancellation. When this principle is applied, parasitic inductance can be reduced. Therefore, inner layer 1, closest to the top layer, has a current path that flows from *Q1* to *Q2* at the same time as the current flowing in the opposite direction to the current flowing in the top layer. In the same principle, the same current path as the top layer is selected in inner layer 2 so that the current direction is opposite to that of inner layer 1.

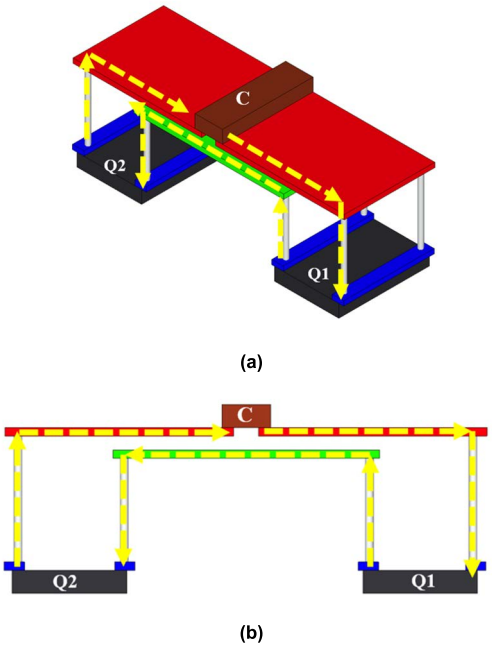


FIGURE 9. Design result of power reference loop. (a) side view of PCB, (b) cross-section of PCB.

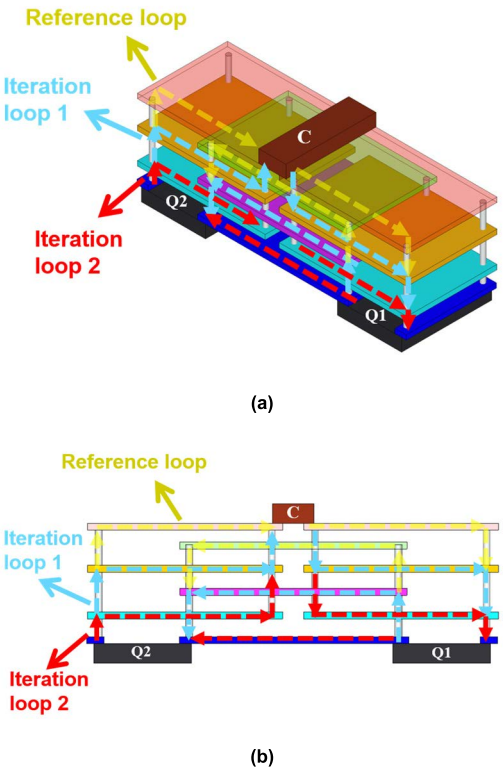


FIGURE 10. Design result of power iteration loop. (a) side view of PCB, (b) cross-section view of PCB.

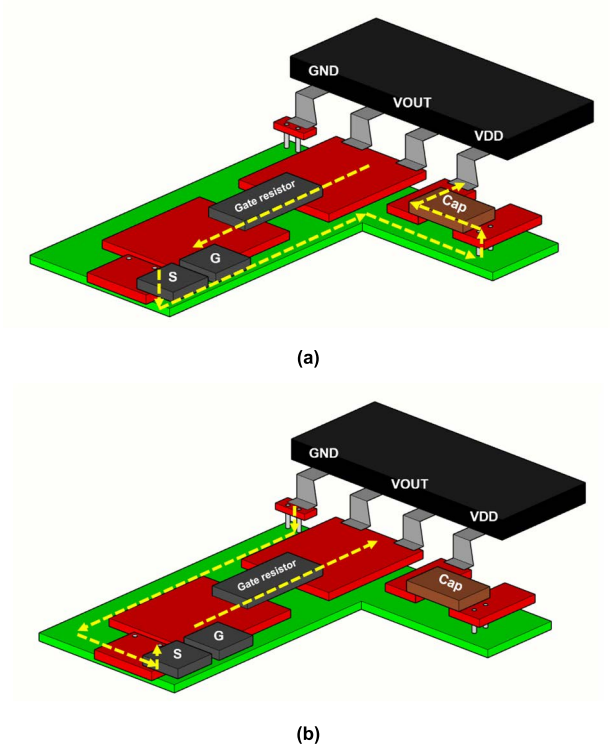


FIGURE 11. Reference gate loop design. (a) current path at turn-on, (b) current path at turn-off.

2) Config the iteration loops; When iteration loops to repeat the designed reference loop are configured, the structure shown in Fig. 8(b) is formed.

This procedure can significantly reduce the parasitic inductance by increasing flux cancellation between PCB layers

III. DESIGN EXAMPLE WITH PROPOSED VERTICAL LATTICE LOOP

This chapter details an example of the design of a half-bridge power circuit using the six-layered PCB with the proposed vertical lattice loop structure. The designed layer configuration of the power circuit PCB is the same as shown in Figure 8. The input capacitor C is placed on the top layer of the PCB, and GaN HEMT (Q1 and Q2) are placed on the bottom layer to reduce the parasitic inductance by minimizing the loop area [19].

Figure 9 shows an example of a power reference loop design. The power reference loop is designed with a top layer (on which capacitors are mounted) and an inner layer close to the top layer. Figure 10 shows an example of a power iteration loop design. There are two iteration loops; iteration loop 1 consists of inner layers 3 and 4, and iteration loop 2 consists of inner layer 5 and the bottom layer.

Figure 11 shows an example of a gate reference loop design. In this figure, the black square is the gate driver IC, *S* is the source, and *G* is the gate of GaN HEMT. Figure 11(a) and (b) show the current flow during turn-on and turn-off, respectively. To reduce the parasitic inductance in the gate loop, the distance between the gate driver IC and

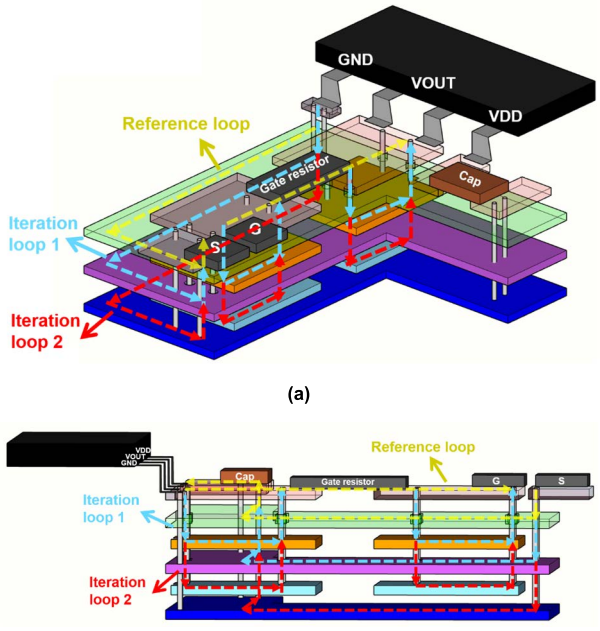


FIGURE 12. Iteration gate loop design during turn-on. (a) side view of PCB, (b) cross-section view of PCB.

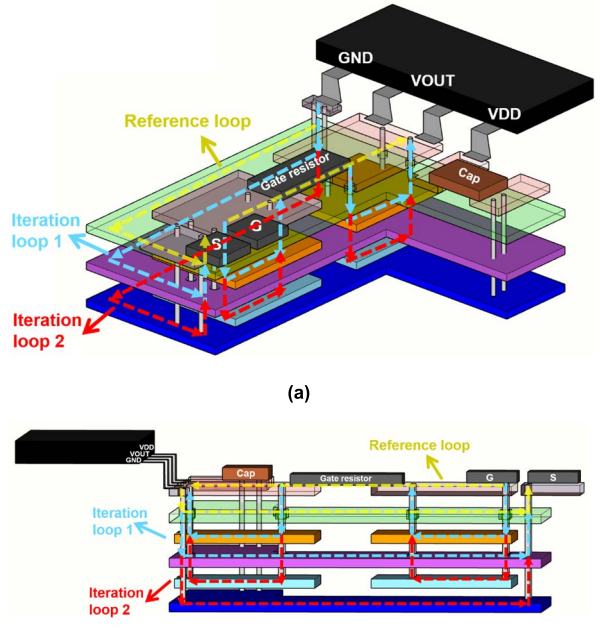


FIGURE 13. Iteration gate loop design during turn off. (a) side view of PCB, (b) cross-section view of PCB.

transistor should be marginal and flux cancellation should be considered as shown in Figure 11. Figure 12 shows a design result of a gate iteration loop during turn-on. Iteration loop 1 consists of inner layers 3 and 4, and iteration loop 2 consists of inner layer 5 and the bottom layer. Figure 13 shows design result of a gate iteration loop during turn-off. Iteration loop 1 consists of inner layers 3 and 4, and iteration loop 2 consists of inner layers 5 and the bottom layer.

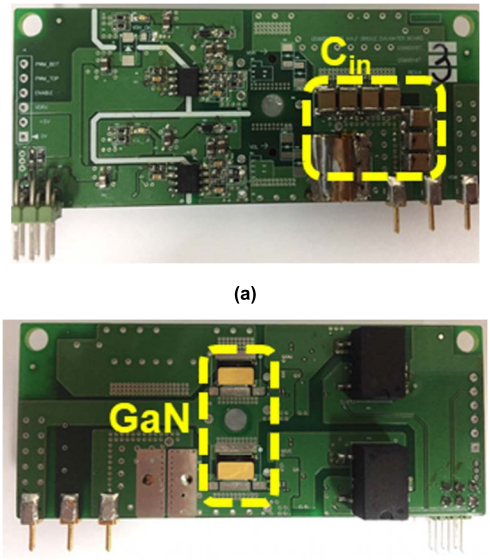


FIGURE 14. A photograph of the PCB with the proposed vertical lattice loop design. (a) top view, (b) bottom view.

TABLE 2. Comparison of parasitic inductance.

Parameter	Without proposed vertical lattice loop [nH]	With proposed vertical lattice loop [nH]
$L_{D,u}$	1.41	1.55
$L_{S,u}$	0.02	0.02
$L_{D,d}$	3.45	1.76
$L_{SS,d}$	1.00	0.50
$L_{S,d}$	6.25	2.01
$L_{Gon,d}$	5.43	2.94
$L_{Goff,d}$	7.35	3.58

TABLE 3. System parameters.

Parameter	Value
Drain current	20 [A]
Gate-source voltage (on)	6 [V]
Gate-source voltage (off)	-3 [V]
DC voltage	200 [V]
Load inductance	200 [nH]
Gate resistor (on)	10 [Ω]
Gate resistor (off)	2 [Ω]

Figure 14 shows the manufactured prototype PCB based on the design result. Table 2 shows the parasitic inductance analysis results based on Ansys Q3D simulation. $L_{D,u}$ is the drain inductance of the top switch, $L_{S,u}$ is the source inductance of the top switch, $L_{D,d}$ is the drain inductance of the bottom switch, $L_{S,d}$ is the source inductance of the bottom switch, and $L_{SS,u}$ is the parasitic inductance of the source shared by the gate loop and power loop. $L_{Gon,d}$ and $L_{Goff,d}$ are the parasitic inductances when the gate loop is turned on and off, respectively.

Figure 15 is the equivalent circuit reflecting the inductance analysis results. The dotted and solid lines represent the

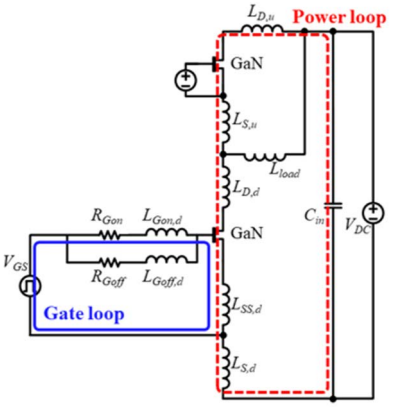


FIGURE 15. Double pulse test circuit with the parasitic inductance components.

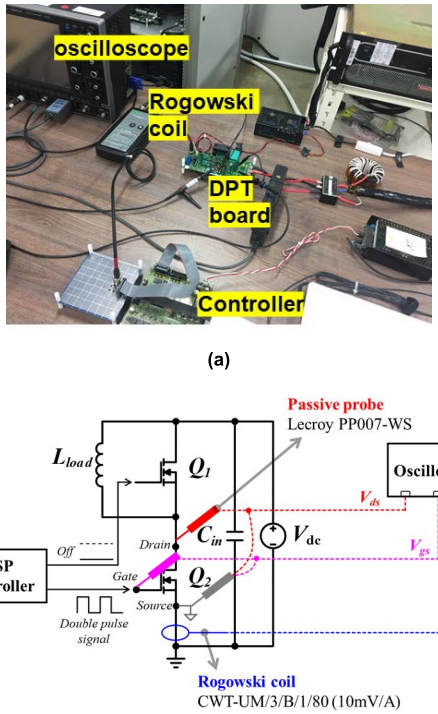
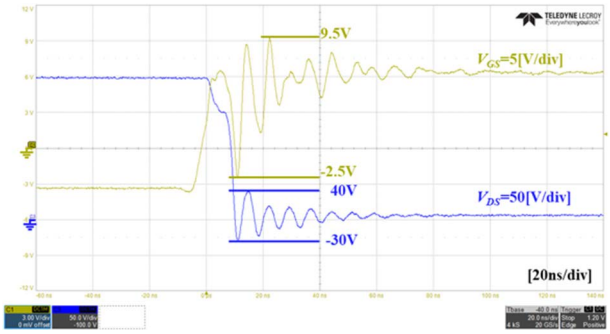


FIGURE 16. Experimental configuration. (a) Photograph of an experiment setup, (b) an overall diagram of electrical wiring and measurement equipment.

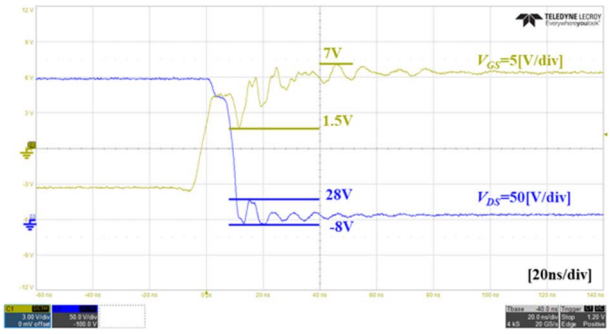
power loop and gate loop, respectively. From Table 2 and Figure 15, when the vertical lattice loop structure is applied, the gate loop inductance at turn on, gate loop inductance at turn off, and power loop inductance are calculated as 3.44 nH, 4.08 nH, and 5.84 nH, respectively. In contrast, for an identical PCB condition without the vertical lattice loop structure, the values are 6.43 nH, 8.35 nH, and 12.13 nH, respectively. Therefore, these three leakage inductance parameters are reduced by approximately 50%.

IV. PERFORMANCE VERIFICATION

To verify the effect of a reduction in parasitic inductance based on the proposed method, a double pulse test

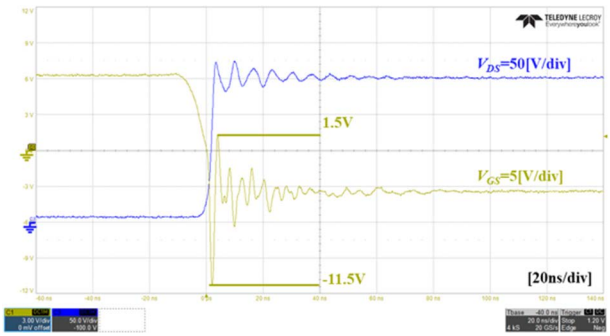


(a)

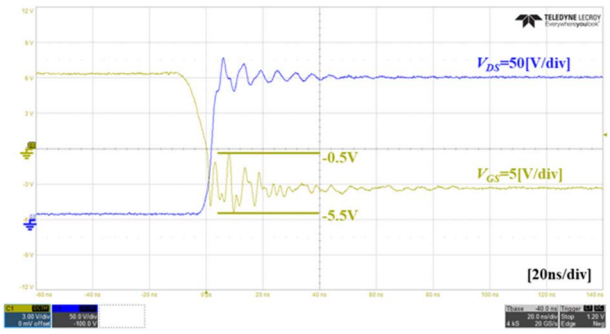


(b)

FIGURE 17. Gate-source voltage and drain-source voltage waveform during turn-on, (a) without vertical lattice loop structure (b) with proposed vertical lattice loop structure.



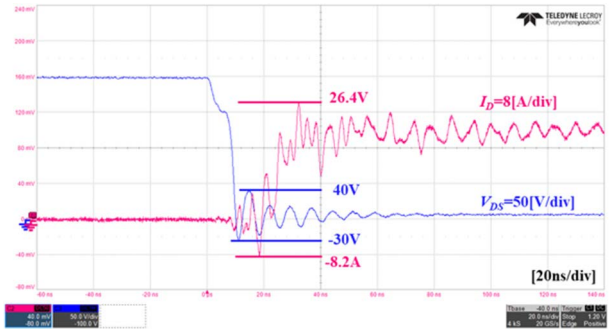
(a)



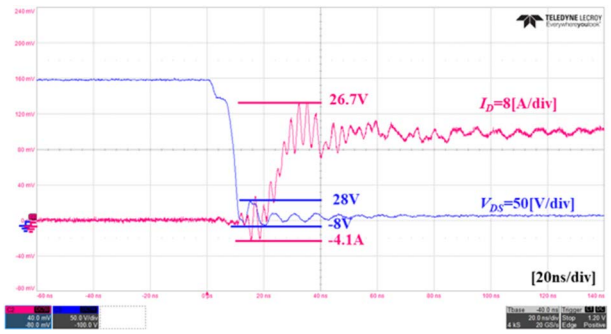
(b)

FIGURE 18. Gate-source voltage and drain-source voltage waveform during turn-off, (a) without vertical lattice loop structure (b) with proposed vertical lattice loop structure.

is performed. The experimental parameters are presented in Table 3.



(a)



(b)

FIGURE 19. Drain current and drain-source voltage waveform during turn-on, (a) without vertical lattice loop structure (b) with proposed vertical lattice loop structure.

Figure 16 shows the experimental configuration. It consists of an oscilloscope (Lecroy); Rogowski coil (PEM, CWT-UM/3/B/1/80); digital signal processors and controller (TMS320F28335, Texas Instruments); and a double-pulse test board with GaN HEMT (GS66508T, GaN Systems). Figure 17 is an experimental waveform showing the gate-source voltage and drain-source voltage at turn-on. Figure 17(a) and (b) show the gate-source waveform without and with vertical lattice loop structure, respectively. When the vertical lattice loop structure is applied, the gate-source voltage ringing size is reduced from 12 V to 5.5 V, and the drain-source voltage ringing size is reduced from 70 V to 36 V. Figure 18 is a waveform showing the gate-source voltage and drain-source voltage at turn-on. Figure 18(a) and (b) show the gate-source waveform without and with vertical lattice loop structure, respectively. The gate-source voltage ringing size is reduced from 13 V to 5 V when the vertical lattice loop structure is applied.

Figure 19 is an enlarged waveform of the drain-source voltage and drain current for deriving the switching energy. Figure 19(a) shows a waveform without vertical lattice loop structure, whereas Figure 19(b) shows a waveform to which the vertical lattice loop structure is applied. A comparison of the two waveforms reveals the difference in overshoot and ringing size. The size of the drain current ringing is reduced from 34.6 A to 30.8 A. From experimental results, it can be seen that the ringing and overshoot of the gate-source voltage, the drain-source voltage, and the drain current are effectively

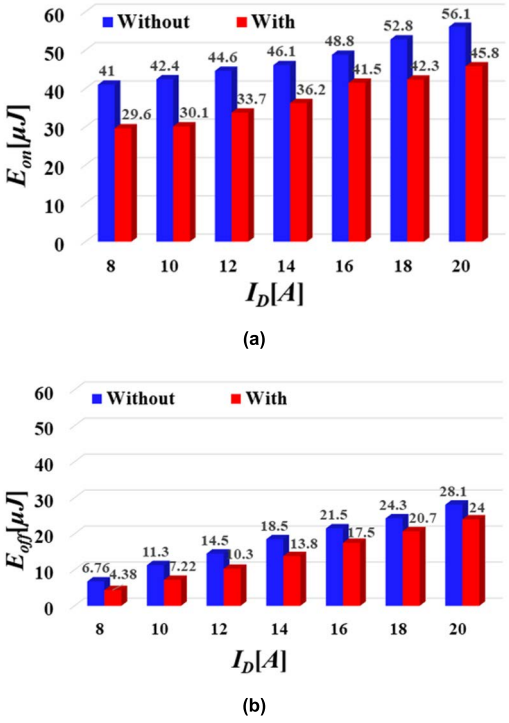


FIGURE 20. GaN switching energy analysis (a) turn-on, (b) turn-off.

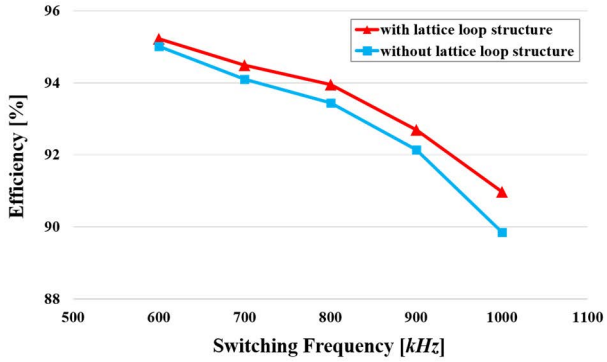


FIGURE 21. Comparison of efficiency based on 125 W buck converter.

reduced with proposed vertical lattice loop structure. This reduction makes driving GaN HEMTs stable and decreasing switching energy at the same time.

Figure 20 shows the switching energy at turn-on and turn-off. The switching energy is calculated based on the variation in current. Figure 20(a) and (b) shows the switching energy at turn-on and turn-off, respectively. E_{on} means consumed switching energy from when V_{gs} is 10% until V_{ds} is 0 V. In addition, E_{off} means switching energy from when V_{gs} is 90% until I_d is 0 A. Furthermore, to verify the effect of ringing due to the parasitic inductance, the second ringing is included, which is V_{ds} and I_{ds} reached the second zero values. Through these results, it can be seen that both turn-on and turn-off energy can be reduced when the proposed method is applied.

For additional verification of the effect of a reduction in parasitic inductance, a design with a 125 W buck converter (input voltage of 50 V, input current of 2.5 A, the output voltage of 25 V, and output current of 5A) is designed based on the PCB shown in Figure 14. Figure 21 is an efficiency curve of the buck converter with or without a vertical lattice loop structure. At 1 MHz, the efficiency when the vertical lattice loop is applied is approximately 1.2% higher than that when it is not applied. This is because the switching loss is reduced by the reduced parasitic inductance. Through these experimental results, it is verified that the proposed vertical lattice loop structure is effective in improving efficiency and high-frequency operation. Furthermore, it was verified that the proposed structure is more efficient when the GaN HEMTs are driven at high frequency and light loads.

V. CONCLUSION

In this paper, the vertical lattice loop structure to reduce parasitic inductance was proposed. The proposed vertical lattice loop structure is designed with reference loop and iteration loop. Based on the simulation analysis, the parasitic inductance is reduced by 40% with the proposed vertical lattice loop structure. In design example, it shows how the proposed vertical lattice loop structure is applied to the power loop and gate loop respectively. A half-bridge circuit is designed with the proposed structure and a double-pulse test is conducted. From the experimental results, it can be seen that the circuit with the proposed method has a smaller overshoot and ringing size. When the proposed vertical lattice loop structure was applied at the buck converter, it shows that there is an efficiency increase of 1.2% at 1 MHz.

The proposed method can effectively reduce the parasitic inductance, and through this, the turn-on and turn-off characteristics of the GaN HEMT driving circuit are stably improved, and the effect of improving the efficiency is further verified. In addition, the proposed method has versatility because it can be applied regardless of the package type of GaN HEMT. Further, improved stable operation and efficiency increase of power conversion systems can be expected.

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