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RESEARCH ARTICLE

A Charge Loss Aware Advanced Model of Dickson Voltage Multipliers

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ABSTRACT In this paper an advanced and accurate model of the Dickson Voltage Multiplier (DVM) accounting for charge-loss nonidealities, like reverse and substrate currents of the charge transfer devices, is proposed. Analytical equations for the single current loss and the various metrics are given. In particular, by inspection of the open-circuit output voltage, it is shown that such currents limit the range of the suitable clock frequency, suggesting the introduction of a further switching limit, namely deep slow switching limit, which is not predictable by the well-known models. Gathered results can be fruitfully exploited to improve the design accuracy of the DVMs for low-voltage, low-power applications. Simulation using SPICE and measurement results on silicon prototypes implemented in 130-nm HV-CMOS and a 65-nm standard CMOS technology confirm the accuracy of the proposed model with a maximum error of 5.5%.

INDEX TERMS Charge pump, DC-DC converter, Dickson voltage multiplier, energy harvesting, charge losses.

I. INTRODUCTION

In modern applications, such as energy-autonomous systems for the Internet of Medical Things (IoMT) or Wireless Sensor Networks (WSNs), voltage multipliers are ubiquitous blocks that allow on-chip step-up power conversion [1], [2], [3], [4], [5], [6], [7], [8], [9], [10]. The reason can be found in the energy autonomy of the nodes, which is enabled by adopting energy scavengers, whose output voltage form and level are often unsuitable to directly feed the equipped blocks (e.g., data processors, transceivers, sensors, and actuators). Therefore, power converters are mandatory to adapt the voltage to the needed DC profile and level. At this purpose, switched capacitors circuits are the most widespread solutions for IC systems. Focusing on the class of DC-DC boost converters, the most common adopted topology is the Dickson Charge Pump (CP), also known as Dickson Voltage Multiplier (DVM) [11], [12], [13], [14], [15], [16], [17], [18], [19].

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A lot of works dealt with this topic. Some of them are focused on key parameters, as the settling time (defined as the time required to settle to the nominal output voltage), the voltage gain, the conversion efficiency and their relationships with DVM design parameters and first order components' nonidealities (like top and bottom parasitic capacitances of the used pumping capacitors and finite threshold voltage, on-resistance and reverse current loss of the switches) [20], [21], [22], [23], [24].

Other works aim to rig up new optimization design strategies exploiting the introduced models to selectively improve the afore-mentioned key parameters [25], [26], [27], [28], [29], [30], [31]. New perspectives are also opening about these converters affirming them as a very versatile block. Some examples are reported in the recent works where the DVM is proposed to amplify signals [31], [32] or as a ramp generator [33]. In these applications a biasing current is mandatory to set the quiescent point of the DVM or to change the slope of the generated ramp. Moreover, controlled currents, opportunely sunk from each single stage, has revealed a promising while novel method to regulate the output voltage of the multiplier [34], [35]. Thus, a certain interest on

understanding as the DVM performances change when charge is lost from different sections of the DVM is increasing.

In all the previous literature, however, it is also assumed that both the charge losses toward the substrate of the active devices used as inter-stage switches and charge losses of the stage capacitors are negligible. However, such assumptions are not valid anymore in scaled technologies, where the current losses due to charge to the substrate of the inter-stage switches and the capacitors are comparable to the CP output current.

In this work we aim to accurately investigate the effect of charge loss nonidealities on the behavior of the DVM including the limits of the charge transfer between the stages. Analytical results have been extensively validated through both SPICE simulations and measurements on a 4-stage latched DVM implemented using a 130-nm HV-CMOS technology and 2-, 4- and 6-stage DVM in a 65-nm standard CMOS technology.

The remainder of the paper is organized as follows. Section II shows a DVM dynamic model as resulting from the state-of-the-art. Section III reviews such model considering charge parasitic losses loss. Section IV gathers simulation and measurement results and, finally, conclusion remarks and some application notes are done. An Appendix dealing with some technological considerations on the devices' parasitic effects is also included.

II. DVM DYNAMIC MODEL: STATE-OF-THE-ART

Figure 1 shows the simplified block diagram of a DVM. Without loss in consistence, the number of stages, N, can be assumed an integer arbitrary value. Each switch is considered a two-terminals building block and is referred to as Charge Transfer Device, (CTD).

The purpose of the CTD, which can be a simple diode, a diode-connected transistor or a more complex multi-transistor circuit [36], [37], [38], is to unidirectionally transfer the charge from one stage to the following one. Each pumping capacitor has a constant capacitance value, C, and the voltage gain per stage is assumed to be the same for each stage, supposing the amplitudes of the counter-phase clock signals, V_{CK} and V_{CKn}, equal to the input voltage, V_{IN}. Moreover, the charge losses are assumed to be the same for each device. Finally, the load is constituted by the capacitance C_L and current I_{OUT}.

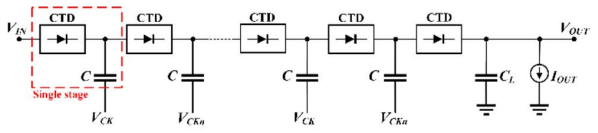


FIGURE 1. Schematic diagram of the conventional DVM.

As shown in [25], assuming that DVM in Fig. 1 works in Slow Switching Limit (SSL), i.e. assuming that in each clock semi-period the charge is totally transferred from one pumping capacitor to the following, we can model it with the RC-equivalent circuit in Fig. 2. In this figure ΔV_{IN} and ΔV_{OUT} represent input and output voltage increments in steady state, respectively. The ideal transformer models the power conversion given by the charge pumping mechanism, whose ideal conversion factor, G_{DVMi}, is equal to $N + 1$. Finally, ideal output resistance and self-capacitance of the DVM are expressed by

$$R_{OUT,i} = \frac{N}{fC} \tag{1a}$$

$$C_{EQ,i} = \frac{A(N)}{N+1} C \tag{1b}$$

where f is the clock frequency and $A(N)$, function of the number N, is defined in [21].[1]

According to the model in Fig. 2, the DVM time-domain dynamic within the SSL is only characterized by the time constant

$$\tau_{DVM,i} = R_{OUT,i} \left(C_{EQ,i} + C_L \right) \tag{2}$$

in which the product $R_{OUT,i} \cdot C_{EQ,i}$ represents the ideal intrinsic time constant of the voltage multiplier. Neglecting the output capacitive load, parameter $\tau_{DVM,i}$ decreases as $1/f$, since the output resistance shows this behavior. In this case, DVM settling time, T_S, whose value is strictly dependent by $\tau_{DVM,i}$, is function of the number of stages and clock frequency only.

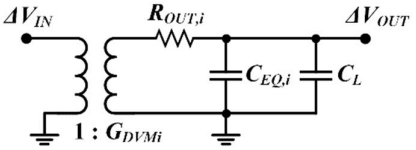


FIGURE 2. First order equivalent model of Dickson voltage multiplier.

In a more realistic case, the finite resistance of the CTD, R_D, and the top stray capacitances of the pumping capacitors, C_T, limit the charge transfer deviating the output dynamic from that predicted by (2). And an accurate model of the output resistance was proposed in [39]. The model in [40], confirming that one already predicted in [23], has the form

$$R_{OUT} = \frac{R_D}{\delta} \left(\frac{\delta}{\tau f} \right) \left[N \coth \left(\frac{\delta}{\tau f} \right) + \operatorname{csch} \left(\frac{\delta}{\tau f} \right) \right] \tag{3}$$

where $\delta \leq 0.5$ is the duty cycle of the clock signal and the time constant $\tau = R_D(C + C_T)$ leads the inter-stage conduction transient. By inspection of (3), R_{OUT} shows the same behavior of (1a) when $\delta/f \gg \tau$, i.e. when the clock frequency is enough small to allow the total charge transfer (i.e., SSL).

When $\delta/f \leq \tau$ the charge is partially transferred from one stage to the other and R_{OUT} approaches its minimum $R_D (N + 1)/\delta$. Thus, in this regime, which is referred to as Fast

[1]The function A(N), introduced in [21], is equal to $A(N) = \frac{N\left(4N^2+3N+2\right)}{12(N+1)}$, for even N; $A(N) = \frac{4N^2-N-3}{12}$, for odd N.

Switching Limit (FSL), the voltage multiplier shows an output resistance given by the effective resistance of the single CTD, R_D/δ, times their number $N+1$, in the full respect of the knowledge about switched capacitor converters [23].

Note that the factor $1/\delta$ comes from the fact that the charge transfer through each switching device is limited by the minimum conduction time window δ/f.

Generalizing, intrinsic time constant in (2) assumes the expression in (4)

$$\tau_{DVM} = R_{OUT}\left(C_{EQ} + C_L\right) \tag{4}$$

where C_{EQ} includes also parasitic effects of the top stray capacitances, thus

$$C_{EQ} = \frac{A(N)}{N+1}\left(C + C_T\right) \tag{5}$$

Furthermore, another effect of C_T is to decrease the effective gain of the DVM due to charge partition with C, also affected by a possible drop voltage, V_D, due to nonidealities of the charge transfer device. Hence, the gain is reduced from its maximum, $N+1$, to

$$\begin{aligned} G_{DVM} &= \left(\frac{N}{1+{C_T}/{C}} + 1\right)\left(1 - \frac{V_D}{V_{IN}}\right) \\ &= \left(\frac{N}{1+\alpha_T} + 1\right)\left(1 - \frac{V_D}{V_{IN}}\right) \end{aligned} \tag{6}$$

The parameter α_T, that is equal to the ratio between top stray capacitance and the pumping capacitance, is often used in the modeling and design. It only depends by the adopted technology, if connections and CTD parasitic capacitances can be neglected.

The complete expression of the output voltage, including an output demanded current, I_{OUT}, and assuming the output initial voltage set to 0, results

$$V_{OUT} = V_{IN}G_{DVM}\left[1 - \exp\left(-\frac{t}{\tau_{DVM}}\right)\right] - R_{OUT}I_{OUT} \tag{7}$$

For a complete overview of the DVM, besides the output voltage behavior, an analysis of the power conversion efficiency (PCE), defined as the ratio between output and input power, must be carried out. As first, it should be noted that input power is constituted by a main term related to the output supplied power and the gain of the DVM. A simple inspection of Fig. 2, shows that this first term is

$$P_{IN} = P_{OUT}\left(1 + G_{DVM}R_{OUT}\frac{I_{OUT}}{V_{OUT}}\right) \tag{8}$$

Expression in (8) highlights as the power conversion operated by the DVM is intrinsically inefficient and that to increase efficiency of this block (i.e., making P_{IN} closer to P_{OUT}), the output DVM resistance should be made as small as possible, for example increasing the pumping capacitance or the clock frequency and lowering the CTD on-resistance.

In practical cases, a further term can be added to (8) in order to take into account the switching power losses of the stray capacitances tied to the bottom plate of each pumping capacitor.

Like for digital circuits, the switching power losses are due to continuous commutations on the switched nodes. In the DVM, in particular, commuted nodes are essentially connected to the pumping capacitors plates. Moreover, in steady state all nodes experience the same voltage variation, equal to the clock amplitude, V_{CK}. Therefore, naming C_B the contribute of the bottom plate capacitance of each CP capacitor, the total switching power losses can be valued as

$$P_{LOSS,SW} = N(C_B + C_T)f\,(V_{IN})^2 \tag{9}$$

Eq. (9) must be added to the second term of (8), resulting on the whole power conversion efficiency expressed by

$$PCE = \frac{P_{OUT}}{P_{IN}} = \left(1 + G_{DVM}R_{OUT}\frac{I_{OUT}}{V_{OUT}} + \frac{N(C_B + C_T)f\,(V_{IN})^2}{V_{OUT}\cdot I_{OUT}}\right)^{-1} \tag{10}$$

III. THE PROPOSED MODEL

Starting from the considerations discussed in the previous sections, to analyze a more realistic scenario for a DVM the computation of charge loss nonidealities must be accounted (see Appendix). At this purpose, let us consider the generic single-stage equivalent circuit shown in Fig.3a.

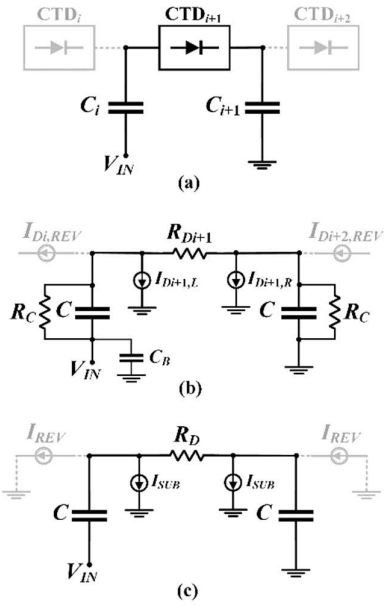


FIGURE 3. (a): single-stage of a DVM; (b): equivalent model with parasitic current loss; (c): and the simplified one used in the analytical explanation.

Besides CTD's voltage drop V_D and charge partition between C and C_T, already considered as voltage losses, and the switching-resistance R_D/δ, the circuit in Fig. 3b shows

four current sinks and the leakage resistances of the pumping capacitors.

The current sinks $I_{Di+1,L}$ and $I_{Di+1,R}$ model constant charge leakages seen at the left (input) and the right (output) terminal of the CTD, respectively. Their sizes can be different, like for a diode, or, at the least of any asymmetries, be the same as for a diode-connected MOSFET where the charge losses coincide, as first approximation, with the reverse saturation current of the reverse biased diffusion S/D to substrate junctions. However, it is worth noting that in the stage cascade the right terminal of the i-th and the left terminal of the $(i+1)$-th CTD, where $i = 1, 2 \ldots N$, are electrically connected together and, assuming the current losses be the same for all CTDs, their effect results in a whole output referred current loss $I_{SUB} = I_{D,L} + I_{D,R}$, so considered hereinafter.

Concerning the currents that reversely flow through the interdicted CTDs (i.e., $I_{Di+1,REV}$ and $I_{Di+2,REV}$ in Fig. 3b), being in steady state the voltages that turn-off the CTDs equal to $2V_{IN}$ [25], the two generators can be assumed equally sized. And this allows to consider the value of both generators equals to I_{REV}. Consider, however, that such currents act differently on the capacitors involved in the charge path during the single clock semi-cycle. In particular, looking at Fig. 3c the left-most current generator effectively sinks charge from the nearest pumping capacitor.

From the point of view of the simplified model, a current I_{REV} is subtracted to the transferred one and apparently lost but, excluding the first stage where the turned-off CTD sees the input voltage source tied to its left side, the current provides a charge injection to the pumping capacitor of the previous stage.

This mode described above characterizes the working principle of the right-most current generator, which instead increases the level of charge in its nearest capacitor. Intuitively it is apparent that such current is not lost. However, analysis results, as confirmed by the validation ones, show that reverse currents determine self-power consumptions and functional limitations of the DVM.

As last, leakage resistance, R_C, models nonideality of the dielectric of the pumping capacitor, while C_B represents its bottom plate stray capacitance. It is worth noting that C_B does not considerably affect the DVM open-circuit output transient response if the driving capability of the clock drivers is high enough. This condition is satisfied almost always, and, for this reason, such contribute is neglected in this paper. Similarly, the effect of R_C can be neglected if the intrinsic inter-stage time constant τ is sufficiently lower than $\tau_C = CR_C$, which is equivalent to assume $R_C \gg R_D$. This assumption is accounted in the following analytical explanation also.

A. ANALYTICAL EXPLANATION

This subsection discusses an enhanced version of the switch-resistance-aware DVM model already introduced in [26].

In particular, the equation between V_{OUT} and I_{OUT} is carried out including the reverse and substrate current losses

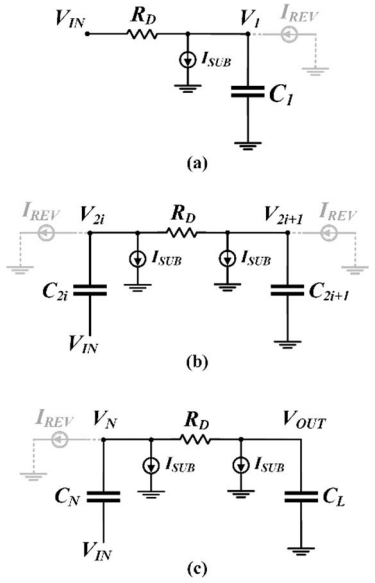


FIGURE 4. Voltage diagram of a) first, b) intermediate and c) last stage during the charge transferring time slot in the steady state.

and assuming the charges not fully transferred due to the resistance R_D of the CTD. Without loss in consistence, the effect of the constant voltage drop, V_D, of the CTDs and the parasitic capacitance C_T are neglected in this analysis.

Fig. 4(a)–(c) shows several combinations among the voltage multiplier in steady state. The period when the switch turns on, δT, is assumed to be equal to the period when the switch turns off and T $(=1/f)$ is the period of the clock. Let us indicate as $V_i = V_i(t)$ the voltage at node i $(1 \le i \le N)$, with $V_{i,i}$ the initial voltage of V_i in the first half of the period and with $V_{i,f}$ the final voltage of V_i in the same half-period. Additionally, let us indicate with $\tilde{V}_{i,i(f)}$ the initial (final) voltage of V_i in the second half of the period.

Although the CTD on-resistance varies with the node voltages, it is assumed that R_D is constant and represents the averaged value during δT. From Fig. 4(a)–(c), eqs. 11a-c hold during δT

$$C\frac{dV_1}{dt} = \frac{V_{IN} - V_1}{R_D} + (I_{REV} - I_{SUB}) \tag{11a}$$

$$\begin{cases} -C\dfrac{dV_{2i}}{dt} = \dfrac{V_{2i} - V_{2i+1}}{R_D} + (I_{REV} + I_{SUB}) \\ C\dfrac{dV_{2i+1}}{dt} = \dfrac{V_{2i} - V_{2i+1}}{R_D} + (I_{REV} - I_{SUB}) \end{cases} \tag{11b}$$

$$-C\frac{dV_N}{dt} = \frac{V_N - V_{OUT}}{R_D} + (I_{REV} + I_{SUB}) \tag{11c}$$

The initial and final voltages at each capacitor node in each half-period are related one another as follows:

$$\tilde{V}_{2i-1,f} - V_{IN} = V_{2i-1,i} \tag{12a}$$

$$\tilde{V}_{2i-1,i} = V_{2i-1,f} + V_{IN} \tag{12b}$$

$$\tilde{V}_{2i,f} + V_{IN} = V_{2i,i} \tag{12c}$$

$$\tilde{V}_{2i,i} = V_{2i,f} - V_{IN} \tag{12d}$$

And the steady state indicates the following relations for each pumping capacitor:

$$C\left(V_{1,f}-V_{1,i}\right)=\left[I_{OUT}+(N+1)\,I_{SUB}+I_{REV}\right]T - I_{SUB}\,(1-\delta)\,T \tag{13a}$$

$$\begin{cases} C\left(V_{2i,f}-V_{2i,i}\right)=-\left[I_{OUT}+(N+2-2i)\,I_{SUB}+I_{REV}\right] \times T+I_{SUB}\,(1-\delta)\,T \\ C\left(V_{2i+1,f}-V_{2i+1,i}\right) \\ \quad=\left[I_{OUT}+(N+1-2i)\,I_{SUB}+I_{REV}\right]T \\ \qquad -I_{SUB}\,(1-\delta)\,T \end{cases} \tag{13b}$$

$$C\left(V_{N,f}-V_{N,i}\right)=-\left(I_{OUT}+2I_{SUB}+I_{REV}\right)T + I_{SUB}\,(1-\delta)\,T \tag{13c}$$

where $(I_{OUT}+I_{SUB})T$ is the charge transferred to the output terminal in a period and $I_{SUB}(1-\delta)T$ the part of charge not transferred during the conduction phase.

From the conditions $V_1(0)=V_{1,i}$ and $V_1(\delta T)=V_{1,f}$, (11a) we get

$$V_{1,f}=\left[V_{IN}-R_D\left(I_{SUB}-I_{REV}\right)\right](1-\xi)+V_{1,i}\xi \tag{14}$$

where ξ is equal to $\exp(-\delta T/CR_D)$.

The first and second part of (11b) have to be combined to obtain differential and common mode equations (i.e., $d(V_{2i}-V_{2i+1})/dt$ and $d(V_{2i}+V_{2i+1})/dt$, respectively). Thus singularly solving and using them to obtain the final node voltage values, yield

$$V_{2i,f}=\frac{1}{2}\left[V_{2i,i}\left(1+\xi^2\right)+V_{2i+1,i}\left(1-\xi^2\right) - R_D I_{REV}\left(1-\xi^2\right)-2\frac{\delta T}{C}I_{SUB}\right] \tag{15a}$$

$$V_{2i+1,f}=\frac{1}{2}\left[V_{2i+1,i}\left(1+\xi^2\right)+V_{2i,i}\left(1-\xi^2\right) + R_D I_{REV}\left(1-\xi^2\right)-2\frac{\delta T}{C}I_{SUB}\right] \tag{15b}$$

Finally, (11c) results in

$$V_{OUT}=\frac{V_{N,f}-V_{N,i}\xi}{1-\xi}+R_D\left(I_{REV}+I_{SUB}\right) \tag{16}$$

Let us calculate the final voltage at each nodes whose sum will give the output voltage. From (14) and (13a), $V_{1,f}$ is calculated as

$$V_{1,f}=V_{IN}-\left[I_{OUT}+(N+\delta)\,I_{SUB}+I_{REV}\right]\frac{T}{C}\frac{\xi}{1-\xi} - R_D\left(I_{SUB}-I_{REV}\right) \tag{17a}$$

From the first to the last stage, exact solution of voltage in each intermediate node needs the knowledge of the voltage value of the node itself, its previous and its following ones in an entire clock period. This is allowed considering that during the second half period, equations that describe the node voltage of stages that transfer charge, superscripted with "$\sim$", show the same form of (11b) which results in (15a) and (15b). Therefore, from (15a) and using conditions (12a), (12b) and (12d), voltage of the odd-order nodes at the end of a complete cycle results

$$V_{2i-1,i}=\frac{1}{2}\left[V_{2i-1,f}\left(1+\xi^2\right)+V_{2i,f}\left(1-\xi^2\right)\right] - \left[\left(V_{IN}+\frac{R_D I_{REV}}{2}\right)\left(1-\xi^2\right)+\frac{\delta T}{C}I_{SUB}\right] \tag{17b}$$

which is completed by replacing the bottom placed relationship of (13b)

$$V_{2i,f}=V_{2i-1,f}+A_{2i} \tag{17c}$$

$$A_{2i}=2V_{IN}-\left[I_{OUT}+(N-2i+2\delta)\,I_{SUB}+I_{REV}\right] \times\frac{T}{C}\frac{2}{1-\xi^2}+R_D I_{REV} \tag{17d}$$

Similarly, from (15b) and (13b),

$$V_{2i+1,f}=V_{2i,f}+B_{2i+1} \tag{17e}$$

$$B_{2i+1}=-\left[I_{OUT}+(N+\delta-2i+1/2)\,I_{SUB}+I_{REV}\right] \times\frac{T}{C}\frac{2\xi^2}{1-\xi^2}-\frac{TI_{SUB}}{C}\frac{2\delta-1}{1-\xi^2}+R_D I_{REV} \tag{17f}$$

Summarizing, from (17c) and (17e), the following relationship are given

$$\begin{aligned} V_{2,f}&=V_{1,f}+A_2 \\ V_{3,f}&=V_{2,f}+B_3 \\ V_{4,f}&=V_{3,f}+A_4 \\ V_{5,f}&=V_{4,f}+B_5 \\ &\vdots \\ V_{N,f}&=V_{N-1,f}+A_N \\ \hline V_{N,f}&=V_{1,f}+\sum_{i=1}^{N/2}A_{2i}+\sum_{i=1}^{N/2-1}B_{2i+1} \end{aligned} \tag{17g}$$

Therefore, replacing (17a), (17d), (17f) in the last of (17g), yields

$$V_{N,f}=(N+1)\,V_{IN}+NR_D I_{REV}-\left(I_{OUT}+I_{REV}\right)\frac{T}{C} \times\left(N\frac{1+\xi^2}{1-\xi^2}+\frac{\xi}{1+\xi}\right) -\left\{\left[(N+1)/2+\delta\right]\frac{T}{C}\left(N\frac{1+\xi^2}{1-\xi^2}+\frac{2\xi}{1-\xi^2}\right) +R_D-\frac{(1+\delta)\,\xi}{1-\xi}\right\}I_{SUB} \tag{18}$$

From (16) and (13c), we get

$$V_{OUT}=V_{N,f}+R_D\left(I_{REV}+I_{SUB}\right) - \left[I_{OUT}+(1+\delta)\,I_{SUB}+I_{REV}\right]\frac{\xi}{1-\xi} \tag{19}$$

and, finally, from (18) and (19) yields

$$V_{OUT} = (N+1)(V_{IN} + R_D I_{REV}) - \{I_{OUT} + [(N+1)/2 + \delta] I_{SUB} + I_{REV}\} \times \frac{T}{C}\left(N\frac{1+\xi^2}{1-\xi^2} + \frac{2\xi}{1-\xi^2}\right) \quad (20)$$

Equation (20) can be re-written in a more compact form as

$$V_{OUT} = G_{DVMi}(V_{IN} + R_D I_{REV}) - \{I_{OUT} + [(N+1)/2 + \delta] I_{SUB} + I_{REV}\} R_{OUT} \quad (21)$$

where R_{OUT} is the DVM output resistance given by (3), in which the exponential terms have been replaced with the hyperbolic functions.

By inspection of (21) it is straight evident as the various current sources weight on the DVM output behavior. In particular, the effect of each single type of current is measured by the coefficient for that it is multiplied. For simplicity, each single coefficient is reported in the following

$$-\frac{\partial V_{OUT}}{\partial I_{OUT}} = \frac{T}{C}\left(N\frac{1+\xi^2}{1-\xi^2} + \frac{2\xi}{1-\xi^2}\right) = R_{OUT} \quad for\ I_{OUT} \quad (22a)$$

$$-\frac{\partial V_{OUT}}{\partial I_{SUB}} = [(N+1)/2 + \delta]\frac{T}{C}\left(N\frac{1+\xi^2}{1-\xi^2} + \frac{2\xi}{1-\xi^2}\right) = [(N+1)/2 + \delta] R_{OUT} \quad for\ I_{SUB} \quad (22b)$$

$$-\frac{\partial V_{OUT}}{\partial I_{REV}} = \frac{T}{C}\left(N\frac{1+\xi^2}{1-\xi^2} + \frac{2\xi}{1-\xi^2}\right) - (N+1) R_D = R_{OUT} - (N+1) R_D \quad for\ I_{REV} \quad (22c)$$

i.e. the coefficients in (22a) - (22c) have the same meaning of equivalent resistive contributions which weight the effect of the single current on the steady-state output voltage.

It is worth noting that when $I_{REV} = I_{SUB} = 0$, (21) differs from (7) only for the factor G_{DVM} that gathers the effect of the top stray capacitance of the pumping capacitors and the CTD voltage drop.

For completeness, another effect of the capacitance C_T is the increase of the total capacitive contribution of the single charge path, that is equivalent to have $(C + C_T)$ instead of C in all the equations reported in this section.

Relationship (21) is here validated by the first three plots reported in Fig. 5 where, more specifically, (22a), (22b) and (22c) are compared with SPICE simulation results as a function of the normalized clock frequency for DVMs with various number of stages. In these plots, R_D has been set to 10 kΩ, $C = 100$ pF, $\delta = 0.5$ and $C_T = 0$.

As it can be noted, there is a very good accuracy between simulations and the compared equations, with a maximum relative percentage error equal to 5.2%, 3.7% and 4.4% for Eq. (23a), (23b) and (23c), respectively. Thus, confirming the accuracy of the proposed model.

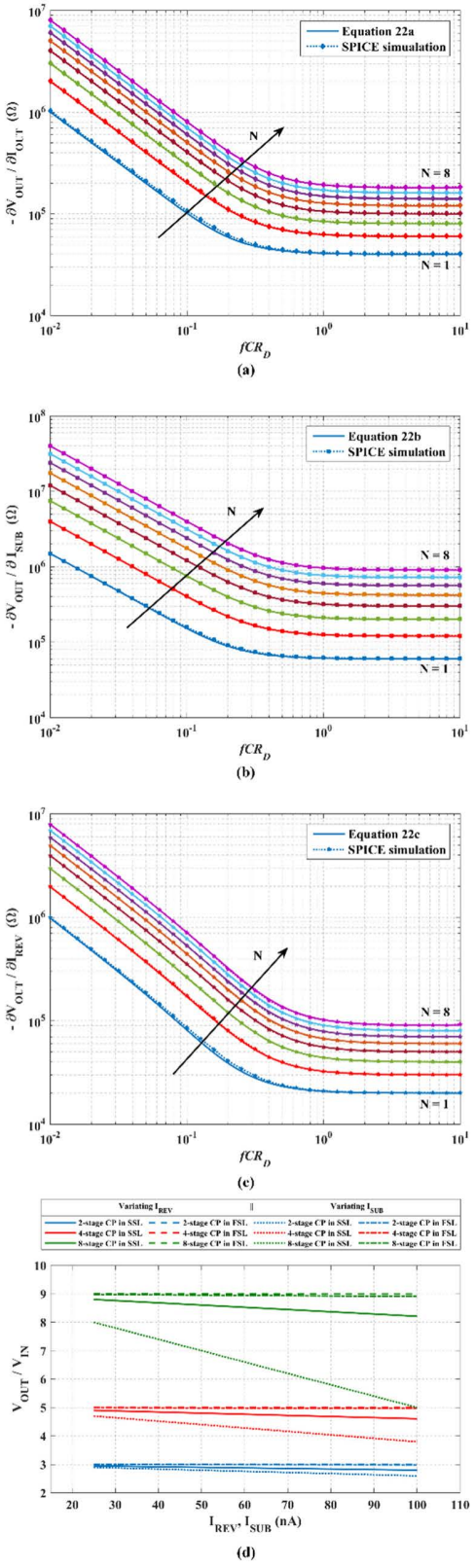


FIGURE 5. Analytical model to SPICE simulations comparison: (a) eq. (22a), (b) eq. (22b) and (c) eq. (22c); and voltage gain versus current losses (d).

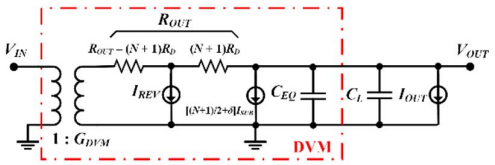


FIGURE 6. The proposed advanced model of Dickson voltage multiplier.

The effects of the two losses on the voltage gains are further shown in Fig. 5d, where output-to-input voltage ratio is plot for 2-, 4- and 8-stage CPs when the CP work in the two extremes of SSL and FSL.

The last term of each equation (22) shows as the parameter is in relationship with the DVM output resistance R_{OUT}. This comparison allows to introduce an advanced equivalent model which accounts for charge loss nonidealities. In particular, the current sinks, functions of I_{REV} and I_{SUB}, are added as compared to the conventional model, according to the model in Fig. 6, where V_{IN} and V_{OUT} are replaced to their increments.

It is worth noting that nullifying the output current, for the proposed model the DVM open-circuit output voltage depends by the clock frequency. In fact, two drawbacks caused by current losses are:

- reduction of the maximum open-circuit output voltage;
- introduction of an undesired like-pole behavior in the voltage gain, as it can be seen in Fig. 7.

This point is not predicted by previous models.

Figure 8a and 8b show as the voltage gain curves change for different values of current I_{SUB} and I_{REV}, distinctly. As can be seen output nodes reach their maximum values as slow as the current increases. In that figure, the output voltage of a sub-group of DVMs (to be precise, only the DVMs with even number of stages) has been reported but we assure that the results are independent by the order of N.

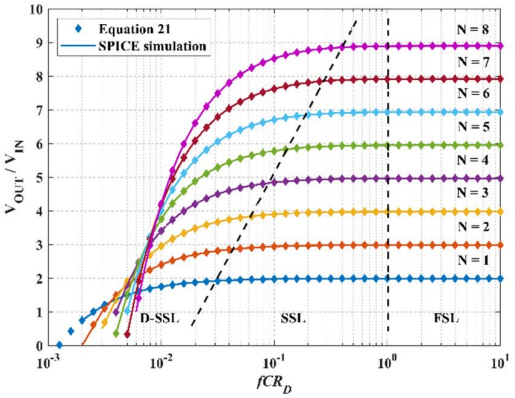


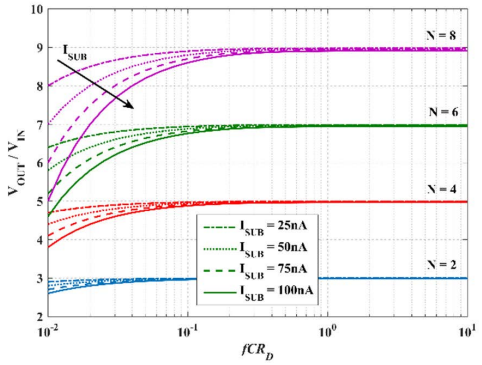
FIGURE 7. Simulation results of open-circuit voltage gain vs. normalized frequency for the various DVMs ($I_{REV} = I_{SUB} = 100$nA).

An analytical expression for the general poles is found by searching the clock frequency at which the output voltage approaches its halved maximum value, which is equivalent to the definition of the root at -3 dB in a Bode magnitude diagram. Thus, from (21) assuming these frequencies fall in SSL dominion, we obtain

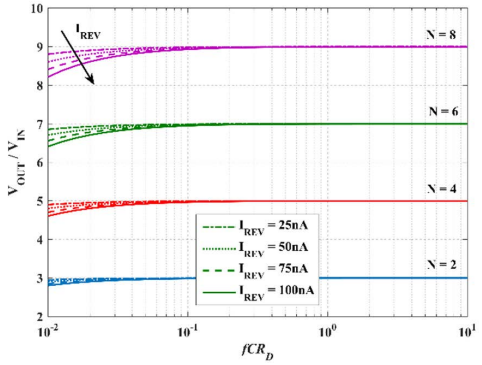
$$f_{p,I_{SUB}} = \frac{1}{2\pi} \frac{(G_{DVM}-1)(G_{DVM}+1) I_{SUB}}{C\left[G_{DVM} V_{IN} + 0.5 G_{DVM}(G_{DVM}+1) R_D I_{SUB}\right]} \tag{23a}$$

$$f_{p,I_{REV}} = \frac{1}{2\pi} \frac{G_{DVM}-1}{G_{DVM}} \frac{2I_{REV}}{C(V_{IN}+3R_D I_{REV})} \tag{23b}$$

The presence of these poles, which effectively limit the response of the DVM when exploited in low-power applications, suggests the introduction of a new limit, which we refer to as Deep-SSL.



(a)



(b)

FIGURE 8. Simulation results of open-circuit voltage gain vs. normalized frequency for the even-order DVMs and various (a) I_{SUB} and (b) I_{REV}.

Finally, the charge loss nonidealities determine self-power dissipations for the DVM, which must be accounted in the evaluation of PCE. Such power losses can be calculated starting from the coefficients expressed in (22) and are given by

$$P_{LOSS,I_{SUB}} = R_{OUT}\left(\frac{N+2}{2} I_{SUB}\right)^2 \tag{24a}$$

$$P_{LOSS,I_{REV}} = (R_{OUT} - (N+1) R_D) I_{REV}^2 \tag{24b}$$

Relations (24) have to be added to (8) and (9) to completely compute the input power.

IV. SIMULATION AND MEASUREMENT RESULTS

Validation of the proposed model has been carried out by exploiting DVMs with different number of stages and implemented by using two scaled and different technology

nodes: a 130-nm HV-CMOS and a 65-nm standard CMOS. Transient measurements were executed for DVMs with a number of stages equal to 2, 4 and 6 when designed with the 65-nm technology, while a single 4-stage DVM is implemented using the 130-nm one.

The topology of the CTD for all the DVMs is chosen to be the latched CMOS inverter-based structure (also known as dual-branch cross-coupled CPs) depicted in Fig.9a [39]. Such choice is adopted for two main reasons. Firstly, the latched CTDs, are widely adopted for their advantages in terms of output voltage ripple, self-starting mechanism, low reverse current losses (even if they suffer of reduced performances when work with input voltage lower than the threshold of the used transistors). Secondly, since the MOSFETs of complementary pairs involved in the chain work in triode region when turned on, it allows us to model their behavior by using a simple resistance, formally coincident with R_D, and a voltage generator with $V_D = 0$V.

Figures 9b and 9c reports microphotographs of the two dies whose area is equal to 0.03 mm^2 and $N \times 0.003$ mm^2 (for the single DVM in 65-nm CMOS).

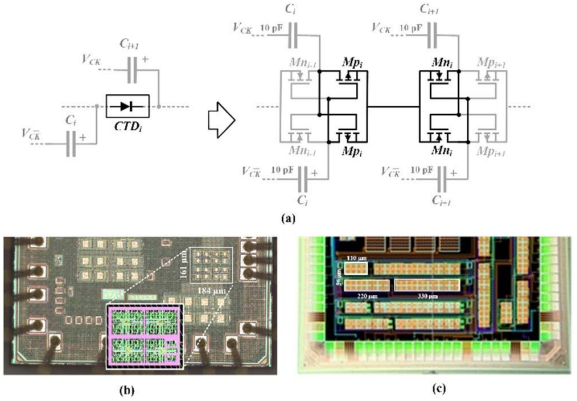


FIGURE 9. (a) Topology of the CTD and microphotographs of dies in (b) 130-nm HV-CMOS and (c) 65-nm standard CMOS technologies.

To emphasize the contribution of the frequency to the main performance of the circuit and contextually preserve silicon area (as compact as possible to that of the entire chip), the transistors have been sized to have $R_D = 10$ kΩ for each CTD, consequently, aspect ratio are equal to $(W/L) = 26/0.26$ (μm/μm) and 10/0.1 (μm/μm) for the 130-nm and the 65-nm technology, respectively. Note that the transistor channel length is not set to the minimum value to increase resistance of the CTD in the off state.

The comparison between various DVMs has been carried out for an equal input voltage, $V_{IN} = 400$ mV. The capacitors, which are all set equal to 10 pF, are implemented using the Metal-Insulator-Metal (MIM) option, which is available in both the considered technologies. The clock frequency ranges as 100 Hz $\leq f \leq$ 30 MHz and the duty-cycle is set to the maximum for this application, i.e. 0.5. It is worth nothing that the chosen values for the various parameters are consistent with the typical values used for the actual applications [1], [2], [15].

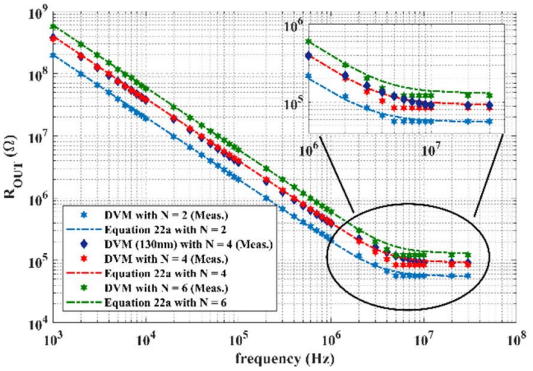


FIGURE 10. Output resistance vs. clock frequency.

Figure 10 reports the measured output resistance of the various DVMs versus the switching frequency as compared with the theoretical curve predicted by eq. (22a). A good superposition (maximum percentage error in the worst case is equal to 14.2%) of the various curves confirms the analytical predictions.

In order to indirectly evaluate the various parasitic contributions, the following measurement have been carried out. Open-circuit output voltage has been used to find C_T. Analogously, measurements of the input power consumption are performed at a relatively high frequency (in this case 10 MHz) when the output node is unloaded, in order to account for only the switching power losses, but neglect other contributes due to current loss, see eqs. (24a) and (24b), as well as the output power, see (9). Therefore, having calculate C_T, from the input power consumption we can find C_B.

TABLE 1. Measured voltage multiplier parameters for 10 samples.

	Parameter	Measured Value: μ	σ	$(\sigma/\mu)_{\%}$
130-nm	C_T (fF)	190 (1.9% of C)	13	5
	C_B (fF)	340 (3.4% of C)	7	8.1
	R_D (kΩ)	9.2	0.2	2.2
	I_{SUB} (pA)[a]	1	NA	
	I_{REV} (pA)	10	NA[b]	
65-nm	C_T (fF)	51 (0.5% of C)	12	23.5
	C_B (fF)	320 (3.5% of C)	79	24.7
	R_D (kΩ)	9.2	0.3	3.2
	I_{SUB} (pA)[a]	100	NA	
	I_{REV} (nA)	5.5	0.3	5.6

a: simulated
b: variations below the instrument resolution, the value of σ cannot be valued.

Finally, the output measured resistance in FSL has been used to obtain the R_D value. The average input powers in such case are 7.4 μW for the 4-stage DVM in 130-nm CMOS technology and 5.32, 9.93, 14.59 μW for 2-, 4- and 6-stage DVM in 65-nm, respectively.

Curves in Fig. 10 and input power allow to evaluate parasitic parameters C_T, C_B and R_D as reported in Table 1.

Finally, predicted and measured ratios of the open-circuit output voltage over the input voltage of the considered DVMs

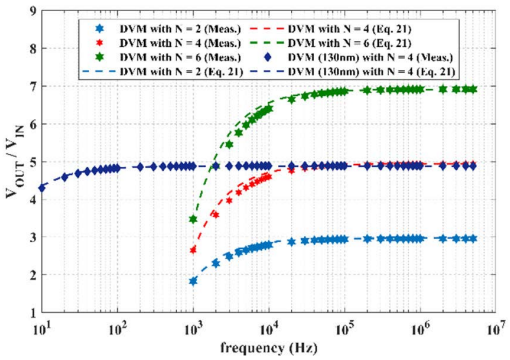


FIGURE 11. Open-circuit output voltage over input voltage vs. clock frequency.

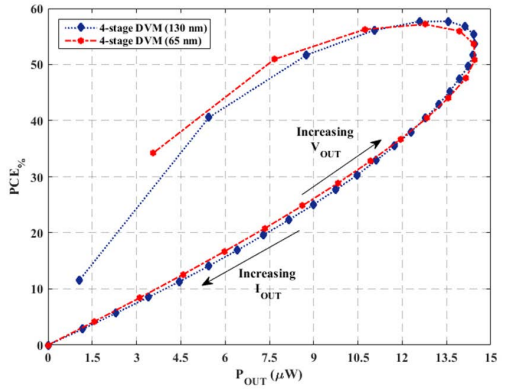


FIGURE 12. 4-stage DVMs power conversion efficiency vs. output power.

are shown in Fig. 11. From the graphical comparison in Fig. 11, it is possible to deduce that the proposed model in (21) accurately describes the response of the DVMs. Indeed, the maximum percentage error is lower than 5.5%, 13.9% and 2.8%, within Deep-SSL, SSL and FSL, respectively, as compared to the analytical model. The error is probably caused by the EPR of the pumping capacitors, which is the worsen in the most scaled technology. A good superposition of the various curves confirms again the accuracy of the analytical model. Moreover, by inspection of the curves of both 4-stage DVMs is evident that CTDs suffer of different reverse and substrate current losses which depend by the transistor sizing and the used technology. Position of the pole allows to evaluate the reverse current reported in Table 1, while the substrate loss has been simulated.

Concluding, Fig. 12 compares the power conversion efficiencies of 4-stage DVMs only, in order to save space. However, almost the same results are found for the other topologies. Being the current losses different for the two multipliers, a difference in the power conversion curves is registered. As it can be observed, the higher are the current losses, the lesser are the maximum achievable output power and PCE.

V. CONCLUSION

In this paper an advanced model for the Dickson voltage multiplier which accounts for charge loss nonidealities is introduced. Theoretical analysis, simulations and measurement results have showed that current losses, until now categorized as second order nonidealities, can heavily affect DVM performances, like maximum output voltage, and make it intrinsically inefficient in terms of settling time and power conversion.

Relationships between each loss source and the main performance parameters are carried out. In particular, by inspection of the open-circuit output voltage it can be noticed that such currents limit the range of the suitable clock frequency suggesting the introduction of a further switching limit, namely deep-SSL.

APPENDIX
TECHNOLOGICAL CONSIDERATIONS

In the DVM, the voltage difference that pumping capacitors have to sustain increases with the number of stages. Hence, it is not negligible the choice of these devices. Silicon-based technologies provide different kind of capacitors: from the Meta-Oxide-Silicon (MOS) and Metal-Oxide-Metal (MOM) capacitors to those which requires optional manufacturing steps as the Poly-Poly (PP) and high-K Metal-Insulator-Metal (MIM) capacitors.

Typically, three main parameters, namely:
- the breakdown voltage (BV),
- the capacitance per unit of area, and
- the parasitic percentage

have to be accounted to select the kind of capacitors of a VMs.

Typically, more the component is far from the substrate, lower are the capacitive parasitic contributions. Indeed, the MOS capacitors, which are the nearest to the substrate, usually exhibit high parasitic capacitances.

Concerning the MOS capacitors, one of these parasitic contributions shows a non-linear behaviour, being a junction capacitance, making their use less interesting, especially for low input voltage applications [12]. However, when operating in accumulation region, the reduced thickness and the low resistivity of the oxide make this device a good solution for compact DVMs whose output voltages are limited to the MOS structure breakdown, like voltage doublers and triplers [22].

As another example, the MIM capacitors, which are the farthest from the substrate, exhibit low parasitic linear capacitances and high dielectric constant, which make them among the best choices for efficient DVMs. However, high-K materials (compound or elements whose relative dielectric constant is higher than that of the silicon dioxide) often exhibit heavy resistive losses, thus increasing power losses.

Moreover, the distance between the plates is set by technology constrains in almost all devices, which means to have a given breakdown voltage. To skip this limitation in applications requiring the generation of a voltage higher than the maximum voltage supply one, such as solid-state memories or piezoelectric actuation, two main solutions can be adopted. The pumping capacitors that must sustain a voltage higher than its own breakdown voltage (e.g., those closest to the output node) can be implemented by the series of two or more

capacitors, or by using MOM caps with opportunely spaced fingers. Unfortunately, in both cases an unavoidable increase of the silicon occupied area occurs.

The above reported considerations suggest the definition of the following three quality factors to assess the suitability of a capacitor type

$$\alpha_T = \frac{C_T}{C} \tag{A.1a}$$

$$\alpha_B = \frac{C_B}{C} \tag{A.1b}$$

$$\tau_C = CR_C = (\varepsilon_0 k_i)\,\rho_i \tag{A.1c}$$

Equations (A.1a) and (A.1b) are the ratio between top and bottom parasitic over the nominal pumping capacitance C, respectively. The first one has been already introduced in Section II. The third expression, which is equal to the product between the nominal capacitance and the parallel equivalent resistance, R_C, is an intrinsic time constant characterizing the pumping capacitor.

When the form factors of the capacitor are given, it is found that area and distance of the plates (thickness of the dielectric) coincide with the section and the length of R_C, respectively. This allows to obtain the right-most term in eq. (A.1c), which is a function of the vacuum permittivity ε_0, the relative dielectric constant, k_i, and the resistivity, ρ_i, of the insulator used as dielectric. It must be noted that all the introduced factors, α_T, α_B and τ_C, are technology dependent parameters.

Analogously, CTDs are implemented by using active devices, such as bipolar and/or unipolar transistors, whose more influent nonidealities are the threshold voltage, on-resistance, reverse current losses, parasitic capacitances, and current losses through the substrate. Being strictly related to the exploited switch topology, solutions to alleviate the effects of the first three contributions on the DVM performance can be widely found in literature [15]. Moreover, the charge losses due to currents toward the substrate are not often negligible when the DVM is designed to generate micro- and nano-currents or works as a voltage generator with the output node left open.

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