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RESEARCH ARTICLE

Evaluation and Perspective of Analog Low-Dropout Voltage Regulators: A Review

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ABSTRACT Low-dropout regulators (LDOs) are widely adopted in power management integrated circuits (PMICs) and serve as a bridge between the switching regulators and individual on-chip modules to provide a smooth, regulated output voltage. Compared to digital LDOs (DLDOs), analog LDOs (ALDOs) lead in the advantage of low output ripple and large power supply rejection (PSR). However, the preference of achieving high performance in terms of load transient, high PSR, good load and line regulation, while maintaining a low quiescent current and low dropout voltage for high efficiency, remains the key challenge in ALDO design. For operation with a low quiescent current, the bandwidth is reduced due to low transconductance, resulting in the limited gate driving capabilities in terms of charging and discharging the large gate capacitance of the pass or output transistor. In addition, the preference for system-on-chip design in the absence of large off-chip capacitors arises stability issues. In this paper, recent reported state-of-the-art architectures for ALDOs are revisited and reviewed. The performance of these ALDOs is compared and their applications are investigated.

INDEX TERMS Linear low-dropout regulators (LDOs), power management integrated circuits (PMICs), analog LDOs (ALDO), capacitor-less output, adaptive biasing, bulk modulation, power supply rejection (PSR), flipped voltage follower (FVF), charge pump.

I. INTRODUCTION

The industrial revolution known as Industry 4.0 has inspired the explosive growth of personal mobile and portable devices. The Internet of Things (IoT) and Internet of Everything (IoE) represent the core of Industry 4.0 [1], [2] and are crucial to cater to the growing demand for technologies based on mobile and portable devices, such as radio frequency identification (RFID) [3], smart factories equipped with advanced technologies, machine-to-machine (M2M) and machine-to-human (M2H) communication [4], along with IoT edge sensors [5]. As these applications of IoTs are now becoming mainstream, system-on-chip (SoC) modules are a viable option [6] due to the wide variety of such applications. SoCs consist of multiple individual blocks, with dedicated voltage, power and current requirements, as shown in Fig. 1, which illustrates the power management IC (PMIC) module for IoT applications [7]. The integration of these individual blocks into the SoC platform, as shown in Fig. 2, can reduce the need for bulky off-chip components such as discrete inductors and capacitors, while conforming to the increasing demand for power [8].

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The conversion efficiency of a PMIC becomes critical with limited battery life in IoT devices. For example, with massive deployment and distribution of IoT sensors, frequent battery replacement is challenging or near impossible, which is further complicated with the integration of limited capacity batteries for IoT miniaturization [5]. These challenges give rise to the need to design PMICs and LDOs for an SoC with low current consumption [5] and high conversion efficiency for extended battery life [7]. Furthermore, concerns over safety and pollution of the environment arise from the battery disposal process [2]. To address these issues, various energy-harvesting techniques have been developed, such as radio frequency (RF) [9], [10], [11], [12], [13], vibration [13], photovoltaic [13], [14], thermoelectric [15], and piezoelectric [16] methods. Compared to the other energy-harvesting techniques, RF energy harvesting (RFEH) has the key advantage of high reliability in the energy source (in far-field RFEH) and the small physical form factor of the transducer (antenna) [10]. With design techniques such as maximum power point tracking (MPPT) [16] and simultaneous wireless information and power transfer (SWIPT) [11], RFEH is becoming a viable solution as designers take advantage of mainstream short-range low-power (LP) communication methods such as WiFi or Bluetooth low-energy (BLE), which operates in the 2.45 GHz band, to design more compact and cheaper IoT sensors [12]. Depending on the power requirement of different IoT applications, IoT modules may be fully battery-less [1], [2], [3] or may use a combination of energy harvesting and energy storage, such as a supercapacitor or battery [16], which provides flexibility in terms of power supply options for IoT applications. Despite the milestone offered by energy harvesting solutions, fluctuations in the available energy for harvesting require the integration of a power management unit (PMU), which is crucial for providing a stable supply voltage to the modules in IoT sensors [2], [9], [12], [13], [14], [15], [16]. As shown in Figs. 1 to 3, the PMIC modules or PMUs in a typical SoC consist of switching power converters at the input, and the LDO which bridges the output of the switching converter to the individual blocks in the SoC to achieve low ripple in the supply voltage [17], [18].

The LDOs used in PMICs and PMUs can be categorized into DLDOs, ALDOs, and hybrid LDOs, which combine analog and digital LDOs within the control circuit. Compared to ALDOs, DLDOs can perform better under low-voltage conditions as they do not suffer in stability with incurred compensation issues and it is processed scalable [19]. However, the bottleneck due to power supply rejection (PSR) and output voltage ripple remains the key design challenge in DLDOs [18]. Furthermore, the requirement for a clock signal in DLDOs gives an additional challenge in terms of reducing the current consumption or the quiescent current of a DLDO and consequently limits efforts to improve its efficiency [19], [20]. ALDOs exhibit better performance in terms of voltage ripple and superior PSR compared to DLDOs [20], although continuous process scaling resulting in chip area downsizing and the reduction or elimination of external components present new design challenges for ALDOs [21]. ALDOs with large output capacitor has better load transient response compared to ALDOs without large off-chip capacitor, in which the output voltage droop is buffered by the large external capacitor [18]. Despite the advantage of good load transient response and PSR, the large output capacitor has to be integrated externally, as the capacitor consumes larger area for an on-chip integration [22] and even occupying relatively larger printed circuit board (PCB) area in the miniaturization of modern discrete circuits [23]. Thus, output-capacitorless LDOs (OCL-LDO) architectures are preferred for the minimum form factor and pin counts in

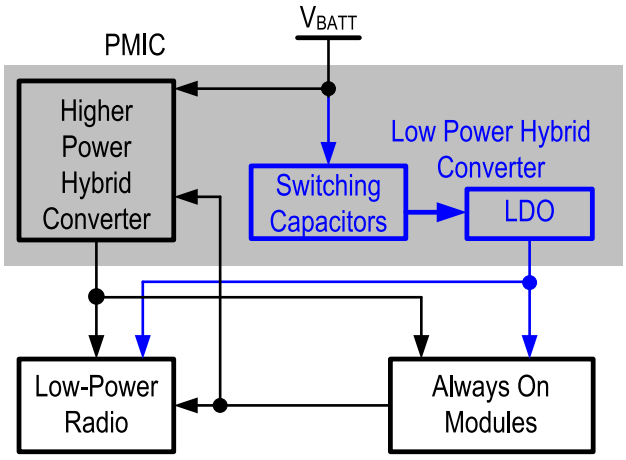

FIGURE 1. PMIC for IoT applications [7].

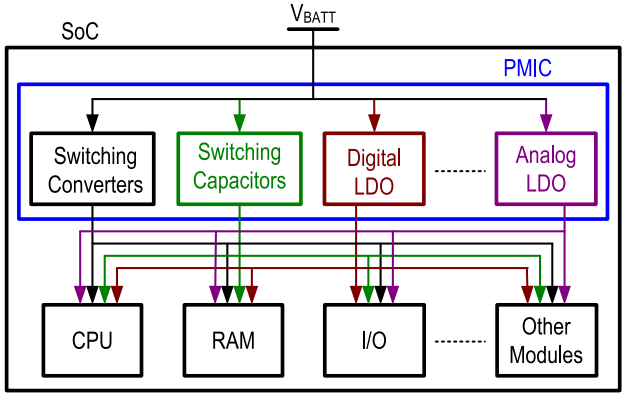

FIGURE 2. SoC solutions with integrated PMIC modules [8].

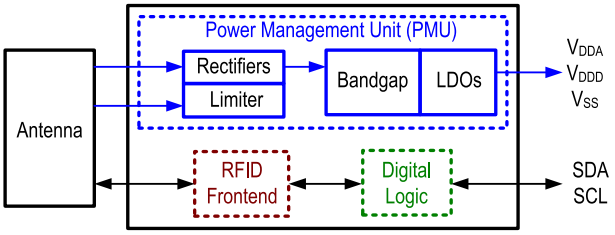

FIGURE 3. RFEH SoC solutions with integrated PMUs [3].

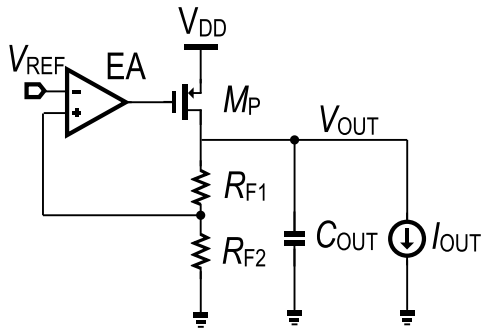

FIGURE 4. Basic architecture of the classic LDO.

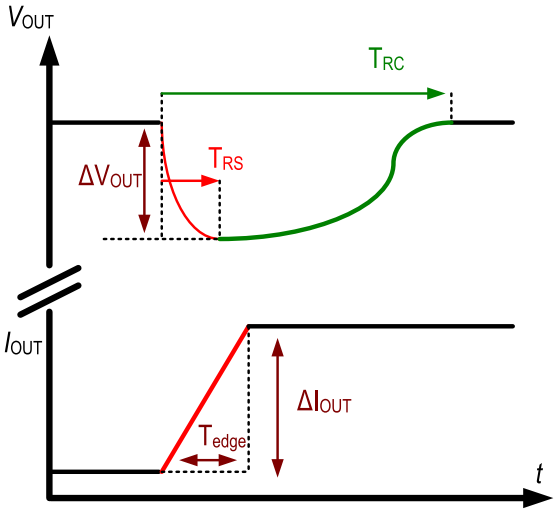

FIGURE 5. Output voltage of an LDO showing the output voltage droop, ΔV_{OUT}, response time, T_{Rs}, and recovery time T_{Rc}, during transient load.

the applications of IoT [1], [2], [3], [4], [5], [6], [7], [8], IoE [20] and RFID [3].

To address these design bottlenecks, innovative architectures and circuit design techniques for ALDOs have been proposed in recent years. Brief reviews were presented in [18] and [22], which addressed the recent advances in linear LDOs. However, more detailed comparison and benchmarking are needed to evaluate the performance of these state-of-the-art LDO architectures, in terms of the critical parameters and the design constraints. In this paper, circuit architectures and design techniques for LDOs are reviewed and discussed. The structure of this paper is as follows. The performance indicators used for the ALDOs and the respective design constraints based on the critical parameters are discussed in the subsequent section. In Section III, architecture and design technique for various state-of-the-art ALDOs are reviewed and discussed. Section IV presents a comparison of the performance in recent reported state-of-the-art ALDOs. In the last section, the conclusion and future directions for research on ALDOs are given.

II. PERFORMANCE INDICATORS FOR LDOs

The primary role of an LDO is to provide a regulated voltage with low ripple to the individual functional blocks in an SoC by filtering the residual ripples from the switching converters. The basic architecture of an LDO is shown in Fig. 4. It is defined based on an operational amplifier (opamp) which is configured as an error amplifier to control the pass transistor, M_P, in order to provide a regulated output voltage, V_{OUT}. The LDO must be able to provide a fast response time, T_{Rs}, and recovery time, T_{Rc}, against a load transient with an edge time, T_{edge}, as shown in Fig. 5 [22].

A. DROPOUT VOLTAGE AND EFFICIENCY

The voltage drop between the input and output of the LDO is known as the dropout voltage. The mathematical relation between the input voltage, V_{DD}, the output voltage, V_{OUT}, and the dropout voltage, V_{DO}, can be expressed as:

$$V_{DO} = V_{DD} - V_{OUT} \tag{1}$$

To reduce the power loss due to dropout voltage, V_{DO} must be kept small, and is typically in the range of 200 mV for state-of-the-art architectures [23], [24], [25]. There have also been reports of design innovations that have achieved smaller dropout voltages [26], [27], [28], [29], [30], [31], [32], [33], [34], with some reaching as low as 50 mV [35], [36]. A low dropout voltage is crucial in terms of increasing the power efficiency, η_{power}, of the LDO [19]:

$$\eta_{power} = \frac{I_{OUT}}{I_{OUT} + I_Q} \cdot \frac{V_{DD} - V_{DO}}{V_{DD}} = \frac{I_{OUT}}{I_{OUT} + I_Q} \cdot \frac{V_{OUT}}{V_{OUT} + V_{DO}} \tag{2}$$

where I_{OUT} is the output current delivered to the load and I_Q is the quiescent current consumed by the LDO control circuit. In addition to the power efficiency, an LDO is commonly benchmarked based on the parameter of current efficiency, $\eta_{current}$, which can be given as [19]:

$$\eta_{currnet} = \frac{I_{OUT}}{I_{OUT} + I_Q}. \tag{3}$$

B. FIGURE-OF-MERIT (FoM) ON LOAD TRANSIENT RESPONSE

Several versions of the figure-of-merit (FoM) have been defined in several prior works to benchmark the load transient performance of an LDO [36], [37], [38], [39], [40], [41], [42], [43], [44], [45], [46], [47], [48], [49], [50], [51], [52], [53], [54], [55], [56]. To evaluate the transient response of an LDO with respect to the change in the load current, two FoMs were proposed in [37]. The first of these is defined based on the response time, T_{Rs}, output capacitance, C_{OUT}, change in output voltage, ΔV_{OUT}, quiescent current, I_Q, and maximum load current, $I_{OUT(MAX)}$, as follows:

$$FoM_1 = T_{Rs} \cdot \frac{I_Q}{I_{OUT(MAX)}} = \frac{C_{OUT} \cdot \Delta V_{OUT} \cdot I_Q}{I^2_{OUT(MAX)}} \tag{4}$$

where T_{Rs} is defined as:

$$T_{Rs} = \frac{C_{OUT} \cdot \Delta V_{OUT}}{I_{OUT(MAX)}} \tag{5}$$

The second FoM addresses the issue of process dependency [37], as follows:

$$FoM_2 = \frac{FoM_1}{FO4} = \frac{C_{OUT} \cdot \Delta V_{OUT}}{FO4 \cdot I_{OUT(MAX)}} \cdot \frac{I_Q}{I_{OUT(MAX)}} \quad (6)$$

where $FO4$ is the estimated fan-out of four delays of the process [37].

FoM_1 and FoM_2 serve as performance indicators relating to the output capacitance, C_{OUT}, output voltage droop, ΔV_{OUT}, maximum output current, $I_{\mathrm{OUT(MAX)}}$, and quiescent current, I_{Q}. FoM_1 and FoM_2 have units of time, in ps, where a lower value indicates better performance, with a smaller output capacitance. FoM_1 and FoM_2 have been widely adopted for benchmarking in many state-of-the-art works [29], [30], [31], [32], [33], [34], [35]. Several authors have modified FoM_1 and FoM_2 for the purpose of benchmarking. In [38], the process scaling factor was included in FoM_1, and subsequently defined as FoM_3:

$$FoM_3 = \frac{C_{OUT} \cdot \Delta V_{OUT} \cdot I_Q}{\alpha \cdot I^2_{OUT(MAX)}} \quad (7)$$

where α represents the process scaling factor. Since the edge time of the load transient is not included in FoM_3, a design with a higher edge time can achieve a better FoM, as highlighted by the authors of [38]. The process scaling factor and active area, $area$, were introduced into FoM_1 by Bu et al. in [39], and the FoM was defined as:

$$FoM_4 = \frac{C_{OUT} \cdot \Delta V_{OUT} \cdot I_Q}{I^2_{OUT(MAX)}} \cdot area. \quad (8)$$

In FoM_4, a compact and small active area will result in a better FoM metric, which is achieved through the elimination of the area-hungry signal boosting circuit with a favorable improvement in the speed of the load response, as described in [39]. In FoM_1 to FoM_4, the minimum load current is not considered. However, in the design of an LDO, there is a minimum load requirement to maintain stability, as explained by Guo and Leung in [40]. In order to consider the minimum load current requirement, FoM_5 was proposed in [41] as follows:

$$FoM_5 = \frac{C_{OUT} \cdot \Delta V_{OUT} \cdot (I_Q + I_{OUT(MIN)})}{I^2_{OUT(MAX)}} \quad (9)$$

where $I_{OUT(MIN)}$ is the minimum load current of the implemented LDO. Another FoM that included the minimum load current requirement was proposed in [42] and later adopted by [35], as follows:

$$FoM_6 = \frac{C_{OUT} \cdot \Delta V_{OUT} \cdot I_Q}{(I_{OUT(MAX)} - I_{OUT(MIN)})^2} = \frac{C_{OUT} \cdot \Delta V_{OUT} \cdot I_Q}{\Delta I^2_{OUT}} \quad (10)$$

where ΔI_{OUT} is the change in the load current during the load transient.

Both the FoM_5 and FoM_6 benchmarks are similar to FoM_1 except that they include an additional factor representing the minimum load requirement, whereas an LDO design with a lower minimum load current will give a better overall performance metric. Concerning the current trend towards scaling down the supply voltage, the authors of [43] report that for the same maximum load current and a lower supply voltage, a larger pass transistor, M_{P}, is required, leading to a larger gate capacitance to be driven. To represent the gate capacitance penalty due to voltage scaling, the authors of [43] proposed FoM_7:

$$FoM_7 = \frac{C_{OUT} \cdot \Delta V_{OUT} \cdot I_Q}{\Delta I^2_{OUT}} \cdot (\frac{V_{DD}}{1V})^2. \quad (11)$$

A normalizing voltage of 1 V is included in FoM_7 to ensure that the units of FoM_7 are in time, in a similar unit of FoM_1 to FoM_6. However, since the gate capacitance of the pass transistor is inversely proportional to the square of the maximum overdrive in the pass transistor, scaling of the supply voltage in FoM_7 is inaccurate without considering the pass transistor's threshold voltage.

Unlike the response time, the settling time T_{Settle} (which is equivalent to the recovery time, T_{Rc}, as shown in Fig. 5) was considered in [44]:

$$FoM_8 = T_{Settle} \cdot \frac{I_Q}{I_{OUT(MAX)}}. \quad (12)$$

FoM_8 was proposed to evaluate the current efficiency (the ratio between the quiescent current, I_{Q}, and the maximum current, $I_{\mathrm{OUT(MAX)}}$) against the settling time for a load transient. FoM_8 assesses the time taken for the output voltage to settle rather than the response time of the LDO, as in FoM_1. In comparison to FoM_1, which measures the time for the LDO to respond to the load transient, FoM_8 measures the performance of the LDO based on the settling of the output voltage after a load transient.

These FoMs are used to evaluate the performance of an LDO based on the response or settling time against the quiescent current and the load current. However, in view to the current trend toward output-capacitor-less LDO (OCL-LDO) architectures, the work in [40] highlighted the dependency on the output capacitance in FoM_1 and FoM_2 where the performance metric is not suitable for use as performance indicators for an OCL-LDO. Instead, the edge time, T_{edge}, is a key parameter that affects the response speed of OCL-LDO, explicitly reported in [38]. Hence, the work in [40] proposed a modified FoM that included an edge time factor, K:

$$FoM_9 = K(\frac{\Delta V_{OUT} \cdot I_Q}{\Delta I_{OUT}}) \quad (13)$$

where K is defined as

$$K = \frac{T_{edge}\ used\ in\ the\ measurement}{the\ smallest\ T_{edge}\ among\ the\ design\ for\ comparison} \quad (14)$$

With the benchmarking defining different load transient edge time, FoM_9 is deemed more suitable than FoM_1 to FoM_8, and is widely adopted to compare the performance of LDOs when different edge times are involved. FoM_9 is further

optimized by factoring in the process technology dependency and minimum channel length, as described in [45] and [46]. As a result, the process scaling factor, α is included [45]:

$$FoM_{10} = K(\frac{\Delta V_{OUT} \cdot I_Q}{\alpha^2 \cdot \Delta I_{OUT}}). \quad (15)$$

The process scaling factor, α, is squared in the definition of FoM_{10} due to the dependency of the dominant pole in an OCL-LDO on the gate-to-drain capacitance, C_{gd}, of the pass transistor, M_P, which varies as $1/\alpha^2$ due to the Miller effect [45]. Alternately, the minimum channel length, L, was adopted in [46]:

$$FoM_{11} = K(\frac{\Delta V_{OUT} \cdot I_Q}{L^2 \cdot \Delta I_{OUT}}). \quad (16)$$

Similar to FoM_{10}, the term L is squared in FoM_{11}. The parasitic capacitance is proportional to the width and length, $(W \times L)$, with W being proportional to L when considering an identical aspect ratio of the transistor [46], [47], [48]. In addition, the process technology, *Tech*, the normalized area, *NA*, and the line regulation, *LRg*, are essential performance metrics for benchmarking LDOs. Hence, a new FoM was defined in [49] as:

$$FoM_{12} = \frac{FoM_9 \cdot LRg \cdot I_Q \cdot NA}{I_{OUT(MAX)}} \quad (17)$$

where *NA* is defined as:

$$NA = \frac{area}{Tech^2} \quad (18)$$

A lower value of FoM_{12} indicates that the LDO exhibits favorable characteristics such as a fast load transient, high line regulation, small area, large maximum load current, and low quiescent current consumption [49].

In addition to the edge time in FoM_9, the recovery time, T_{Rc}, is also a key parameter in evaluating the performance of an OCL-LDO. The authors of [50] claimed that an FoM that considers the response time is not sufficient for evaluating the performance and proposed a modified FoM that includes the recovery time factor, R_{Rc}, leading to the following definition:

$$FoM_{13} = R_{Rc} \cdot K(\frac{\Delta V_{OUT} \cdot I_Q}{\Delta I_{OUT}}) \quad (19)$$

where R_{Rc} is given as:

$$R_{Rc} = \frac{T_{Rc}\ used\ in\ the\ measurement}{the\ smallest\ T_{Rc}\ among\ the\ design\ for\ comparison} \quad (20)$$

With the recovery time embedded in FoM_{13}, the response of an LDO respective to the recovered output voltage against the load transient can be measured using FoM_{13}. The minimum load current is not considered in FoM_8 to FoM_{13}, despite the performance parameter proofed to be crucial in defining the stability [40]. The introduction of adaptively biased LDO designs [44], [48] suggest that the quiescent current of the LDO could be adjusted by the biasing circuit to cater to a wide range of load currents. Thus, the quiescent current can vary from a minimum of $I_{Q(MIN)}$ for low load current to a maximum of $I_{Q(MAX)}$ for the maximum load current. FoM_8 was adjusted to consider the factors of minimum load current requirement and varying quiescent current in [51], as follows:

$$FoM_{14} = K \cdot \frac{\Delta V_{OUT} \cdot (I_{Q(MIN)} + I_{OUT(MIN)})}{\Delta I_{OUT}} \quad (21)$$

and

$$FoM_{15} = K \cdot \frac{\Delta V_{OUT} \cdot I_{Q(MAX)}}{\Delta I_{OUT}} \quad (22)$$

FoM_{14} assesses the performance of the LDO at minimum load current and minimum quiescent current, whereas FoM_{15} benchmarks the performance of the LDO at maximum load current and maximum quiescent current.

Attempts to combine the benefits of the FoM proposed by Hazucha et al. [37] and Guo and Leung [40] have been made in several research works [52], [53]. In [52], the authors proposed an FoM which establishes a sub-linear relationship between ΔV_{out} and K while dependent on a process-dependent factor, *FO4*, as in FoM_2, to obtain a process-normalized FoM:

$$FOM_{16} = K^{1/3} \cdot \frac{\Delta V_{OUT} \cdot (I_Q + I_{L(MIN)})}{FO4 \cdot \Delta I_{OUT}} \quad (23)$$

FoM_{16} includes the edge time ratio, as in FoM_9, while normalizing the process-dependent factor, as in FoM_2. The parameter *FO4* is an estimated value [37] and may not give an accurate benchmarking compared to FoMs that consider the process dependency via the process scaling factor, α, or the minimum channel length, L. In contrast to the FoM proposed in [52], the authors of [53] proposed a modified FoM that combines the expressions given in [37] and [40]:

$$FoM_{17} = K \cdot \frac{C_{OUT} \cdot \Delta V_{OUT} \cdot I_{Q(MIN)}}{\alpha \cdot \Delta I_{OUT}^2} \quad (24)$$

FoM_{17} includes the edge time ratio, K, and the ratio of the technology dependency parameter, α, to evaluate the performance of the LDO.

In [54], the authors proposed an FoM that benchmarks the performance based on the active chip area of the LDO, the load transient ripple, which is equivalent to the change in the output voltage, ΔV_{OUT}, and the value of the output decoupling capacitor, C_{OUT}:

$$FoM_{18} = \frac{area \cdot \Delta V_{OUT}}{C_{OUT}}. \quad (25)$$

FoM_{18} does not evaluate the performance of the LDO based on the load current and quiescent current, and hence, the current efficiency is not considered in this measure. OCL-LDOs are particularly suitable for integration into SoC designs due to the absence of a bulky output capacitor, which enables on-chip integration of the LDO with the functional blocks [55]. As reported in [40], in additional to the output capacitance, the edge time, T_{edge}, is a key parameter that affects the response speed of an OCL-LDO, as reported in [38]. Hence, FoM_9 to FoM_{15}, which considers the edge time, is more suitable for evaluating the load transient performance

of an OCL-LDO. Due to the nature of the estimated value $FO4$, FoM_2 and FoM_{16} are less accurate when normalized with a process factor compared to FoM_{10}, FoM_{11} and FoM_{12}. However, FoM_1 to FoM_{18} neglects the dropout voltage, which is crucial in order to define the power efficiency of the LDO, as described in (1) and (2). To evaluate the load transient performance of an LDO with the dropout voltage, two FoMs are proposed that consider the minimum load and quiescent current:

$$FoM_{19} = T_{Rc} \cdot K \cdot \frac{\Delta V_{OUT} \cdot (I_Q + I_{OUT(MIN)}) \cdot V_{DO}}{\Delta I_{OUT} \cdot (1V)^2} \quad (26)$$

and evaluates the performance with active area:

$$FoM_{20} = T_{Rc} \cdot K \cdot \frac{\Delta V_{OUT} \cdot I_Q \cdot V_{DO}}{\Delta I_{OUT} \cdot (1V)^2} \cdot \frac{area}{Tech^2}. \quad (27)$$

The normalization factor $(1\text{V})^2$ is included in FoM_{19} and FoM_{20} to enable the result to be presented in the dimensions of unit time. The mathematical definition of FoM_{19} includes the dropout voltage, and this metric evaluates the load transient response against the power efficiency of the OCL-LDO, whereas FoM_{20} evaluates the load transient response against the power efficiency and active area. With an SoC solution, the power efficiency for each built-in circuit module should be high, to reduce the overall power loss and concurrently minimize the temperature rise during operation.

As there is no industry-standard FoM, the appropriate choice depends on the application of the LDO [52]. For an example, the differential circuits used in the error amplifier of the ALDO can reject small supply variations at low and moderate frequency. As the settling error of LDOs are usually due to insufficient phase margin or large Q of the loop response, the ripples that gradually settle are inherently low-frequency, typically around the loop gain bandwidth (GBW) of the LDO, which is often not high. In contrary, the voltage droop can be large and has high-frequency components and may not be rejected by the differential circuits. In this case, the settling time is not less harmful and critical than the response time. In the application of high-density SoC, which is crucial for IoE, IoT and RFID, a better slewing performance is preferred [44], where the settling time becomes the key factor since OCL-LDO is preferred [50] for reduced pin count, smaller form factor and footprint [22].

FoM_1 and the variations derived from FoM_1 have been widely adopted for benchmarking in many state-of-the-art works [29], [30], [31], [32], [33], [34], [35], [36], [37], [38], [39] as the response time is an approximate perfect reflection for the combination of large- and small-signal performance, where the GBW in the FoM for single-stage differential circuit can be directly measured. The recovery time, however, is more complicated. It may cover more metrics, such as phase margin or Q, but it also makes the other terms in the FoM difficult to tradeoff, while maintaining the same performance. Although the scalability of FoM_{19} may not be as good as FoM_1, in the application of high-density SoC, where OCL-LDO is preferred, the settling/recovery time becomes the key factor [50].

The best types of FoMs are those with linear or nearly linear relationships between the parameters and avoids duplication of the same effect. For an example, for the case of FoM_1, a linear relationship exists between T_{Rs}, I_{Q}, and I_{out}. Besides that, the output capacitance, C_{OUT} and the output voltage droop, ΔV_{OUT}, are inversely proportional. Where C_{OUT} and ΔV_{OUT} scales linearly and a smaller FoM reflects a shorter response time, leading to a better design. With the same design, one can easily trade, for instance, C_{OUT} for smaller ΔV_{OUT} without affecting the FoM. Hence, FoM_1 is fundamentally about the response time, T_{Rs}, quiescent current, and load current change. The expanded form of FoM_1 containing the term C_{OUT} is due to replacing T_{Rs} with an analytical expression from Equation (5). However, when evaluating the performance for OCL-LDO using FoM_1, the response time needs to be measured in the time domain directly rather than using the derivation of ΔV_{OUT} as shown in Equation (5). Besides that, when using the expression in Equation (5) for calculation, the edge time, T_{Edge} must be much smaller than the response time, which is sometimes difficult to do as explained in [40]. Indeed, [40] also found that ΔV_{OUT} will differ with different edge time, which is difficult to establish a linear relationship. For the case of FoM_{12}, the line regulation does not scale linearly with other parameters. Similarly, FoM_{18} is not a particularly good FoM, in which does not evaluate the performance of the LDO based on the load current and quiescent current. Although the edge time (or equivalently, K) does not scale linearly with either the T_{Rc} or T_{Rs}, the edge time is a key parameter in affecting the performance for OCL-LDO [38]. Whilst In high-density SoC, a better slew performance is preferrable [44], where T_{Rc} is another key factor [50]. Hence, to evaluate OCL-LDO in the application for high-density SoC, the parameters T_{edge} and T_{Rc} should be accounted in evaluating the performance of the architecture.

For LDO architectures using external capacitor, FoM_1 and the variations derived are suitable in evaluating the performance as the response time is reflecting the combination of large- and small-signal performance. Whilst for OCL-LDO, which is becoming the trend in application for SoC in IoE, IoT and RFID, the dependency of the output capacitance of FoM_1 and the variations derived are less suitable for use as performance indicators [40]. Instead, the edge time, T_{edge}, becomes the key parameter in affecting the performance [38]. Besides that, an improved slewing performance is preferred in high-density SoC [44], where T_{Rc} is another key factor [50]. Hence, to evaluate OCL-LDO in the application for high-density SoC for IoE, IoT and RFID, the parameters T_{edge} and T_{Rc} should be incorporated in evaluating the performance of the architecture.

The parameters incorporated into evaluating the performance of the LDO architectures and topologies by using the FoMs discussed reflect the design constraints. These parameters are interrelated, which will be covered in the subsection discussing the design constraints for LDO.

C. NOISE AND POWER SUPPLY REJECTION

In addition to the load transient response, the power supply rejection (PSR) is another key performance indicator for an LDO, as it measures the amount of ripple and noise from the supply voltage, V_{DD}, which can be suppressed by the LDO upon reaching the output terminal [55]. The primary noise contributors in LDOs are the voltage reference noise and supply noise [24]. The noise from the reference circuit can be reduced by implementing a low noise reference circuit, or by connecting a low pass filter between the output of the reference circuit and the input of the error amplifier integrated in the LDO [55].

The C_{OUT}, as in the case of LDO with external output capacitor, functions as a buffer for load transient, and attenuates the power supply noise and ripples through a bypass path from output node, V_{OUT}, to the ground for supply ripples at a frequency above the GBW of the LDO [27]. However, for OCL-LDO with a much smaller C_{OUT}, the PSR depends on the GBW of the LDO, which is a design challenge for OCL-LDO [24]. This is due to the GBW and the loop gain of the LDO is dependent on the quiescent current, I_{Q}, which determines the transconductance of the pass transistor, $g_{\mathrm{m,MP}}$ which in turn determines the open loop gain, $A_{\mathrm{v(loop)}}$ and the GBW of the LDO [40]. The design constraints of the parameters will be discussed in the following sub-section.

With regard to the relationship between $g_{\mathrm{m,MP}}$, $A_{\mathrm{v(loop)}}$ and the DC to low-frequency PSR for a typical LDO, PSR_{DC}, can be expressed as [55]:

$$PSR_{dc} = \frac{v_{out}}{v_{DD}} = \frac{(g_{m,MP} + g_{bs,MP}) \cdot R_{OUT}}{1 + A_{v(loop)}} \tag{28}$$

where v_{DD} and v_{out} are the AC ripple of the supply voltage and the resulting output voltage ripple, respectively. $g_{\mathrm{bs,MP}}$ represents the bulk transconductance of the pass transistor, M_{P}. R_{OUT} denotes the resistance of the load. In benchmarking with the PSR, the authors of [56] proposed:

$$FoM_{21} = \cdot \frac{T_{Settle} \cdot I_Q}{PSR \cdot I_{MAX}}. \tag{29}$$

FoM_{21} evaluates the performance of the LDO respective to the settling time, current efficiency, and the PSR. However, due to the inherent parasitic capacitance of the circuit, the PSR is frequency-dependent. To evaluate the performance in terms of the PSR bandwidth of the LDO, the FoM is further modified to:

$$FoM_{22} = \cdot \frac{T_{Settle} \cdot I_Q}{BW_{PSR} \cdot PSR \cdot I_{MAX}} \tag{30}$$

where BW_{PSR} represents the gain bandwidth of the LDO on a logarithmic scale measured from DC. The proposed FoM_{22} evaluates the performance of the LDO architecture by considering the PSR and the gain bandwidth of the LDO. Due the fluctuations in the available energy for harvesting, providing a stable supply voltage to the modules such as precision analog-to-digital converters (ADC) and voltage-controlled oscillators (VCO) in IoT devices [2], OCL-LDOs in these applications require fast settling time (T_{Settle} or T_{Rc}) while still achieving high PSR and low noise [56]. Thus, the FoM such as FoM_{21} and FoM_{22} are employed in evaluating the performance in terms of PSR, T_{Settle} or T_{Rc}, and quiescent current, I_{Q}, in power efficient noise-sensitive applications.

The FoMs reviewed will be used to benchmark the performance of the state-of-the-art LDO architectures.

D. DESIGN CONSTRAINTS ON ALDOs

Over the years, various architectures have been proposed to address the critical parameters for ALDOs [36], [37], [38], [39], [40], [41], [42], [43], [44], [45], [46], [47], [48], [49], [50], [51], [52], [53], [54], [55], [56], [57], [58], [59], [60], [61], [62], [63], [64], [65], [66], [67], [68], [69], [70], [71], [72], [73], [74], [75], [76], [77], [78], [79], [80], [81], [82], [83], [84], [85], [86], [87], [88], [89]. These parameters such as the dropout voltage, line regulation, load regulation, quiescent current, load transient response, settling/recovery time, and PSR are interrelated, and the trade-offs need to be considered in designing an ALDO. The design constraints on these parameters are summarised in Fig. 6. For much of the operation time, IoT devices are in standby mode, and are only active for a short period in which low current and power consumption operation are highly desirable [25], [32].

On the other hand, to achieve good dynamic output voltage regulation, the recovery time of the load transient is a critical factor affecting the performance of an LDO. This parameter measures how fast the output voltage recovers to a steady state [55], as shown in Fig. 5. The bandwidth of the LDO and the slew rate of the gate driving capability to the pass transistor is crucial in achieving fast recovery and response time for the LDO [30], [67], [79]. However, to achieve high bandwidth and improved slew rate, the increase in power consumption becomes the crucial design trade-off [67], [86]. In addition, decreasing the quiescent current increases the impedance of the internal nodes, and reduces the transconductance of the pass transistor, leading to a lower pole frequency and degrading the phase margin, which affects the loop stability of the LDO [32], [88]. A large loop gain and high transconductance of the pass transistor are required to improve steady-state or DC load regulation, reflecting that a higher quiescent current is needed [25]. Hence, a large quiescent current is required to achieve a fast load transient response and good stability [30]. In this view, the trade-off between low power consumption and good steady-state and dynamic (load transient response) load regulation remains a design challenge, which has led to the development of multiple biasing and compensation technique [53], [67], [70] as discussed in the previous section.

Another constraint in the design of an ALDO the design tradeoff of achieving low power consumption/high power efficiency and the sizing of the pass transistor, $(W/L)_{\mathrm{MP}}$, which leads to area efficiency. Respective to (2) and (3), in addition in reducing the quiescent current, I_{Q}, the dropout voltage, V_{DO}, can also be reduced to achieve high power efficiency, which minimizes the power loss due to the pass transistor. The work in [26] shows that to achieve a low V_{DO}, the width of the pass transistor needs to be increased;

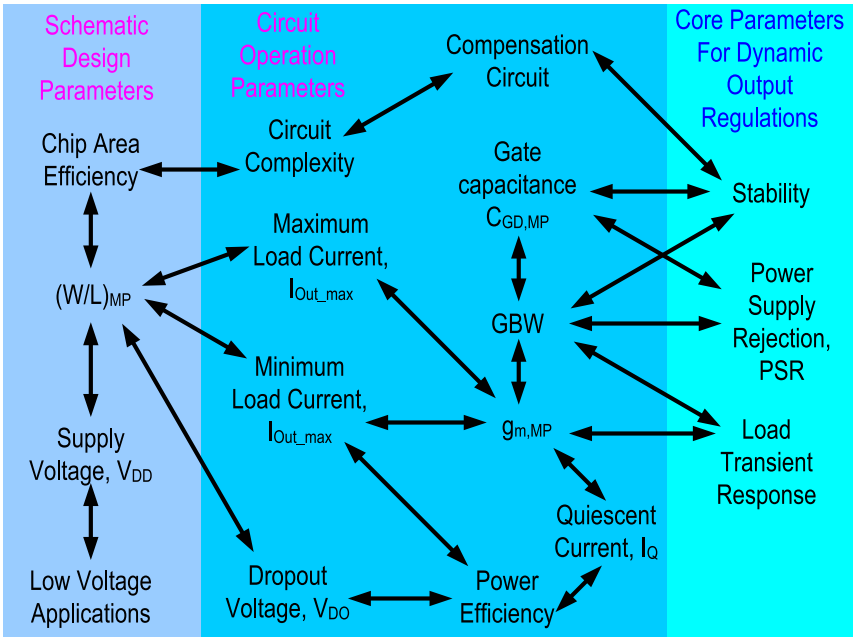

FIGURE 6. Design constraints on the ALDO variants.

however, this will increase the gate capacitance of the pass transistor, leading to the need for a larger gate driving capability from the error amplifier to achieve the desired slew rate. The limitation of increasing the gate width of the pass transistor were discussed in detail in [86], and it is observed that a larger width will decrease the bandwidth, which constrains the output voltage droop in the load transient response. In addition, a larger gate capacitance introduces stability issues and complicates the design of the compensation circuit. Hence, when finalising the gate width of the pass transistor, factors such as the load current capacity, the output voltage droop in the load transient response, the desired dropout voltage, and stability issue should be considered.

This design tradeoff between the quiescent current and other parameters such as the output voltage droop, response time and recovery time are reflected in the FoMs discussed, except for FoM_{18}. With a lower quiescent current, achieving comparable performance in terms of the output voltage droop, response time and recovery time gives a lower value of FoM, in the unit of time (*ps*), indicating better performance in terms of current efficiency [40]. On the other hand, with a similar quiescent current and edge time, achieving a lower value of FoM such as FoM_9 and FoM_{19}, verify the OCL-LDO performs better in terms of response time and recovery time.

Due to the absence of an external output capacitor, the dominant pole of the OCL-LDO is present at the gate-to-drain capacitance, C_{gd}, of the pass transistor, M_P, creating a hump in the PSR frequency response [27], [81]. Hence, besides the sizing of the pass transistor gate, the bandwidth of the ALDO should be high, which pushes the PSR hump to a higher frequency, with the trade-off of reduced loop gain for a wide range of load current [27].

The impact of reducing the dropout voltage, V_{DO} to the loop gain and bandwidth of the LDO can be deduced, by investigating the gain of the pass transistor, A_{MP}, which can be expressed as [36]:

$$A_{MP} = g_{m,MP} \cdot R_{OUT}. \tag{31}$$

At full load current, the pass transistor is pushed into the linear region [26], in which the gain of the pass transistor becomes [36]:

$$A_{MP} = \frac{V_{DS}}{V_{GS} - V_{TH}} = \frac{V_{DO}}{V_{GS} - V_{TH}} \tag{32}$$

where V_{GS} and V_{TH} are the gate to source voltage and threshold voltage of the pass transistor, respectively, while $V_{GS}-V_{TH}$ represents the gate overdrive voltage, and the drain to source voltage, V_{GS} equals to the dropout voltage, V_{DO}. From Equation (32), to achieve a higher efficiency according to Equation (2) by reducing the dropout voltage, can potentially reducing the gain provided by the pass transistor, which in turn reducing the overall loop gain of the LDO, $A_{v(loop)}$. The reduced loop gain will impact the performance in line regulation and load regulation based on the findings in [55].

Besides the gain of the pass transistor, the gain of the error amplifier, A_{EA} also contributes to the overall loop gain of the LDO, $A_{v(loop)}$ which can be observed in Fig. 4:

$$A_{v(loop)} = A_{EA} \cdot A_{MP}. \tag{33}$$

The gain, A_{EA} is affected by the quiescent current, I_Q [23], where a low I_Q results in low value of A_{EA} and reducing the

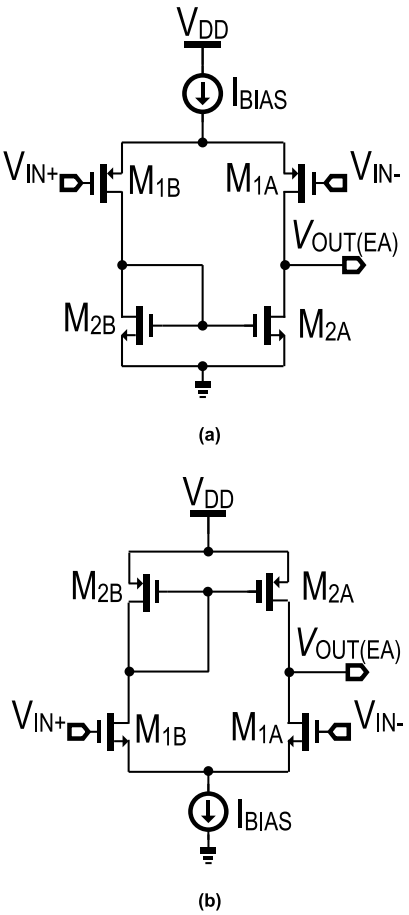

FIGURE 7. Basic configuartion of a differential amplifier (a) PMOS differential pair and (b) NMOS differential pair [55].

loop gain. As illustrated in Fig. 7, the biasing current of the differential amplifier, I_{BIAS} is part of the I_Q. However, with a lower loop gain, line regulation and load regulation will be impacted [55]. Apart from a lower loop gain, a lower I_Q of the error amplifier also reduces the gate driving capability of the error amplifier, which reduces the slew rate at the gate of the pass transistor.

Hence, a lower I_Q degrades the load transient response [47], leading to a slow response time and settling/recovery time [55]. Besides that, the PSR depends on the loop gain and GBW of the LDO for OCL-LDO, which is also affected by I_Q [40]. The configuration of the differential amplifier also plays an important role in the PSR performance. Respective to the findings in [55], with the same loop gain, $A_{v(loop)}$, the configuration in Fig. 7 (b) provides a better PSR at low frequency compared to the configuration in Fig. 7 (a).

III. STATE-OF-THE-ART ALDO TOPOLOGIES

With the development of SoC modules, LDOs are being integrated with single-chip solutions to achieve on-chip power management. Compared to a DLDO, an ALDO offers fast load transient response, high PSR, and large bandwidth with low quiescent current [17]; it also alleviates the need for a clock signal, which is important as the issue of clock glitch presents additional design challenges [17]. When integrating an LDO into an SoC module, an OCL-LDO architecture is preferred, as the need for a bulky external capacitor is removed; this reduces the pin counts of the chip and eliminates the inherent parasitic related to the external capacitor, which can adversely impact the performance at high frequency [22]. Over the years, various ALDO architectures have been proposed, in particular for OCL-LDOs. The following section reviews these state-of-the-art ALDO topologies.

A. FLIPPED VOLTAGE FOLLOWER ALDOs

Flipped voltage follower (FVF) ALDOs have been adopted in several works and have the considerable advantage of maintaining stability in the absence of output capacitors, as in the architecture of OCL-LDOs [40]. Some of the earlier FVF ALDOs was proposed in [37] and [40], based on the structure shown in Fig. 8 [57]. However, the folded circuit topology decreases the loop gain of the FVF LDO, resulting in a degraded load regulation, which is predicted to worsen in nano-scale technology implementations [40]. In addition, there is a minimum load requirement for the FVF LDO in order to sustain stability [59] and to alleviate the degradation due to the overdrive voltage requirement for the pass transistor, M_P, which could potentially drive the control transistor M_1 into the triode region [58], [59]. Despite the shortcomings highlighted above, the advantage of loop stability has encouraged other reported works to propose and refine FVF architectures. Among the circuit techniques that have been developed are mirrored control [60], [61], [62], adaptive and dynamic biasing [34], [63], adaptive and dynamic compensation [23], [25], super source follower (SSF) buffers [24], [30], [36], [64], and Class D with multi-level pulse width modulation (MLPWM) gate control [31]. These techniques aim to provide the necessary fast response to the load current transient improving load regulation while maintaining high current efficiency.

Fig. 9 shows the basic structure of the FVF-based LDO adopting a mirrored control transistor, where the gate-to-source voltage of the mirror transistor, M_{Mir}, is mirrored to the control transistor, M_1, which regulates the output voltage at the source of M_1. The signal paths are divided into slow and fast loops, as shown in Fig. 9. The slow loop, which is located between the error amplifier and the mirrored transistor, provides the necessary voltage gain to control the steady-state output voltage, while the fast loop, located within the FVF structure, provides control over the load transient response [23]. In [61] and [62], both the mirror voltage, V_{Mir}, and the output voltage, V_{OUT}, are fed back to the error amplifier. In these feedback loops, the aspect ratio of the input transistors is carefully selected so that V_{Mir} and V_{OUT}, are fed back according to a preset ratio [62]. However, due to PVT and load variation, the inherent mismatch between V_{Mir} and V_{OUT} is inevitable. The aspect ratio is selected such that V_{OUT}

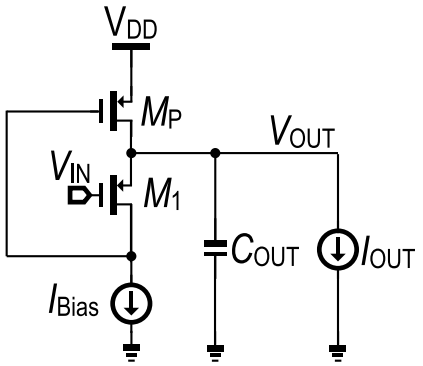

FIGURE 8. Basic architecture of an FVF structure [57].

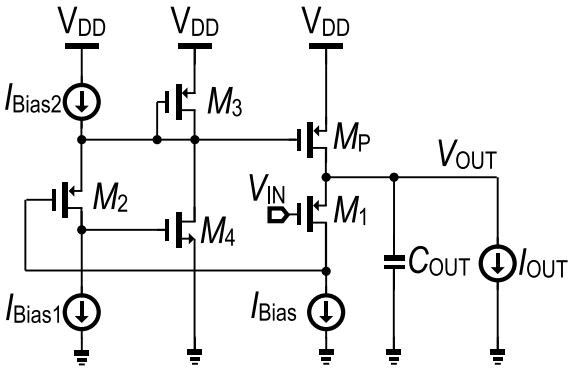

FIGURE 10. FVF LDO with super source follower [64].

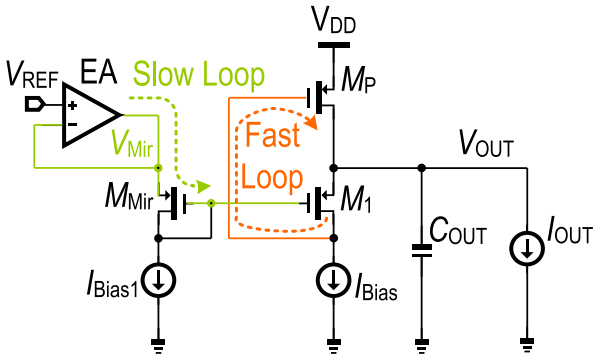

FIGURE 9. FVF LDO with mirror control [23].

is closer to the reference voltage, V_{Ref}, rather than the mirror voltage V_{Mir} [61]. Thus, careful selection of the aspect ratio is essential to prevent the output voltage from deviating from the reference voltage.

In [34], the proposed LDO features a dynamic biasing technique known as a signal- and transient-current boosting (STCB) to improve the load transient response. The signal path between the control transistor and the pass transistor is cascaded with a string of diode-connected transistors to reduce the impedance throughout the signal path. The proposed architecture can maintain a good PSR from DC up to 1 MHz, with undershoot and overshoot at the output voltage of approximately 30 mV during load transient. However, the requirement for an output capacitor of 1 μF with an equivalent series resistance (ESR) of 0.6 Ω to maintain stability reflects that the technique is unsuitable for OCL-LDO applications.

An alternate adaptive biasing method is proposed in [25], in which a bias shaper block is adopted that limits the biasing current at high loads while maintaining linear dependency on the output current at moderate loads. Zero tracking and bulk modulation are included to improve load and line regulation [43], and this enables the proposed FVF LDO to operate at an input voltage of 0.8 V while consuming a quiescent current of only 16 nA and maintaining good PSR from DC up to 100 kHz with an output voltage undershoot of 70 mV along with a load transient of 10 mA. Although the reported findings are suitable for battery-powered IoT devices, the requirement for an output capacitor of 1 μF makes it an unlikely fit for OCL-LDO in SoC applications, as in [34]. Another approach of dynamic biasing is proposed in [63], where this scheme is based on a string of inverter gates. The input to the inverter gate detects the voltage drop of the pass transistor gate when driving a large load current, which then pulls down the gate voltage further to allow the gate transistor to conduct more current, consequently reducing the load transient response time from 80 to 0.1 μs.

Rather than monitoring the gate voltage of the pass transistor as in [63], a string of inverter gates is used to monitor the output voltage in [25]. In this work, the gate voltage is concurrently tracked through another transistor, where the gate and source terminals are configured in parallel with the pass transistor and work in tandem to increase the dynamic response to the load transient.

Due to the need of a large dimension for the pass transistorto accommodate the load current capacity, the gate capacitance observed at the pass transistor is also large [65], which decreases the slew rate and bandwidth [66]. To increase the gate driving capability, an SSF is used as a buffer to drive the gate of the pass transistor in SSF-FVF architectures. The basic architecture of an SSF-FVF LDO is shown in Fig. 10, in which the SSF introduces a local shunt feedback unit to reduce the output impedance [64] and improve the gate driving capability. In [24], circuitry for damping factor control and a feedforward capacitor were included to extend the range of the load current and load capacitance, enabling the proposed FVF-LDO in [24] to operate with a load capacitance ranging from 0 to 2 nF. In addition, slew rate enhancement circuitry is included to provide additional gate current driving capability to the pass transistor; this improves the load transient response, allowing the scheme to achieve an output voltage undershoot and overshoot of 80 mV and 77 mV, respectively, with load current stepping from 0.1 mA to 50 mA and an edge time of 2 ns. The measured values of the PSR are identical for output capacitances of 0 nF and 2 nF at frequencies below 1 MHz, where the bandwidth of the error amplifier

in the slow loop plays a crucial role in the PSR performance. The feedforward capacitor is integrated between the source and drain of the control transistor in [24], whereas in [30], the feedforward capacitor is connected to the feedback network in parallel with the feedback resistor R_{F1}. In addition, a 1 pF on-chip capacitor is integrated at the output of the error amplifier, which establishes a dominant pole in improving the stability. To enhance the response to the load transient, an inverter-based overshoot detection circuit is integrated to reduce the overshoot of the output voltage when the load current is stepped down from 20 mA to 0.1 mA. In [36], a self-powered differential output error amplifier is employed, which is sustained by the filtered output voltage of the LDO. The differential output of the error amplifier provides both the control voltage and transient enhancement for the SSF-FVF output stage. The self-powered error amplifier consumes a minimum output current from the LDO. Due to low supply voltage headroom, the gain boosting technique is employed in the SSF-FVF LDO architecture proposed in [36].

An SSF-FVF LDO is combined with a mirrored control circuit in [64] to address the problems with the use of a folded cascade input stage to drive the capacitive load. However, the feedback signal is taken at the mirrored node, V_{Mir}, instead of the output node, V_{OUT}, resulting in the output voltage being unaligned in a direct feedback loop. As a design trade-off for pushing the internal pole frequency to be much higher than the unity gain frequency (UGF), the quiescent current consumed by the LDO is observed to be 100 μA, which is higher than other state-of-the-art architectures. To enhance the performance, the mirrored control, SSF and dynamic compensation technique are combined in [23], and a UGB of above 400 MHz is achieved with a good PSR from DC up to 1 MHz while maintaining a minimum quiescent current at 27 μA.

In contrast to the control methods described above, Class D MLPWM gate driving is employed in [31] to drive the FVF-LDO. To control the gate of the pass transistor, a feedforward transition-detection path (FFTDP) is incorporated to enhance the switching at high loads, from 0 to 300 mA. The class D control method provides a fast response, small overshoot and ripples at the output voltage while measuring a dropout voltage of 50 mV. However, the technique is less favorable for SoC integration due to the requirement for an output capacitor of 1 μF and is worsened by a quiescent current consumption of 300 μA, which is higher than for other reported state-of-the-art FVF-LDO architectures.

B. ALDOs WITH CHARGE PUMP

In the circuit architecture of an ALDO using an NMOS as the pass transistor, the gate capacitance of the NMOS is much smaller compared to the PMOS; this results in a wide UGB, which improves the load transient response and PSR [3]. In addition, good loop stability is achieved due to the low output resistance in the source follower configuration of the NMOS pass transistor [48]. However, a high dropout voltage is observed, as the gate overdrive of the NMOS transistor needs to overcome the threshold voltage. To address the problem of high dropout voltage, charge-pump-based NMOS ALDO architectures are proposed in [47], [48], [67], [68], and [69]. The basic architecture of a charge-pump-based NMOS ALDO is shown in Fig. 11, in which the charge pump provides a high gate drive to the NMOS-based pass transistor to overcome the threshold voltage, thus reducing the dropout voltage. The ALDOs proposed in [47] and [48] share similar architectures, differing only with a dynamic biasing scheme is adopted in [47] and an adaptive biasing scheme in [48]. With a low output impedance of an NMOS, the ALDOs in [47] and [48] achieves a settling time of 20 ns, measured through an output capacitance of up to 50 pF. However, the quiescent current of 130 μA is still higher than for other reported state-of-the-art architectures. In [67], the gate voltage of the pass transistor is mirrored to another transistor that supplies the reference current for the biasing circuit, and a hybrid mixture of dynamic and adaptive biasing schemes is adopted. The mirrored transistor also provides the reference signal to the clock signal generator to drive the charge pump. Furthermore, the biasing circuit drives a dynamic pull-down circuit, which reduces the overshoot at the output voltage during load transient. With the hybrid biasing technique, the

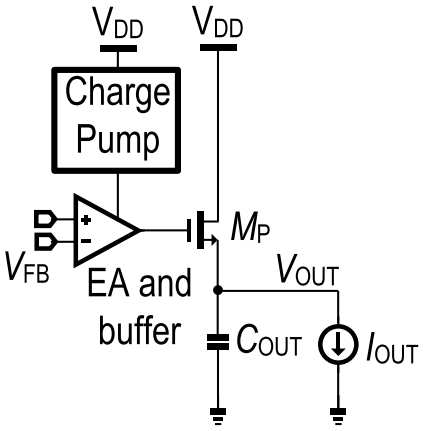

FIGURE 11. Basic architecture of a charge-pump-based LDO with NMOS pass transistor.

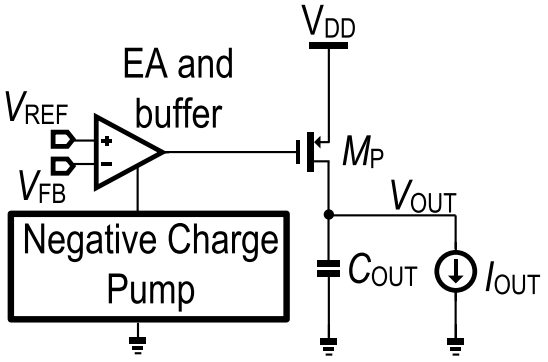

FIGURE 12. Basic architecture of a negative charge-pump-based LDO with PMOS pass transistor.

proposed ALDO gives an output voltage of 1 V with an undershoot of 135 mV at a load current step of 150 mA, while maintaining a minimum quiescent current of 1.24 μA. However, the requirement of a load capacitor between 1 μF and 47 μF results in the ALDO being less attractive as an SoC solution. To emulate higher capacitance in the range of nF at the output node, a high-bandwidth capacitance multiplier (C-multiplier) is adopted in [68]. The ALDO proposed in [69] integrates dual-pass transistors, using an approach that is explicitly discussed in the following subsection.

With the downscaling of the supply voltage, the available voltage headroom for the analog circuit is reduced. As highlighted in [19], the performance of analog circuits at low supply voltage is degraded due to reduced gain. To address the constraint of low supply voltage, the authors of [26] and [29] propose a charge-pump-based ALDO with a PMOS pass transistor. In [26], a negative charge-pump-based ALDO with the basic architecture shown in Fig. 12 is described. Compared to other charge-pump-based NMOS ALDO architectures, which may require multiple stages of charge pumps, the single-stage negative charge pump implemented in [26] to achieve lower voltage stress. In this work, the charge pump provides a negative voltage to the error amplifier and buffer circuit, thus establishing an extended voltage headroom to drive the PMOS pass transistor. With the assistance of the negative charge pump, the input voltage can be lowered down to 0.6 V, providing an output voltage of 0.5 V and supplying a load current of up to 45 mA while maintaining a quiescent current of 21 μA. In contrast, the scheme in [29] includes a positive charge pump to power the error amplifier and buffer. With a higher voltage supplied to the error amplifier and buffer, the input voltage can be lowered to 0.5 V, and an output voltage of 0.4 V can be provided while a load current of up to 100 mA is supplied with a quiescent current of 21 μA maintained.

Although a charge-pump-based ALDO with NMOS pass transistor has the advantage of low output impedance, the requirement for a charge pump may give rise to reliability issues [18]. Nevertheless, with the downscaling of the supply voltage, a charge-pump-based ALDO with PMOS as the pass transistor is a relatively new architecture that has the potential to be further improved, in the context of circuit reliability.

C. SINGLE PASS TRANSISTOR ALDOs

Due to the constraint of low loop gain leading to a degraded load regulation performance in an FVF LDO, and the pressing reliability issues of charge pump-based LDOs, recent research work has focused on developing ALDO architectures with a single output pass transistor, as shown in Fig. 1. Various circuit architectures have been proposed to address the constraints of load transient response and PSR, for example using adaptive biasing [53], dynamic biasing [70], an adaptive compensation technique [56], multiple feedback loops [33], a feedforward technique [41], pole tracking/movements [32], pole-zero cancellation [71] or a combination of these and other innovative techniques, as briefly discussed in this section.

The adaptive and dynamic biasing technique is discussed in [70]. This approach maintains the current efficiency while providing the much-needed gate driving capability to the pass transistor for high load conditions, especially during load transient. In adaptive biasing, the bias current is proportional to the load current, as reported in [45], [53], [73], and [74], where the quiescent current is reduced to 1.6 μA at minimum load current and is increased to 200 μA for a full-scale load current. Unlike adaptive biasing, dynamic biasing provides a momentary large gate driving current to the pass transistor during the load transient [70] while providing a consistent steady-state low biasing current, as highlighted in [70] and [75].

Due to the dependency of the load current on the output transconductance of the pass transistor, the pole frequency is shifted with respect to the load current, which may lead to stability issues in OCL-LDOs [55]. To address the issue of stability degradation, innovative compensation techniques have been proposed, such as adaptive compensation [56], dynamic compensation [76], active compensation [28], [39], nested Miller compensation [77], pole-zero cancellation [71], non-dominant pole movement [32] and loop gain stabilisation [27].

In circuit topologies with multiple feedback loop techniques, such as that in [33], the feedback signal paths are separated into a slow loop and a fast loop. The slow loop is the main loop in which the error amplifier provides steady-state voltage regulation, while the fast loop enables the LDO to improve its response to the load transient [76]. For the auxiliary loop, various techniques can be employed, such as frequency compensation [33], adaptive biasing [53], and multiple loops for dynamic biasing [78].

ALDO architectures with an NMOS used as the pass transistor without the need for the integration of a charge pump are proposed in [78], [79], and [80]. As the requirement for a charge pump is eliminated, the high gate bias voltage required for the NMOS pass transistor is derived from a second supply voltage, which is extracted from the battery in the proposed design. This approach addresses the limitation in the need for a high gate bias voltage while maintaining a low dropout voltage across the pass transistor. However, additional wires will be required in this approach, and a careful layout is crucial to avoid introducing additional interference from the interconnection for the second supply voltage.

To address the issue of PSR, various compensation methods have been explored. The ALDO reported in [80] and [81] generates a replica of the power supply ripple signal to compensate for the supply ripple. In [80], the supply ripple is sensed through an auxiliary amplifier, following which an out-of-phase replica of the ripple signal is injected into the buffer to cancel out the voltage supply ripple. In [81], the supply ripple is tracked by an adaptive supply ripple circuit, and a replica of the in-phase ripple signal is injected into the body of the pass transistor. As an alternative to cancellation

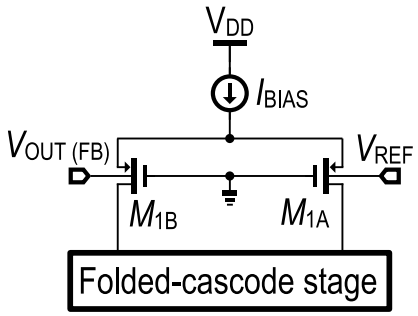

FIGURE 13. A bulk-driven PMOS differential pair as the input to the error amplifier in [83].

through replica ripple generation, capacitance manipulation techniques are proposed in [38] and [82]. A negative capacitance circuit and a voltage damper are employed in [38] to enhance the PSR. In the negative capacitance circuit, supply noise coupling through the gate capacitance of the pass transistor is canceled by integrating the negative capacitance circuit into the gate of the pass transistor, which nullifies the gate capacitance and enhances the PSR. Rather than using a negative capacitance circuit as in [38], the scheme in [82] adopts a via-based capacitor, in which an output capacitor in the range of nF is realized by using coaxial through silicon technologies. This approach achieves a higher capacitive density. However, the coaxial through silicon technology requires modification in the fabrication process, which might not be straightforward in existing foundries.

With the continuous downscaling of the supply voltage, analog circuits such as ALDOs are suffering from limitations of low voltage headroom, due to the degradation in the gain of the error amplifier [19]. To address this issue, instead of using a gate-driven (GD) differential pair as the input stage of the error amplifier for an ALDO, a bulk-driven (BD) PMOS differential pair is employed as shown in Fig. 13 [83]. As shown in Fig. 13, the input reference voltage, V_{REF}, and the feedback from the output voltage, $V_{\mathrm{OUT(FB)}}$, are connected to the bulk terminal (or the body of the PMOS for a BD PMOS differential pair), while the gate terminals of both PMOSs are grounded. Compared to the GD differential pair, the BD PMOS differential pair achieves a larger input common-mode voltage range, which provides the necessary voltage headroom for the operation of analog circuits, and allows the proposed ALDO to operate at a supply voltage as low as 0.6 V, with an output voltage of 0.5 V. However, the bulk voltage of the PMOS should be kept above the source voltage to avoid the parasitic *pn* junction of the PMOS to be forward biased, which requires a diligent design approach. In addition in employing a BD differential pair as in [83], current feedback is adopted in [35] to alleviate the limitation of low voltage headroom. In [35], a supply-voltage-insensitive reference current is generated and a constant-g_m circuit is integrated with the design, which allows the ALDO to operate at a supply voltage as low as 0.58 V and with a dropout voltage of 50 mV. Although the proposed ALDOs in

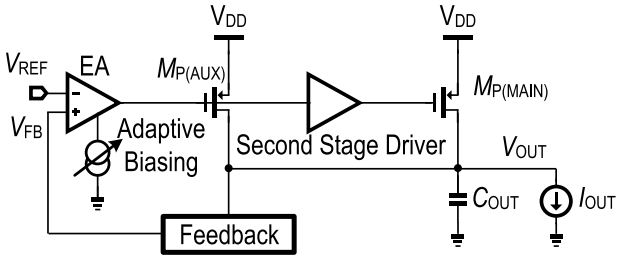

FIGURE 14. Basic block diagram of a dual PMOS LDO [51].

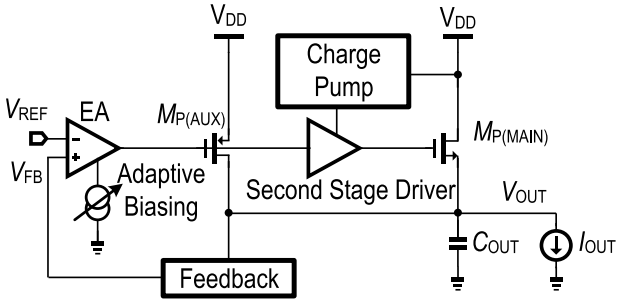

FIGURE 15. Basic block diagram of a dual-pass transistor LDO with a combination of NMOS and PMOS [69].

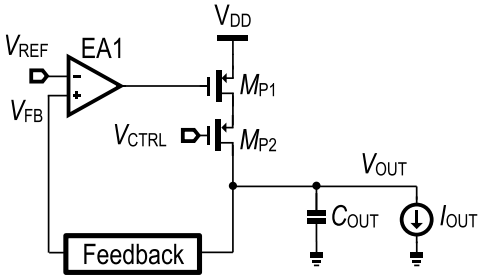

FIGURE 16. Basic block diagram of a dual-pass transistor LDO with stacked PMOS [85].

[35] and [83] can operate at a supply voltage of around 0.6 V, the load current capacity is limited to 3 mA and 0.75 mA, respectively. Nevertheless, the proposed ALDOs demonstrate the possibility of low voltage, sub-1-V analog circuit design.

D. DUAL PASS TRANSISTOR ALDOs

An ALDO with a single pass transistor is expected to accommodate an extended range of load current while maintaining current efficiency and providing a fast load transient response. Although additional gain stage are required to provide good regulation over the range of load current, this increases the current consumption, introduces additional poles into the control loop, and introduces complications associated with the shifting of the pole frequency due to load current changes. The constraint proves to be challenging for a multistage circuit topology [84], due to the design tradeoffs between the dropout voltage, pass transistor gate width, supply voltage, bandwidth, and stability [85]. To address these challenges, circuit techniques such as the adaptation

of a dual-pass transistor have been proposed [17], [51], [69], [84], [85].

Fig. 14 shows a basic block diagram of a parallel dual-pass transistor architecture with a PMOS for each pass transistor [51], [84]. It is observed that at low load current, only the auxiliary pass transistor, $M_{P(AUX)}$, with a smaller gate width is turned on, while the main pass transistor, $M_{P(MAIN)}$ is turned off at low load current to maintain the stability. As the load current increases, the main pass transistor is turned on to increase the gain [84], which provides a balance between the quiescent current consumption and the load transient performance. To maintain stability when transitioning, i.e., with the main pass transistor turned on and off, adaptive circuit techniques with feedforward biasing and frequency compensation are used [51].

PMOS and NMOS combinations are used as the pass transistors in [17] and [69]. In [17], the NMOS pass transistor serves as an auxiliary device to maintain a stable gate voltage. However, no available reported data are presented to describe the performance of the load transient response. In [69], a PMOS provides a high-speed path for the load transient response, whilst an NMOS provides a low output impedance path to enhance the stability under light load condition, as shown in Fig. 15. Charge pumps are required to drive the NMOS pass transistor, and these have similar limitations to those of a charge-pump-based ALDO using a single-pass transistor [17]. The sizing of the pass transistor, $(W/L)_{MP}$ is critical to establishing a good balance between the design tradeoffs respective to efficiency, load transient response, stability, and PSR.

In the architecture presented by Pashmineh et al. as shown in Fig. 16, the dual pass transistors are stacked in series configuration two pass devices in series [85], as compared to other dual pass transistors configured in parallel as shown in Fig. 14 and 15. Stacked dual pass transistor LDOs offer the advantages in improving PSR besides able to operate at higher operating voltage. However, due to the stacking of pass transistors, the voltage headroom required is higher, which is challenging to implement in low voltage applications such as the applications in [83], [86], [87], [88], [89], [90], [91], [92], [93], [94], and [95].

IV. BENCHMARKING OF STATE-OF-THE-ART ALDOs

In this section, a detailed comparison of the reported state-of-the-art ALDOs is presented. The most recent ALDO designs are benchmarked, and the performance of each architecture is discussed. From the benchmarkings, the perspectives of the applications of ALDOs are discussed.

A. BENCHMARKING STATE-OF-THE-ART ALDOs

The best performing state-of-the-art ALDOs are evaluated using FoMs involving the recovery time, the edge time of the load current change, T_{edge}, and the output voltage droop, ΔV_{OUT}. To provide a comparison between the architectures in terms of the load transient response, the change between the minimum and maximum load current should be considered; this is because the operating region of the pass transistor, M_P, transitions between the deep sub-threshold when the load current approaches 0 μA and towards the saturation and triode region when the load current approaches the maximum designated load current [26], [55].

Table 1 shows that the FVF-LDO architecture has faster settling and recovery times compared to other designs, as the fast loop is located within the FVF structure, which improves the load transient response [23]. However, due to the DC requirement to boost the bandwidth of the FVF [60], the overall quiescent current consumed by the FVF-LDO architectures is higher than for the other proposed schemes. This shortcoming can be addressed by adopting a dynamic biasing scheme, as discussed in [25], in which a lower quiescent current was reported with this approach.

The graph describing the evaluation using FoMs (Figs. 17 and 18) is plotted against the quiescent current. The best-performing design exhibits a lower FoM score and consumes the least quiescent current. As mentioned in [44], the settling time, $T_{RC,}$ and the voltage droop during the load transient affect the overall accuracy. Hence, the settling time, T_{RC}, is a key parameter of an OCL-ALDO [31], [47], [56], and is more important than the response time, T_{RS} [50], evidently shown in Fig. 5. When evaluating the performance of an ALDO, FoMs involving the settling time can assess the load transient response more accurately than those based on the response time [50], which differentiates the performance of the architectures with respect to fast recovery time, which is favorably reflected with the achievement of a lower score.

During a load transient, the operating region of the pass transistor transitions between the deep sub-threshold, saturation and triode region as the load current rises from 0 μA to the maximum designated load current [26], [55]. Hence, the change between the minimum and maximum load current, and the minimum load current itself, should be considered when evaluating the performance using an FoM, to enable a fair benchmarking between designs. FoM_{19} considers the dropout voltage, V_{DO}, which is essential in achieving superior efficiency [36], when evaluating the load transient response against the efficiency.

As can be observed from Fig. 17, the ALDO with the FVF topology achieves a lower FoM compared to other reported architectures and exhibits faster settling and recovery times compared to other topologies since the fast loop within the FVF structure helps to improve the load transient response [23]. However, the overall quiescent current consumed by the FVF-LDO architecture is higher than the other topologies, due to the DC requirement in boosting the bandwidth [60]. For IoT devices that are active for only a short period, and spends most of the time in standby mode, low current and power consumption are highly desirable [25], [32]; this favors the designs located at the bottom left of the FoM graph in Fig. 17, such as the works reported in [25], [33], and [51].

The results for the PSR show that the low-frequency PSRs of the FVF-LDO architectures are generally much lower than those of the other designs, due to the low loop gain

TABLE 1. Comparison of recent state-of-the-art works of ALDO regulators with best performance.

Design	[23]^{Exp}	[34]^{S}	[36]^{Exp}	25]^{Exp}	[67]^{Exp}	[26]^{Exp}	[43]^{Exp}	[74]^{Exp}	[39]^{Exp}	[53]^{Exp}	[79]^{Exp}	[51]^{Exp}
Topology of Output Stage	FVF	FVF	FVF	FVF	Charge Pump NMOS	Charge Pump PMOS	Single PMOS	Single PMOS	Single PMOS	Single PMOS	Single NMOS	Dual PMOS
Process (nm)	65	65	28	65	250	65	55	180	65	180	28	180
Active Area (mm^2)	0.053	N/A	0.0086	0.0042	0.11	0.045	0.042	0.0285	0.0021	0.0297	0.034	0.055
V_{DD} (V)	1.2	1	0.9	1	1.5	0.6	0.8	1.4	1	1.8	2	1.2
V_{OUT}(V)	1	0.85	0.85	0.8	1.26	0.5	0.6	1.2	0.8	1.6	1.8	1
V_{DO} (V)	0.2	0.15	0.05	0.2	0.24	0.1	0.2	0.2	0.2	0.2	0.2	0.2
C_{OUT} (F)	300 p	1 μ^{ECap}	36 p	10 p	1 μ^{ECap}	100 p	1 μ^{ECap}	1 μ^{ECap}	25 p	1 μ^{ECap}	1 μ^{ECap}	100 p
Minimum I_{Load} (µA)	5	0	0	0.1	0	1	100	10	0	10	0	0
Maximum I_{Load} (mA)	20	50	20	10	150	45	10	50	25	50	1	100
I_Q (µA)	2.7	3.54	33	0.03	1.24	21	0.016	1.6	1.6	1.3	35	0.407
Load Regulation (mV/mA)	0.015	0.027	0.26	1.22	0.17	0.047	1.05	0.1	0.281	0.32	0.006	0.77
Line Regulation (mV/V)	N/A	12.57	17.5	N/A	N/A	1	0.5	5.5	0.7	1.1	0.23	0.283
ΔV_{OUT} (V) (Undershoot)	0.059	0.031	0.176	0.231	0.16	29	0.07	0.024	0.035	0.026	0.01	0.117
$\Delta V_{out,pk\text{-}pk}$(V) (Undershoot + Overshoot)	0.13	0.059	0.24	0.394	0.225	94	0.074	0.074	0.071	0.046	0.02	0.152
Load current step ΔI_{Load} (mA)	19.9	50	20	9.9999	150	44	9.9999	50	24.99	49.99	1	100
T_{edge} (ns)	0.8	1	0.1	200	10	1000	20	10	100	10	100	300
T_{Rs} (ns)	0.9	28	N/A	N/A	900	N/A	N/A	N/A	N/A	N/A	N/A	N/A
T_{Rc} (ns)	20*	100*	220*	100	20,000	1,000*	5,000*	1,000	100	5,000*	4,000*	1,000
PSR (dB) @ 1 kHz	42	46.7	30	26	44	70	42.7	30	50	26	76	46.82
PSR (dB) @ 1 MHz	42	42.9	24	24	35	25	N/A	30	26	35.5	53	37.7
Current Efficiency (%)	99.6	99.99	94.4	99.99	99.93	99.95	99.99	99.6	99.04	99.46	99.9	99.75
FoM_9 (mV)	0.32	0.011	0.145	0.694	0.066	69.2	0.011	0.038	1.12	0.034	0.175	0.714
FoM_{13} (mV)	6.4	1.1	31.9	69.4	1320	6920	56.6	38.4	112	171	700	714
FoM_{19} (ps)	1.52	0.165	1.6	60.2	317	7250	12.0	55.7	22.4	297	140	143
FoM_{20} (µs)	303	39	2040	3,290	5,080	1,640,000	3,740	23,700	5,300	1,050	8,280	4,410
FoM_{21} (ps)	0.64	0.15	12.1	0.012	3.76	6.67	0.187	1.07	0.128	5	1.84	0.087
FoM_{22} (ps)	0.11	0.025	2.02	0.002	1.25	2.22	0.037	0.152	0.0256	1	0.368	0.015

*Recovery/settling times estimated from the graph.

^{Exp}Experimental Results presented. ^{S}Simulation Results Presented. ^{ECap}External Output/Load Capacitor.

of the FVF-LDO, which results in degraded load regulation [30]. However, the PSR-affiliated FoMs such as FoM_{21} and FoM_{22} result in a comparable benchmarking for the reported FVF-LDO architectures, due to the fast settling and recovery time–during load transient. Since the bandwidth of the LDO is considered in FoM_{22}, the design proposed in [25] yields a value that is an order of magnitude lower than the other architectures, as shown in Table 1 and Fig. 18.

B. PERSPECTIVE APPLICATIONS OF ALDOs

The continuous scaling down in process and supply voltage leads to a design challenge where at reduced supply voltage, the performance of ALDOs degrades due to reduced open loop gain [19] and reduced voltage headroom [83]. To address the issue of reduced voltage headroom, bulk-driven, or a combination of bulk-driven and gate-driven transistors can be employed in the circuit design, which increases the input voltage headroom. This approach allows the ALDO to operate at a low supply voltage, which finds application in micro energy harvesting [83] and Bluetooth Low-Energy (BLE) transmitters operating at a low supply voltage of 0.5 V [90] and 0.2 V [91].

In IoT application, the device usually operates in standby mode and is only active for a short period [25], besides that, various modules in the device can be turned on and off, causing a wide variation in the load current. Such requirements mandate the PMU and the ALDO to consume low quiescent current and provide a fast response to the load current variation [83]. To address this design demand, the combination of dynamic and adaptive biasing can be incorporated, which provides low quiescent current to cater to standby mode, and

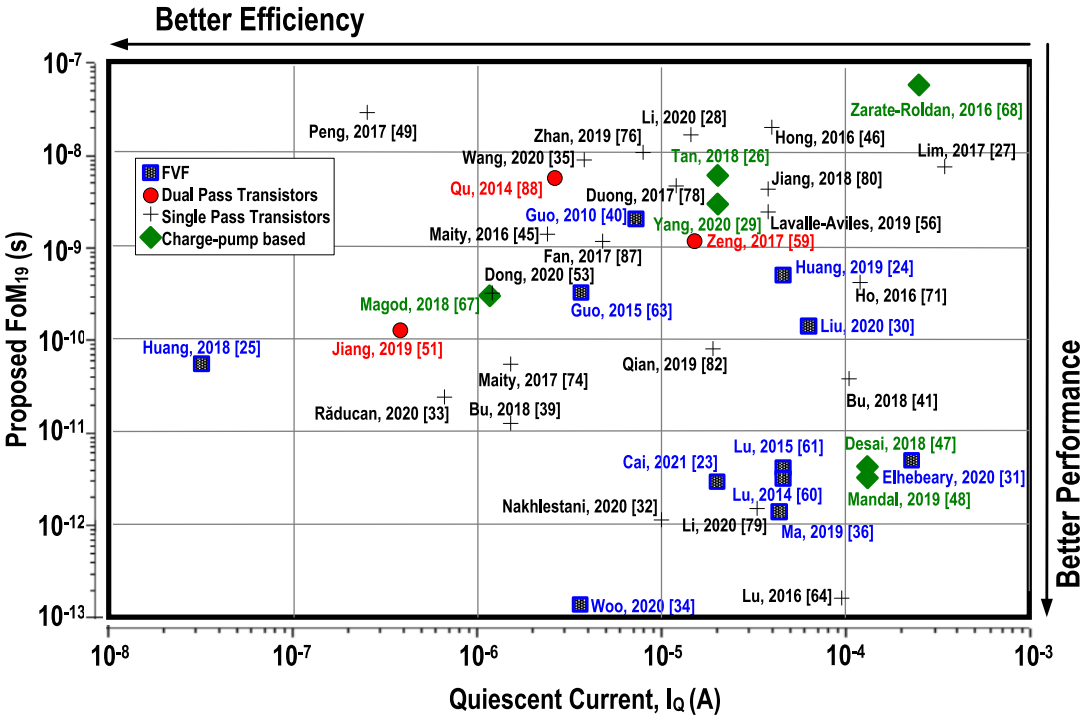

FIGURE 17. Assessments for state-of-the-art ALDO architectures using the proposed FoM_{19} versus quiescent current.

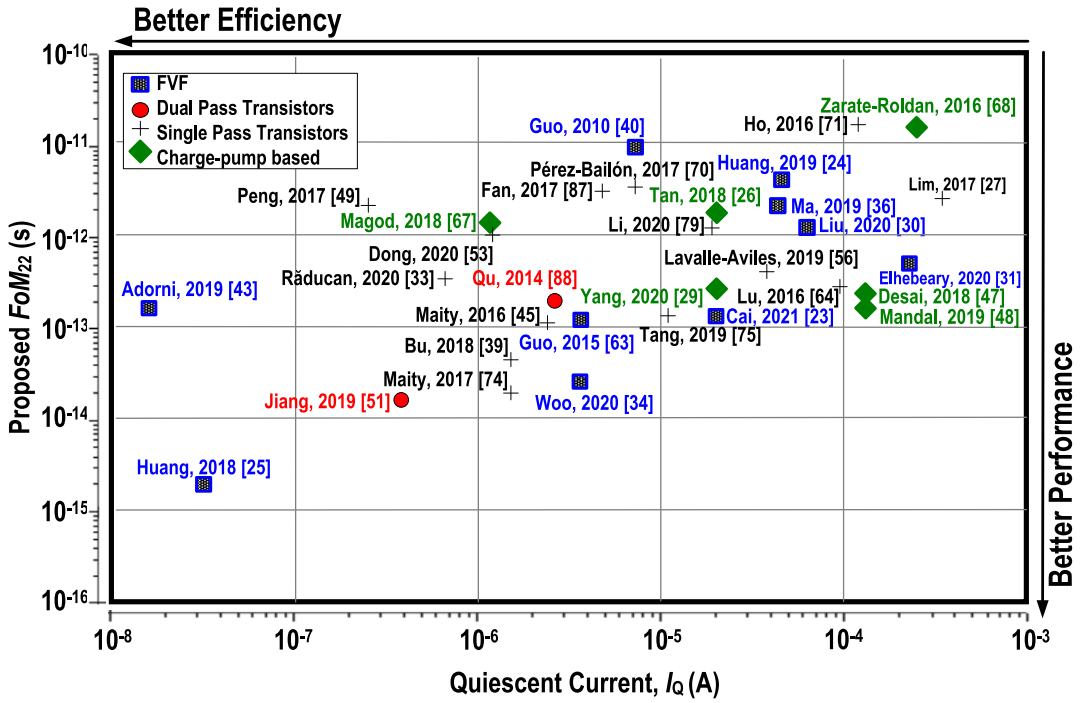

FIGURE 18. Assessments for state-of-the-art ALDO architectures using the proposed FoM_{22} versus quiescent current.

provides the fast response and fast recovery time needed for the fast load current change.

In a wireless-powered system, RFEH is incorporated, and the rectified harvested voltage is regulated by the ALDO in the PMU. This can be found in the wireless-powered material spectroscopy application, where the oscillator for the transmitting antenna operating at 1 V while drawing 4 mA of current is powered by the ALDO [92]. The trend for mobile application demands for ALDO to fulfill the requirements of low quiescent current consumption, fast response time, and fast recovery time to load transient while able to operate at low voltage, which can be below 1 V as in [90] and [91].

In wireless and wireline communications, the special requirement for low-voltage output with low noise ALDOs is to design an ultra-low jitter phase-locked loop (PLL) [93], in which some sub-blocks are under 0.9-V supply and the NMOS-only LC-tank voltage-controlled oscillator (VCO) has a supply voltage of 0.5 V. Considering that the systems require a unified global voltage, the ALDO needs to regulate this voltage gap between other functional circuits with a global voltage and NMOS-only LC-tank VCOs of the low supply voltage [94], [95]. Thus, for the noise-sensitive PLL and VCO, the low output noise is the primary concern for ALDOs.

V. CONCLUSION

Voltage regulators (e.g., LDOs) are essential to provide a stable voltage to the sensitive analog circuits in devices used for IoT, IoE, and mobile applications. To reduce the component count, the pin numbers, and the footprint on the circuit board, on-chip regulators such as the OCL-LDO can be integrated into the SoC solution. However, the innovative design of the OCL-LDO involves many important trade-offs. The absence of the dominant pole contributed by the external output capacitor leads to design challenges in context of stability, load transient response, and PSR. In this paper, we have carried out a performance review on the state-of-the-art LDOs based on circuit innovation and key design parameters. FoMs proposed by various authors for evaluating the performance of the presented LDO architectures, based on the critical parameters affecting the design of an LDO, have also been reviewed. With the continuous trend toward downscaling of CMOS technology, design challenges arise in relation of balancing the efficiency, load transient response, stability, PSR, and active chip area consumption. For the optimal implementation of an on-chip OCL-LDO in PMIC for IoT, IoE, and other mobile applications, the architecture should exhibit a fast load transient response while consuming low quiescent current with minimal dropout voltage for high efficiency, while occupying a small active area.

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