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RESEARCH ARTICLE

Frequency Domain Impedance Based Protection for Flexible DC Distribution Grid

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ABSTRACT The flexible DC distribution grid is suitable for distributed energy resource integration and DC load power supply. However, the fast-increasing fault current has a great impact on the system when a short circuit fault occurs. Besides, the existing main protections are easily affected by high resistance faults and converters. To solve the aforementioned problems, a pilot protection method using frequency domain (FD) impedance was proposed. Firstly, a direction criterion based on the polarity of FD reactance is constructed to identify the reverse fault. Furthermore, the values of FD reactance and resistance are used to distinguish the forward internal and external faults. The method uses only local information to identify the close-up fault, and the pilot protection criterion to identify the remote-end or high resistance faults. This combination of single-end and pilot protection criteria makes the method have high reliability and fast speed. Moreover, no data synchronization is needed. Finally, extensive simulations were utilized to verify the effectiveness of the proposed method.

INDEX TERMS Frequency domain impedance, pilot protection, flexible DC distribution grid, converter, S transform.

I. INTRODUCTION

With the development of renewable power generation like wind power and solar photovoltaic technology, the demand for grid access has been increasing. Owing to the advantages of flexible operation, such as large power supply capacity and high reliability, the modular multilevel converter (MMC)-based flexible DC distribution grid has a certain application in distribution systems [1], [2], [3], [4]. However, the pole-to-pole fault (PPF) poses a great threat to the flexible DC distribution grid. The fault process can be divided into two stages: the discharge process of capacitance in MMC and the current injection process on the AC side. The voltage drops rapidly, and the current rises up to a very high peak value during the sub-module capacitance discharge within several milliseconds. If the fault line cannot be isolated rapidly, the MMC may be blocked under overcurrent, which will decrease the reliability of the DC grid [5]. To avoid the aforementioned problem, it is very important for protection to distinguish the fault reliably [6], [7], [8], [9].

Generally, the existing main protection methods applied in flexible DC distribution system may be divided into two categories: unit protection and non-unit protection. Through sharing fault information at both line terminals, the unit protection methods can achieve absolute selectivity. The methods proposed in [10], [11], and [12] were based on the current differential protection principle, which has strong selectivity but requires strict data synchronization. To improve the above shortcoming, researchers have proposed several new protection methods. In [13], a protection scheme was built using the current correlation coefficient, which is unsusceptible to the distributed capacitance and noise; however, its algorithm is complex. A traveling wave-based protection for the DC distribution grid was proposed in [14]. However, this method requires a high sampling rate, and it is difficult to identify the head of the initial traveling wave because of the short feeder in the distribution grid. In [15], a directional comparison pilot protection based on transient high-frequency impedance

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was proposed. Nonetheless, the protection threshold is easily influenced by the topology and system operating conditions. A double-ended protection using the voltage polarity of current limiting inductance (CLI) at both line terminals was proposed in [16]. The principle and algorithm of the protection are simple, but the extraction of voltage across the CLI is a problem in practical engineering. The study in [17] proposed a unit protection method based on the fault component current. Nevertheless, the load current and reverse power flow caused by the grid connection of renewable energy will decrease the reliability of the protection.

The non-unit protection is usually set as the main protection due to its high speed of fault identification. Since the CLI can effectively prevent high-frequency signals, many non-unit protections were proposed based on the CLI. However, these protections are often difficult to identify the remote-end fault and are susceptible to fault resistance. In [18], single-ended protection based on the initial current traveling wave was proposed. The polarity of the initial current traveling wave was used to identify the fault direction, and the estimated time constant was applied to identify the fault section. However, for short feeder and remote-end faults, the reliability of protection is extremely affected. Single-ended protection based on the initial zero-sequence current traveling wave was proposed in [19]. The method can identify the fault with high resistance and noise, but the sampling rate is relatively high, which will increase the economic cost. The positive sequence voltage at both terminals of CLI was used in [20], and a protection based on the initial traveling wave was proposed in [21]. Both of these two methods are difficult to identify the wave head when the near-end fault occurs. The scholars in [22] and [23] applied the first and second derivatives of fault transient current as fault identification criteria. These methods can detect the fault within a few milliseconds. Still, they are susceptible to the interference of noise and fault resistance. The transient voltage on CLIs was used as the protection criterion in [24] and [25]. The voltage amplitude difference between reactors on positive and negative poles was used to select the fault poles [24]. This method has good robustness for the high resistance fault, but its setting value depends on the simulation result. In [25], a square difference of transient voltage-based protection was proposed. This method is suitable for various fault types, but the calculation based on wavelet transformation is complex. In [26] and [27], the methods can detect the fault location using the inductance value from the fault point to the measuring point in the time domain. However, the methods are only applicable to the radial topology and easily affected by the branch line.

In order to eliminate the influence of high resistance fault and converter on the protection, this paper proposes a novel pilot protection method. By combining the local information and the logical signal from the opposite protection unit, the protection criteria based on the S-transformed FD impedance are constructed. The polarity of FD reactance is responsible for identifying the fault direction and the values of FD reactance and resistance can distinguish the forward internal and external faults.

The contributions of our study are:

1) The directional criterion and FD impedance-based criterion using only local information can quickly identify the fault close to the protection unit, which can shorten the identification time of close-up fault.

2) For the remote-end or high resistance faults, the proposed pilot protection criterion, which is combined by the local information and the logical signal from the opposite terminal, can cope with the influence of converter and fault resistance on the protection reliability. Additionally, the pilot protection needs no data synchronization.

The rest of this paper is organized as follows. In Section II, an analysis of the fault characteristic in the frequency domain is presented that is the basis of protection. Section III explains in detail the protection criteria based on the FD impedance. In Section IV, several simulations are conducted to verify the effectiveness and reliability of the protection. Finally, Section V summarizes the conclusions of the article.

II. ANALYSIS OF FLEXIBLE DC DISTRIBUTION GRID

In comparison with the high voltage direct current (HVDC) grid, the flexible DC distribution grid has lower voltage and smaller capacity. Therefore, the symmetrical monopole topology and small current earthing mode are often applied in the flexible DC distribution grid. The faults of flexible DC distribution grid mainly include PPF and single pole-to-ground fault (SPGF). When the PPF occurs, the fault current is mainly provided by the discharging of sub-module capacitance in MMC before MMC is blocked. The voltage between the two poles drops to zero rapidly, and the fault current rises extremely fast, which may endanger the semiconductor component, and result in MMC being blocked [28], [29]. When the SPGF occurs, the current loop cannot be formed, and the bridge capacitance of MMC does not discharge. Thus, the SPGF only changes the voltage's zero point of the DC side and has little influence on the current. As a result, when the SPGF occurs, the system can operate for a period of time. Since the damage of PPF is much greater than that of SPGF in the flexible DC distribution grid, the PPF is mainly analyzed in this article.

A. FAULT CHARACTERISTIC ANALYSIS IN THE FREQUENCY DOMAIN

The main contribution of the fault current is the bridge capacitance of MMC in the early stage of PPF occurring in the DC line. In general, the MMC can be equal to the series connection of inductance L_S and capacitance C_S, as shown in Fig.1 [28]. In the complex frequency domain, since the initial voltage of the equivalent capacitance and the initial current of the equivalent inductance are not zero after the fault occurs, there is an additional power source in the circuit. Considering that the major supply of the fault current is the discharge of the sub-module capacitance, the additional initial current power produced by the inductance can be neglected. Besides, the

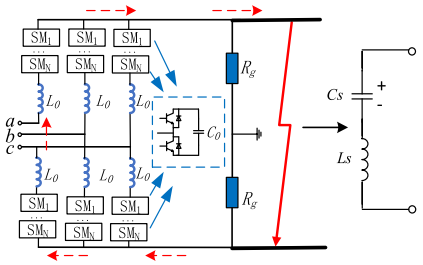

FIGURE 1. Equivalent circuit of MMC.

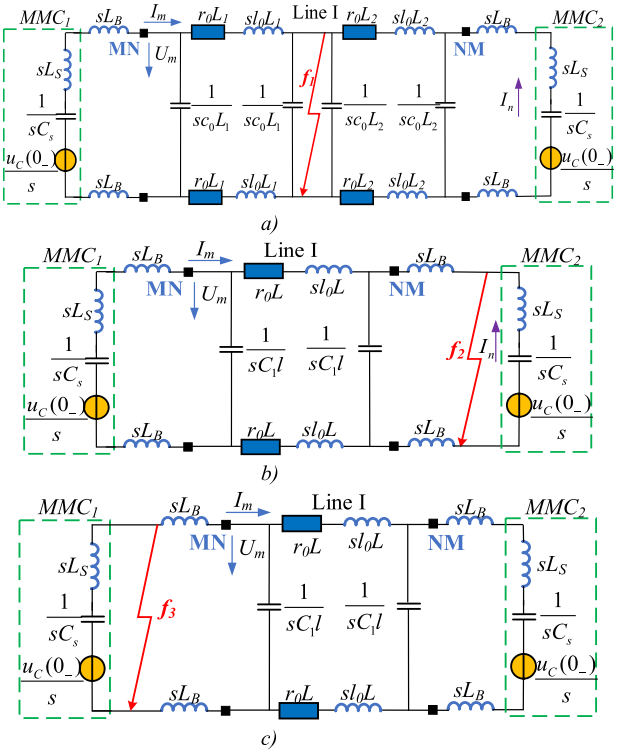

FIGURE 2. Equivalent fault circuit diagram: a) Internal fault, b) Forward external fault, c) Backward external fault.

sub-module capacitance of MMC is much larger than that of the DC line, and the discharge of the distributed capacitance in the DC line is also ignored.

Taking the two-terminal DC distribution system as an example, the DC line is equivalent to the lumped parameter circuit. The equivalent circuit for metallic PPF in the complex frequency domain is shown in Fig. 2, where r_0, l_0, and c_0 represent the unit resistance, unit inductance, and unit capacitance, respectively. L_1, L_2 and L are the line length, and L_B represents the CLI; U_m and I_m represent the measuring voltage and current, respectively. sL_s and $1/sC_s$ represent the equivalent inductive reactance and capacitive reactance of MMC, respectively; $u_c(0_-)/s$ is the additional voltage source of capacitance. MN and NM are the places of protection installation.

As shown in Fig. 2 a), the PPF occurs at f_1 in line I. Due to the symmetry of the two poles, the voltage from the measuring point to the ground is used in this paper. The positive direction of the current is from the bus to the DC line. We define the complex FD measuring impedance z_m as the ratio of voltage to current in the complex frequency domain at the measuring point, as shown in Eq. (1):

$$z_m(s) = \frac{U_m(s)}{I_m(s)} \tag{1}$$

Then, the complex FD impedance z_{m_f1} at the point MN can be obtained as shown in Eq. (2):

$$z_{m\_f1}(s) = (r_0L_1 + sl_0L_1)//\frac{1}{sc_0L_1} \tag{2}$$

Therefore, the complex FD impedance z_{m_f1} reflects the impedance from the measuring point to the fault point. The imaginary and real parts of the complex FD impedance can be expressed as follows:

$$\begin{cases} real(z_{m\_f1}) = \dfrac{r_0(\omega^2 l_0c_0L_1^2 - 1)}{\omega^2(c_0^2r_0^2L_1^4 + 4l_0c_0L_1^2 - 2\omega^2c_0^2l_0^2L_1^4) - 1} \\ im(z_{m\_f1}) = \dfrac{wc_0^2r_0^2L_1^4 + \omega l_0L_1(\omega^2 l_0c_0L_1^2 - 1)}{\omega^2(c_0^2r_0^2L_1^4 + 4l_0c_0L_1^2 - 2\omega^2c_0^2l_0^2L_1^4) - 1} \end{cases} \tag{3}$$

The line parameters are shown in Table 1, and it can be seen that $\omega^2 l_0c_0L_1^2 \ll 1$; then, $\omega^2 l_0c_0L_1^2$ can be ignored. Therefore, the line capacitance in the FD impedance can be ignored. Therefore, The Eq. (3) can be approximately expressed as follows:

$$\begin{cases} real(z_{m\_f1}) = r_0L_1 \\ im(z_{m\_f1}) = \omega l_0L_1 \end{cases} \tag{4}$$

As shown in Eq. (4), the imaginary and real parts of the FD impedance are the line resistance and line reactance from the measuring point to the fault point, respectively. Thus, the FD reactance can be defined as the imaginary part of the FD impedance, and the FD resistance can be defined as the real part of the FD impedance.

Similarly, as shown in Fig. 2 b), when the forward external metallic PPF occurs at f_2 (the most serious faults occurring at the forward bus), the complex FD impedance can be expressed as:

$$z_{m\_f2}(s) = \frac{1}{2}\left[2r_0L + 2sL_0L + (2sL_B//\frac{1}{sc_0L})\right]//\frac{1}{sc_0L} \tag{5}$$

In comparison with Eq. (2), it can be seen that the complex FD impedance under the forward external PPF is equivalent to adding the parallel part of CLI and line capacitance to the FD impedance under the internal PPF. Since $L_B \gg c_oL$, the complex FD impedance can be approximately expressed as:

$$z_{m\_f2}(s) \approx (r_0L + sL_0L + sL_B)//\frac{1}{sc_0L} \tag{6}$$

Therefore, when forward external PPF occurs, the imaginary and real parts of the complex FD impedance can be expressed as in (7), shown at the bottom of the next page.

As previously mentioned, since $\omega^2(l_0L + L_B)c_0L \ll 1$, $\omega^2(l_0L + L_B)c_0L$ can be ignored. Thus, the FD reactance and resistance can be approximately expressed as shown in Eq. (8):

$$\begin{cases} real(z_{m\_f2}) = r_0L \\ im(z_{m\_f2}) = \omega(l_0L + L_B) \end{cases} \tag{8}$$

As shown in Fig. 2 c), when the reverse external metallic PPF occurs at f_3 (the most serious faults occurring at the backward bus), the complex FD impedance can be expressed as:

$$z_{m\_f3}(s) = -R_L - sL_B \tag{9}$$

Thus, the FD reactance and resistance can be expressed as shown in Eq. (10):

$$\begin{cases} real(z_{m\_f3}) = -R_L \\ im(z_{m\_f3}) = -\omega L_B \end{cases} \tag{10}$$

in which R_L is the resistance between the measuring point MN and the fault point. According to Eqs. (4), (8), and (10), when PPF occurs, the values of FD reactance and resistance under the forward external fault are constantly larger than those under the internal fault. Besides, the polarity of FD reactance or resistance is positive in the case of forward fault. However, in the case of reverse fault, the polarity of FD reactance or resistance is negative.

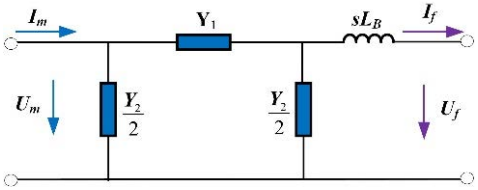

FIGURE 3. Equivalent circuit of DC line with lumped parameters.

TABLE 1. Parameter values of DC cable.

Parameters	Values and units
Inductance (l_0)	0.4927-0.6474 mH/km
Capacitance (c_0)	0.1922 -0.5311 uF/km
Resistance (r_0)	0.727-0.0470 Ω / km
CLI (L_B)	5 mH

B. ANALYSIS OF FREQUENCY

Due to the short line and low voltage of the DC distribution grid, the DC line is equivalent to the lumped parameter. For an external fault, the equivalent circuit of the DC line is depicted

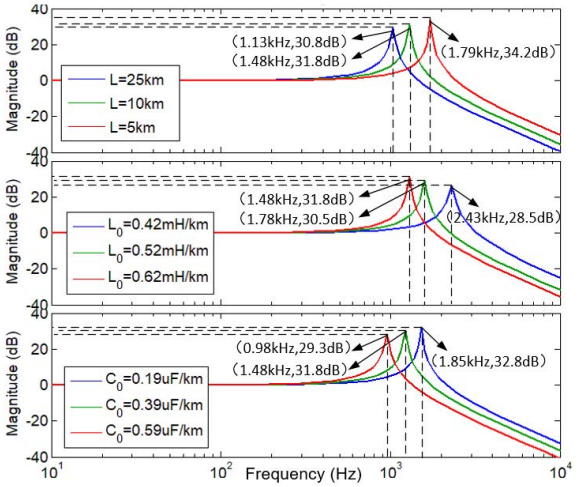

FIGURE 4. Amplitude-frequency characteristics of H(s).

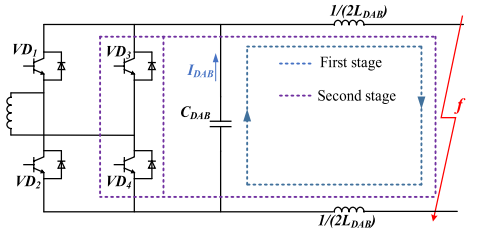

FIGURE 5. Fault current circuit of DC/DC at the high voltage side.

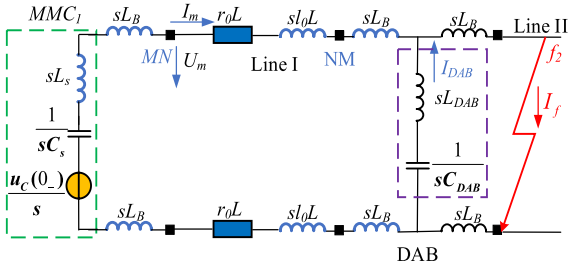

FIGURE 6. Fault equivalent circuit when bus contains DC/DC converter.

in Fig.3; Y_1 and Y_2 are equivalent admittances of the DC line, and L_B is the CLI. The parameters at both terminals are the measuring point voltage U_m (s), measuring point current I_m(s), fault point voltage U_f(s), and fault point current $I_f(s)$.

The transfer function is defined as:

$$H(s) = \frac{I_f(s)}{I_m(s)} = \frac{1}{1 + (Y_2/Y_1) + (L_BY_2^2/Y_1) + 2Y_2L_B} \tag{11}$$

$$\begin{cases} real(z_{m\_f2}) = \dfrac{\omega^2 r_0(l_0L + L_B)c_0L - r_0}{\omega^2(c_0^2r_0^2L^4 + 4l_0c_0L^2 - 2\omega^2c_0^2l_0^2L^4) - 1} \\ im(z_{m\_f2}) = \dfrac{[wc_0^2r_0^2L^4 + \omega(l_0L + L_B)(\omega^2L_1c_0L^2 - 1)]}{\omega^2\left[c_0^2r_0^2L^4 + 4(l_0L + L_B)c_0L - 2\omega^2c_0^2L^2(l_0L + L_B)^2\right] - 1} \end{cases} \tag{7}$$

where

$$\begin{cases} Y_1 = 1/(r_0 L + s l_0 L) \\ Y_2 = g_0 L + s c_0 L \end{cases} \tag{12}$$

In Eq. (12), r_0, l_0, g_0, and c_0 represent the unit resistance, unit inductance, unit conductance and unit capacitance, respectively, and L represents the line length.

Medium voltage cables have different modes that have different electrical parameters, which are listed in Table 1. Since the cable's resistance is hardly influenced by the frequency, it will not be analyzed here. According to the parameters, the amplitude-frequency characteristic curves of the transfer function H(s) can be calculated as shown in Fig. 4, in which the line length, unit inductance, and unit capacitance take different values. L_B is chosen as 5mH. From Fig. 4, it can be seen that the amplitude-frequency curve of 20lg|H(s)| increases gradually from zero for the same line when the frequency is in the range of $0<f<f_0$, where $f_0$is the line resonant frequency. When $f>f_0$, the transfer function |H(s)| obviously decays. With the increase of the line length, unit inductance, and capacitance, the frequency at the resonant peak decreases gradually. When the value of unit line capacitance is 0.59 uF/km, the f_0 reaches its minimum value of 0.98 kHz.

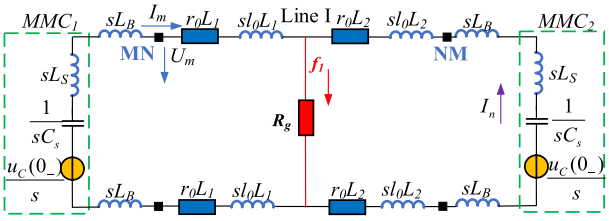

FIGURE 7. Fault equivalent circuit for internal high resistance fault.

TABLE 2. Calculated values of FD reactance and FD resistance.

$R_g(\Omega)$	FD reactance	FD resistance	Rate_ FD reactance	Rate_ FD resistance
20	15.44	1.32	-0.13%	186.96%
30	15.43	1.74	-0.19%	278.26%
50	15.41	2.61	-0.32%	467.39%
100	15.34	4.75	-0.78%	932.61%

Therefore, the DC line and CLI have strong attenuation on high-frequency signals. Considering the length and resonance frequency of the DC line, the specific frequency band is determined as 500-1000 Hz.

C. ANALYSIS OF SPECIFIC PROBLEMS FOR PROTECTION

In a DC distribution grid, the DC bus requires a DC/DC or DC/AC converter to interact with the load or distributed generation. Given that the high voltage side of the above converter is usually connected with large capacitance in parallel, the FD impedance is affected. Here, taking the DC/DC converter at the bus as an example, the analysis for a DC/AC converter is similar to that of a DC/DC converter.

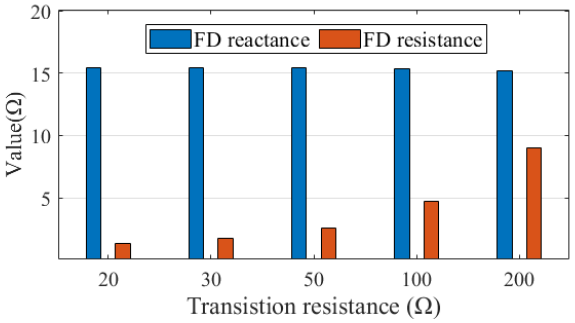

FIGURE 8. FD reactance and FD resistance under different fault resistances.

When the PPF occurs in the DC line, since the high-frequency transformer in the DC/DC converter with the dual active bridge (DAB) has the function of electrical isolation, the side of the DAB module near the fault mainly affects the fault characteristics of the DC/DC converter. The fault current circuit of the DC/DC at the high voltage side is shown in Fig. 5. The fault characteristics of the DC/DC converter can be divided into two stages: capacitance discharging stage and inductance after-flow stage. Due to the rapid increase of current in the capacitance discharging stage, which has a great impact on the system, this paper focuses on the capacitance discharging stage. The DC/DC converter in the stage of capacitance discharge can be equivalent to the series connection of equivalent capacitance C_{DAB} and equivalent inductance $L_{\mathrm{DAB}}$of DAB module [30], [31].

The fault equivalent circuit when the bus contains a DC/DC converter is shown in Fig. 6. Since the line capacitance has limited influence on the FD impedance, the influence of line distributed capacitance is ignored here. For the internal metallic PPF, the DC/DC converter does not affect the FD reactance of the measurement points at two terminals of the DC line. For the PPF occurring at f_2 in line II, in comparison with the case without DC/DC converter, the DC/DC converter is added to the FD impedance as a parallel part, which only affects the imaginary part of FD impedance. If the discharging of the equivalent capacitance is ignored in the DC/DC converter, the FD reactance at the point MN can be shown in Eq. (13):

$$\begin{aligned} im(z_{mn}) &= j\omega(L_B + l_0 L) \\ &\quad + j\omega \frac{C_{DAB}(\frac{L_B}{C_{DAB}} - 2\omega^2 L_B L_{DAB})}{2(1 - \omega^2 L_{DAB} C_{DAB} - \omega^2 L_B C_{DAB})} \end{aligned} \tag{13}$$

After comparing Eqs. (8) and (13), when the parameters satisfy Eq. (14), the DC/DC converter will cause the FD reactance to decrease.

$$\frac{C_{DAB}(\frac{L_B}{C_{DAB}} - 2\omega^2 L_B L_{DAB})}{1 - \omega^2 L_{DAB} C_{DAB} - \omega^2 L_B C_{DAB}} < 2L_B \tag{14}$$

According to [30] and [31], the parameters of C_{DAB} and L_{DAB} can be chosen as $200uF$ and $3mH$, respectively. It can be

calculated from Eq. (14) that when the frequency meets with the condition $f > 134.57$Hz, the DC/DC converter causes the FD reactance to decrease. According to the aforementioned analysis, the FD reactance in the selected frequency band will be reduced; the parallel part only leads to the decrease of FD reactance but cannot change its polarity.

For the high resistance fault, the fault resistance will affect the FD impedance, which may result in protection misoperation. As shown in Fig. 7, when a high resistance fault occurs at f_1, under the superposition effect of the additional power supply at both line terminals, the FD impedance Z_{mn} can be obtained as:

$$Z_{mn} = \frac{u_{m1} + u_{m2}}{i_{m1} - i_{m2}} = \frac{i_{m1} \cdot z_{m1} - i_{m2} \cdot z_{m2}}{i_{m1} - i_{m2}} \tag{15}$$

where u_{m1}, i_{m1}, and z_{m1} are the voltage, current, and FD impedance, respectively, when the left power supply acts alone; u_{m2}, i_{m2}, and z_{m2} are the voltage, current, and FD impedance, respectively, when the right power supply acts alone.

Therefore, according to Fig. 7, the FD impedance can be obtained as in Eq. (16), shown at the bottom of the page. After comparing Eqs. (4) and (16), it can be seen that the fault resistance affects both the real and imaginary parts of the FD impedance. According to the parameters in Table 1, the FD reactance and resistance can be obtained under different fault resistances, as shown in Table 2 and Fig.8, where the frequency is taken as 1000 Hz. In comparison with the metallic PPF, the maximum changing rate of the FD reactance is only -0.78%, while the changing rate of FD resistance is 932.61%. Therefore, the influence of fault resistance on FD resistance is much greater than that of FD reactance.

Thus, both the DC/DC converter and fault resistance affect the FD impedance. The DC/DC converter mainly affects the FD reactance, while the fault resistance mainly affects the FD resistance. If only the FD reactance is used to identify the fault section, it will lead to protection misoperation easily. If only the value of resistance is used, it also leads to protection misoperation. Based on the above analysis, to solve the protection misoperation conducted by the converter and high resistance fault, the FD reactance and resistance measurements are combined to identify the fault.

III. FD IMPEDANCE BASED PROTECTION CRITERIA

A. PRINCIPLE OF S TRANSFORM

The S transform is the inheritance and development of short-time Fourier transform and wavelet transform. It uses the Gaussian function, whose width is inversely proportional to the frequency as the window function. It has high-frequency resolution in low-frequency bands and high time resolution in high-frequency bands; thus, it is more suitable for feature extraction of non-linear and non-stationary signals. If $x[n/(NT)]$ is a discrete sampling sequence of $x(hT)$, the discrete S transform is:

$$\begin{cases} S\left[hT, \dfrac{n}{NT}\right] = \displaystyle\sum_{m=0}^{N-1} X\left[\dfrac{n}{NT}\right] e^{-\frac{2\pi^2 m^2}{n^2}} e^{h\frac{j2\pi m}{N}}, & (n \neq 0) \\ S\left[hT, 0\right] = \dfrac{1}{N} \displaystyle\sum_{k=0}^{N-1} x(kT), & (n = 0) \end{cases} \tag{17}$$

where h, m, and n range from 0 to N-1; N is the signal length, and $e^{-\frac{2\pi^2 m^2}{n^2}}$ is the Fourier spectrum of Gaussian window function.

Therefore, the time-frequency characteristic matrix $S\left[hT, \frac{n}{NT}\right]$ is the S transform result of the discrete signal $x[n/(NT)]$. The row of the matrix n/NT corresponds to the frequency sampling point, the column of the matrix hT corresponds to the time sampling point, and the matrix element contains the size and amplitude information of the corresponding sampling point.

As analyzed in Section II.B, when the frequency band is 500-1000Hz, the attenuation of measuring voltage and current is small. Therefore, the S transform selects the frequency band to process the voltage and current information. Then the S transform of the signal at time q is defined as:

$$S[p, q] = \sum_{p=500}^{p=1000} S(p, q) \tag{18}$$

in which, p and q are the frequency and time, respectively.

B. PROTECTION CRITERION

1) CRITERION OF FAULT DIRECTION

According to the discussion in Section II.A, for the forward PPF, the polarity of FD reactance is positive. Besides, the FD reactance and resistance values of the internal fault are all smaller than those of the external fault; for the backward PPF, the polarity of the measuring FD reactance is negative. The polarity difference of FD reactance is applied to determine the fault direction. Since the single frequency point is vulnerable to interference, the frequency band is chosen as 500Hz-1000Hz. When PPF occurs, the values of FD reactance at the two poles are the same. Therefore, the S-transformed FD reactance of any pole can be selected as the fault direction criterion:

$$XL_{mn} > 0 \tag{19}$$

$$Z_{mn} = \frac{1}{2} \frac{(2r_0 l_1 + 2j\omega l_0 l_1)(2R_g + \frac{1}{j\omega C_s} + j\omega L_s + 2j\omega L_B + 2r_0 l_1 + 2j\omega l_0 l_1)}{\frac{1}{j\omega C_s} + j\omega L_s + 2j\omega L_B + 2r_0 l_1 + 2j\omega l_0 l} \tag{16}$$

and,

$$XL_{mn} = im(\sum_{500}^{1000} \frac{S_{U_{mn}(p,q)}}{S_{I_{mn}(p,q)}}) \tag{20}$$

where XL_{mn} is the S-transformed FD reactance. When the S-transformed FD reactance satisfies Eq. (19), it is identified that the forward fault occurs at the measuring point MN; otherwise, it is a reverse fault.

2) CRITERIA OF FAULT IDENTIFICATION

When the forward fault occurs, the S-transformed FD resistance is selected as the fault identification criterion:

$$R_{mn} < k_{r1} R_{set} \tag{21}$$

and,

$$R_{mn} = real(\sum_{500}^{1000} \frac{S_{U_{mn}(p,q)}}{S_{I_{mn}(p,q)}}) \tag{22}$$

where, R_{mn} is the S-transformed FD resistance, k_{r1} is the reliability coefficient, and R_{set} is the setting threshold value.

According to Section II.C, the FD resistance is easily affected by a high resistance fault, while the FD reactance is less affected by fault resistance. Therefore, the S-transformed FD reactance is constructed as an auxiliary criterion. The combination of the two protection criteria can prevent the influence of the converter and high resistance fault on protection reliability. The FD reactance criterion is expressed as follows:

$$XL_{mn} < k_{r2} XL_{set} \tag{23}$$

where k_{r2} is the reliability coefficient, and XL_{set} is the setting threshold.

The setting principle of the FD impedance criterion at one terminal is as follows: the minimum FD impedance is selected when the forward external fault occurs. Generally, the near-end forward external fault has the minimum FD impedance. Thus, the setting value can be calculated. For the measuring point MN in Fig. 2, the minimum FD impedance is at the point f_2 in Fig. 2(b). Therefore, according to the equivalent line circuit, the setting values of FD reactance and resistance can be set as follows:

$$\begin{cases} XL_{set} = \omega l_0 L_{line} + \omega L_B \\ R_{set} = r_0 L_{line} \end{cases} \tag{24}$$

where, l_0, and r_0 are the inductance and resistance of unit length of line, *and* L_{line} is the line length.

C. PROTECTION SCHEME

Based on the above analysis, a pilot protection scheme based on the S-transformed FD impedance is proposed for a multi-terminal flexible DC distribution grid. The scheme is mainly composed of three parts: fault starting, fault direction discrimination, and fault identification. The flowchart of the protection for the single-side measuring point at the DC line is presented in Fig. 9, in which Part I and II are the parts of fault direction discrimination and fault identification, respectively.

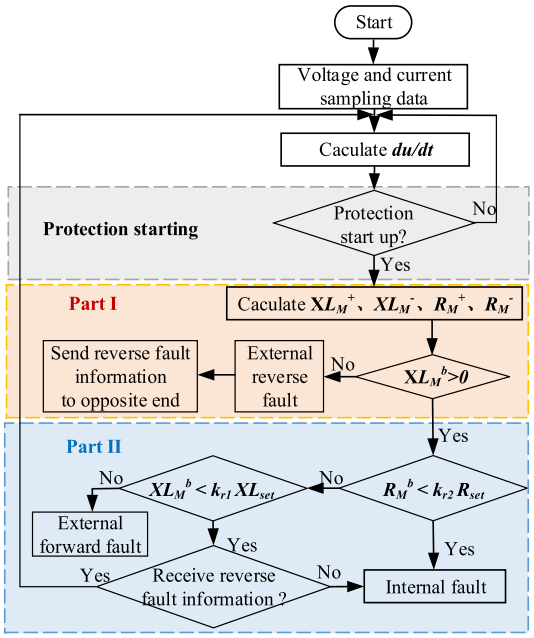

FIGURE 9. Protection flowchart for single-side measuring point of DC line.

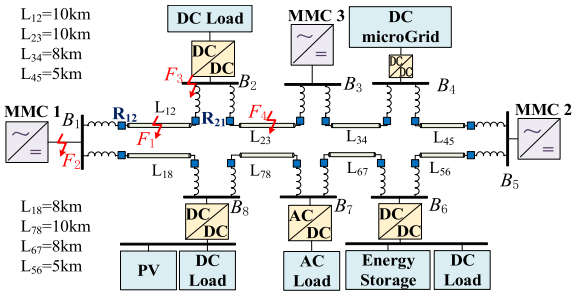

FIGURE 10. Single-line schematic diagram of three-terminal flexible DC distribution grid.

TABLE 3. Parameter values of converter.

Parameters	Values
Rated DC voltage/kV	10
Rated AC voltage /kV	110
Number of sub-modules in each bridge arm	21
CMI /mH	5
Sub-module capacitance/uF	6667

The main steps of the protection scheme are as follows:

1) FAULT STARTING

By referring to the experience of conventional DC line protection, the changing rate of the voltage is used as the protection starting criterion.

2) FAULT DIRECTION DISCRIMINATION

The polarity of the S-transformed FD reactance is detected. If $XL_{mn} > 0$, it is a forward fault; otherwise, it is an external

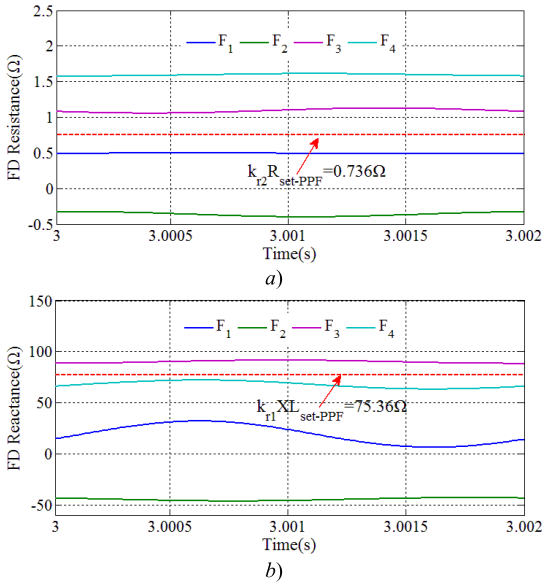

FIGURE 11. Simulation results at R_{12}: a) Simulations of FD resistance, b) Simulations of FD reactance.

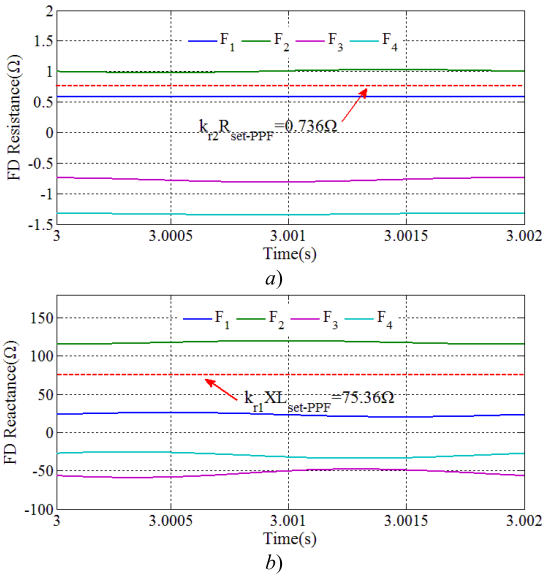

FIGURE 12. Simulation result at R_{21}: a) Simulations of FD resistance, b) Simulations of FD reactance.

reverse fault, and the logical signal of the reverse fault is sent to the protection unit at the opposite end.

3) FAULT IDENTIFICATION

For the forward fault, if $R_{mn} < k_{r1}R_{set}$, it is an internal fault (corresponding to the close-up fault); otherwise, the FD reactance of the fault pole is detected continuously. If it cannot meet the condition of $XL_{mn} < k_{r2}XL_{set}$, it is an external forward fault; otherwise, the protection unit will wait for the reverse fault signal from the opposite terminal. If the protection unit receives the signal, it is an external fault; otherwise, it is an internal fault.

IV. RESULTS AND ANALYSIS

A. SIMULATION MODEL

To verify the performance of the proposed protection scheme, a model of a three-terminal flexible DC distribution grid is constructed in PSCAD, as illustrated in Fig. 10, where blue blocks represent the relay. The parameters of the converter station are shown in Table 3. The model mainly includes an MMC converter, DC/DC converter, DC line and load. The DC side exchanges energy with the AC grid through the three MMC converter stations, and it is connected to the DC load by DC/DC converter. The symmetrical monopole wiring mode is adopted. To reduce the fault current, the MMC adopts the high resistance earthing mode on the DC side. Besides, in order to avoid the increase in insulation cost, long-time operation is not allowed when the SPGF occurs. The system applies a master-slave control mode. The cable is chosen for the DC distribution line, which is separated into 8 parts, and each part is equipped with a protection unit at both terminals.

As shown in Fig.10, we take the protection units $R_{12}$and R_{21}on line L_{12} as an example to verify the feasibility of the proposed protection. The sampling frequency of the protection is 40kHz, and the time window is selected as 2ms after the fault occurs. According to Eq. (24), the setting thresholds XL_{set} and R_{set} of protection unit R_{12} and R_{21}can be obtained when fault at F_3occurs. Based on the line parameters shown in Table 1, the setting thresholds XL_{set} and R_{set} are calculated as 94.2Ω and 0.92Ω, respectively. The reliability coefficients k_{r1} and k_{r2} are taken as 0.8, considering the measurement error and certain margin.

B. SIMULATION ANALYSIS

1) SIMULATIONS OF TYPICAL FAULT

To verify the analysis in Section II, different faults are set in the simulation model. As shown in Fig. 10, the internal fault is set at the midpoint F_1 of line L_{12}, and the external faults are set at F_2, F_3, and F_4. All the faults are metallic.

The simulation results of the S-transformed FD reactance and resistance at R_{12} and R_{21} are shown in Figs. 11 and 12, respectively. It can be seen that when the fault occurs at F_1, the polarities of the FD reactance detected by $R_{12}$and $R_{21}$are both positive. Besides, the values of FD resistance are all smaller than the threshold. It can be judged that the fault is internal fault for $R_{12}$and R_{21}. When the fault occurs at F_2, the polarity of the FD reactance at $R_{12}$is negative and positive at R_{21}; the value of the FD reactance and FD resistance at R_{21} are both larger than the threshold. Thus, the fault at F_2 can be assessed as forward external fault for R_{21}, and backward external fault for R_{12} separately. From Fig. 11, when the fault occurs at F_3, the polarity of the FD reactance is positive at R_{12}. Then, the fault is evaluated as reverse fault for R_{21}, and the reverse fault signal needs to send to R_{21}. Similarly, as shown in Fig. 12, the fault at F_3 can be judged as forward external fault.

As shown in Fig. 11, when the fault occurs at F_4, there is a DC/DC converter between the fault point and the measuring point. The FD reactance value at R_{12} is smaller than the

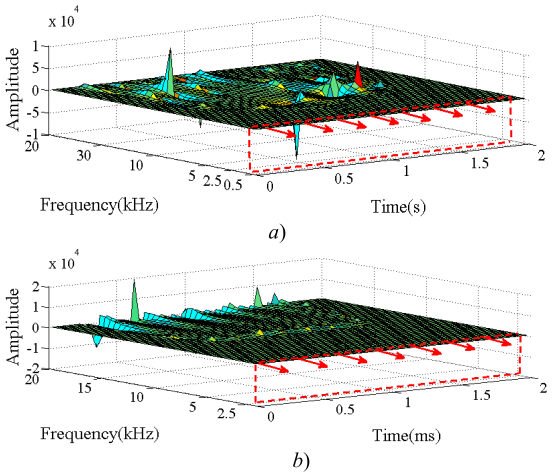

FIGURE 13. Simulation results of full frequency band at R_{12}: a) Simulation of FD reactance. b) Simulation of FD resistance.

TABLE 4. Simulation results with different fault resistances.

Fault resistance (Ω)	Protection unit	X_{fm} (Ω)	R_{fm} (Ω)	Identification Result
10	R_{12}	25.87	0.79	Internal fault
10	R_{21}	25.31	0.66	
30	R_{12}	25.11	1.69	Internal fault
30	R_{21}	24.58	1.32	
50	R_{12}	24.33	8.03	Internal fault
50	R_{21}	24.02	7.59	

TABLE 5. Simulation results when $L_B = 15mH$.

Fault point	Protection unit	R_{fm} (Ω)	X_{fm} (Ω)	Identification Result
F_1	R_{12}	0.64	25.12	Internal fault
F_1	R_{21}	0.77	27.34	
F_2	R_{12}	-0.41	-135.01	Backward
F_2	R_{21}	1.53	195.32	external fault
F_3	R_{12}	1.46	181.52	Forward external
F_3	R_{21}	-0.63	-119.38	fault

threshold, which is different from the fault at F_3. However, the value of FD resistance is larger than the setting value at R_{12}, and there is no reverse fault signal received at R_{21}, as shown in Fig. 12. Therefore, it can be concluded that the external fault occurs at $F_4$for $R_{12}$and R_{21}. Hence, the proposed protection scheme could accurately identify the fault section.

2) SIMULATIONS OF FULL FREQUENCY BAND

The PPF at point F_3 is taken as an example to verify the influence of frequency on the proposed protection. As shown in Fig. 13, the FD reactance and resistance at R_{12} in the full frequency band are simulated in a three-dimensional diagram. It can be seen that with the increase in frequency, the FD reactance has different degrees of peaks and troughs at different time points. Also, the FD resistance value is less affected by the frequency change. The amplitudes of the FD reactance and resistance are relatively stable under the frequency band

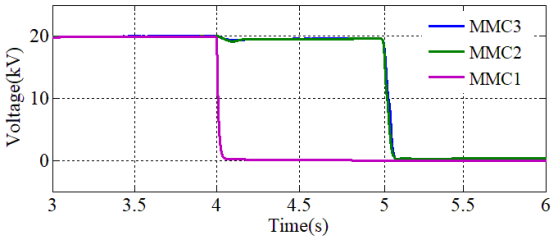

FIGURE 14. Voltage waveform when MMC exits operation.

TABLE 6. Simulation results when MMC exits operation.

Fault point	Protection unit	R_{fm} (Ω)	X_{fm} (Ω)	Identification Result
F_1	R_{12}	0.39	23.13	Internal fault
F_1	R_{21}	0.55	24.56	
F_2	R_{12}	-0.21	-41.23	Backward
F_2	R_{21}	1.13	115.37	external fault
F_3	R_{12}	1.09	82.17	Forward external
F_3	R_{12}	-0.69	-49.81	fault

of 1000 Hz, which is in agreement with the previous theoretical analysis. Therefore, the selected frequency band from 500 Hz to 1000 Hz is suitable for the proposed protection scheme.

C. PERFORMANCE OF PROPOSED PROTECTION

1) INFLUENCE OF FAULT RESISTANCE

The maximum fault resistance of the PPF in the flexible DC grid is about 50Ω. In order to analyze the sensitivity of the proposed protection with high resistance fault, PPFs with fault resistances of 10, 30, and 50Ω are set at F_1, as shown in Fig.10. The simulation results at R_{12} and $R_{21}$are shown in Table 4, in which the average value is within 2 ms. As shown in Table 4, the FD resistance increases and is much larger than the threshold when compared with the value in Figs.11 and 12. Although the value of FD reactance also becomes larger, it is far less than the threshold. Therefore, the FD resistance criterion has the problem of protection misoperation for the internal fault with high resistance, but the FD reactance criterion can be used for accurate identification.

2) INFLUENCE OF THE CLI

To investigate the influence of the CLI on the proposed protection, the inductance is set at 15mH, and other parameters remain unchanged. As shown in Table 5, when the fault occurs in F_1, F_2, and F_3, the FD resistance and reactance increase with the increase of CLI as compared with the values in Figs.10 and 12. Meanwhile, the FD reactance and resistance of the internal fault are smaller than those of the external fault, and the FD reactance of the reverse fault is less than zero; this is consistent with the PPF characteristics of the previous analysis. Due to the increase of CLI, the FD reactance and resistance of near-end forward external PPF increase. The threshold value of the protection criterion should be changed adaptively according to Eq. (24).

3) INFLUENCE OF DIFFERENT OPERATION CONDITIONS

When the MMC in a multi-terminal flexible DC distribution grid is out of operation due to a fault or maintenance, the other converters can maintain the normal operation. To investigate the adaptability of the proposed protection method, MMC1 exits operation, and the faults are set at F_1-F_3, as shown in Fig.10. The voltage waveform at the exit of each converter is shown in Fig. 14. MMC1 exits operation at 4s, and PPF occurs at 5s. To maintain the voltage balance, the MMC2 changes the control mode into constant voltage, since the control mode of the MMC1 is constant voltage. As shown in Fig. 14, the voltage can remain unchanged after the MMC1 quits from the system. The simulation results at R_{12} and R_{21} are shown in Table 6. It can be shown from the table that the protection can identify the fault effectively in this operating condition.

4) COMPARISON

The proposed protection method is compared with the conventional current differential protection to highlight its advantages. The current differential protection has been studied more in the DC micro-grid and distribution network [10], [32]. However, the current differential protection has the problem of data synchronization. Besides, the fault resistance will reduce the sensitivity of the current differential protection.

To obtain strict synchronization, the GPS clock is widely used to ensure data synchronization in the transmission line. The unit price of a high-quality GPS receiver is about $100, and the unit price of a chip-scale atomic clock is more than $2500 [33]. Thus, for the three-terminal flexible DC distribution grid, as shown in Fig.10, the additional cost for synchronization equipment will be up to $41600. Therefore, the cost of differential current protection in engineering is very high. The proposed protection only sends the logical signal of reverse fault to the opposite end, and needs no data synchronization. Then the investment in synchronization equipment can be saved, and the protection can be realized at a relatively low cost.

To analyze the influence of the fault resistance on the current differential protection, the internal fault $F_1$is set at the midpoint of line L_{12}, and the fault resistance is 75Ω, as shown in Fig.10. The simulation result of differential current is 0.18kA, and the restraint current is 0.21kA, in which the restraint coefficient is set as 0.5. It can be obtained that the differential current is smaller than the restraint current, and the protection cannot identify the internal fault. Therefore, the fault resistance affects the sensitivity of the current differential protection. The proposed protection has high reliability, which applies the FD reactance criterion to cope with the influence of fault resistance.

V. CONCLUSION

An FD impedance-based protection scheme is proposed for a flexible DC distribution grid. The polarity of FD reactance is used as the direction criterion, and the values of FD reactance and resistance are used as fault identification criteria. Then, the corresponding protection scheme is formed.

The proposed protection can quickly identify the fault close to the protection unit by using local information. For the remote-end or high resistance faults, the proposed pilot protection criterion combined by the local information and the logical signal from the opposite side can cope with the influence of converter and fault resistance on the protection reliability. Compared with the conventional current differential protection, the protection needs no data synchronization and is robust with fault resistance, which has great reliability and selectivity. Besides, the fault identification can be realized quickly and accurately within 3-4ms (considering the communication delay time is 1-2ms).

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