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RESEARCH ARTICLE

Modeling and Suppression of the Crosstalk Issue Considering the Influence of the Parasitic Parameters of SiC MOSFETs

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ABSTRACT Due to the extremely fast switching speed of the SiC MOSFET, its crosstalk issue is more serious than that of the Si IGBT. Therefore, in order to ensure the reliability of the SiC MOSFET converters, the crosstalk problem must be solved firstly. Most of the existing crosstalk suppression methods are aimed at decreasing the crosstalk voltage introduced by the parasitic gate-drain capacitance (Miller capacitance), ignoring the influence of other parasitic parameters on the crosstalk voltage, such as the common source inductance, which may also lead to more serious reliability problems. Thus, this paper firstly establishes the mathematical model of the switching process of the SiC MOSFET half-bridge inverter. Then, the effects of various parasitic parameters (the gate-source capacitance, the gate-drain capacitance, the common source inductance, the gate inductance, the drain inductance) on the crosstalk voltage are analyzed and modeled in detail, which is verified by experiments. Based on the analyses and models, a novel crosstalk voltage suppression circuit is proposed, which can not only suppress the crosstalk caused by the gate-drain capacitance, but also solve the crosstalk issue considering the influence of other parasitic parameters, such as the common source inductance. Finally, a double pulse test platform is established to verify the effectiveness of the designed crosstalk suppression circuit under different voltage/current conditions.

INDEX TERMS SiC MOSFET, crosstalk, parasitic parameter, Miller capacitance, common source inductance, crosstalk suppression circuit.

I. INTRODUCTION

Today, the wide bandgap semiconductor devices, silicon carbide (SiC) MOSFETs, are gradually widely used in high voltage, high capacity and high switching frequency converters. They bring a lot of performance improvements to converters, but also some more serious reliability problems, such as the crosstalk issue [1], [2], [3]. On the one hand, the large *di/dt* and *dv/dt* of the SiC MOSFET will increase the level of the crosstalk issue [4] On the other hand, the threshold voltage of the SiC MOSFET is lower and the maximum allowable negative voltage value is smaller, which means the smaller safety zone of the gate-source voltage of the SiC MOSFET [5], [6]. So, the traditional crosstalk suppression method which is widely used in the Si IGBT cannot be applied to the SiC MOSFET directly [5]. Moreover, because of the large *di/dt* and *dv/dt* when the SiC MOSFET switches, the influence of the parasitic parameters, such as the common source inductance, on the crosstalk issue becomes more and more obvious [7]. Thus, how to suppress the crosstalk of

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the SiC MOSFET in a better way, especially considering various parasitic parameters, becomes a focus in academia and industry [8], [9].

At present, some crosstalk suppression methods have been proposed. The simplest method is to increase the drive resistance of the SiC MOSFET, which can reduce the *di/dt* and *dv/dt* by slowing down the switching speed of the active SiC MOSFET [10]. The effect of this method is not good because the large drive resistance also increases the crosstalk voltage value of the disturbed SiC MOSFET [11]. For this reason, the unidirectional conduction performance of the diode is used to create two resistance paths for turn-on and turn-off in [12] and split output drivers are used to design turn-on resistance and turn-off resistance respectively in [13]. They can improve the crosstalk suppression effect but will lead to the increase of the switching loss because of the large drive resistance. Except for increasing the drive resistance, the second kind of the method is to increase the value of the negative voltage of the driver. In [14], a diode and a capacitor are connected in parallel to generate a larger turn-off voltage. Although it can prevent false turn-on of the switch, the risk of reverse breakdown of the gate insulation layer will increase [15]. Thus, passive resonant level shifters are used to suppress the positive and negative crosstalk voltage [16]. This method suppresses crosstalk by decreasing the turn-off voltage of devices when it is suffered to the positive crosstalk. Correspondingly, the method suppresses crosstalk by increasing the turn-off voltage of devices when it is suffered to the negative crosstalk. The passive resonant circuit is composed of passive components only, so the system reliability is not good. Active components are used to adjust the gate level of devices [17], [18], [19], [20], [21], [22]. The negative feedback control method can automatically adjust the gate-source voltage of the devices, but the design is difficult [23]. The third kind of the method is the Miller clamp method, which suppresses the crosstalk voltage by connecting additional capacitances in parallel between the gate and source of the SiC MOSFETs. Because directly connecting capacitances in parallel will increase the switching loss, auxiliary switches or auxiliary transistors are used to control the connection timing of the additional capacitances, which does not affect the switching speed of the active switch, and can achieve the effect of suppressing the gate crosstalk voltage of the disturbed SiC MOSFET [24], [25], [26], [27]. A passive suppression method with a gate-parallel diode is adopted, which can suppress crosstalk effectively. However, high performance of components is required [28].

Most of the existing SiC MOSFET crosstalk suppression methods are only aimed at the crosstalk voltage caused by the gate-drain capacitance. The impedance of the drive loop of the disturbed SiC MOSFET is mostly low in these methods. However, some current researches indicate that the expected suppression result cannot be obtained by merely reducing the impedance of the drive loop. Even the opposite effect occurs because there are other parasitic parameters that have a great impact on the gate-source voltage in the half-bridge, such as

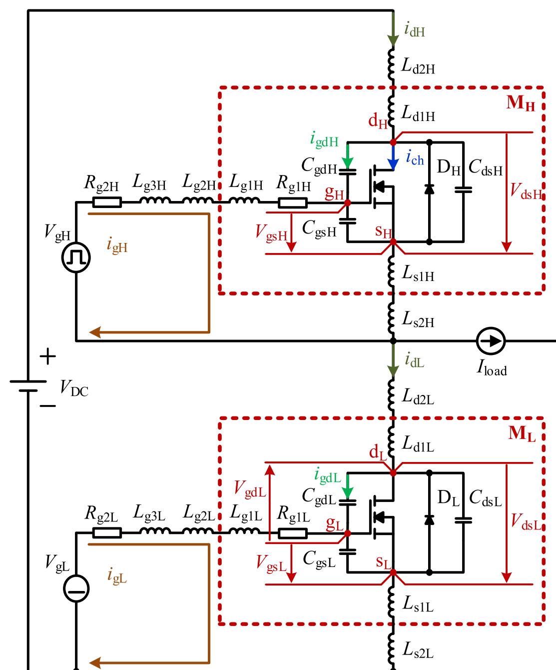

FIGURE 1. Double-pulse test circuit containing various parasitic parameters.

the common source inductance [29]. There are few studies on crosstalk suppression circuits when the parasitic parameters are considered. This paper analyzes the effects of various parasitic parameters on the crosstalk voltage in detail and proposes a reasonable, effective and easy-to-implement crosstalk suppression circuit, which can solve the crosstalk issue considering the influence of various parasitic parameters.

The structure of this paper is as follows: Second II analyzes models the relationship between each parasitic parameter and the crosstalk voltage. Section III proposes a novel crosstalk suppression circuit, which can automatically adjust the gate impedance when the various parasitic parameters are considered. The working principle and parameter design are discussed in detail in this section. Section IV verifies correctness of the established model and the effectiveness of the proposed crosstalk suppression circuit under different working conditions through experiments. Section V concludes the paper.

II. INFLUENCE OF VARIOUS PARASITIC PARAMETERS ON THE GATE SOURCE VOLTAGE OF THE SIC MOSFET

In order to analyze the relationship between parasitic parameters and the crosstalk issue, a double-pulse test circuit containing various parasitic parameters is shown in Figure 1. The detailed parasitic parameters inside of the SiC MOSFET (M_L) package are shown in red dotted box. The internal parasitic parameters of SiC MOSFET (M_L) include parasitic capacitances C_{gsL}, C_{gdL} and C_{dsL}, the parasitic inductance L_{g1L}, L_{d1L} and L_{s1L} on the bonding wires, and internal gate resistance R_{g1L}. L_{g2L}, L_{d2L}, and L_{s2L} are the parasitic inductance of the pins. The L_{g3L} is the parasitic inductance

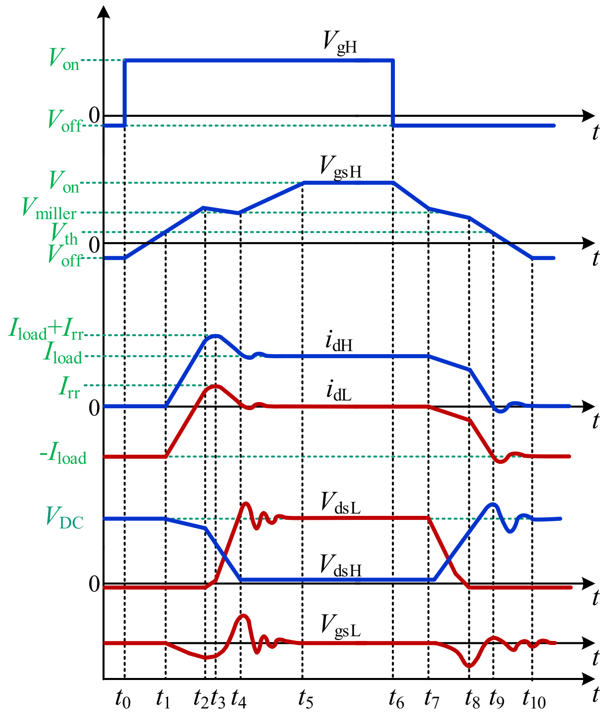

FIGURE 2. Switching waveforms during the turn-on and turn-off transition of the active switch M_H.

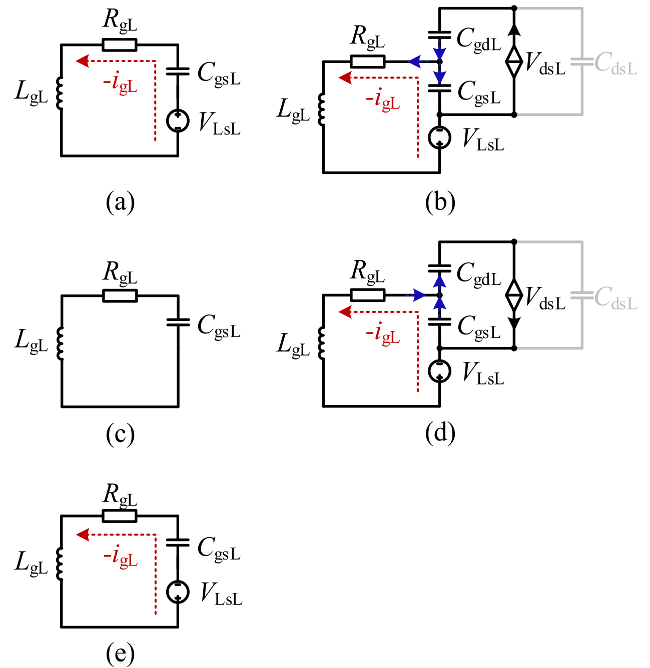

FIGURE 3. Equivalent circuit of M_L at each stage: (a) Stage 2 [t_1-t_2], (b) Stage 4 [t_3-t_4], (c) Stage 6 [t_5-t_6], (d) Stage 8 [t_7-t_8], (e) Stage 9 [t_8-t_9].

of the drive loop and D_L is a body diode. In addition, additional gate resistance R_{g2L} will be set in the drive loop to ensure the safety and reliability of the switching process.

Note that the parasitic parameters of M_H are similar to those of M_L and the reference directions of vector variables are shown in Figure 1. For the convenience of analyses, set $L_{gL} = L_{g1L} + L_{g2L} + L_{g3L}$, $L_{dL} = L_{d1L} + L_{d2L}$, $L_{sL} = L_{s1L} + L_{s2L}$, $R_{gL} = R_{g1L} + R_{g2L}$. In Figure 1, V_{gL}, i_{gdL}, i_{gL} and i_{dL} respectively represent the driver supply voltage, Miller current, gate currents, and drain currents of M_L. V_{gsL} is the gate-source voltage of M_L, which is the voltage between g_L and s_L. V_{gdL} is the gate-drain voltage of M_L, which is the voltage between g_L and d_L. V_{dsL} is the drain-source voltage of M_L, which is the voltage between d_L and s_L. Moreover, V_{DC} is the input voltage. I_{load} is the load current. i_{ch} is the channel current of M_H.

A. THE MATHEMATICAL MODEL OF V_{gsL} CONSIDERING VARIOUS PARASITIC PARAMETERS WHEN M_H TURNS ON

The piecewise linearized equivalent waveforms of the half-bridge inverter operation are shown in Figure 2. V_{on} represents high level and V_{off} represents low level.

Stage 1 [(t_0-t_1) in Figure 2]: At t_0, V_{gH} changes from the low level to the high level, and the gate current of M_H starts to charge C_{gsH} and C_{gdH}. Before V_{gsH} reaches the threshold voltage V_{th}, the drain-source voltage V_{dsL} and V_{dsH} remains unchanged and the drain current i_{dH} is zero because M_H is in OFF-state. There is no crosstalk phenomenon at this stage.

Stage 2 [(t_1-t_2) in Figure 2]: At t_1, V_{gsH} rises to V_{th} and M_H begins to turn on. The channel current i_{ch} of M_H increases from zero. At the same time, the amplitude of the current flowing through D_L decreases, which means that the positive increase of i_{dL}. Therefore, voltage induced on L_{sL} appears. V_{dsL} remains unchanged, resulting in that Miller current is not generated and the transfer current of C_{gdL} does not flow into C_{gsL}. Therefore, crosstalk is only affected by the induced voltage source $L_{sL}di_{dL}/dt$. During this stage, the V_{gsL} fluctuates negatively and the first negative spike appears.

The equivalent circuit of the driver of M_L in this stage is shown in Figure 3(a), and the circuit equation obtained as

$$V_{gsL} + L_{gL}\frac{di_{gL}}{dt} + R_{gL}i_{gL} + V_{LsL} = 0 \tag{1}$$

where

$$\begin{cases} i_{gL} = C_{gsL}\frac{dV_{gsL}}{dt} \\ V_{LsL} = L_{sL}\frac{di_{dL}}{dt} \end{cases} \tag{2}$$

Combining with (1) and (2), V_{gsL} can be expressed as

$$V_{gsL} = -V_{LsL} + \frac{V_{LsL}}{b_1 - a_1}\left(b_1 e^{-a_1\omega_1 t} - a_1 e^{-b_1\omega_1 t}\right) \tag{3}$$

where

$$\begin{cases} \omega_1 = \frac{1}{\sqrt{L_{gL}C_{gsL}}} \\ a_1 = \varepsilon_1 - \sqrt{\varepsilon_1^2 - 1} \\ b_1 = \varepsilon_1 + \sqrt{\varepsilon_1^2 - 1} \\ \varepsilon_1 = \frac{R_{gL}}{2}\sqrt{\frac{C_{gsL}}{L_{gL}}} \end{cases} \tag{4}$$

where ω_1 is the natural frequency, ε_1 is the damping coefficient. ε_1 increases with the increase of R_{gL} and C_{gsL}. Then, the changing rate of V_{gsL} in (3) slows down. When R_{gL} is large enough, the changing rate of V_{gsL} is close to zero, which means that V_{gsL} is maintained at the initial voltage. At this stage, the i_{dL} and i_{ch} can be expressed as

$$i_{\mathrm{dL}} = i_{\mathrm{ch}} - I_{\mathrm{load}} \tag{5}$$
$$i_{\mathrm{ch}} = g_{\mathrm{f}}\left(V_{\mathrm{gsH}} - V_{\mathrm{th}}\right) \tag{6}$$

g_{f} is the transconductance coefficient. Combining (2), (5) and (6), V_{LsL} can be represented as

$$V_{\mathrm{LsL}} = L_{\mathrm{sL}} g_{\mathrm{f}} \frac{dV_{\mathrm{gsH}}}{dt} \tag{7}$$

According to (7), V_{LsL} increases as L_{sL} or dV_{gsH}/dt increases, then V_{gsL} in (1) becomes larger negatively.

V_{gsH} can be obtained in [11]

$$V_{\mathrm{gsH}} = V_{\mathrm{gH}} - \frac{V_{\mathrm{gH}}}{b_2 - a_2}\left(b_2 e^{-a_2\omega_2 t} - a_2 e^{-b_2\omega_2 t}\right) \tag{8}$$

where

$$\begin{cases} \omega_1 = \dfrac{1}{\sqrt{\left(L_{\mathrm{gH}} L_{\mathrm{sH}}\right) C_{\mathrm{gsL}}}} \\ a_1 = \varepsilon_2 - \sqrt{\varepsilon_2^2 - 1} \\ b_1 = \varepsilon_2 + \sqrt{\varepsilon_2^2 - 1} \\ \varepsilon_2 = \dfrac{R_{\mathrm{gH}}}{2}\sqrt{\dfrac{C_{\mathrm{gsH}}}{L_{\mathrm{gH}} + L_{\mathrm{sH}}}} + \dfrac{L_{\mathrm{sH}} g_{\mathrm{f}}}{2\sqrt{C_{\mathrm{gsH}}\left(L_{\mathrm{gH}} + L_{\mathrm{sH}}\right)}} \end{cases} \tag{9}$$

According to (9), ε_2 increases, as C_{gsH}, L_{sH} become larger, and then V_{gsL} increases slowly in the negative direction.

When the current in $\mathrm{D_L}$ drops to zero, the reverse recovery process begins. This stage ends when i_{dL} approaches to the peak value of the reverse recovery current of the body diode.

Stage 3 [(t_2-t_3) in Figure 2]: i_{dL} continues to rise on the basis of the previous stage, and this stage ends when i_{dL} reaches the peak value I_{rr}. During this stage, (1) and (2) is still correct, and di_{dL}/dt approximately satisfies (10) and rapidly closes to 0.

$$\frac{di_{\mathrm{dL}}}{dt} = \frac{2Q_{\mathrm{rs}}}{I_{\mathrm{rr}}^2} \tag{10}$$

where I_{rr} is the peak reverse recovery current of $\mathrm{D_L}$. Q_{rs} is the transfer charge of $\mathrm{D_L}$ in this stage.

During this stage, the changing rate of i_{dL} becomes slower, the effect of $L_{\mathrm{sL}} di_{\mathrm{dL}}/dt$ on crosstalk voltage becomes smaller, the waveform of V_{gsL} gets flatten.

Stage 4 [(t_3-t_4) in Figure 2]: At t_3, the blocking voltage of $\mathrm{D_L}$ starts to increase, resulting in the increase of V_{dsL}. As V_{dsL} increases, the Miller current flowing out of C_{gdL} increases, then the rising rate of V_{gsL} increases, which causes the positive fluctuation of V_{gsL}. The equivalent circuit of the driver of $\mathrm{M_L}$ is established in Figure 3(b). And the key equations can be listed as follows.

$$V_{\mathrm{gsL}} = V_{\mathrm{gdL}} + V_{\mathrm{dsL}} \tag{11}$$
$$i_{\mathrm{gL}} = C_{\mathrm{gsL}} \frac{dV_{\mathrm{gsL}}}{dt} + C_{\mathrm{gdL}} \frac{dV_{\mathrm{gdL}}}{dt} \tag{12}$$
$$i_{\mathrm{dL}} = C_{\mathrm{eqL}} \frac{dV_{\mathrm{dsL}}}{dt} \tag{13}$$

where C_{eqL} is the equivalent capacitance of $\mathrm{M_L}$. Combined with (1), (11)-(13), the expression of V_{gsL} can be gotten as

$$V_{\mathrm{gsL}} = V_{\mathrm{c}} - \frac{V_{\mathrm{c}}}{b_3 - a_3}\left(b_3 e^{-a_3\omega_3 t} - a_3 e^{-b_3\omega_3 t}\right) \tag{14}$$

where

$$\begin{cases} V_{\mathrm{c}} = \left(\dfrac{L_{\mathrm{gL}} C_{\mathrm{gdL}}}{C_{\mathrm{eqL}}} - L_{\mathrm{sL}}\right)\dfrac{di_{\mathrm{dL}}}{dt} + \dfrac{R_{\mathrm{gL}} C_{\mathrm{gdL}}}{C_{\mathrm{eqL}}} i_{\mathrm{dL}} \\ \omega_3 = \dfrac{1}{\sqrt{L_{\mathrm{gL}}\left(C_{\mathrm{gdL}} + C_{\mathrm{gsL}}\right)}} \\ a_3 = \varepsilon_3 - \sqrt{\varepsilon_3^2 - 1} \\ b_3 = \varepsilon_3 + \sqrt{\varepsilon_3^2 - 1} \\ \varepsilon_3 = \dfrac{R_{\mathrm{gL}}}{2}\sqrt{\dfrac{C_{\mathrm{gdL}} + C_{\mathrm{gsL}}}{L_{\mathrm{gL}}}} \end{cases} \tag{15}$$

According to (15), V_{c} becomes larger as R_{gL} increases, and then V_{gsL} expressed in (14) becomes larger. However, ε_3 becomes large with the increase of R_{gL}, which resulting the changing rate of V_{gsL} will decrease. Hence, the influence of R_{gL} on the amplitude of the V_{gsL} is uncertain. ε_3 becomes large with the increase of C_{gsL}, which resulting the changing rate of V_{gsL} will decrease. This stage ends when V_{dsL} rises to the bus voltage V_{DC}.

At this stage, i_{dL} drops from I_{rr} to 0, then induced voltage direction of $L_{\mathrm{sL}} di_{\mathrm{dL}}/dt$ changes, which is different from that in stage 2 and 3. The induced voltage source $L_{\mathrm{sL}} di_{\mathrm{dL}}/dt$ and induced current source $C_{\mathrm{gdL}} dV_{\mathrm{dsL}}/dt$ both lead to the positive fluctuation of V_{gsL}, which generates the first positive spike.

Stage 5 [(t_4-t_5) in Figure 2]: At t_4, V_{gsH} continues to rise, and this stage ends when V_{gsH} equals to V_{on}. At this stage, the parasitic inductance of the power loop begins to cause the oscillation of V_{dsL}.

Stage 6 [(t_5-t_6) in Figure 2]: At t_5, the turn-on process of $\mathrm{M_H}$ ends and the circuit enters a steady state. The equivalent circuit of the driver of $\mathrm{M_L}$ is shown in Figure 3(c).

In conclusion, during the turn-on process of $\mathrm{M_H}$, the induced voltage of L_{sL} aggravate the fluctuation of crosstalk voltage.

B. THE MATHEMATICAL MODEL OF V_{gsL} CONSIDERING VARIOUS PARASITIC PARAMETERS WHEN $\mathrm{M_H}$ TURNS OFF

Stage 7 [(t_6-t_7) in Figure 2]: At t_6, V_{gH} changes from the high level to the low level, and C_{gsH} discharges through the drive loop. Before V_{gsH} drops to V_{th}, $\mathrm{M_H}$ is in a saturated conduction state, and V_{dsH}, V_{dsL} and i_{dL} remain unchanged. There is no crosstalk phenomenon at this stage. This stage ends when V_{gsH} falls below V_{miller}.

Stage 8 [(t_7-t_8) in Figure 2]: At t_7, V_{gsH} drops below V_{miller}, and the on-state resistance of $\mathrm{M_H}$ rapidly increases, causing V_{dsH} to rise and V_{dsL} to fall. As shown in Figure 3(d),

the decrease of V_{dsL} causes the generation of Miller current and part of the Miller current flow through C_{gsL}, which causes V_{gsL} to fluctuate negatively. In addition, the impedance of M_H increases, causing a little amount of current I_{load} to flow through the D_L and then i_{dL} increases in negative direction. The positive direction of $L_{sL}di_{dL}/dt$ is downward and $L_{sL}di_{dL}/dt$ induces V_{gsL} to fluctuate positively. At this stage, the effects of $L_{sL}di_{dL}/dt$ and $C_{gdL}dV_{dsL}/dt$ on V_{gsL} are contradictory. If the effect of $C_{gdL}dV_{dsL}/dt$ on V_{gsL} is dominant, the V_{gsL} negatively fluctuate. When the effect of $L_{sL}di_{dL}/dt$ is dominant on V_{gsL}, the V_{gsL} positively fluctuate.

Stage 9 [(t_8-t_9) in Figure 2]: When V_{dsL} drops to the on-state voltage of the D_L and V_{dsL} remains unchanged. The current I_{load} begins to divert from the channel of M_H to D_L. i_{dL} increases rapidly in the negative direction. However, V_{dsL} tends to be steady, and there is no Miller current flowing out of C_{gdL}. The V_{gsL} is affected by $L_{sL}di_{dL}/dt$ alone. The direction of current of $L_{sL}di_{dL}/dt$ is the same as stage 8, and V_{gsL} increases positively. The equivalent circuit of V_{gsL} in this stage is shown in Figure 3(e). The circuit equation of V_{gsL} is the same as that in the stage 2, but $di_{dL}/dt<0$. In stage 9, the relevant parasitic parameters affected V_{gsL} in the same way as in stage 2.

Stage 10 [(t_9-t_{10}) in Figure 2]: At t_9, V_{gsH} drops to V_{th}, and the channel of M_H is turned off. V_{gsL} oscillates due to parasitic inductance and parasitic capacitance. The reason for the oscillation is the same as in stage 5. This stage ends when V_{gsH} falls to zero.

Stage 11 [(t_{10}-) in Figure 2]: At t_{10}, the turn-off process of M_H ends and the circuit is in a steady state.

In conclusion, in stage 2 and 9, L_{sL} affects crosstalk voltage V_{gsL} alone. In stage 4 and 8, the parasitic parameters L_{sL} and C_{gdL} affect V_{gsL}.

III. PROPOSAL OF THE CROSSTALK SUPPRESSION CIRCUIT

According to the analyses in stage 2 during the turn-on process of M_H in Section II, the increase of R_{gL} can reduce the influence of the induced voltage of L_{sL} on the crosstalk. In stage 4 during the turn-on process of M_H, the fluctuation direction of V_{gsL} is positive. In this paper, the high gate impedance of M_L combined with negative-level OFF-state voltage is proposed and used to suppress the crosstalk voltage during the turn-on process of M_H. The high gate impedance of M_L is used to weakens the effect of L_{sL}, which induces V_{gsL} to fluctuate negatively. Then negative-level OFF-state voltage is used to restrain the influence of C_{gdL}, which induces V_{gsL} to fluctuate positively.

Note that the high gate impedance of M_L means that the gate-source of M_L is equivalent to the open-circuit state.

During the turn-off process of M_H, the direction where V_{gsL} fluctuates is mainly depended on the balance between the Miller current of C_{gdL} and the induced voltage on L_{sL}. Changing the impedance R_{gL} of the drive loop will change the balance. In this paper, additional impedance branch combined with zero-level OFF-state voltage is proposed and used to

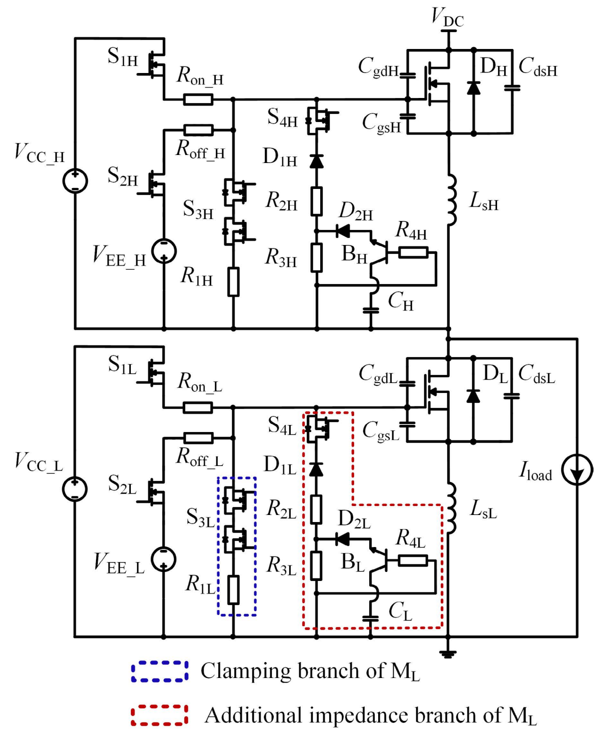

FIGURE 4. Proposed active crosstalk suppression circuit for SiC MOSFETs.

suppress the crosstalk voltage during the turn-off process of M_H. The specific circuit design is shown in Figure 4. The clamping branch of M_L consists of S_{3L} and R_{1L}. The clamping branch can adjust the off-state voltage of the SiC MOSFET during the turn-on and turn-off process of M_H. The additional impedance branch of M_L consists of S_{4L}, resistance R_{2L}, R_{3L} and R_{3L}. diodes D_{1L} and D_{2L}, and transistor B_L. In addition, the resistance R_{4L} whose value is 0Ω is connected in series at the base of B_L to suppress high-frequency noise. The additional impedance branch can automatically adjust the drive loop impedance of M_H during the turn-off process of M_H so that it suppresses the crosstalk voltage caused by L_{sL} and C_{gdL}.

As shown in Figure 4, V_{CC_L} and V_{EE_L} represent driving voltages. V_{CC_L} provides positive driving voltage for M_L, and V_{EE_L} provides negative driving voltage for M_L. Note that when V_{EE_L} provides a negative driving voltage for M_L, V_{gsL} is equal to $-V_{EE_L}$. To make gate loop in the high impedance state, the drain of the MOS devices S_{4L} is connected to the cathode of additional diode D_{1L}. When the MOS device S_{4L} is turned off, the additional impedance branch becomes high impedance. The S_{3L} is dual-channel MOS where the MOS devices inside of it are connected by source-source. When S_{3L} is turned off, the clamping branch becomes high impedance.

Note that the design of the gate loop of M_H are similar to those of M_L. For the convenience of discussion, the clamping branch and the additional impedance branch mentioned below all refer to those of M_L. unless stated otherwise.

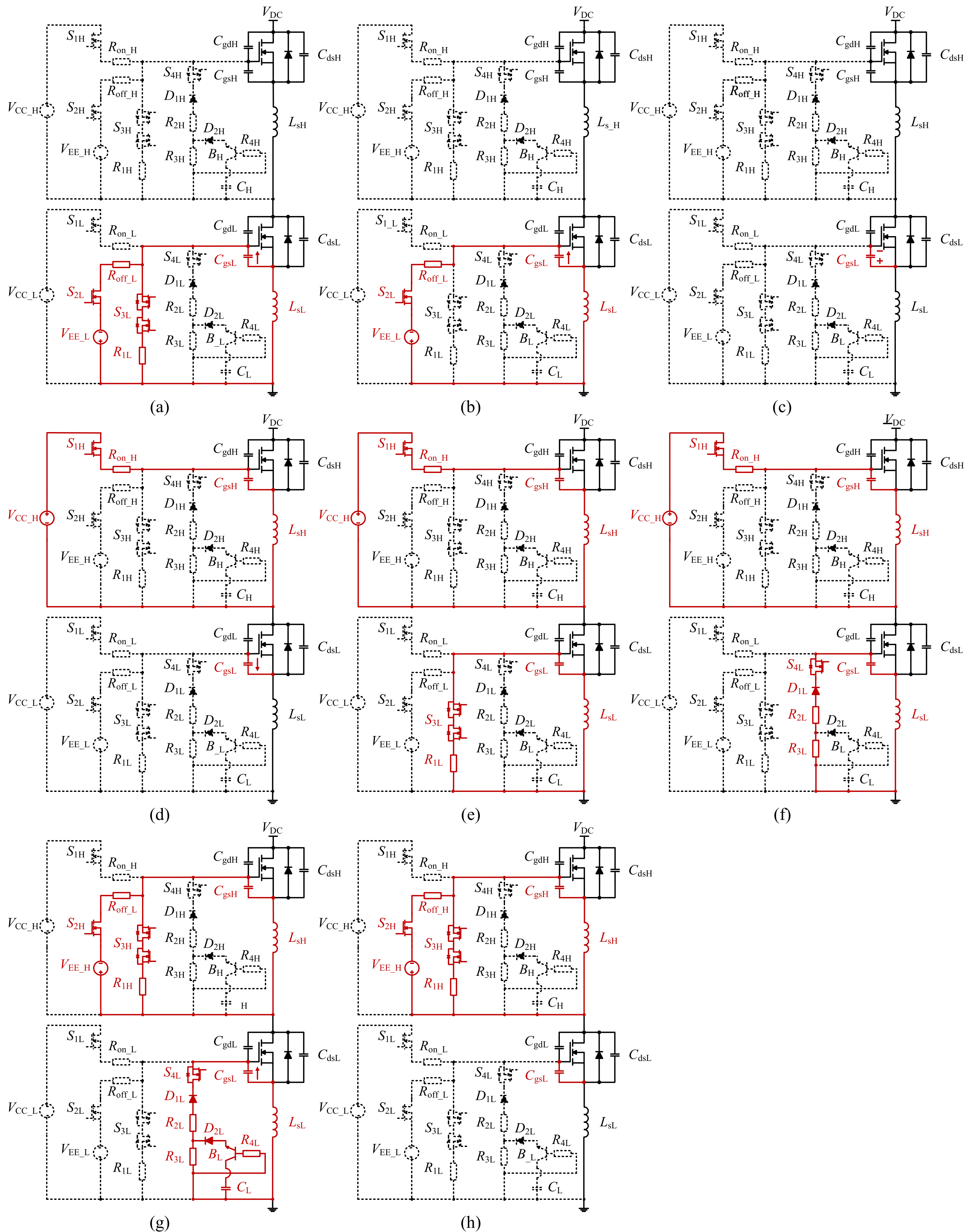

FIGURE 5. Equivalent circuit of the proposed crosstalk suppression circuit in each stage: (a) Stage 1 [before t1], (b) Stage 2 [t1-t2], (c) Stage 3 [t2-t3], (d) Stage 4 [t3-t4], (e) Stage 5 [t4-t5], (f) Stage 6 [t5-t6], (g) Stage 7 [t6-t7], (h) Stage 8 [t7-t8].

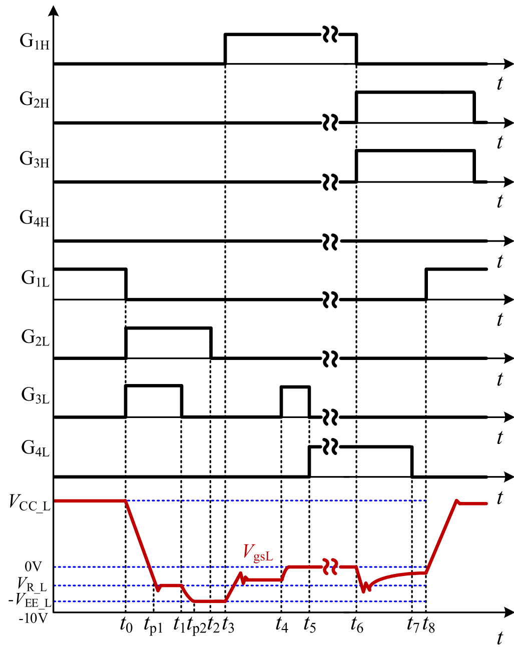

FIGURE 6. Logic signals of switches in driver.

A. ANALYSES OF THE WORKING PROCESS OF THE PROPOSED CIRCUIT

The working process of the drive circuit can be divided into 8 stages, as shown in Figure 5. G_{1H}, G_{2H}, G_{3H} and G_{4H} are the driving signals of the upper gate driver, and G_{1L}, G_{2L}, G_{3L} and G_{4L} are the driving signals of the lower gate driver. V_{R_L} is the recommended turn-off voltage. The logic signals of each stage are shown in Figure 6.

Stage 1 [(beforet_1) in Figure 6]: Before t_0, M_L is in ON-state and M_H is in OFF-state. As shown in Figure 5(a), at t_0, S_{1L} is turned off. S_{2L} and S_{3L} are turned on. M_L begins to turn off. S_{1H}, S_{2H}, S_{3H}, S_{4H} and S_{4L} are in OFF-state at the time. The time for V_{gsL} declining from V_{CC_L} (at t_0) to V_{R_L} (at t_{p1}) can be calculated by equation (16).

$$t_{VgsL1} = R_{g1L}C_{gsL}\ln\left(\frac{V_{R_L} - V_{CC_L}}{V_{R_L} - V_{tp1}}\right) \tag{16}$$

where V_{tp1} is the voltage of C_{gsL} at t_{p1}. The time from t_{p1} to t_1 is a time margin to make sure that the oscillation of V_{gsL} disappears. S_{3L} is turned off at t_1 and this stage ends, which is also the beginning of stage 2.

Stage 2 [(t_1-t_2) in Figure 6]: The equivalent circuit is shown in Figure 5(b). M_H and M_L are in OFF-state. At t_1, S_{1H}, S_{2H}, S_{3H}, S_{4H} S_{1L} and S_{4L} are still in OFF-state and S_{2L} remains ON-state, but S_{3L} is turned off at the time. V_{gsL} continues to be charged on the basis of V_{R_L}. According to equation (17), the time that the V_{gsL} decreases from V_{R_L} (at t_1) to -V_{EE_L} (at t_{p2}) can be obtained.

$$t_{VgsL2} = (R_{off_L} + R_{g1L})C_{gsL}\ln\left(\frac{-V_{EE_L} - V_{R_L}}{-V_{EE_L} - V_{tp2}}\right) \tag{17}$$

where V_{tp2} is the voltage of C_{gsL} at t_{p2}. S_{2L} is turn off after a time margin and this stage ends, which prepares for the suppression of crosstalk caused by the turn-on process of M_H.

Stage 3 [(t_2-t_3) in Figure 6]: The equivalent circuit is shown in Figure 5(c). M_H and M_L are in OFF-state. At t_2, the S_{2L} is turned off, and S_{1L}, S_{3L} and S_{4L} are in OFF-state. During this stage, S_{1H}, S_{2H}, S_{3H} and S_{4H} are still in OFF-state. All branches where S_{1L}, S_{2L}, S_{3L} and S_{4L} are located between gate and source of M_L are disconnected, and M_L is in the high gate impedance state. This stage ends when the S_{1H} is turned on.

Stage 4 [(t_3-t_4) in Figure 6]: The equivalent circuit is shown in Figure 5(d). M_L is still in OFF-state. At t_3, S_{1H} and M_H are turned on. S_{2H}, S_{3H}, S_{4H}, S_{1L}, S_{2L}, S_{3L} and S_{4L} are in OFF-state. Because M_L is in the high gate impedance, the L_{sL} is equivalent to be disconnected and the induced voltage on L_{sL} will not charge C_{gsL}. At this time, the Miller current of C_{gdL} only flows through C_{gsL} and the direction of Miller charge does not change, which induces V_{gsL} to fluctuate positively.

To prevent the positive crosstalk spike of V_{gsL} from exceeding the threshold voltage V_{th}, causing the false turn-on of M_L, C_{gsL} needs to be pre-charged by V_{EE_L} to counteract the influence of Miller current on C_{gsL}.

The charge flowing into C_{gsL} by C_{gdL} can be expressed as

$$Q_{gdL} = \int_0^{V_{gdL}} C_{gdL}(v)dv \tag{18}$$

The value of C_{gdL} can be obtained from data sheet [30]. V_{gdL} is approximately equal to V_{dsL}, so (18) can also be expressed as

$$Q_{gdL} = \int_0^{V_{dsL}} C_{gdL}(v)dv \tag{19}$$

Therefore, V_{EE_L} can be obtained as

$$V_{EE_L} = -k\left(V_{th} - \frac{Q_{gdL}}{C_{gsL}}\right) \tag{20}$$

In (20), the coefficient k is the margin to prevent the disturbance caused by the variation of the parameters and other factors. Let k equals 1.2 [29]. The minimum threshold voltage of C2M0160120D is 2V [30]. So, the V_{EE_L} is at least 5.9V under the condition of V_{DC} is 400V. However, when V_{EE_L} is 5.9V, M_L has the risk of breaking through the threshold voltage, so V_{EE_L} is finally set to 8V in this paper. According to the data sheet of C2M0160120D, the recommended off-state voltage is −5V and the maximum negative voltage is −10V. If the SiC MOSFET is turned off at −8V, there is a risk that the maximum negative voltage will be exceeded during the turn-off process of the M_L. Thus, it is necessary to make the off-state voltage of M_L reasonable by using clamping branch. Connected in the drive loop, the clamping branch can divide V_{EE_L} into the recommended turn-off voltage. R_{1L} should satisfy

$$\frac{R_{1L} + R_{S3L}}{R_{1L} + R_{S3L} + R_{off_L}} V_{EE_L} = 5V \tag{21}$$

where R_{off_L} can be set to 10Ω. The internal resistance of S_{3L} is 0.7Ω. According to (21), R_{1L} is 16Ω at this time.

In this stage, the duration time of crosstalk can be estimated according to turn-on delay time $t_{d(on)}$ and rise time t_r in datasheet of the selected SiC MOSFET. Considering a certain amount of time margin, S_{3L} is turned on after the crosstalk is finished. When S_{3L} is turned on, this stage ends.

Stage 5 [(t_4-t_5) in Figure 6]: The equivalent circuit is shown in Figure 5(e). M_H is in ON-state and M_L is in OFF-state. S_{3L} is turned on at t_4. S_{1H} is still in ON-state, and S_{2H}, S_{3H}, S_{4H}, S_{1L}, S_{2L} and S_{4L} are in OFF-state. After S_{3L} is turned on, C_{gsL} discharges through clamping branch of M_L. According to equation (22), the time C_{gsL} discharges to 0 is obtained.

$$t_{VgsL3} = (R_{1L} + R_{S3L})\, C_{gsL} \tag{22}$$

where R_{S3L} is the on-state resistance of S_{3L}. S_{3L} is turned off and S_{4L} is turned on when the discharge of C_{gsL} is finished, which means this stage ends.

Stage 6 [(t_5-t_6) in Figure 6]: The equivalent circuit is shown in Figure 5(f). This stage is a transitional stage. M_H is in ON-state and M_L is in OFF-state. S_{1H} is still in ON-state, and S_{2H}, S_{3H}, S_{4H}, S_{1L}, S_{2L} and S_{3L} are in OFF-state. S_{4L} is turned on to prepares to suppress the turn-off crosstalk voltage of M_H. The duration time of this stage is determined by the actual turn-off signal of active M_H.

Stage 7 [(t_6-t_7) in Figure 6]: The equivalent circuit is shown in Figure 5(g). M_L is still in OFF-state. At t_6, S_{1H} is turned off and S_{2H} and S_{3H} are turned on, then M_H is turned off. S_{4H}, S_{4L} is in ON-state and S_{1L}, S_{2L} and S_{3L} are in OFF-state. The crosstalk voltage of M_L is suppressed by the additional impedance branch. The suppression process and the design of its related parameters will be discussed in detail in Section III-B. The duration time of crosstalk can be estimated according to turn-off delay time $t_{d(off)}$ and fall time t_f in datasheet of the selected SiC MOSFETs. When crosstalk is finished, considering a time margin, S_{4L} is turned off and this stage ends.

Stage 8 [(t_7-t_8) in Figure 6]: The equivalent circuit is shown in Figure 5(h). M_H and M_L are in OFF-state. S_{2H} and S_{3H} are in ON-state. S_{1H}, S_{4H}, S_{1L}, S_{2L}, S_{3L} and S_{4L} are in OFF-state.

After a steady-state process, S_{1L} is turned on. S_{2H} and S_{3H} are turned off before S_{1L} is turned off again.

To display the switching time more clearly, the duration time of some stages is shown in Table 1.

TABLE 1. Duration time of some stages.

stage	duration time
t_0-t_1	$(2\sim3)\cdot t_{VgsL1}$
t_1-t_2	$(2\sim3)\cdot t_{VgsL2}$
t_2-t_3	/
t_3-t_4	$(5\sim10)\cdot(t_{d(on)}+t_r)$
t_4-t_5	$(1\sim2)\cdot t_{VgsL3}$
t_5-t_6	/
t_6-t_7	$(5\sim10)\cdot(t_{d(off)}+t_f)$
t_7-t_8	/

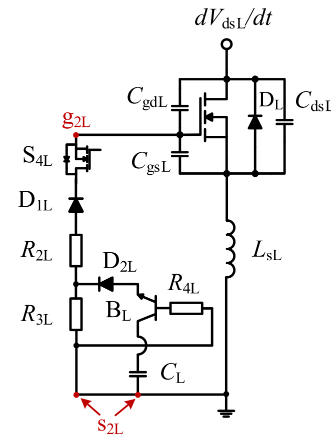

FIGURE 7. Schematic diagram of where the additional impedance branch is connected.

B. THE OPERATING PRINCIPLE OF THE ADDITIONAL IMPEDANCE BRANCH DURING THE TURN-OFF PROCESS OF M_H AND DESIGN OF ITS RELATED PARAMETERS

The C_{gsL} discharges to zero through the clamping branch before M_H is turned off, then the initial voltage of V_{gsL} is 0V. As shown in Figure 7, the additional impedance branch is connected at g_{2L} and S_{2L}. The impedance value of the branch is determined by V_{gs2L}, where V_{gs2L} is the voltage between g_{2L} and s_{2L}. During turn-off process of M_H, S_{4L} remains ON-state and the additional impedance branch begins to suppress crosstalk. Note that the loop where S_{1L} is located, the branch where S_{2L} is located and the clamping branch of M_L are all in open-circuit states at this time.

Stage 7-1: As shown in Figure 8(a), before V_{gs2L} drops to the ON-state voltage of D_{1L}, the additional impedance branch is equivalent to be in open-circuit states, which makes the gate impedance of M_L is in high impedance and the induced voltage source $L_{sL}di_{dL}/dt$ is disconnected. At this time, C_{gsL} is merely affected by the Miller current of C_{gdL} and V_{gsL} fluctuates negatively.

Stage 7-2: As shown in Figure 8(b), after D_{1L} is turned on, the gate resistance value of the drive loop of M_L in this stage is sum of R_{2L} and R_{3L}. At this time, R_{2L} and R_{3L} should be used to restrain the effect on C_{gsL} caused by $L_{sL}di_{dL}/dt$, which keeps V_{gsL} away from the threshold voltage. In this stage, the voltage between the two nodes of g_{2L} and s_{2L} is large enough to make D_{2L} and B_L conduct. When diode D_{2L} and transistor B_L are turned on and R_{3L} is bypassed by capacitance C_L, this stage ends.

As shown in Figure 9, when the sum of R_{2L} and R_{3L} gets larger, the positive voltage fluctuation is suppressed, but the negative voltage fluctuation of V_{gsL} becomes larger (as shown by the blue line). Therefore, the value of gate impedance

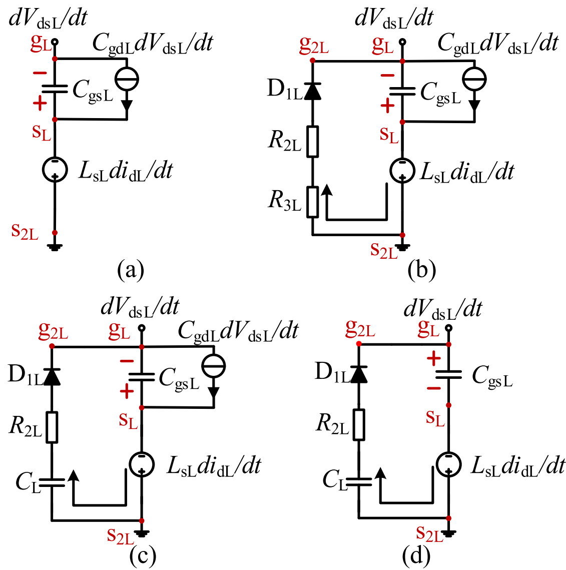

FIGURE 8. The flow chart when the additional impedance branch is used during the turn-off process of M_H: (a) Stage 7-1, (b) Stage 7-2, (c) Stage 7-3, (d) Stage 7-4.

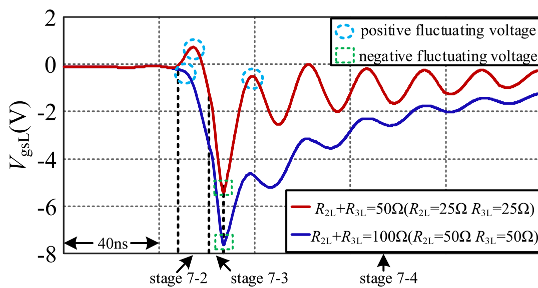

FIGURE 9. The effects of different impedance values of M_L on V_{gsL} when M_H is turned off.

of M_L should decrease when crosstalk voltage negatively fluctuates.

Stage 7-3: As shown in Figure 8(c), the gate resistance value of M_L at this stage becomes R_{2L}. The negative crosstalk voltage is further suppressed. In the experiments, the value of C_L is 10μF. To ensure the loop where C_L is located conducted, the value of R_{3L} should meet

$$\Delta V_{R3L} = \frac{-V_{gs2L} - 0.7\text{V}}{R_{2L} + R_{3L}} R_{3L} > 0.8\text{V} + 0.7\text{V} \quad (23)$$

where 0.8V is the base-emitter voltage of B_L and 0.7V is the ON-state voltage of D_{2L}. The on-state resistance of S_{4L} and D_{2L} can be ignored. When there is no Miller current flowing out of C_{gdL}, this stage ends.

Stage 7-4: As shown in Figure 8(d), V_{dsL} gradually becomes stable, and there is no more Miller current flowing out of C_{gdL}. The crosstalk voltage only depends on $L_{sL}di_{dL}/dt$ and V_{gsL} starts to fluctuate positively. When V_{gs2L} is smaller than ON-state voltage of D_{1L}, the induced voltage source $L_{sL}di_{dL}/dt$ is disconnected, which means the V_{gsL} is no longer

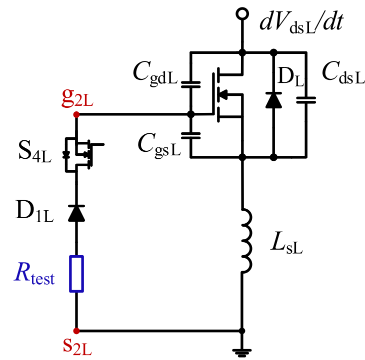

FIGURE 10. Schematic diagram of the turn-off test circuit under different working conditions.

affected by the induced voltage of L_{sL} and the crosstalk suppression during the M_H turn-off process ends.

In summary, when the impedance of the drive loop is the sum of R_{2L} and R_{3L}, the positive voltage fluctuation can be suppressed, and when the impedance of the drive loop is R_{2L}, the negative voltage fluctuation can be suppressed.

During the turn-off process of M_H, the gate impedance value of M_L is automatically adjustable. The location where the R_{test} is connected is shown in Figure 10. The R_{test} is used to obtain the minimum value of R_{2L} and the maximum value of the sum of R_{2L} and R_{3L}.

The minimum value of R_{2L} should satisfy the requirement that the maximum positive spike of crosstalk is smaller than the threshold voltage V_{th} under all operating conditions. The maximum value of the sum of R_{2L} and R_{3L} should ensure the value of negative voltage spike of V_{gsL} larger than the maximum allowable turn-off voltage of the SiC MOSFETs under all operating conditions.

According to the above requirements, the test results as follows: R_{2L} is at least set as 25Ω and the maximum value of the sum of R_{2L} and R_{3L} is 600Ω.

After determining the values of R_{2L} and R_{3L}, once the branch where C_L is connected, the crosstalk voltage will be restrained within the safety voltage range of SiC MOSFET during the turn-off process of M_H.

IV. EXPERIMENTAL VERIFICATION

To verify the influence of various parasitic parameters on the crosstalk and the effectiveness of the proposed crosstalk suppression circuit, the double-pulse test platform is built in the laboratory. The photo of the platform is shown in Figure 11.

Figure 11(a) shows the double-pulse test board, the additional impedance branch, the clamping branch, the FPGA control board, DC power supply, switching mode power supplies, downloader and oscilloscope. The FPGA control board can generate double pulse wave and the pulse signal that the additional impedance branch and clamping branch are needed. DC power supply is used to supply power to the additional impedance branch and camping branch. Switching

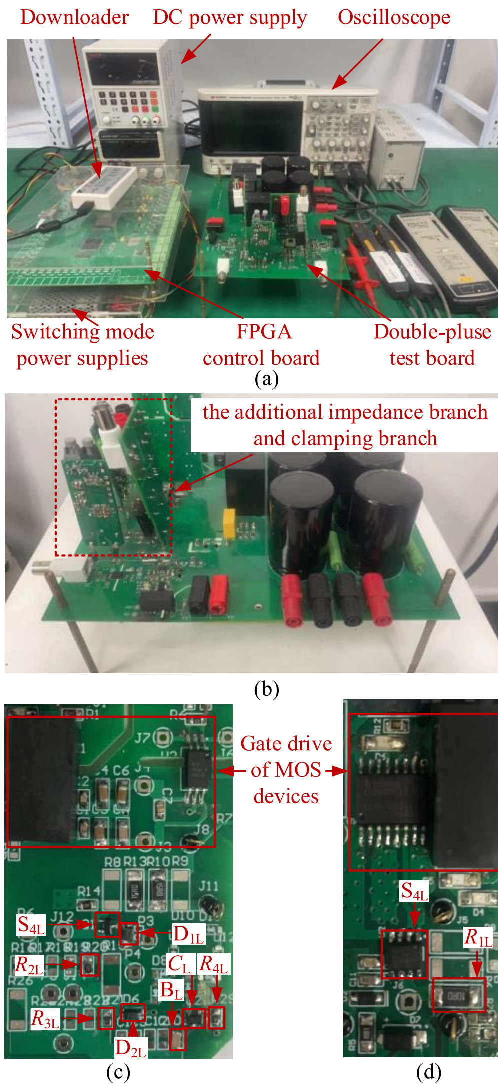

FIGURE 11. Experimental setup: (a) Overall view, (b) Double-pulse test platform, (c) Additional impedance branch of M_L, (d) Clamping branch of M_L.

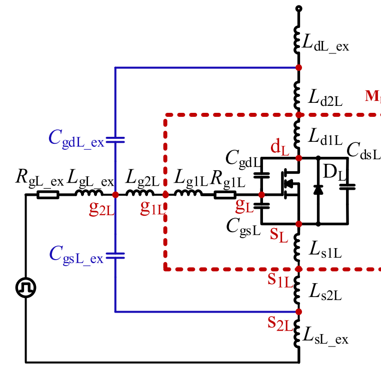

FIGURE 12. Actual position of parasitic parameters of M_L and the location of different voltage nodes.

mode power supplies are used to supply power to the control board. Figure 11(b) shows the details of the double pulse test board. Figure 11(c) and (d) respectively show the details of the additional impedance branch and the clamping branch of M_L. The SiC MOSFETs are C2M0160120D from Cree/Wolfspeed with TO247-3 package in the double-pulse test platform. In the experiment, the lower device M_L acts as the device under disturbance, and the upper device M_H is switching. The voltage and current waveforms are measured by the high bandwidth active voltage probe (TA042 from Pico), high bandwidth current probe (N2783B from Keysight) and the scope (InfiniiVision DSOX3024T from Keysight).

A. CROSSTALK WAVEFORM UNDER DIFFERENT PARASITIC PARAMETERS

The change of parasitic parameters may bring about a large oscillation, so the V_{DC} and I_{load} are set as 300V and 10A in the experiments to ensure that the value of crosstalk voltage of the SiC MOSFETs are within a safe voltage range. The paper conducts the experiments to verify the influence of various parasitic parameters ($L_{sH}, L_{sL}, L_{gH}, L_{gL}, L_{dH}, L_{dL}, C_{gsH}, C_{gsL}, C_{gdH}$ and C_{gdL}) on crosstalk during the turn-on and turn-off process of M_H.

The Figure 12 shows the actual position of added parasitic parameters of M_L and the location of different voltage nodes. The location of the added parasitic parameters of M_H is relative as M_L. Taking the L_{dL} for example, the value of L_{dL} changes by changing the value of added parasitic inductance L_{dL_ex}. At this time, the value of L_{dL} is updated to the sum of L_{d1L}, L_{d2L} and L_{dL_ex}.

Due to the limitation of packaging, the waveforms of V_{gsL} cannot be directly measured in the experiment. According to the experience of academia and the industry, the voltage test points can be selected as g_{1L} and s_{1L}, which is shown in Figure 12. Because g_{1L} and s_{1L} are close to the point g_L and s_L, the variation trend of V_{gsL} is consistent with that of V_{gs1L}. Thus, the waveforms of V_{gs1L} are used to analyze the relationship between parasitic parameters and crosstalk voltage [31].

The crosstalk waveforms of V_{gs1L} during the turn-on and turn-off process of M_H are shown in Figure 13. The first positive spike of V_{gs1L} is shown by the green dashed circle and the first negative spike of V_{gs1L} is shown by the light blue dashed circle. The amplitude of the first positive spike and the first negative spike of V_{gs1L} are marked in Figure 13(a) and (b). Note that the amplitude of first positive spike means the absolute value of the difference between the value of first positive spike and off-state voltage of SiC MOSFETs and the amplitude of first negative spike means the absolute value of the difference between the value of first positive spike and off-state voltage of SiC MOSFETs. The A_{n_on} means the amplitude of first negative spikes during the turn-on process of M_H and the A_{p_on} means the amplitude of first positive spikes during the turn-on process of M_H. The A_{n_off} means the amplitude of first negative spikes during the turn-off process of M_H and the A_{p_off} means the amplitude of first positive spikes during the turn-off process of M_H.

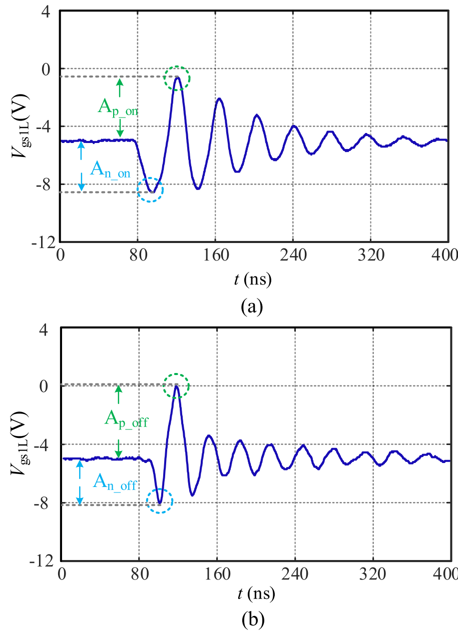

FIGURE 13. Typical measured waveforms of V_{gs1L} during the turn-on and turn-off process of M_H: (a) waveform of V_{gs1L} during the turn-on process of M_H, (b) waveform of V_{gs1L} during the turn-off process of M_H.

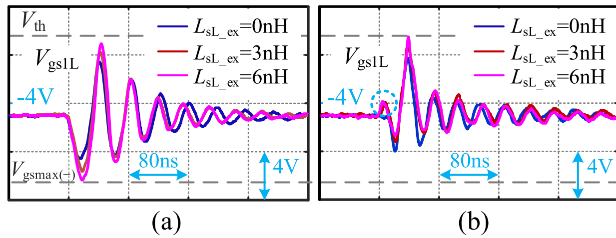

FIGURE 14. Measured crosstalk waveforms during the turn-on and turn-off process of M_H when L_{sL_ex} changes. (a) the waveforms of V_{gs1L} during the turn-on process of M_H, (b) the waveforms of V_{gs1L} during the turn-off process of M_H.

1) INFLUENCE OF THE PARASITIC INDUCTANCE ON CROSSTALK

According to the analyses in Section II and experiment results, parasitic inductance L_{sH} and L_{sL} have great effect on the crosstalk voltage.

The crosstalk waveforms during the turn-on and turn-off process of M_H are shown in Figure 14, when L_{sL} changes. The negative spikes firstly appear the waveforms of V_{gs1L}. The negative spikes are generated due to the charging of the C_{gsL} by the induced voltage on the L_{sL}. Meanwhile, as the L_{sL} increases, the crosstalk becomes more severe, which is shown in Fig 14(a). When L_{sL_ex} is 6nH, the first negative spike is very close to $V_{gsmax(-)}$ ($V_{gsmax(-)}$ is the maximum allowable negative voltage of the SiC MOSFET), which reduces reliability of SiC MOSFETs. This proves that L_{sL} is one of the main parasitic parameters that affecting crosstalk. With the increase of L_{sL}, the amplitude of first negative spike becomes larger. Because the induced voltage source

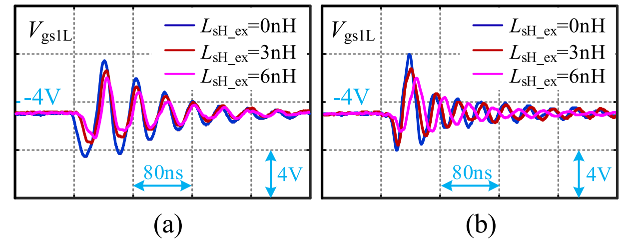

FIGURE 15. Measured crosstalk waveforms during the turn-on and turn-off process of M_H when L_{sH_ex} changes: (a) waveforms of V_{gs1L} during the turn-on process of M_H, (b) waveforms of V_{gs1L} during the turn-off process of M_H.

$L_{sL}di_{dL}/dt$ becomes larger when L_{sL} increases, the amplitude of first negative spike becoming larger. Moreover, with the increase of L_{sL}, the amplitude of first positive spike becomes larger. According to the analyses of stage 4 in Section II, i_{dL} decreases from the peak value of the reverse recovery current of D_L, then the direction of the induced voltage source $L_{sL}di_{dL}/dt$ changes and induces positive fluctuations of V_{gs1L}, which leads to the amplitude of the first positive spike becomes larger.

The Figure 14(b) shows the crosstalk waveforms during the turn-off process of M_H. There is a small positive spike before the first negative spike and the maximum positive spike appear in waveforms during the turn-off process of M_H. Note that the amplitude of the first positive spike refers to the amplitude of the maximum positive spike at this time. In this process, the main parasitic parameters affecting the crosstalk voltage waveform are L_{sL} and C_{gdL}, and the effects of L_{sL} and C_{gdL} on crosstalk voltage are contradictory. M_L is at risk of false turn-on when L_{sL_ex} is 6nH. As L_{sL} increases, the effect of L_{sL} on crosstalk is greater than that of C_{gdL}, which leads to the appearance of the first small positive spike. Then, the influence of C_{gdL} on the crosstalk is greater than that of L_{sL}, and the V_{gs1L} waveform begins to decrease. As L_{sL} increases, the effect of C_{gdL} on crosstalk is weakened, which makes the amplitude of first negative spikes smaller. Moreover, with increase of L_{sL}, the positive spike becomes larger as L_{sL} increases. The reason is the same as the turn-on of M_H. These results satisfy the analyses in section II.

The Figure 15(a) shows the crosstalk waveforms during the turn-on process of M_H when L_{sH} changes. The amplitude of the first negative spike decreases with the increase of L_{sH}. The reason is that increasing L_{sH} limits the changing of V_{gsH}, which causes the change of current flowing through L_{sL} to become slower. Thus, the induced voltage of the L_{sL} become smaller, reducing the effect on crosstalk voltage. The results satisfy (3) (7) (8) and (9) in Section II. When L_{sH} becomes larger, the amplitude of first positive spike becomes smaller. Because the changing rate of V_{dsL} decreases with the increase of L_{sH}, the Miller current flowing from C_{gdL} into C_{gsL} decreases, and the positive spike becomes smaller.

During the turn-off process of M_H, with the increase of L_{sH}, the amplitude of first negative spike becomes smaller,

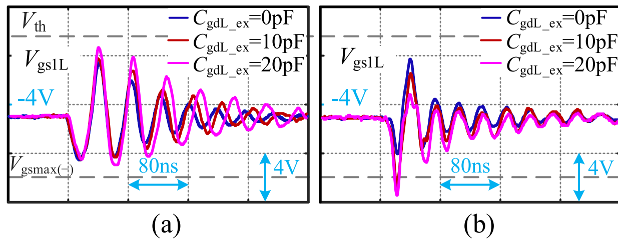

FIGURE 16. Measured crosstalk waveforms during the turn-on and turn-off process of M_H when L_{sH_ex} changes: (a) waveforms of V_{gs1L} during the turn-on process of M_H, (b) waveforms of V_{gs1L} during the turn-off process of M_H.

which is shown in Fig 15(b). The reason is as follows: as L_{sH} increases, the changing rate of V_{dsL} decreases, then Miller current becomes smaller. Hence, the amplitude of first negative spike becomes smaller. Meanwhile, with the increase of L_{sH}, the amplitude of first positive spike becomes smaller.

The other parasitic inductance L_{gH}, L_{gL}, L_{dH} and L_{dL} have little effect on the amplitude of spikes through experiments.

2) INFLUENCE OF THE PARASITIC CAPACITANCE ON CROSSTALK

The parasitic capacitance C_{gdL} and C_{gsL} have great effect on crosstalk, according to the analyses in Section II and experiment results.

The crosstalk waveforms during the turn-on and turn-off process of M_H are shown in Figure 16, when C_{gdL} changes.

As shown in Fig 16(a), the amplitude of first negative spikes is almost unchanged when C_{gdL} becomes larger. There is no Miller current, and the negative spike is only affected by the induced voltage of L_{sL} which is also does not change, so with the increase of C_{gdL}, the negative spike is almost unchanged. Moreover, the amplitude of first positive spikes becomes larger with the increase of C_{gdL}. As C_{gdL} increases, the Miller current of C_{gdL} becomes larger, inducing the positive fluctuation of V_{gs1L}, which leads to the amplitude of first positive spike becomes larger.

As shown in Fig 16(b), the amplitude of negative spikes becomes larger. When C_{gdL_ex} is 20pF, the value of the first negative spike is less than $V_{gsmax(-)}$, resulting in the unreliability of device. The reason is as follows: with the increase of C_{gdL}, the Miller current flowing through C_{gsL} gets larger, then the charging rate of C_{gsL} becomes faster, the first negative amplitude becomes larger. Meanwhile, when C_{gdL} increases, the amplitude of the first positive spike of the crosstalk voltage becomes very small, and the influence of L_{sL} which make crosstalk voltage positively fluctuate remains unchanged, so the amplitude of the first positive spike decreases.

In addition, with the increase of C_{gdH}, the changing rate of V_{dsL} becomes slower, Miller current becomes smaller and the influence of the induced current source $C_{gdL}dV_{dsL}/dt$ on the crosstalk becomes smaller.

According to (3), (7), (8) and (9), as C_{gsH} increases, the changing rate of i_{dL} becomes slower, and then the induced voltage source $L_{sL}di_{dL}/dt$ becomes smaller, which weakens the crosstalk.

TABLE 2. Effects of measured parasitic parameters on crosstalk voltage.

	A_{n_on}	A_{p_on}	A_{n_off}	A_{p_off}
L_{gH}	–	–	–	–
L_{gL}	–	–	–	–
L_{sH}	↓	↓	↓	↓
L_{sL}	↑	↑	↓	↑
L_{dH}	–	–	–	–
L_{dL}	–	–	–	–
C_{gdH}	–	↓	↓	↓
C_{gdL}	–	↑	↑	↓
C_{gsH}	↓	↓	↓	↓

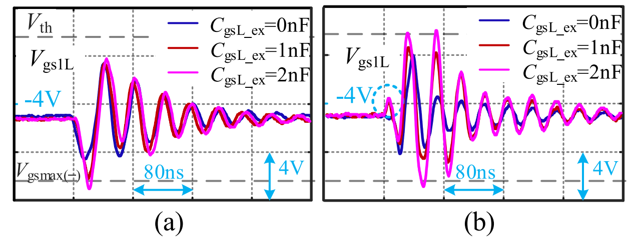

FIGURE 17. Measured crosstalk waveforms during the turn-on and turn-off process of M_H when L_{sH_ex} changes: (a) waveforms of V_{gs1L} during the turn-on process of M_H, (b) waveforms of V_{gs1L} during the turn-off process of M_H.

3) THE EFFECT OF PARASITIC PARAMETERS ON CROSSTALK

Table 2 shows the effect of the increase of parasitic parameters on the amplitudes of the first positive spike and the first negative spike in the waveforms of V_{gs1L}. In Table 2, the "↑" means that the amplitudes of the first positive spike and the first negative spike become larger as the parasitic parameter increases. The "↓" means that the amplitudes of the first positive spike and the first negative spike become smaller with the increase of parasitic parameter. The "—" means that the amplitudes of the first positive spike and the first negative spike hardly changes as the parasitic parameter increases. The influences of parasitic parameters on the amplitude of crosstalk voltage are consistent with the theoretical analyses in Section II.

From Table 2, the parasitic parameters L_{dH}, L_{dL}, L_{dH} and L_{dL} have little effect on the amplitude of crosstalk. The L_{sH}, L_{sL}, C_{gsH}, C_{gdH} and C_{gdL} are the parasitic parameters which have effect on the amplitude of crosstalk.

4) DISCUSSION OF INFLUENCE OF THE ADDED C_{GSL_EX} ON CROSSTALK VOLTAGE

The Figure 17 shows the crosstalk waveforms during the turn-on and turn-off process of M_H when C_{gsL_ex} changes. As shown in Figure 17(a), the crosstalk voltage becomes more serious with the increase of C_{gsL_ex}. When C_{gsL_ex} is 2nF, the value of first negative spike exceeds $V_{gsmax(-)}$,

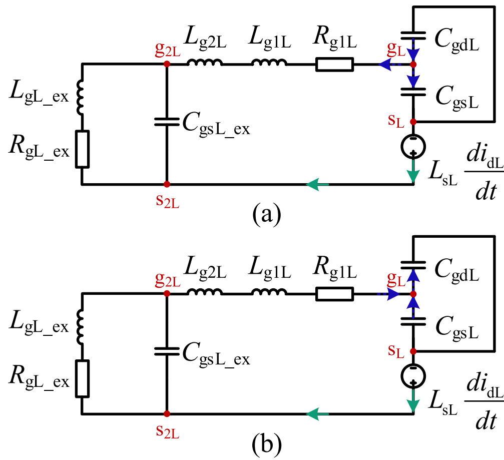

FIGURE 18. Equivalent circuit diagram when C_{gsL_ex} is added: (a) when M_H is turned on, (b) when M_H is turned off.

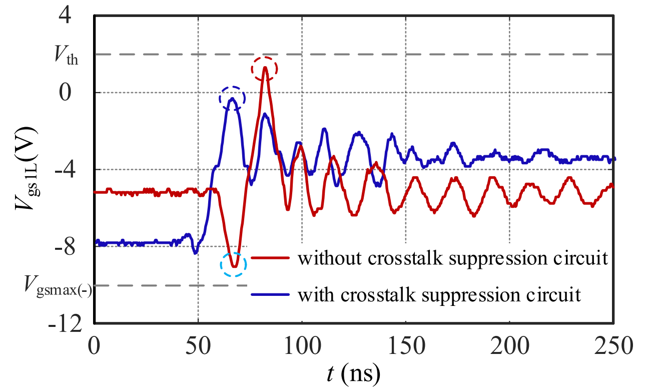

FIGURE 19. Measured waveforms of V_{gs1L} during turn-on process of M_H when two methods are used.

causing device unreliable. The amplitude of negative spikes becomes larger as C_{gsL_ex} increases, which contradicts with analyses in (8) and (9) of Section II. In (8) and (9), as C_{gsL} increases, ε_2 increases, the changing rate of V_{gs1L} decreases, and crosstalk is suppressed during the turn-on and turn-off of M_H. Note that limited by device packaging, the actual connection position of C_{gsL_ex} during the experiments is shown in Figure 12. Equivalent circuit diagram when C_{gsL_ex} is added is shown in Figure 18. The C_{gsL_ex} is connected to the outside of the package, and the equivalent impedance between the g_{2L} and s_{2L} becomes smaller with the increase of C_{gsL_ex}. Then the voltage shared from induced voltage source $L_{sL}di_{dL}/dt$ by C_{gsL} indirectly increases, which makes the amplitude of the first negative spike larger. When C_{gsL_ex} is connected, the equivalent impedance between the g_{2L} and s_{2L} gets smaller, then induced voltage source $L_{sL}di_{dL}/dt$ induces crosstalk voltage to fluctuate positively and C_{gdL} induces crosstalk voltage to fluctuate negatively, which finally causes the amplitude of the first positive spike almost unchanged.

As shown in Figure 17(b), the turn-off waveform of V_{gs1L} also has a small positive spike at first. Note that, the amplitude of the first positive spike refers to the amplitude of the next positive spike at this time. The Miller current of C_{gdL} is very small, and L_{sL} is the main factor affecting the crosstalk waveform at this time, which induces V_{gs1L} to fluctuate positively. As the Miller current increases, C_{gdL} is the main factor affecting the crosstalk voltage. With the increase of C_{gsL_ex}, the equivalent impedance between the g_{2L} and s_{2L} becomes smaller, which indirectly leads to smaller V_{gs1L} and the amplitude of the first negative becomes smaller. Then the Miller current of C_{gdL} decreases, so L_{sL} plays a dominant role in the influence of V_{gs1L} and it makes crosstalk voltage fluctuate positively. As the increase of C_{gsL_ex}, the equivalent impedance between the g_{2L} and s_{2L} gets smaller, then the influence of L_{sL} becomes larger and the amplitude of the first positive spike becomes larger.

Hence, connecting a capacitance between the gate and source of the SiC MOSFET in parallel, which has no suppression effect on the crosstalk voltage in some cases.

B. VERIFICATION OF THE EFFECTIVENESS OF THE PROPOSED CIRCUIT

The experiments are conducted to verify the effectiveness of the proposed circuit in crosstalk suppression under the condition of different I_{load} when V_{DC} is 400V.

1) CROSSTALK SUPPRESSION CIRCUIT IS USED DURING THE TURN-ON PROCESS OF M_H

The Figure 19 shows the waveforms of V_{gs1L} when the crosstalk suppression circuit is not used and the waveforms of V_{gs1L} when the crosstalk suppression circuit is used during the turn-on process of M_H. When the crosstalk suppression circuit is not used, the first negative spike of V_{gs1L} is shown by the light blue dashed circle and the first positive spike of V_{gs1L} is shown by the red dashed circle, and the crosstalk voltage oscillates violently. The value of first positive spike is close to the threshold voltage V_{th}, which influences the reliability of devices.

When the proposed circuit is used, the first positive spike of V_{gs1L} is shown by the dark blue dashed circle and the off-state voltage of the SiC MOSFET changes from −5V to −8V. The negative spike almost disappears and the value of the first positive spike is not higher than the threshold voltage V_{th}. When using the proposed circuit, the gate loop of the M_L is in high impedance state, so the induced voltage on the L_{sL} cannot charge the C_{gsL}, which greatly reduces the negative spike. After using the crosstalk suppression circuit, only C_{gdL} charges C_{gsL}, which reduces the amplitude of negative spike. The results satisfy the analyses in Section III.

As shown in Figure 20, when the proposed circuit is not used, with increase of I_{load}, the values of first positive spike approaches the threshold voltage V_{th}. However, the values of the first positive spike when the proposed circuit is used are always smaller than 0. This makes the reliability of the device be guaranteed. It also demonstrates the superiority

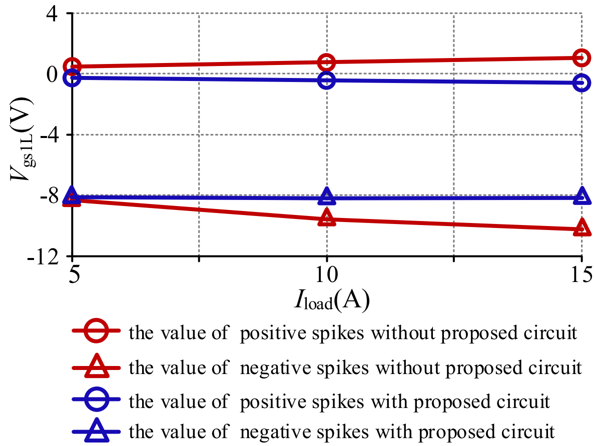

FIGURE 20. Values of spikes with the two methods during the turn-on process of M_H.

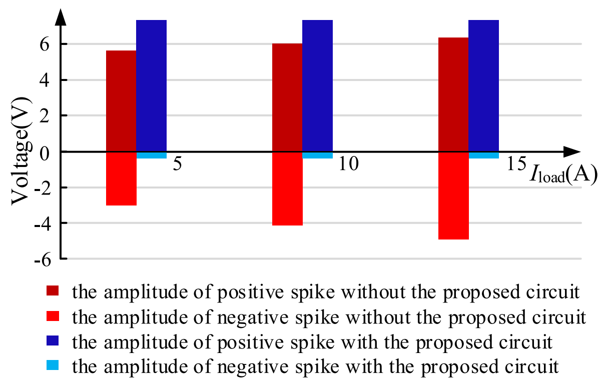

FIGURE 21. Amplitudes of the first positive spike and the first negative spike of the crosstalk voltage under different currents during the turn-on process of M_H.

of the proposed circuit during the turn-on process of M_H. Meanwhile, the values of the first negative amplitudes with the proposed circuit are always bigger than those without the proposed circuit.

The Figure 21 shows the positive and negative magnitudes of the crosstalk voltage under different currents during the turn-on process of M_H. Note that the amplitudes of first negative spikes are placed on the negative semi-axis for a more intuitive display. When the proposed circuit is not used, the dark red histogram represents the amplitude of the first positive spike and the red histogram represents the amplitude of the first negative spike. When the proposed circuit is used, the dark blue histogram represents the amplitude of the first positive spike and the light blue histogram represents the amplitude of the first negative spike. As the current increases, the amplitudes of the first positive spike and the first negative spike without the proposed circuit become larger. When the proposed circuit is not used, the reason for the increase of the amplitude of the first negative spike is as follows: the increase of I_{load} leads to the increase of the induced voltage source, which eventually leads to the negative increase of V_{gs1L}. The

TABLE 3. Switching condition of the additional impedance branch.

	Switching condition	Impedance of drive loop
①	$-V_{gs2L} < 0.7$	high impedance
②	$0.7 < -V_{gs2L} < \dfrac{(0.8+0.7)(R_{2L}+R_{3L})}{R_{3L}} + 0.7$	R_{2L}+R_{3L}
③	$\dfrac{(0.8+0.7)(R_{2L}+R_{3L})}{R_{3L}} + 0.7 < -V_{gs2L}$	R_{2L}

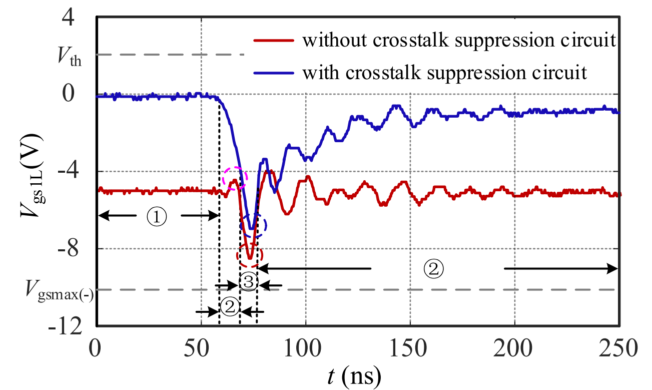

FIGURE 22. Measured waveforms of V_{gs1L} during turn-off process of M_H when two methods are used.

reason for the increase of the first positive spike is that with the increase of the current in the positive direction of the D_L, the di_{dL}/dt increases at stage 4 of Section II, and the positive influence of $L_{sL}di_{dL}/dt$ on V_{gsL} becomes larger. Moreover, the amplitude of the first negative spike is almost unchanged when the proposed circuit is used. Because the gate loop of M_L is in high impedance state during the turn-on process of M_H, so the induced voltage source can not charge C_{gsL}. Furthermore, the amplitude of the $L_{sL}di_{dL}/dt$ first negative spike becomes smaller when the proposed circuit is used. The reason of it has been explained.

2) CROSSTALK SUPPRESSION CIRCUIT IS USED DURING THE TURN-OFF PROCESS OF M_H

The value of the driver impedance of M_L is automatically adjusted according to the V_{gs2L} when the additional impedance branch is used, which is shown in Table 3.

The waveforms of V_{gs1L} during the turn-off process of M_H is shown in Figure 22. A small positive spike marked by pink dashed circle firstly appears in the turn-off waveform of V_{gs1L}, and the reason why it occurs has be explained in Section IV-A. When the suppression circuit is not used, the first negative spike is close to the $V_{gsmax(-)}$, which influences the reliability of devices. When the proposed circuit is used, the off-state voltage of SiC MOSFET becomes 0V and the amplitude is large, but the value of the first negative spike is

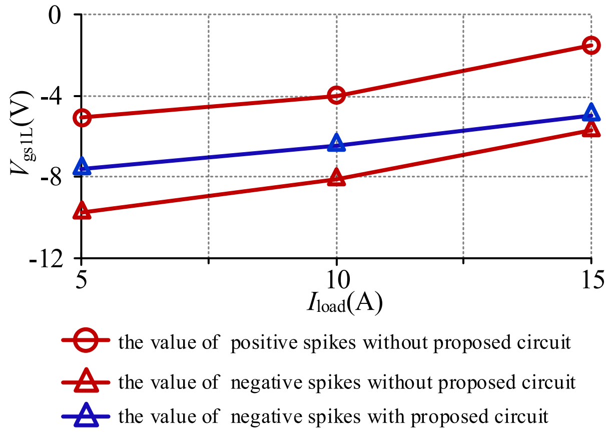

FIGURE 23. Values of spikes of the two methods during the turn-off process of M_H.

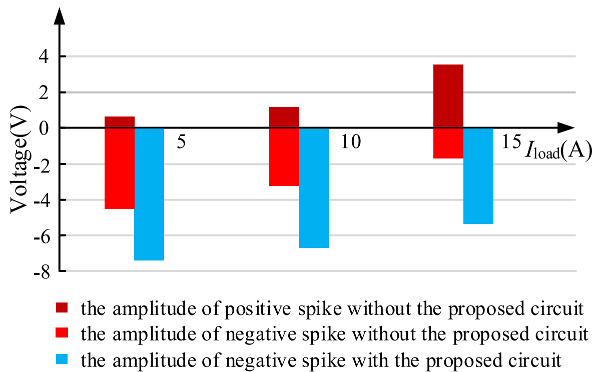

FIGURE 24. Amplitudes of first positive spike and first negative spike of the crosstalk voltage under different currents during the turn-off process of M_H.

larger than that without crosstalk suppression circuit. This is because the additional impedance branch balances the influence of the transfer current of C_{gdL} and the induced voltage on L_{sL} on crosstalk. This also satisfies the analyses in Section III.

Note that the values of the first positive spikes with the proposed circuit are not shown in Figure 23, because the value of the positive spike is smaller than the negative voltage of the driver (0V), as shown is Figure 22. As shown in Figure 23, with the increases of I_{load}, the absolute values of positive and negative spikes become smaller when the proposed circuit is not used and the absolute values of negative spikes also become smaller when the proposed circuit is used. Moreover, the value of the first negative spikes when the proposed circuit is used is always larger than that of the proposed circuit is not used, which also demonstrates the superiority of proposed circuit.

The Figure 24 shows the positive and negative amplitudes of the crosstalk voltage under different currents during the turn-off process of M_H. Note that there is no dark blue histogram shown in Figure 24, because the value of the positive spike is smaller than the negative voltage of the driver (0V), which can be seen in Figure 22.

As the current increases, the amplitude of the first positive spike becomes larger when the proposed is not used. With the increase of I_{load}, the induced voltage source $L_{sL}di_{dL}/dt$ become larger, which results in the positive fluctuation of crosstalk voltage. The amplitudes of negative spike become smaller. Because the induced voltage source $L_{sL}di_{dL}/dt$ gets larger as current increases, the negative spikes are induced to fluctuate positively. Moreover, the amplitude of the first negative spikes with the proposed circuit are larger than those without the proposed circuit. When the proposed circuit is used, the impedance of the drive loop is larger than that when the proposed circuit is not used. The effect of induced voltage source $L_{sL}di_{dL}/dt$ inducing the first negative spike to fluctuate positively is weakened, so the amplitudes of the first negative spikes with the proposed circuit are larger than those without the proposed circuit.

V. CONCLUSION

From this paper, the crosstalk issue for the SiC MOSFET should be paid careful attention in the converter design. Different from the existing methods, this paper considers the influence of complex parasitic parameters on the crosstalk voltage, especially the common-source inductance. The influence of various parasitic parameters on V_{gsL} during the turn-on and turn-off process of M_H is modeled and analyzed respectively. C_{gdL} and L_{sL} are two key factors that affect crosstalk. Therefore, a novel suppression circuit is proposed in this paper, which uses a high impedance branch combined with a turn-off voltage offset to suppress the crosstalk during the turn-on process of M_H and uses an additional impedance branch combined with zero-level gate voltage to suppress the crosstalk during the turn-off of M_H. It can balance the influence of the Miller current of C_{gdL} and the induced voltage on L_{sL} on crosstalk and the effect of the two on crosstalk can cancel each other out during the turn-off of M_H. Finally, a large number of experiments have verified the influence of various parasitic parameters on crosstalk and the effectiveness of the proposed circuit. Moreover, the experimental results also indicate paralleling capacitance between gate and source of the disturbed SiC MOSFET will even aggravate crosstalk in some cases.

REFERENCES

[1] Z. Liang, P. Ning, and F. Wang, "Development of advanced all-SiC power modules," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2289–2295, May 2014.

[2] J. Millan, P. Godignon, X. Perpina, A. Perez-Tomas, and J. Rebollo, "A survey of wide bandgap power semiconductor devices," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2155–2163, May 2014.

[3] F. Xu, T. J. Han, D. Jiang, L. M. Tolbert, F. Wang, J. Nagashima, S. J. Kim, and S. Kulkarni, "Development of a SiC JFET-based six-pack power module for a fully integrated inverter," *IEEE Trans. Power Electron.*, vol. 28, no. 3, pp. 1464–1478, Mar. 2013.

[4] S. Jahdi, O. Alatise, P. Alexakis, L. Ran, and P. Mawby, "The impact of temperature and switching rate on the dynamic characteristics of silicon carbide Schottky barrier diodes and MOSFETs," *IEEE Trans. Ind. Electron.*, vol. 62, no. 1, pp. 163–171, Jan. 2015.

[5] L. Zhang, X. Yuan, X. Wu, C. Shi, J. Zhang, and Y. Zhang, ''Performance evaluation of high-power SiC MOSFET modules in comparison to Si IGBT modules,'' *IEEE Trans. Power Electron.*, vol. 34, no. 2, pp. 1181–1196, Feb. 2019.

[6] Z. Zhang, W. Zhang, F. Wang, L. M. Tolbert, and B. J. Blalock, ''Analysis of the switching speed limitation of wide band-gap devices in a phase-leg configuration,'' in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE)*, Sep. 2012, pp. 3950–3955.

[7] J. Wang and H. S.-H. Chung, ''Impact of parasitic elements on the spurious triggering pulse in synchronous buck converter,'' *IEEE Trans. Power Electron.*, vol. 29, no. 12, pp. 6672–6685, Dec. 2014.

[8] F. F. Wang and Z. Zhang, ''Overview of silicon carbide technology: Device, converter, system, and application,'' *CPSS Trans. Power Electron. Appl.*, vol. 1, no. 1, pp. 13–32, Dec. 2016.

[9] N. Teerakawanich and C. M. Johnson, ''Design optimization of quasi-active gate control for series-connected power devices,'' *IEEE Trans. Power Electron.*, vol. 29, no. 6, pp. 2705–2714, Jun. 2014.

[10] N. Idir, R. Bausiere, and J. J. Franchaud, ''Active gate voltage control of turn-on di/dt and turn-off dv/dt in insulated gate transistors,'' *IEEE Trans. Power Electron.*, vol. 21, no. 4, pp. 849–855, Jul. 2006.

[11] D. Yuan, Y. Zhang, X. Wang, and J. Gao, ''A detailed analytical model of SiC MOSFETs for bridge-leg configuration by considering staged critical parameters,'' *IEEE Access*, vol. 9, pp. 24823–24847, 2021.

[12] S. Jahdi, O. Alatise, J. A. O. Gonzalez, R. Bonyadi, L. Ran, and P. Mawby, ''Temperature and switching rate dependence of crosstalk in Si-IGBT and SiC power modules,'' *IEEE Trans. Ind. Electron.*, vol. 63, no. 2, pp. 849–863, Feb. 2016.

[13] Y. Li, M. Liang, J. Chen, T. Q. Zheng, and H. Guo, ''A low gate turn-off impedance driver for suppressing crosstalk of SiC MOSFET based on different discrete packages,'' *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 7, no. 1, pp. 353–365, Mar. 2019.

[14] H. Zaman, X. Wu, X. Zheng, S. Khan, and H. Ali, ''Suppression of switching crosstalk and voltage oscillations in a SiC MOSFET based half-bridge converter,'' *Energies*, vol. 11, no. 11, p. 3111, Nov. 2018.

[15] J. Wang and H. S.-H. Chung, ''A novel RCD level shifter for elimination of spurious turn-on in the bridge-leg configuration,'' *IEEE Trans. Power Electron.*, vol. 30, no. 2, pp. 976–984, Feb. 2015.

[16] H.-T. Tang, H. Shu-Hung Chung, J. Wing-To Fan, R. Shun-Cheung Yeung, and R. Wing-Hong Lau, ''Passive resonant level shifter for suppression of crosstalk effect and reduction of body diode loss of SiC MOSFETs in bridge legs,'' *IEEE Trans. Power Electron.*, vol. 35, no. 7, pp. 7204–7225, Jul. 2020.

[17] Z. Zhang, F. Wang, L. M. Tolbert, and B. J. Blalock, ''Active gate driver for crosstalk suppression of SiC devices in a phase-leg configuration,'' *IEEE Trans. Power Electron.*, vol. 29, no. 4, pp. 1986–1997, Apr. 2014.

[18] B. Zhang, S. Xie, J. Xu, Q. Qian, Z. Zhang, and K. Xu, ''A magnetic coupling based gate driver for crosstalk suppression of SiC MOSFETs,'' *IEEE Trans. Ind. Electron.*, vol. 64, no. 11, pp. 9052–9063, Nov. 2017.

[19] Z. Zhang, J. Dix, F. F. Wang, B. J. Blalock, D. Costinett, and L. M. Tolbert, ''Intelligent gate drive for fast switching and crosstalk suppression of SiC devices,'' *IEEE Trans. Power Electron.*, vol. 32, no. 12, pp. 9319–9332, Dec. 2017.

[20] Y. Zhu, Y. Huang, H. Wu, Z. Din, and J. Zhang, ''A multi-level gate driver for crosstalk suppression of silicon carbide MOSFETs in bridge arm,'' *IEEE Access*, vol. 9, pp. 100185–100196, 2021.

[21] C. Liu, Z. Zhang, Y. Liu, Y. Si, and Q. Lei, ''Smart self-driving multilevel gate driver for fast switching and crosstalk suppression of SiC MOSFETs,'' *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 1, pp. 442–453, Mar. 2020.

[22] H. Li, Y. Jiang, Z. Qiu, T. Shao, and Y. Wang, ''A multi-step active gate driver for suppressing crosstalk of SiC MOSFET,'' in *Proc. IEEE 9th Int. Power Electron. Motion Control Conf. (IPEMC-ECCE Asia)*, Nov. 2020, pp. 1868–1873.

[23] T. Shao, T. Q. Zheng, H. Li, J. Liu, Z. Li, B. Huang, and Z. Qiu, ''The active gate drive based on negative feedback mechanism for fast switching and crosstalk suppression of SiC devices,'' *IEEE Trans. Power Electron.*, vol. 37, no. 6, pp. 6739–6754, Jun. 2022.

[24] P. Wang, L. Zhang, X. Lu, H. Sun, W. Wang, and D. Xu, ''An improved active crosstalk suppression method for high-speed SiC MOSFETs,'' *IEEE Trans. Ind. Appl.*, vol. 55, no. 6, pp. 7736–7744, Nov. 2019.

[25] C. Bi, H. Ou, Q. Kang, R. Li, and L. Cheng, ''A novel driver circuit on crosstalk suppression in SiC MOSFETs,'' in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2021, pp. 1–5.

[26] Y. Xu, B. Duan, J. Song, D. Yang, and C. Zhang, ''A novel gate driver of SiC MOSFET for crosstalk suppression in bridge configuration,'' in *Proc. Chin. Autom. Congr. (CAC)*, Nov. 2020, pp. 1173–1178.

[27] H. Li, Y. Zhong, R. Yu, R. Yao, H. Long, X. Wang, and Z. Huang, ''Assist gate driver circuit on crosstalk suppression for SiC MOSFET bridge configuration,'' *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 2, pp. 1611–1621, Jun. 2020.

[28] J. Zhao, L. Wu, Z. Li, Z. Chen, and G. Chen, ''Analysis and suppression for crosstalk in SiC MOSFET turn-off transient,'' in *Proc. IEEE 9th Int. Power Electron. Motion Control Conf. (IPEMC-ECCE Asia)*, Nov. 2020, pp. 1145–1150.

[29] C. Li, Z. Lu, Y. Chen, C. Li, H. Luo, W. Li, and X. He, ''High off-state impedance gate driver of SiC MOSFETs for crosstalk voltage elimination considering common-source inductance,'' *IEEE Trans. Power Electron.*, vol. 35, no. 3, pp. 2999–3011, Mar. 2020.

[30] CREE. (2021). *C2M0160120D Data Sheets*. [Online]. Available: https://assets.wolfspeed.com/uploads/2020/12/C2M0160120D.pdf

[31] L. Salvo, M. Pulvirenti, A. G. Sciacca, G. Scelba, and M. Cacciato, ''Gate-source voltage analysis for switching crosstalk evaluation in SiC MOSFETs half-bridge converters,'' in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE)*, Oct. 2021, pp. 15–22.

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