IEEE Access
Multidisciplinary ⋮ Rapid Review ⋮ Open Access Journal

Received 30 September 2022, accepted 21 October 2022, date of publication 25 October 2022, date of current version 8 November 2022.

Digital Object Identifier 10.1109/ACCESS.2022.3216922

RESEARCH ARTICLE

Design of Cylindrical Surrounding Double-Gate MOSFET With Fabrication Steps Using a Layer-by-Layer Approach

NAVEENBALAJI GOWTHAMAN, (Senior Member, IEEE), AND VIRANJAY M. SRIVASTAVA, (Senior Member, IEEE)
Department of Electronic Engineering, Howard College, University of KwaZulu-Natal, Durban 4041, South Africa
Corresponding author: Naveenbalaji Gowthaman (dr.gnb@ieee.org)

ABSTRACT The semiconductors with nanometer-scale are subjected to various patterns and scaling using the latest technology. The most widely used methods are top-down approaches in the design of complex heterostructures. The top-down approach involves the photolithography to ion sequentially beaming of the materials. In this context, the alternative layer-by-layer approach with cylindrical structures has been discussed and supported by the subsequent results to make Cylindrical Surrounding Double-Gate (CSDG) MOSFETs in this research work. This method involves the making of cylindrical structures with high-resolution morphological structures of CSDG MOSFETs. The process has been described in detail to design the CSDG MOSFETs with high-ƙ dielectric materials to make them suitable for low-frequency RF applications. The fast modulation of the Single Nano Wire (SNW) has been adopted for complex heterostructure modeling. The high-ƙ dielectric materials are placed in between the spacer and the gate material to overcome the Short Channel Effects (SCEs). This method produces symmetrical and concentric cylindrical structures of the CSDG MOSFETs with suitable layers. The minimum layer thickness achieved is about 10 nm axial length along with the core of the SNW. This gives enough insight for the proposed cylindrical structure to fabricate over the core of 2DEG. In this type of structure development, many cylindrical structures with various properties can be designed. The parameters focused on the cylindrical structure will be periodic, non-periodic, symmetric, asymmetric structures, and gaps/dots of nanometer scale. This innovative method introduces the method of designing the symmetric CSDG MOSFET concerning the center core. In this work, the authors focus on the suitable novel technique of designing cylindrical structures with unique dimensions and physical properties using various semiconductor materials.

INDEX TERMS Channel dopant, cylindrical surrounding double-gate (CSDG) MOSFET, double-gate (DG) MOSFET, gate modeling, high-ƙ dielectrics, nanotechnology, VLSI.

I. INTRODUCTION

In this nano-technological era, lithography tools have been used widely to design and pattern the semiconductor nano-material in heterostructures by the nanometer approach [1]. This kind of lithography mainly works on scaling the length in the nanometer regime. This has a wide range of applications such as computer systems to motion detection sensors in handheld mobile phones and wearable gadgets. Silicon is still a suitable material to design complex nanos-tructures. The heterostructures were designed using the arbitrary alloy of semiconductors and found their applica-tions in nano-photonics, wearable nanomaterial gadgets, and opto-electromechanics [2]. Further research reveals that the latest technology supports the patterning of the heterostruc-tures with proper resolution and higher fidelity with pre-cision. Christesen et. al. [3] had performed the patterning of semiconductors with nanometer-scale precision using a

The associate editor coordinating the review of this manuscript and approving it for publication was Mostafa Rahimi Azghadi.

cornerstone of modern technology. Top-down methods, ranging from photolithography to focused ion-beam milling are typically used to fabricate complex nanostructures.

In this perspective, the authors discuss an alternative bottom-up method to encode similar high-resolution morphology in semiconductor nanowires (NWs). The process ''Encoded Nanowire GRowth and Appearance through VLS and Etching (ENGRAVE)'' combines fast modulation of nanowire composition during Vapor−Liquid−Solid (VLS) growth with composition-dependent wet-chemical etching. Bavir et. al. [4] after calibrating the models and parameters used in the simulations based on experimental data, by using the opposite doping in the channel and between the gates in an asymmetric Double-Gate Junction Less (JL) transistor with the *3 nm* gate length, a Charge Sheet (CS) were created. Also in AC analysis and at *1 MHz* frequency, by using CS the parasitic capacitances were reduced.

The gate currents of SiC MOSFETs are actively controlled in such a way that several devices can switch faster (within *50 ns*) even in the presence of a moderate amount of gate pulse delay mismatch and jitter in the gate pulse. This enables the active gate driving to share gate pulse signal information [5]. Gowthaman and Srivastava [6] have realized an analytical model of the lightly doped Cylindrical Surrounding Double-Gate (CSDG) MOSFET. Capacitive modeling was performed for this cylindrical structure. This modeling has been analyzed for all operating regions of the transistors, capacitance estimation, and electrical field dependence on the capacitance. It has been observed that the transconductance (G_m) values have been raised to $0.0106\ S/\mu m$ from $0.000645\ S/\mu m$ with the inclusion of 2D electron gas in the core of CSDG MOSFET.

This research paper has been organized as follows: Section II describes the development of the cylindrical structures of the design and its characteristics. Section III explains the fabrication based on the concentric layer approach of nanomaterial deposition. Section IV supports the CSDG MOSFET fabrication possibilities with the results that support the argument, based on a single strand of SNW. Finally, Section V concludes the work with supportive results for the proposed technique and also provides future considerations.

II. DEVELOPMENT OF CYLINDRICAL DESIGN

Several Lithographic methods of patterning the semiconductor materials based on MOSFETs have become prominent in the recent year of research [7]. In the modern electronic era, the scaling of the MOSFETs has been carried out from micrometer to nanometer regime with enhanced performance. The patterning has become a great tool for designing transistors that can be used in mobile phones and other electronic gadgets. This method is used to pattern the Silicon wafers to make them suitable to place several components to work as a block [8]. Nanophotonics makes the circuit suitable to work with various optoelectrical properties and can be used in sensor replacement areas. The trade-off is the main concern about patterning and placing the devices. The leading material in device design is Silicon even after a few decades of focused research carried out in the field. But, it has a few disadvantages that can be overcome by using arbitrary alloys in place of the conventional material. To improve the lithographic methods, high cost is needed and it will reflect in the trade-off. As a result of this, chemical growths are carried out to reduce the budget of the same device design. The chemical growth has the potential to reduce the budget compared to the conventional methods of device design [5], [10]. This progress method gives the best device design with increased resolution and greater fidelity to work under RF environments. The meta-stable methods such as the non-lithographic technique of building the heterostructures have become recent research insight to the engineering fraternity [11], [12], [13]. The meta-stable structures designed are the spheres, cubes, and also concentric cylindrical heterostructures. The Single Nano Wire (SNW) is the fundamental structure of the cylindrical structure of the heterostructure device and it makes the base for constructing the consecutive layers. The morphological stability is widely observed at the SNW and hence significant research effort has been made to grow the wire using the Vapor-Liquid-Solid (VLS) mechanism [14], [15]. By the VLS mechanism, Lim et. al. [16] modulated the diameter of III−V single nanowire by altering the environment, allowing a $\sim 25\%$ improvement of the SNW dimensions. The generalized version of the resultant SNW design can be used in the modulated version for the concentric cylindrical structures using VLS-grown SNW. By altering the parameters for the VLS growth process, the periodic structures can be designed over cross-sectional dimensions and the period of growth. The sawtooth morphological growth can be observed in the SNW designed using the novel atomic force microscopy (AFM) method concerning bulk [12], [17].

The alteration in the temperature and pressure parameters will reflect the characteristics of the device. A variety of periodic structures has been created and it does comply with the periodic and cross-sectional dimensional properties. There has been the latest research in the field of Silicon SNW growth using the rapid depressurized Gold (Au) deposition and it is a suitable substitute for the mask in the ex-situ chemical etching. This type of etching has been widely used in nanomaterial research carried out in pressure chambers. The etching reveals that the SNW has undergone the sawtooth type of growth alongside the cylindrical structure. This can be smoothed further by adding control over the surface material in the core which uses atomic force microscopy to get the soft surface. By the usage of the Gallium Phosphide – Gallium Arsenide compound, the latest researchers were able to create the design of nanowires with superlattices in the concentric cylindrical heterostructures. This shows that the proposed design can be built using arbitrary alloys in place of conventional semiconductor materials for the construction of the CSDG MOSFETs. The arbitrary semiconductor alloy has been in agreement with the novel cylindrical structure design that is suitable for low RF design. This has increased the

selectivity to remove the GaAs segments. The technology of On-Wire Lithography (OWL) can be used to create nanogaps in cylindrical structures [3], [4], [5], [18].

The porous nature of the semiconductor material has been taken into account for the etching process on the concentric cylindrical walls of the CSDG MOSFETs. To perform uniform etching several methods can be deployed and it is evident that the COAxial Lithography (COAL) needs some selective etching process such as Template-Assisted Selective Epitaxy (TASE) or the Encoded Nanowire GRowth and Appearance through VLS and Etching (ENGRAVE) [18], [19], [20]. Recent research were done with the ENGRAVE technology and that is highly submissive to the agreement. The proposed CSDG MOSFET of cylindrical dimension needs a lot of etching after each layer of deposition and it needs to be verified for the clear smooth coating of nanomaterials in the cylindrical structure. The final material after etching should not be less than *5 nm* for the process of the next layer of deposition. The possibility of using the NW has been used to encode the possibilities of specific physical and optical properties which ensure the morphological highlights specify the resolution of Si-NW with the process of ENGRAVE (comparison is shown in fig. 1). This includes the properties that vary from various optical, biological, thermal, and electrical characteristics. Both methods are used only to design a single strand of the SNW at the nanometer regime. The concentric layers of the cylindrical structure have been designed by the top-down approach. The layer of the core has been designed at the initial stage and the consecutive layers have been grown over the surface of the previous layers the imperfections that range from *1 nm* have been planned to etch to get a smooth finish. The smooth layer ensures the complete deposition of the nanomaterial over the layer for concentric deposition over the length of the device.

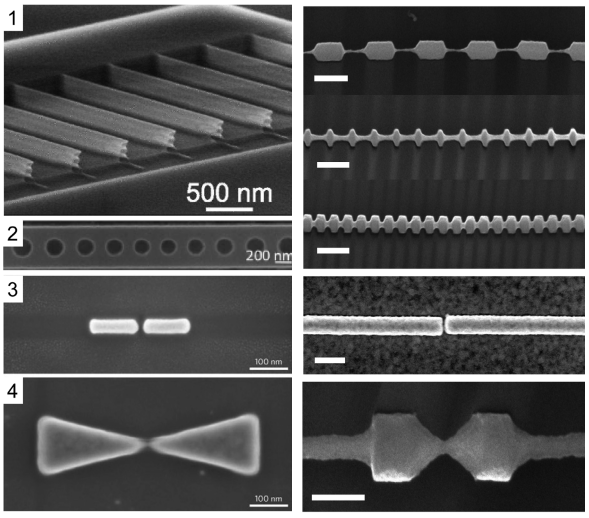


FIGURE 1. Top-down Method of growth (Left: Lithography) and Bottom-up method of growth (Right: Encoded Nanowire Growth and Appearance through VLS and Etching) [3].

The average of the doping concentrations in the CSDG MOSFET [2] has been expressed as:

$$n_{avg} = n_{source}\left[1 - \frac{l_{p-type}}{L}\right] + n_{\max}\left(\frac{l_{p-type}}{L}\right) \tag{1}$$

The halo doping concentration [6] of the dopants in the source and drain terminal has been given as:

$$\begin{aligned} n_{source}(x) &= n_{source}\left(\frac{x}{l_{p-type}}\right) + n_{\max}\left[1 - \left(\frac{x}{l_{p-type}}\right)\right] \\ n_{drain}(x) &= n_{source}\left[\left(\frac{L}{l_{p-type}}\right) - \left(\frac{x}{l_{p-type}}\right)\right] \\ &\quad + n_{\max}\left[1 + \left(\frac{x}{l_{p-type}}\right) - \left(\frac{L}{l_{p-type}}\right)\right] \end{aligned} \tag{2}$$

where 'x' is the distance of the length of the CSDG MOSFET device. The resultant design is a cylindrical structure and this heterostructure will have a non-zero contribution to the Gaussian distribution and it is expressed as:

$$\begin{aligned} -qn_{avg}h_t\Delta x\omega_{dth} &= -\varepsilon_{La_2O_3}E_{rc_1}\Delta x\omega_{dth} + \varepsilon_{La_2O_3}E_{rc_2}\Delta x\omega_{dth} \\ &\quad + \varepsilon_{Si}\{-E_x(x+\Delta x) + E_x(x)\}h_t\omega_{dth} \end{aligned} \tag{3}$$

The work has been an extension lead of the authors' effort in their 2D DG MOSFET in [6]. From fig. 2, it is observed that it serves as a fundamental unit of the CSDG MOSFET.

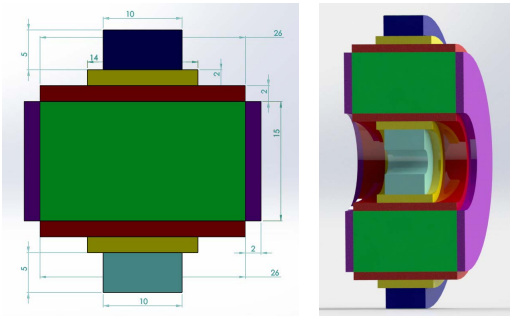


FIGURE 2. Two-dimensional Cross-section of the proposed CSDG MOSFET to be rolled as a cylindrical structure along the axis outside the bottom gate (Pale Blue).

A. THE CONCENTRIC CYLINDRICAL MODEL

The potential involved with the cylindrical structure has been affected by an imaginary capacitor and it is termed 'V'. This potential exists between the concentric layers of the cylindrical structure of the CSDG MOSFET [2], [3], [4], [5], [6]. The inner layer of the cylinder has a radius of rc_2 and the outer layer of the cylinder has a radius of rc_1. The normalized potential between rc1 and rc_2 can be given as,

$$V = \frac{Q}{2\pi\varepsilon_0 L_{S\to D}} \ln r \left|\frac{rc_2}{rc_1}\right. \tag{4}$$

Further reducing (4) it gets:

$$V = \frac{Q}{2\pi\varepsilon_0 L_{S\to D}} \ln \frac{rc_2}{rc_1} \tag{5}$$

The difference in normalized potential between the cylindrical plates can be given as:

$$\Delta V = V_{rc_2} - V_{rc_1} = -\int_{rc_1}^{rc_2} \vec{E} \,.\, \vec{dl} \tag{6}$$

The method of layer-by-layer etching is used for the growth of the cylindrical structure in this work. The etching was done at every layer deposition [21]. The difference in the normalized potential acts as a suitable condition inside the growth chamber to make uniform deposition and take care of morphological properties. The scattering phenomenon was studied widely to analyze the effect of scattering and parameter evaluation. The core of the CSDG MOSFET is maintained to be *1 nm* and all the consecutive layers are grown one by one around the core. The substrate material has been wide enough to exhibit the electrical properties of the CSDG MOSFET and the triangular area of the bulk is $34.54 \times 10^{-20}\ m^2$. The high-ƙ dielectric material has been chosen to reduce the SCEs and the material is Lanthana (La_2O_3) Lanthanum Oxide and it shows greater electrical properties compared to other materials. This has been chosen to be the suitable high-ƙ dielectric material alongside the conventional materials for design.

III. FABRICATION VISIONS OF THE CSDG MOSFET

The fabrication of the proposed CSDG MOSFET is an important step in the design process. The chosen high-ƙ dielectric material is introduced in between the spacer and the gate terminals [22], [23], [24], [25]. The nanomaterial introduced in the spacer has been exhibiting electrical properties to improve the performance of the electron buildup in the channel and is also useful in the distribution of charge carriers [22]. The electron buildup in the channel has been recorded for analysis. The platform is chosen to incorporate the bottom concentric rings in the chamber [23]. The concentric rings of various diameters are placed in the bottom and over it, the layers are grown uniformly. The first layer fabricated is the core and it has been etched to get the uniform deposition. This acts as a base layer for the design of CSDG MOSFET. The cylindrical structure of the core makes the essential for the entire device by growing concentric layers of the heterostructure. The COAL is not feasible for this design since it has numerous layers. This structure can be built on a layer-by-layer approach and utmost care is needed for implementing TASE on the layers. The dimensions of the proposed CSDG MOSFET have been given in Table 1.

Oxidation inside the chamber is a prominent factor to provide uniform deposition of the layers [24], [25], [26]. This work focuses on the effect of oxidation and its impact on the design of CSDG MOSFET. The oxidation has been carried out in two modes: dry and wet; in different orientations of the deposition, 111 and 100. The mathematical approach to the deposition of the silicon had been proposed by Deal-Grove and this model has been compared with the Massoud Term to analyze the results of oxidation to fabricate semiconductor layers [27]. It describes the growth of an oxidation layer over the surface of the semiconductor material inside the oxidation chamber. The later model has been a modified version of the Deal-Grove model which uses the parallel oxidation technique to ensure a uniform layer of growth. The Massoud model term has been submissive to the conventional method of oxidation [28], [29], [30]. This depends on the dimensions of the growth material. In the proposed work, the oxidation layer is maintained to be a concentric layer of the cylindrical structure. A better model of the oxide is taken into consideration.

The fabrication methodology is the extension of the authors' work carried out in [2] and [6]. The fabrication of the CSDG MOSFET (as shown in fig. 3) has been a challenging method since it involves careful involvement of

TABLE 1. Parameters for simulation.

Dimensions of the proposed CSDG MOSFET	
The radius of the core (m)	: 1×10^{-9}
The radius of the gate-1 (m)	: 3×10^{-9}
The radius of the spacer-1 (m)	: 5×10^{-9}
The radius of the oxide-1, La_2O_3 (m)	: 7×10^{-9}
The radius of the bulk (m)	: 11×10^{-9}
The radius of the oxide-2, La_2O_3 (m)	: 13×10^{-9}
The radius of the spacer-2 (m)	: 15×10^{-9}
The radius of the gate-2 (m)	: 17×10^{-9}
Number of points on the circle, gates	: 50
Number of points on the oxide, La_2O_3	: 50
Maximum triangle area, gate-1 (m^2)	: 9.42×10^{-20}
Maximum triangle area, oxide-1 La_2O_3 (m^2)	: 21.98×10^{-20}
Maximum triangle area, spacer-1 (m^2)	: 15.70×10^{-20}
Maximum triangle area, bulk (m^2)	: 34.54×10^{-20}
Maximum triangle area, oxide-2 La_2O_3 (m^2)	: 40.82×10^{-20}
Maximum triangle area, spacer-2 (m^2)	: 47.10×10^{-20}
Maximum triangle area, gate-2 (m^2)	: 53.38×10^{-20}
Simulation Parameters	
Transport Model	: Uncoupled
Scattering	: Allowed
Number of valley(s)	: 1
Number of Eigen-values	: 4
Mesh Fitness Factor	: 5.0
Structure Parameters	
Diameter of the core (m)	: 2×10^{-9}
La_2O_3 oxide thickness (m)	: 1×10^{-9}
Length of the Gate 1/2 terminal (m)	: 8×10^{-9}
Source/Drain extension length (m)	: 8×10^{-9}
Source/Drain doping concentration (cm^{-3})	: 1×10^{20}
Gate Voltage, Start Value (V)	: 0.0
Gate Voltage, Step Size (V)	: 0.04
Gate Voltage, Number of steps	: 11
Drain Voltage, Start value (V)	: 0.4
Drain Voltage, Step Size (V)	: 0.001
Drain Voltage, Number of steps	: 1
Material Parameters	
Core Material	: InGaAs
Crystal Orientation	: 1 1 0
Gate Work Function (eV)	: 4.05

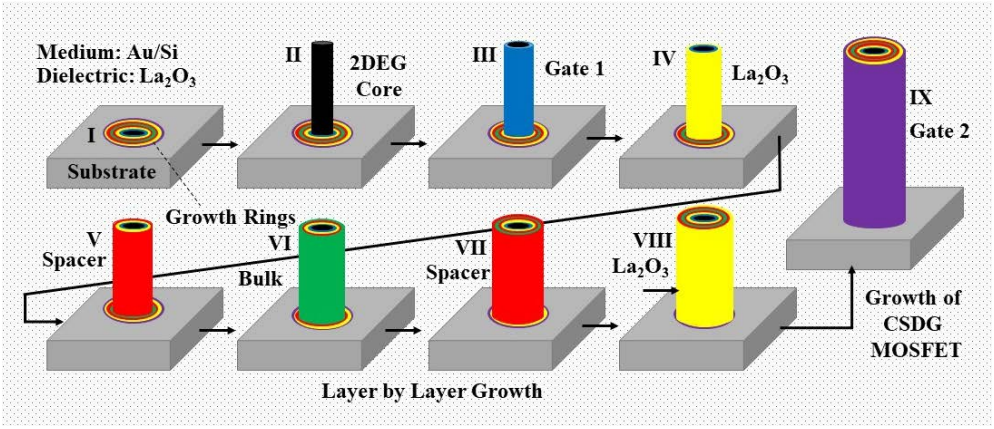


FIGURE 3. Fabrication of CSDG MOSFET in [2] concentric layer (inner to outer) approach in a controlled environment [This work].

the parameters to create a layer-by-layer approach [16], [31]. The core has been grown over the concentric disc placed in the chamber base. The core ranges from *2 nm* in diameter and with uniform distribution. The next layer is the gate-1 terminal which ranges from *6 nm* in diameter. The high-ƙ dielectric layer has been placed next to the gate-1 terminal from *6 nm* to *10 nm* thickness to avoid SCEs. The spacer extends for another *4 nm* from the dielectric material. The concentric cylindrical bulk is the larger region of the device which extends from *14 nm* to *22 nm* in thickness. The second spacer layer has an extension from *22 nm* to *26 nm* with *4 nm* in thickness. The second high-ƙ dielectric terminal has been placed next to the second spacer layer and it extends to a diameter of *30 nm*. The last layer is the gate-2 material and it acts as a surrounding layer with the largest diameter of *34 nm* from the dielectric material.

The fabricated CSDG MOSFET can be cut into the desired length which abides the L/W ratio and can be scaled and applied to different systems [32], [33], [34], [35]. The desired length of the device is fixed as 500 nm in this work. The transport model used in the fabrication is uncoupled and phonon scattering is allowed. The results have been recorded and compared with the conventional methods of fabrication. The results were obtained for the SNW and it has the potential to develop into a concentric multilayer design of CSGD MOSFET.

IV. RESULTS AND DISCUSSIONS

The combination of both models has been used in the growth of the concentric cylindrical layer [28], [29], [30], [36]. The oxidation and its characteristics have been recorded and shown in fig. 4. The dopant concentration in the surrounding concentric cylindrical surface varies from $1 \times 10^{20}\ cm^{-3}$ to $1.57 \times 10^{11}\ cm^{-3}$. The dopant diffusion for the respective layer varies from $9.61 \times 10^{11}\ cm^{-3}$ to $6.31 \times 10^{11}\ cm^{-3}$. The subsequent increase in the layers of the device increases the risk of oxidation between the layers. The chamber is always maintained in optimum condition to achieve exact doping. The dopant in the space is maintained to $7.11 \times 10^{11}\ cm^{-3}$ throughout the length of the device. The iterations of the oxidation for the cylindrical structure have been carried out for *600 minutes* and it is observed to be $2.53 \times 10^{-4}\ \mu.min^{-1}$ in the dry mode of (100). Also, it is observed to be $1.48 \times 10^{-3}\ \mu.min^{-1}$ for the wet oxidation in the same orientation. The oxidation rate of (111) orientation has been observed to be $2.64 \times 10^{-4}\ \mu.min^{-1}$ and $1.51 \times 10^{-3}\ \mu.min^{-1}$ in dry and oxidation modes, respectively.

The oxidant concentration plays a major role in performing uniform oxidation in the cylindrical walls of the heterostructure [37], [38], [39], [40]. The maximum oxidant concentration is observed to be $4.37 \times 10^{16}\ cm^{-3}$ of thickness *0.82 nm* for (100) and $2.56 \times 10^{19}\ cm^{-3}$ of thickness *0.33 nm* for (100) at dry oxidation and wet oxidation respectively. The maximum oxidant concentration is observed to be $3.90 \times 10^{16}\ cm^{-3}$ of thickness *0.96 nm* for (111) and $2.11 \times 10^{19}\ cm^{-3}$ of thickness *0.49 nm* for (111) at dry oxidation and wet oxidation respectively. The oxidation model has been formed by the combination of Deal-Grove and Massoud model terms to improve the oxidation effect over the surface area [38]. This has shown improved results as in fig. 4 and it has been more submissive to both the model of oxidation. This will result in uniform oxidation and can be etched neatly to perform the growth of the consecutive layers in the chamber. By this method, CSDG MOSFETs are immune to minor defects such as small nanogaps and trenches.

The entire simulation has been run for 600 minutes time frame to realize the effect of oxidation and oxidation rate. The maximum mesh triangle area for the gate-1 terminal is $9.42 \times 10^{-20}\ m^2$ and the maximum mesh triangle area for the gate-2 terminal is $53.38 \times 10^{-20}\ m^2$. The maximum mesh triangle area for the bulk region is $34.\ 54 \times 10^{-20}\ m^2$ and it is suitable for developing the channel. The dopant diffusion is the most profitable factor in the design of a cylindrical structure to maintain uniformity and scalability [39], [41]. The dopant concentration is observed at $1 \times 10^{20}\ cm^{-3}$ and

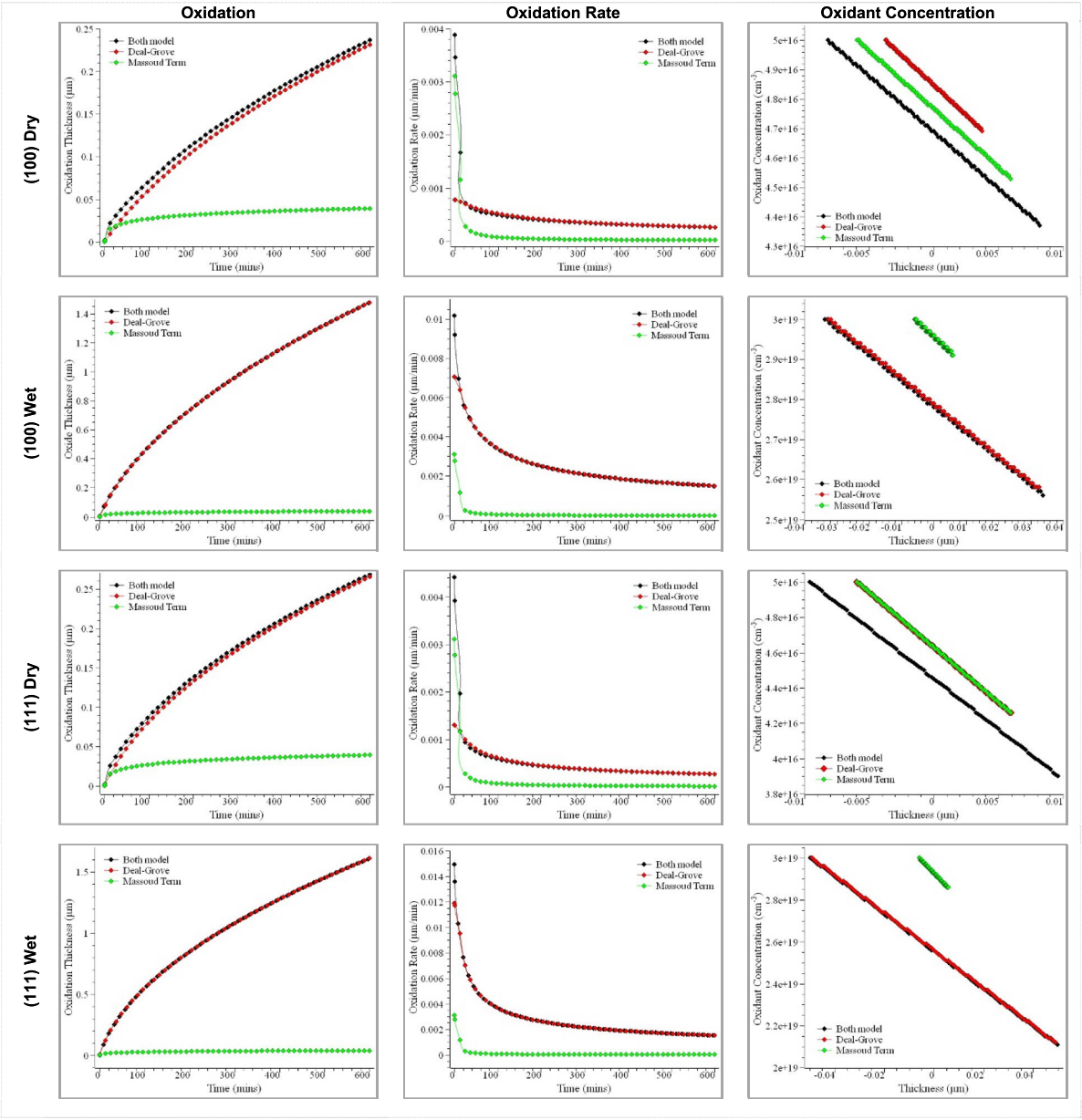


FIGURE 4. Oxidation and oxidation rates for the (100) and (111) orientations. The Deal-Grove and Massoud Model term have been combined to provide uniform oxidation in the concentric cylindrical heterostructure. Rows: Types of oxidation; Columns: Oxidation Parameters.

$7.11 \times 10^{18}\ cm^{-3}$ at the source and drain of the device, respectively.

The CSDG MOSFET has been simulated in an environment close to the experimental setup and the results were recorded. The wave function has been shown in Figure 5 (a) which shows the exact response of the cylindrical structure that exhibits the capacitance between the concentric layers of the walls [41], [42], [43]. This clearly shows that there is a possibility of electron accumulation in the channel of the CSDG MOSFET. Figure 5 (b) depicts the relative change in subthreshold swing concerning the gate length of the device. The effect of gate length variation has been clearly illustrated and the proposed device has been in an argument with the objective. The CSDG MOSFET falls under the 120 nm scaling of operation.

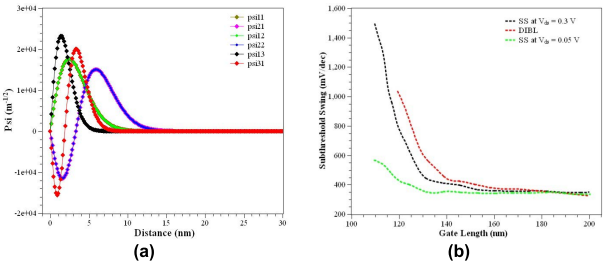


FIGURE 5. Performance of CSDG MOSFET (a) Wave function of the proposed CSDG MOSFET and (b) Subthreshold swing (SS) versus the gate length of the device.

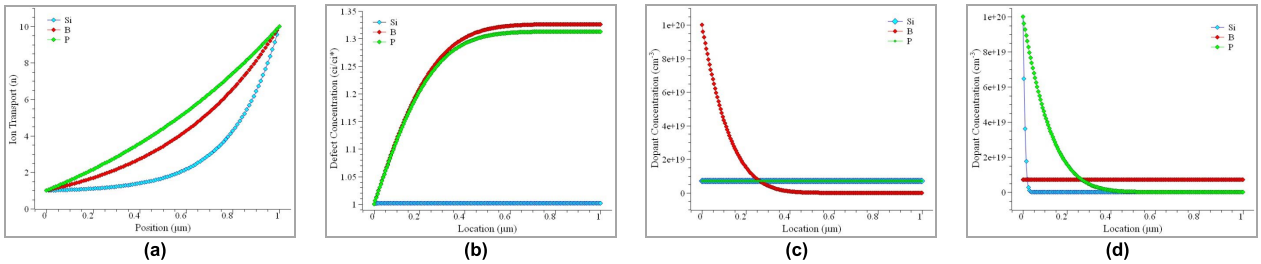


FIGURE 6. Ion transportation is based on Dopant diffusion using various dopants and its characteristics (a) ion transportation inside the cylindrical structure (b) Defect concentration based on doping (c) diffusion of n+ ions in the medium and (d) dopant concentration based on the diffusion.

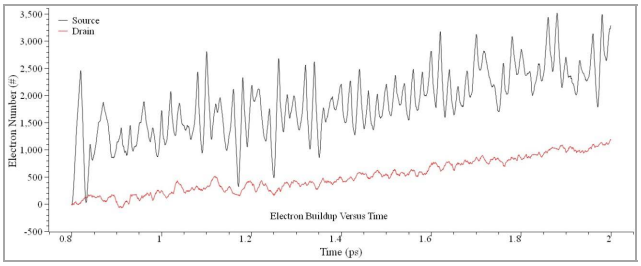


FIGURE 7. The relationship between electron buildup and the time for the CSDG environment.

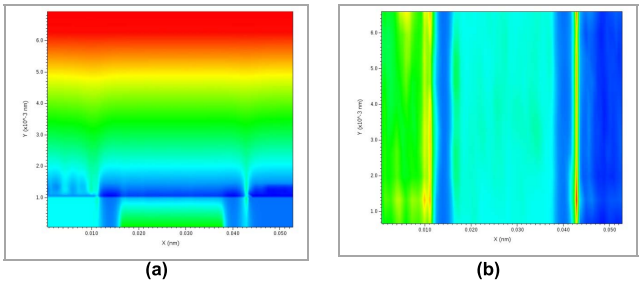


FIGURE 8. The simulation environment of the GD MOSFET. (a) front view of the double-gate MOSFET and (b) the top view of the MOSFET along the horizontal length.

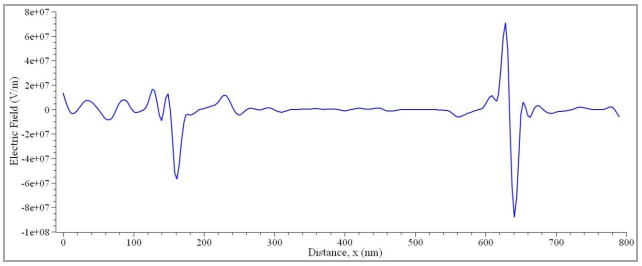


FIGURE 9. The variation of the electric field for the distance from the source terminal.

TABLE 2. Comparison of electron buildup at source and drain terminals.

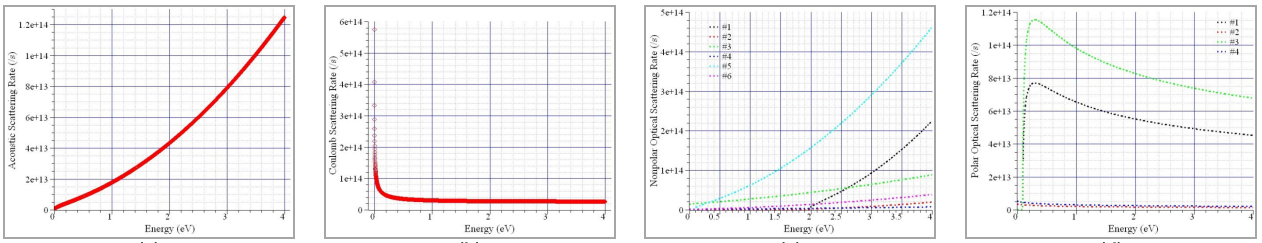
Time (ps)	Source (#)	Drain (#)
0.80	-21 (Absorption)	-14 (Absorption)
0.99	255	251
1.18	2069	281
1.25	501	163
1.30	1674	418
1.35	945	321
1.57	522	582
1.70	3072	861
1.90	2697	967
2.00	3287	1174

*Positive value indicates a buildup of electrons in the device

The ion transportation simulation has been carried out on a remote resource tool by queuing. The total time is calculated as queue time plus the computation time of the whole simulation. It is always unpredictable as it cannot be estimated. It may take several minutes to hours depending on the simulation parameters. The computation time is dependent on the settings chosen for the simulation and it takes usually *10-60 minutes*. The results of the ion transportation have been recorded and illustrated in fig. 6. The dopant diffusion is a process of introduction of dopant atoms in the gas form to the material using doped-oxide layers of cylindrical structures. The monotonical reduction of doping concentration in the chamber increases the chance of uniform distribution depending on the temperature and time taken for diffusion. Figure 7 shows the electron build-up concerning the time for the CSDG paradigm. Table 1 shows the comparison of the electron buildup between the source and drain terminals.

The simulation results of the DG MOSFET (the fundamental unit of CSDG MOSFET) have been illustrated in fig. 8. This exactly shows the variation of the electron buildup inside the device to exhibit the proposed performance. Figure 8(a) exemplifies the electron distribution after the simulation and fig. 8 (b) shows the channel.

Figure 9 displays the variations of the electric field concerning the distance from the source terminal in the channel of the device. The electric field in the cylindrical structure at the source terminal is observed at $1.35 \times 10^7\ Vm^{-1}$, $-1.65 \times 10^6\ Vm^{-1}$, $-1.16 \times 10^6\ Vm^{-1}$, and $-2.35 \times 10^6\ Vm^{-1}$ at 0 nm, *100 nm*, *400 nm*, and *700 nm*, respectively. The peak electric field of the MOSFET is witnessed at *630 nm* with a value of $6.37 \times 10^7\ Vm^{-1}$. The lowest value of $-8.57 \times 10^7\ Vm^{-1}$ has been detected at *640 nm*. The CSDG



(a) (b) (c) (d)

FIGURE 10. Recording of the scattering phenomenon of the proposed device (a) acoustic scattering rate (b) coulomb scattering rate (c) nonpolar optical scattering rate and (d) polar optical scattering rate concerning the energy level associated with the device.

TABLE 3. Comparison of conventional MOSFETs with proposed CSDG MOSFET.

MOSFET Device	Dielectric oxide	L_g(nm)	T_{ox}(nm)	I_{OFF} (μA/μm)	I_{ON}/I_{OFF}	ID_{max} (mA/μm)	G_m (mS/μm)
Chang et. al. [20]	Al_2O3, HfO_2, and HfAlO	60	8	1.8	1000	1.8	2.4
Pease et. al. [1]	HfSiON	15	2.3	0.01	7.73×10^{7}	2.57	0.60
Shahrjerdi et. al.[34]	Al_2O_3/InAlAs gate stack	90	5	5.5×10^{-4}	1.8×10^{3}	0.001	1.32
Duarte et. al. [39]	SiO_2	10	2	1	600	1.4	2.3
Kinoshita et. al.[12]	SiO_2	30	1	0.1	5140	0.514	1.2
Lin et. al.[14]	SiN	22	5	7.4	100	0.950	0.45
Dong S. Lee [42]	Al_2O_3	500	5	10×10^{-8}	8.13×10^{8}	0.813	0.25
This work	La_2O_3	5	2	0.03	290	5.4	8.4

MOSFET will be functional within a safe length of up to *500 nm* with a cylindrical structure. The optimum length of the device is restricted because of the tunneling effect and the skin effect which is present in the concentric structures.

Figure 10 shows the scattering rate with various input parameters concerning the energy associated with the CSDG MOSFET. The acoustic scattering rate has been shown in fig. 10(a) and the lowest available rate is noted at *0.001 eV* with a rate of $2.27 \times 10^{11}\ s^{-1}$. The peak rate goes as high as $2.27 \times 10^{14}\ s^{-1}$ at *4 eV*. The coulomb scattering is illustrated in fig. 10(b). The coulomb scattering rate has been normalized to $2.65\times10^{13}\ s^{-1}$ around *2.28 eV* and maintained till *4 eV*. The non-polar and the polar scattering rate has been shown in the comparison in fig. 10(c) and 10(d) for better understanding. These results support that the SNW is worth developing as a CSDG MOSFET and backings all the electrical characteristics to imply along with the cylindrical structure.

Table 2 shows the values associated with the simulation of CSDG MOSFET for the electron buildup time from source to drain terminal along the length of the channel. The electron buildup time is an essential factor in maintaining the observability and controllability of the device. The source terminal is insufficient for electrons at the beginning of the biasing. The drain terminal accumulates enough electrons to control the device after a certain time of electron buildup as shown in Figure 7. Table 3 was recorded by comparing various conventional methods of device design with the proposed CSDG MOSFET with high-ƙ dielectric materials. This is evident that the arbitrary alloy semiconductor along with high-kappa (ƙ) value materials works well and is submissive to the argument.

V. CONCLUSION AND FUTURE RECOMMENDATIONS

The proposed method has been validated and the results have been obtained. The results were in agreement with the CSDG MOSFET design and are suitable for the fabrication process. The encoded nanowire growth and appearance through VLS and Etching (ENGRAVE) serves as a fundamental unit for the various SNW growth and the device performance enhancement. This can be used as a scaffold and template for building various SNWs with any nanomaterials. Using materials beyond P-doped Si to produce ENGRAVE structures would open the door to new applications. The oxidant concentration plays a major role in performing uniform oxidation in the cylindrical walls of the heterostructure. The maximum oxidant concentration is observed to be $4.37 \times 10^{16}\ cm^{-3}$ of thickness *0.82 nm* for (100) and $2.56\times10^{19}\ cm^{-3}$ of thickness *0.33 nm* for (100) at dry oxidation and wet oxidation, respectively. The resultant circuit is ready to bake in the chamber with cylindrical dimensions.

In the future, Si-doped P-type semiconductor material with arbitrary alloys can be used to make the CSDG MOSFET work in a low RF environment with enhanced performance. The performance evaluation can be done with uniform and halo doping density by taking phonon scattering into account. The other dopants such as B or P can be used in place of Si. This gives future insights into the CSDG regime with enhanced characteristic performance, towards nanotechnology.

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NAVEENBALAJI GOWTHAMAN (Senior Member, IEEE) received the B.E. degree in electronics and communication engineering from Anna University, Tiruchirappalli, Tamil Nadu, India, in 2011, and the M.E. and Ph.D. degrees in VLSI design from Anna University, Chennai, in 2013 and 2019, respectively.

He has worked on the VLSI circuit design using electronic simulators. He is currently a Postdoctoral Research Scholar with the Department of Electronic Engineering, Howard College, University of KwaZulu-Natal, Durban, South Africa. His research interests include cylindrical surrounding double-gate MOSFETs, low-power VLSI circuits, testing of VLSI circuits, and digital electronics. He has more than seven years of teaching and research experience in VLSI design, microprocessors, and microcontrollers. He has supervised various bachelor's and master's projects. He has authored or coauthored more than 100 technical offerings, including articles in international refereed journals, book chapters, and international/national conferences. He has co-edited a book in the title *Advanced Controllers for Smart Cities—An Industry 4.0 Perspective* (Springer Nature, Switzerland AG), which presents applications of advanced microcontrollers that, can control large systems and devices.

Dr. Gowthaman has become an Active Member of IEEE Smart Grid and Smart City Community, India Chapter. Also, he is a member of ISTE, India (a Life Member), IETE, India (a Life Member), and IAENG (a member). He was a recipient of Best Teaching Faculty ('17), Innovative Research and Dedicated Teaching Professional Award ('18), Young Scientist ('18), Outstanding Researcher Award ('18), and Bright Engineer Award ('19). He is an Associate Editor and a Reviewer in many reputed peer-reviewed journals, including IET (C&DT) and Springer (P&UC).

VIRANJAY M. SRIVASTAVA (Senior Member, IEEE) received the bachelor's degree in electronics and instrumentation engineering, in 2002, the master's degree in VLSI design, in 2008, and the Ph.D. degree in the field of RF microelectronics and VLSI design, in 2012.

He has worked on the fabrication of devices and the development of circuit design. He is currently working with the Department of Electronic Engineering, Howard College, University of KwaZulu-Natal, Durban, South Africa. He has more than 20 years of teaching and research experience in the area of VLSI design, RFIC design, and analog IC design. He has supervised various bachelor's, master's, and doctorate theses. He is a Professional Engineer of ECSA, South Africa, and a Life Member of IEEE-HKN, a Senior Member of SAIEE, and a member of IET and IITPSA. He has worked as a reviewer for several journals and conferences, both national and international. He is the author/coauthor of more than 300 scientific contributions, including articles in international refereed journals and conferences, and also the author of various books.