IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received 20 September 2022, accepted 16 October 2022, date of publication 19 October 2022, date of current version 25 October 2022.

Digital Object Identifier 10.1109/ACCESS.2022.3215544

RESEARCH ARTICLE

Low Noise, High PSRR, High-Order Piecewise Curvature Compensated CMOS Bandgap Reference

XIMING FU[1], DALTON MARTINI COLOMBO[2], (Member, IEEE), YADONG YIN[3], AND KAMAL EL-SANKARY[1], (Senior Member, IEEE)

[1]Department of Electrical and Computer Engineering, Dalhousie University, Halifax, NS B3H 4R2, Canada
[2]Electrical Engineering Department, Federal University of Minas Gerais, Belo Horizonte 31270-901, Brazil
[3]School of Physics and Information Engineering, Fuzhou University, Fuzhou, Fujian 350025, China

Corresponding author: Ximing Fu (xm954365@dal.ca)

ABSTRACT A Bandgap reference (BGR) circuit with a new high-order curvature-compensation technique is proposed in this paper. The curvature method operates by adding up two correction voltages. The first one is proportional to the difference in gate-source voltages of two MOS transistors (ΔV_{GS}) operating in weak inversion mode, while the second one (V_{NL}) is generated using a nonlinear current created by a piecewise-linear circuit. To improve the power supply rejection ratio (PSRR) and the line regulation performance, a low-power pre-regulator isolates the circuit power supply and BGR output. Additionally, the chopping technique reduces the output voltage noise and offset. Consequently, the overall PVT robustness of the proposed circuit is significantly improved. The circuit was implemented using a thick-oxide transistor in a standard 0.18 μm CMOS technology with a 3.3 V power supply voltage. The silicon results exhibit a temperature coefficient of 5-15 ppm/°C in the temperature range of -10 °C to 110 °C, whereas the simulated results demonstrate a similar performance within the temperature range of -40 °C to 150 °C. The supply current consumption is 150 μA, and the chip area is 0.56×0.8 mm^2. The measured peak noise at the output is 1.42 $\mu V/\sqrt{Hz}$ @320 Hz, the measured PSRR @ 1 kHz is -80 dB, and the line regulation performance is 10 ppm/V, making the proposed circuit suitable for applications requiring low noise, high-order temperature compensation, and robust PVT performance.

INDEX TERMS Pre-regulator, BGR, curvature compensation, low-power operation, low area, subthreshold, temperature coefficient.

I. INTRODUCTION

The voltage reference is essential for many analog and mixed-signal electronic devices. Such devices include data converters, power management controllers (LDOs and DC-DC converters), oscillators, and phase-locked loops that rely on voltage references that have low-temperature coefficient (T.C.) and high-power supply rejection ratio (PSRR). Moreover, high line/load regulation, low noise, and robustness against the impact of fabrication process effects are also highly desired. Most of these applications require high accuracy, resulting in challenging specifications for the voltage reference design.

The first 1st order temperature compensated BGR circuit was proposed by Widlar and Brokaw [1], [2] in the 1970s. Due to the nonlinearities of voltage V_{BE} temperature compensation is usually limited to 30–100 ppm/°C for first-order temperature compensated references. Several high-order curvature correction compensation techniques have been proposed to overcome the temperature variations limitation of 1st order voltage references [3], [4], [5], [6], [7], [8], [9].

Among them are the quadratic temperature compensation [9], exponential temperature compensation [10], piecewise-linear curvature correction [11], [12], [15], [16],

The associate editor coordinating the review of this manuscript and approving it for publication was Yuh-Shyan Hwang.

[17], [18], [19], [20] and resistor temperature compensation [13], [14]. The continuous-time feedback technique is employed in [15] to reduce noise and offset. The proposed BGR temperature coefficient compensation technique includes five pieces of linear compensation, including a buffer circuit, five V-I converters, and four current subtraction circuits, with an Opamp for each V-I converter. In [17], the adjusted piecewise temperature compensation circuit implements an accurate reference voltage with a good temperature coefficient over a wide temperature range. However, there are no essential techniques for mitigating Opamp noise, offset, and improving PSRR and line regulation performance. In [18], the curvature compensation current has been divided up into multiple parts for fine-tuning. This strategy may be a challenge regarding the stability of the loop. Moreover, the circuit requires multiple clock sequences to operate, resulting in additional (not for the BGR core) circuitry, signals, silicon area, and power consumption – which may be impossible for certain applications.

Besides an excellent temperature coefficient, another critical design specification for voltage references is the output noise at the BGR output. It means that the circuit must be designed to minimize the noise of the internal device (e.g., thermal and flicker noise) and mitigate the noise coming from the supply lines – which is quantified by the PSRR parameter. Furthermore, an excellent line-regulation performance is also demanded to protect the output voltage from DC supply voltage variations. Those mentioned performance parameters are especially important for modern SoC, including high-performance and high-resolution circuits.

One of the main techniques to enhance PSRR and line regulation is the inclusion of cascode or self-cascode structures [10]. Some other approaches have been developed to improve the PSRR of BGR, such as the supply independent current source technique [21], [22], pseudo floating voltage source technique [23], and voltage follower technique with PMOS as input transistor [24].

To summarize the previous analysis, many previously mentioned techniques focus only on generally 1-2 aspects of design specifications for BGR references. In this work, we proposed a BGR topology that employs a new curvature correction method that employs existing methods in a different and optimized way. The temperature performance is achieved at the same time with other important specifications, such as low noise, PSRR, and line regulation. As a result, the proposed circuit is a good candidate for high-resolution and high-performance applications.

II. PROPOSED BGR: AN GENERAL VIEW

Fig. 1 illustrates the system architecture of the proposed BGR. It consists of a non-overlapping clock with the chopper block, a pre-regulator to generate the isolated power supply to the BGR core, and an output buffer with a switched R-C filter. The proposed BGR can cancel high-order nonlinearities of the output voltage by adding two correction voltages at the output node. The first one, named ΔV_{GS} compensation, is generated using the difference of gate-source voltages of two MOS transistors operating in weak inversion mode. The second one, named V_{NL}, is generated using a piecewise nonlinear current compensation unit. These correction voltages have an opposite high-order temperature coefficient to those nonlinear terms generated by the BJT transistor employed in the majority of BGR architectures.

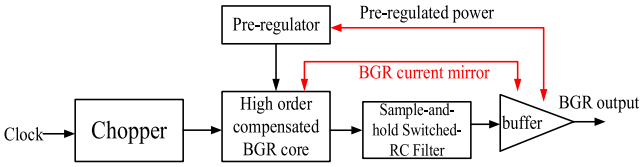


FIGURE 1. Block diagram of the proposed BGR system-level architecture.

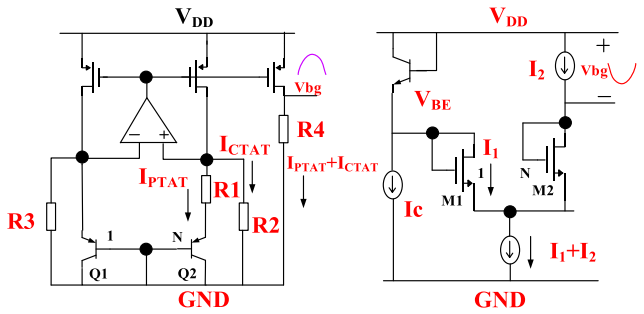


FIGURE 2. (a) 1st order BJT BGR (b) 1st order CMOS BGR [20].

The proposed pre-regulator creates a shielding effect between the main power supply and the BGR output by generating an isolated and process/temperature-insensitive supply voltage for the BGR core. As a result, high PSRR and excellent line regulation are achieved. A low noise unity gain output buffer was included at the output node to drive a load current within 1-2 mA. The buffer is biased by the pre-regulator output voltage and was designed with a large area input transistor to reduce its offset voltage. Consequently, the offset voltage of the output buffer is negligible and does not degrade the temperature performance of the BGR. Additionally, the chopping technique is employed in the BGR architecture to reduce the flicker (1/f) noise and the input offset of the Opamp, thus generating a precise and low noise output voltage. Finally, a sample-and-hold (S/H) switched-RC notch filter is included before the buffer output node to reduce the residual chopping ripple generated by the chopping technique.

This paper is organized as follows: Section III presents the operating principles of the proposed BGR, while its circuit topology is shown in Section IV. Section V focuses on the pre-regulator circuit design with offset and noise reduction by using the chopping technique. Section VI shows the experimental results with the performance table summary and a comparison with the state-of-art works. Section VII concludes the paper.

III. PROPOSED BGR: FUNDAMENTAL THEORY

As it is shown in Fig. 2(a), a standard 1st order BGR uses a bipolar transistor to generate a voltage that is, in the first order, complementary proportional to the absolute temperature (CTAT). Also, the difference between two base-emitter voltages (ΔV_{BE}) is used to generate a voltage proportional to the absolute temperature (PTAT). In Fig. 2(a), ΔV_{BE} and V_{BE} voltages are converted into two currents, I_{PTAT} and I_{CTAT}. In order to determine the reference output voltage, the sum of currents I_{PTAT} and I_{CTAT} is multiplied by the output resistance R4. The mathematical description of the temperature behavior of the output voltage shown in Fig. 2(a) is described by:

$$V_{ref} = V_{PTAT} + V_{CTAT} = (\frac{kTln(N)}{qR1} + \frac{V_{EB1}}{R2,3})R_4 \quad (1)$$

$$V_{EB}(T) = V_{G0}(T_R) - (V_{G0}(T_R) - V_{EB}(T_R))\frac{T}{T_R} - (\eta - \delta)V_T ln(\frac{T}{T_R}) \quad (2)$$

$$V_G(T) = V_{G0} - bT - cT^2 \quad (3)$$

In equation (2), $V_{G0}(T_R)$ is the bandgap voltage at the reference temperature T_R, T_R is the reference temperature, η depends on the structure of NPN or PNP and is a constant, which is approximately about 3.54. Parameter δ is the order of the temperature dependence of the collector current. Where V_{G0} is 1.17885 V to 1.20595 V, b is 9.025×10^{-5}V/K to 2.7325×10^{-4} V/K, c is 3.05×10^{-7} V/K^2 to 0 if the temperature is in the range of 150 K (−123 °C) to 400 K (127 °C) [26]. Note that they are positive constants. When the collector's current of the PNP transistor increases linearly with temperature T, $\delta = 1$; but when it is not related to the temperature T, $\delta = 0$. In equation (2), $(V_{G0}(T_R) - V_{EB}(T_R))\frac{T}{T_R}$ is the first-order temperature-dependent part, and $(\eta - \delta)V_T ln(\frac{T}{T_R})$ is the high-order nonlinearity. Due to the higher-order nonlinearities from the V_{EB} shown in equations (2)-(3), the temperature compensation is limited for the 1st order BGRs.

By grouping the nonlinear terms inserted by V_{EB} (equation 2) into equation 1, $V_{ref\_nonlinear}$ can be written as:

$$V_{ref\_nonlinear} \approx \frac{R4}{R2}V_{EB1}(T) \approx \frac{R4}{R2}[f(T)] \quad (4)$$

$$f(T) = -cT^2 - (\eta - 1)\frac{kT}{q}ln\left(\frac{T}{T_R}\right) \quad (5)$$

Equation $f(T)$ details the high order terms of (4). Taking the simplified Taylor series expansion of the term ln(T) at T_R Equation (5) can be rewritten as (6):

$$ln(T) \approx (T-1) - \frac{(T-1)^2}{2} + \frac{(T-1)^3}{3} - \frac{(T-1)^4}{4} \cdots\cdots$$
$$f(T) \approx \left[-c - 2(\eta - 1)\frac{k}{qT_R}\right]T^2 + (\eta - 1)\frac{k}{2qT_R^2}T^3 \quad (6)$$

Note also that the second-order term $[-c-2(\eta-1)\frac{k}{qT_R}]T^2$ has a negative sign, and therefore, it explains the main reason for the limited temperature compensation and the concave down parabola curve of a 1st BJT BGR.

To get a lower temperature coefficient reference voltage for high-resolution applications, a typical 2nd order compensation, namely exponential curvature compensation for $V_{EB}(T)$ is applied as it is shown in Fig. 3. The emitter-base voltages V_{EB}(T) of Q1 and Q3 can be written as the following:

$$V_{EB3}(T) = V_G(T) - (V_G(T_R) - V_{EB}(T_R))\frac{T}{T_R} - (\eta)V_T ln(\frac{T}{T_R}) \quad (7)$$

$$V_{EB1}(T) = V_G(T) - (V_G(T_R) - V_{EB}(T_R))\frac{T}{T_R} - (\eta - 1)V_T ln(\frac{T}{T_R}) \quad (8)$$

The emitter current flows from Q3 is approximately temperature independent ($\delta = 0$), while the emitter current from Q1 has a positive temperature dependence ($\delta = 1$). Thus, the difference between these voltages, $\Delta V_{EB1,3}$, is nonlinear and can be written as follows:

$$\Delta V_{EB1,3} = V_{EB1}(T) - V_{EB3}(T) = \frac{kT}{q}ln\left(\frac{T}{T_R}\right) = V_{cmp} \quad (9)$$

As a consequence, the output voltage of the circuit in Fig. 3 becomes:

$$V_{bg} = R_6(\frac{\Delta V_{EB1,2}}{R_2} + \frac{V_{EB1}}{R_3} + \frac{\Delta V_{EB1,3}}{R_4}) = \frac{R_6}{R_3}(\frac{R_3}{R_2}\Delta V_{EB1,2} + V_{EB1} + \frac{R_3}{R_4}V_{cmp}) \quad (10)$$

where, $\Delta V_{EB1,3}$ is a nonlinear voltage with a positive temperature coefficient, and it can be used to compensate for the transistor emitter-base voltage nonlinear temperature-dependent term in V_{EB} described by (6), as long as $\frac{R_3}{R_4} = \eta - 1$. The compensation is done by satisfying the following equation:

$$\frac{R_6}{R_3}([-c - 2(\eta - 1)\frac{k}{qT_R}]T^2) + \frac{R_6}{R_4}V_{cmp} \approx 0 \quad (11)$$

However, since $V_{cmp}(\Delta V_{EB1,3})$ is a curvature compensation voltage; it is more susceptible to the effects of the fabrication process. Referring again to the circuit of Fig.3, since a second-order exponential voltage is added to the output voltage equation, the temperature dependency of the output becomes similar to an approximately "sinusoidal" curvature corrected shape instead of a concave down parabola. As a result, a reduced and better TC is achieved. However, the compensation voltage increases dramatically with the temperature increase and may be problematic if not restricted to a specific temperature range. This approach may not be adequate for BGR operating in extended temperature ranges. The proposed BGR architecture also solves this limitation by generating a correction current for a specific range of low temperatures using a piecewise compensation unit. An alternative way to generate the PTAT voltage is by using the

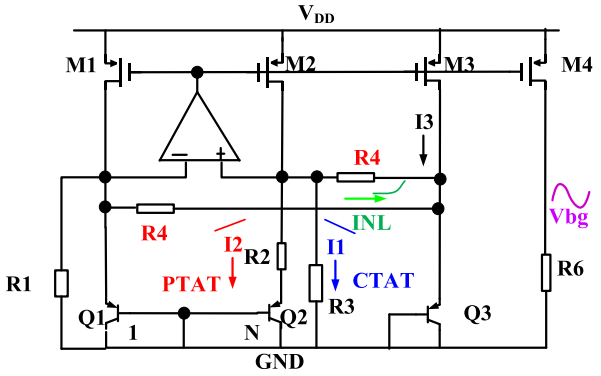


FIGURE 3. Conventional 2nd order exponential compensated BGR [21].

difference of gate-source voltage difference (ΔV_{GS}) between two MOSFETs operating in weak inversion mode. Fig. 2(b) is an example of architecture that employs this strategy. The output voltage of this circuit is described by (12). The only difference between (1) and (12) is the way to generate the PTAT voltage. The proposed BGR architecture also generates a PTAT voltage using ΔV_{GS} as part of the proposed higher-order temperature compensation, as explained in the following section.

$$V_o = V_{BE} + \Delta V_{GS} = V_{BE} + \frac{nkT}{q} ln\left(\frac{I_{D1}(\frac{w}{L})_2}{I_{D2}(\frac{w}{L})_1}\right) \quad (12)$$

IV. PROPOSED HIGH ORDER COMPENSATION BANDGAP

The proposed high-order temperature-compensated bandgap reference employs two correction voltages: ΔV_{GS} and V_{NL}. The first is used for a high-temperature range, and the last is used for a low-temperature range. Figures 4 (a)-(e) demonstrate the simulated step-by-step process to achieve the temperature compensation and its mechanisms. In the sub-sections, it will be explained how these voltages are generated.

A. GENERATION OF THE CORRECTION VOLTAGE: ΔV_{GS} VOLTAGE

Many studies have been conducted on the weak inversion region for MOSFETs [7], [8], [9]. Equation (13) for the drain current of N-channel MOS (NMOS) operating in a weak inversion region can be written as:

$$I_D \approx \mu_n C_{ox} \frac{W}{L} (\frac{nkT}{q})^2 exp^{\frac{q}{nkT}(V_{GS}-V_{th})}(1 - exp^{-\frac{qV_{DS}}{nkT}}) \quad (13)$$

Under the condition of $V_{DS} \gg \frac{kT}{q}$, equation (13) can be simplified as equation (14):

$$I_D \approx \mu_n C_{ox} \frac{W}{L} (\frac{nkT}{q})^2 exp^{\frac{q}{nkT}(V_{GS}-V_{th})} \quad (14)$$

Rewritten and isolating V_{GS}:

$$V_{GS} = V_{th} + \frac{nkT}{q} ln \frac{I_D}{\mu_n C_{ox} \frac{W}{L} (\frac{nkT}{q})^2} \quad (15)$$

Therefore ΔV_{GS} can be solved as:

$$\Delta V_{GS} = \frac{nkT}{q} ln(\frac{I_{D4}(\frac{w}{L})_5}{I_{D5}(\frac{w}{L})_4}) \approx \frac{nkT}{q} ln(N) \quad (16)$$

where V_{GS} is the gate-source voltage, V_{th} is the threshold voltage, k is Boltzmann's constant, q is the electron charge, T is the absolute temperature, V_{DS} is the drain-source voltage, C_{ox} is the oxide capacitance per unit area, μ_n is the effective mobility of carriers in the channel, W is the gate width, and L is the gate length. Equation (16) would be ideally linear with temperature without the parameter "n". This parameter is a function of temperature, and it is one of the limitations of the first-order temperature compensation of BGRs that employ MOSFET in weak inversion mode [10]. According to Tsividis and Ulmer [1], the temperature dependence of "n" can be modeled as $n = E + FT + GT^2$, where E, F, and G are positive constants. Consider Fig. 5 and substituting n(T) into (16), and assuming $\frac{I_{D4}(\frac{w}{L})_5}{I_{D5}(\frac{w}{L})_4} = a$, for a > 1, the difference ΔV_{GS} can be rewritten as:

$$\Delta V_{GS} = \frac{EkT}{q} ln\,(a) + \frac{FkT^2}{q} ln\,(a) + \frac{GkT^3}{q} ln\,(a) \quad (17)$$

If ΔV_{GS} is converted to a current and injected on two resistors in series (R4 and R5, shown in Fig.7), the correction voltage becomes Equation (18):

$$V_{MOS}\,(T) = \frac{kT}{q} \frac{R4 + R5}{R0} k_6 \ln(k_7)(E + FT + GT^2) \quad (18)$$

The coefficients of the second-order term of (18) are positive. The previous analysis shows that MOS/BGR and BJT/BGR have inverse second-order temperature coefficients. In summary: (i) ΔV_{EB} voltage has a positive first-order coefficient, (ii) V_{EB} voltage has first-order, second-order, and third-order coefficients, all negative, and (iii) the temperature coefficients of the first, second, and third-order of ΔV_{GS} are all positive. Therefore, if both second-order temperature coefficient terms can be added through appropriate weights, high-order temperature compensation can be performed, and an improved BGR with a reduced temperature coefficient is achieved. Combining the output voltage of a first-order BGR and a voltage generated by ΔV_{GS} current, (19) is written.

$$V_{sum} = V_{PTAT} + V_{CTAT} + V_{MOS}\,(T) \quad (19)$$

As mentioned before, the third term of the above equation increases rapidly with the temperature, and thus, it should be restricted to a specific and short temperature range. It can be used, for instance, at high temperatures to compensate for the traditional output voltage reduction caused by the non-linearities of V_{EB}. For low temperatures and a reduced range, a nonlinear current compensation, named as V_{NL}, generated by a piecewise-linear circuit is employed, as discussed in sub-section B.

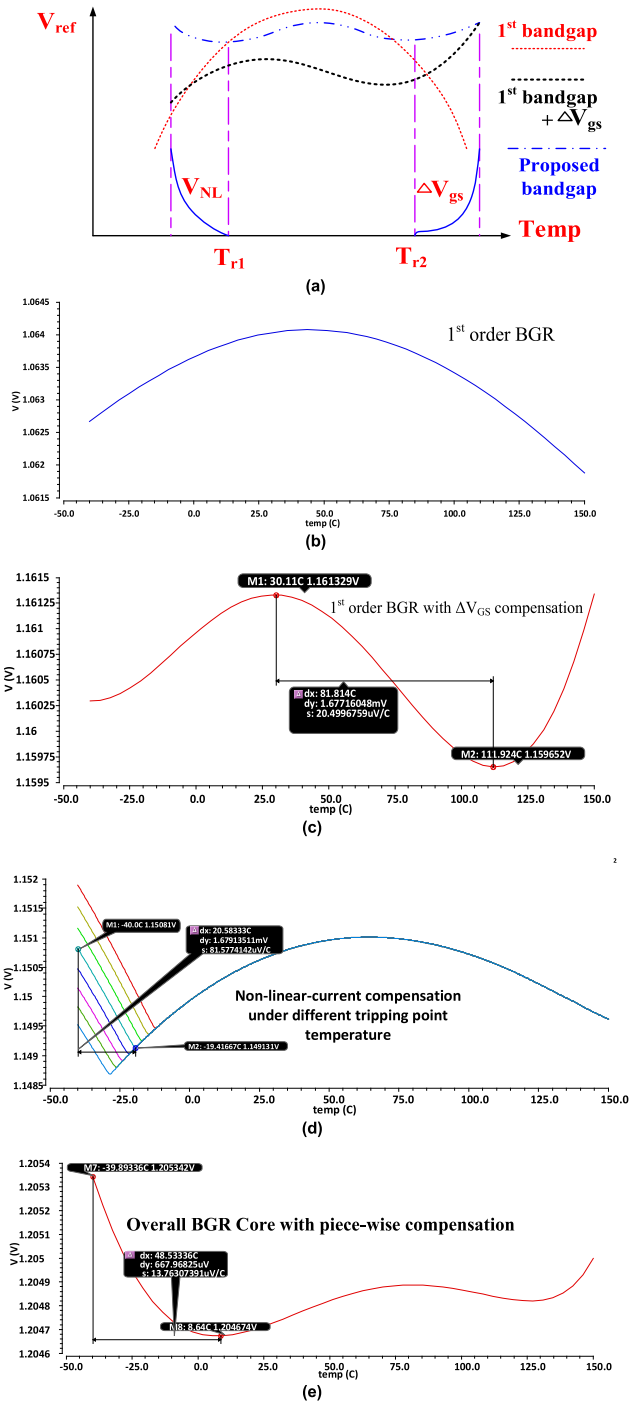


FIGURE 4. (a). The proposed curvature compensation main principle. (b) conventional 1st order BJT BGR (c) 2nd order temperature compensation with ΔV_{GS} compensation (d) temperature compensation in addition to nonlinear current compensation unit (e) temperature coefficient compensation for overall BGR core circuit.

B. GENERATION OF THE CORRECTION VOLTAGE: V_{NL} VOLTAGE

Voltage V_{NL} can be used to mitigate the reduction of the output voltage of the typical BGR. The generation of the nonlinear current compensation for low temperatures, as illustrated

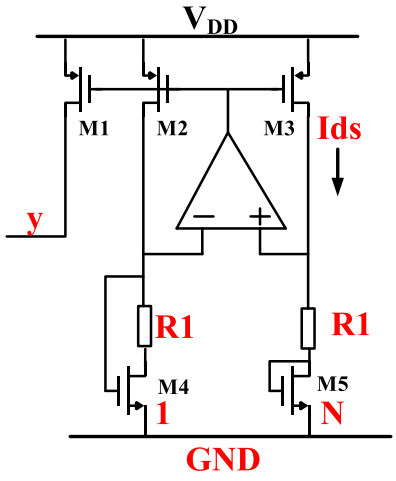


FIGURE 5. ΔV_{GS} compensation unit for the proposed BGR.

in Fig. 4, can be performed by the circuit shown in Fig. 6. Now consider currents I_{PTAT} and I_{CTAT} as given below:

$$I_{CTAT} = \beta_1 \frac{V_{EB}}{R2} \quad \text{and} \quad I_{PTAT} = \beta_2 V_T \frac{ln(N)}{R1} \tag{20}$$

where β_1 and β_2 are the gains of current mirrors formed by any 1st order BJT BGR, respectively. From Fig. 6 and Fig.7, consider that I_{CTAT} is from M24 and I_{PTAT} is from M25 for both nonlinear current compensation cells 1 and 2. The tripping point temperature $T_{r1}, T_{r2} \in (\sim -20\,°C\ -0\,°C)$ is designed by simulation optimization, where there is a temperature compensation between I_{CTAT} and I_{PTAT}, such as $I_{CTAT} = I_{PTAT}$. Therefore, when $T > T_{r1}$, $I_{CTAT} < I_{PTAT}$ and then $I_{NL} = 0$. But for $T < T_{r1}$, $I_{CTAT} > I_{PTAT}$, and $I_{NL} = I_{CTAT} - I_{PTAT}$. The current flowing in M_{26-27} can be written as:

$$I_{M26-27} = \begin{cases} \left(\beta_1 * \dfrac{VEB1}{R2} - \beta_2 * \dfrac{kTln\,(N)}{qR1}\right), & T < Tr1 \\ 0 & T > Tr1 \end{cases} \tag{21}$$

The output voltage Vref can be high-order temperature compensated for by injecting a piecewise-linear compensation current into the node "X," where there is a resistor called R5 connected. The compensation voltage VNL is then given by:

$$\text{VNL1} = \begin{cases} R5 * k3\left(k1 * \dfrac{VEB1}{R2} - k2 * \dfrac{kTln\,(N)}{qR1}\right), \\ \qquad T < Tr1 \\ 0 \quad T > Tr1 \end{cases} \tag{22}$$

$$\text{VNL2} = \begin{cases} R5 * k5\left(k1 * \dfrac{VEB1}{R2} - k4 * \dfrac{kTln\,(N)}{qR1}\right), \\ \qquad T < Tr2 \\ 0 \quad T > Tr2 \end{cases} \tag{23}$$

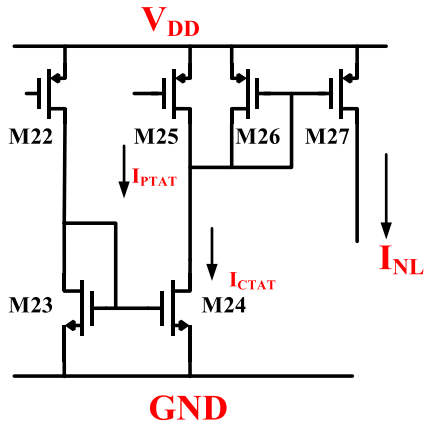


FIGURE 6. Nonlinear current compensation unit for the proposed BGR.

To further optimize the temperature coefficient, the nonlinear current unit cell is repeatedly used twice to provide more freedom in terms of optimization.

C. COMPLETE CIRCUIT

The proposed bandgap reference voltage can be written as follows:

$$V_{ref} = V_{1st\ roder} + \Delta V_{GS} + V_{NL1-2} \tag{24}$$

The complete circuit shown in Fig.7 contains the sub-circuits of figures 5 and 6 and implements equation (24). Its circuit topology is shown in figure 7. The resistor ratio between R3, R4, and R5 was designed to be 1:1:1. Note the node "X" and "Y", where the correction voltages are injected.

D. MONTE CARLO SIMULATION

The temperature performance of the proposed BGR was simulated over the fabrication process corners and using Monte Carlo Analysis, including process and mismatch variations, for 200 samples. Fig.8(a) presents simulated TCs for different MOSFET corners. The maximum variation in this simulation is 1.5 mV over the temperature range of −40 °C to 150 °C. The simulated results indicate that the process variation does not severely affect the reference voltage, and the proposed TC compensation robustness is guaranteed.

The Offset voltage Monte Carlo simulation is shown in Fig. 8(b). The BGR presents a worst-case scenario with a TC of 5-15 ppm/°. Its average mean value is 11.83 ppm/°. Figure 8(c) presents the histogram of TC with its average and standard deviation value.

V. PRE-REGULATOR CIRCUIT DESIGN AND FLICKER NOISE/OFFSET REDUCTION

The pre-regulator is an essential block that safeguards the BGR from fluctuations in the power supply line, guaranteeing a robust line regulation performance, high PSRR, and the effectiveness of the temperature curvature compensation. The pre-regulator is shown in Fig. 9 (a).

TABLE 1. Performance summary and comparison.

Parameter	This work	[18]	[17]	[5]	[4]
Year	**2022**	2021	2017	2015	2014
Technology	**0.18um CMOS**	0.13um CMOS	0.18um CMOS	0.13um CMOS	0.18um CMOS
Temperature range (°C)	**Meas: -10-110**	-40-150	-40-140	-40-120	-40-120
TC(ppm/°C)	**5-15**	5.8-13.5	1.67	9.3	3.4-6.9
Supply (V)	**3.3-2.7**	3.3	1.3-1.8	1.2	1.2
Reference votlage (V)	**1.2**	1.16	0.547	0.735	0.767
Power (μW)	**<150**	396	50	144	45
Line regulation(%/V)	**0.005**	0.03	0.08	----	0.054
Noise	**1.42 μV @320 Hz 112 μV (average noise)**	175 μV (average noise)	0.35 μV @700 Hz	200μV (average noise)	5.402μV @320 Hz
PSRR(dB @ DC)	**-80**	-82	------	-30 @100KHz	-80
Silicon Area mm^2	**0.448**	0.08	0.0094	0.063	0.036

The pre-regulator comprises its own BGR reference, a low-dropout regulator (LDO) with low quiescent current consumption, and a feedforward compensation to achieve high loop gain and small compensation capacitor C_{m1-2} silicon area. This solution provides a higher power-bandwidth efficiency when compared to the conventional simple Miller R_m-C_m compensation and successfully generates the power supply (V_{out} in Fig. 9 (a)) for the curvature-compensated BGR. The design equation for the current generation for the pre-regulator is given below. First, consider that M5 and M6 are operating in weak inversion mode.

Thus, the current flowing into M5 and M6 are described by:

$$I_{DS} \approx \mu_n C_{ox} \frac{W}{L} \left(\frac{nkT}{q}\right)^2 exp^{\frac{V_{GS}-V_{th}}{nV_T}} \tag{25}$$

Considering the loop M5-M6-R1, equation (26) is obtained:

$$V_{GS5} = V_{GS6} + I_s R_1 \tag{26a}$$

Using the equation (16) to describe the gate-source difference between M_5 and M6, current $I_{S.}$ is obtained:

$$I_s = \frac{\Delta V_{GS}}{R_1} = \frac{(V_{GS5} - V_{GS6})}{R_1} = \frac{nV_T ln\,(K)}{R_1} \tag{26b}$$

A. TEMPERATURE ANALYSIS

Fig. 9 (b) shows the output voltage of the voltage regulator. As can be seen, it is temperature compensated. Fig.9 (c) shows the BGR temperature performance as a function of VDD if the temperature-compensated voltage regulator was not employed. It was possible to see that the high-order temperature compensation proposed by this work would not be achieved. This observation is valid for several existing curvature correction techniques in literature and highlights one of the contributions of this work. The authors usually do not show the temperature compensation for different values of VDD.

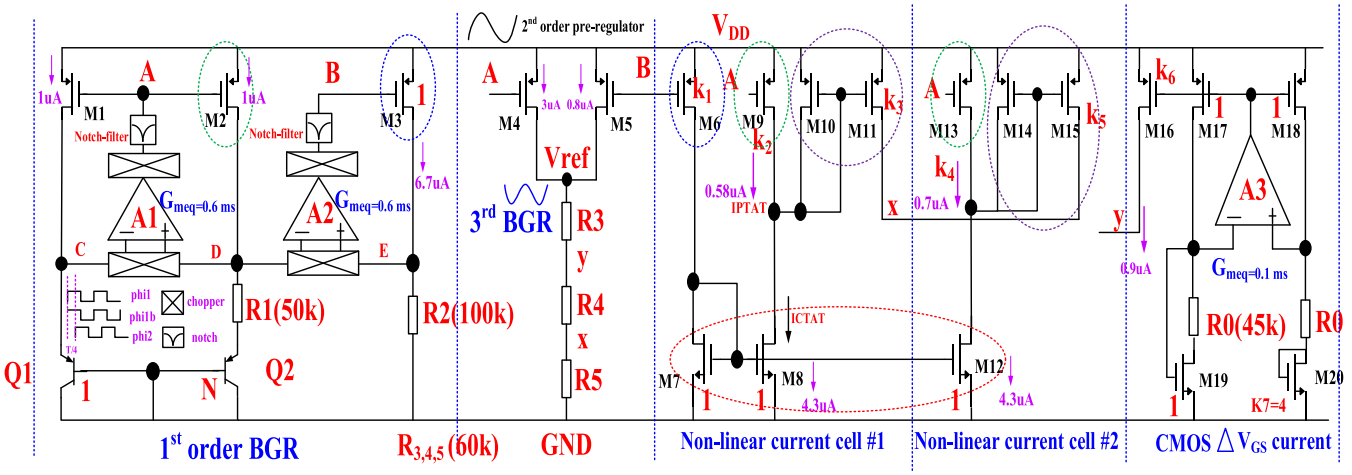


FIGURE 7. Overall BGR core circuit implementation.

Finally, Fig.9 (d) shows the output of the proposed BGR when the pre-regulator is included. The circuit can reject the supply voltage variations (2.7 V – 3.3V), making the circuit robust to PVT fluctuations. By introducing LHP zero along with Miller compensation, feedforward compensation improves the power-bandwidth efficiency of the pre-regulator; Fig.9 (e) illustrates the stability of the pre-regulator; the proposed pre-regulator has a small area, a high bandwidth efficiency, and low power consumption when driving small or moderate capacitive loads.

B. TRANSIENT AND PSRR ANALYSIS

Fig. 10 (a) shows the simulated transient response results of the proposed BGR assisted by the pre-regulator. It shows that the regulator improves the line-regulation performance of the BGR by making it robust against large AC variations in the supply line. The output voltage only changes by 1-2% for an input V_{DD} variation of 400 mV.

Fig.10 (b) presents the start-up process of the BGR reference and the proposed regulator. It shows that the pre-regulator's fast start-up process helps speed up the start-up of the BGR core. When considering the worst corner case (i.e., S.S.), the complete initialization takes just 20 μs.

In addition, the frequency domain perspective is shown in Fig.11. The simulated PSRR for the pre-regulator at 1kHz is about -77 dB, and the final BGR can achieve an improved PSRR of more than -100 dB lower than 100 Hz.

C. CHOPPING ERROR OPAMP USED TO MITIGATE OFFSET AND NOISE

The folded-cascode Opamp, shown in Fig.12, is the error amplifier used in the BGR core. The random input offset of this type of Opamp can be described as:

$$V_{os} = \Delta V_{th1,2} + \Delta V_{th4,5}\frac{g_{m4}}{g_{m2}} + \Delta V_{th8,9}\frac{g_{m8}}{g_{m2}} + \frac{V_{ov1,2}}{2}$$

$$* [\frac{\Delta\frac{W}{L}_{1,2}}{\frac{W}{L}_{1,2}} + \frac{\Delta\frac{W}{L}_{4,5}}{\frac{W}{L}_{4,5}} + \frac{\Delta\frac{W}{L}_{8,9}}{\frac{W}{L}_{8,9}}] \quad (27)$$

where ΔV_{th} and $\Delta\frac{W}{L}$ are the threshold voltage mismatch and the transistor sizes mismatch. From the noise perspective, the error amplifier (A_{1-2} refer to BGR Circuit in Fig.7) is the major dominant contributor according to the noise summary from simulation. The designed folded cascode amplifier reduces the dominant flicker noise (1/f) and the offset voltage by using the chopping technique. The method uses switches at three locations in the schematic: CH1, CH2, and CH3. CH1 switches are at Opamp's input terminal and modulate the input signal to the odd harmonics of the chopping frequency and then amplify it through the input stage. These CH1 switches are designed with small transistor sizes to reduce the impact of charge injection and clock feedthrough. Switches CH2 and CH3 are located at the low-impedance node of the cascode stage, and their sizes were increased to reduce their linear on-resistance and not reduce the voltage swing amplitude. Fig.7 also shows that the notch clock (phi2) is 90° delayed from the chopping clock (phi1) but with the same chopping frequency [25]. The notch filter is employed using the same structure as Fig. 14. Initially, the frequency of the noise integration is chosen such that the chopping frequency is two times the noise integration bandwidth, i.e., $F_{CHOP} > 2F_{NBW}$. Flicker noise is reduced by eliminating the need for degeneration resistance, typically used with M8-9 & M4-5 (refer to Fig.12) to reduce flicker noise, providing increased headroom for future technology advances.

Fig.13 presents the results of the Noise Spectrum simulation (e.g., PSS+Pnoise simulation using Cadence tools) to prove that the chopping error amplifier (EA) and the notch filter reduce the noise at the BGR output voltage. This figure shows two cases: chopper amplifier OFF and ON. As can be seen, the low-frequency noise is dramatically reduced when the chopper of the EA is ON for

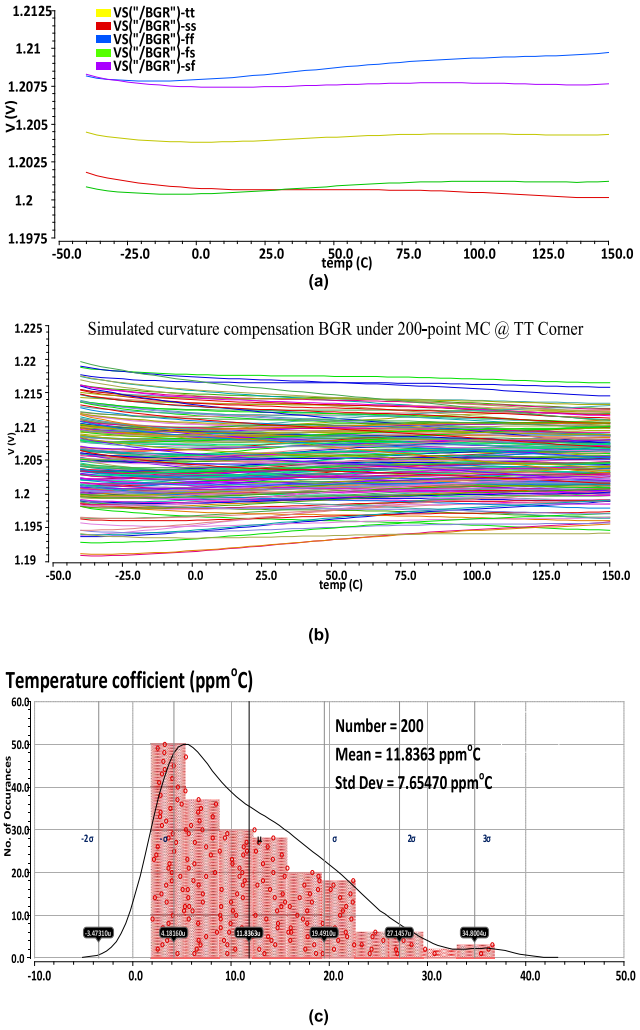


FIGURE 8. **(a). The simulated T.C. simulation results in different MOSFET corners (b). Simulated curvature compensation untrimmed BGR under 200-point MC, (c). Simulated curvature compensation BGR histogram statistics.**

different values of chopping frequencies. Regarding the variability of the output voltage, the complete expression for it considering offset voltages of A_{1-2} is given by equation (28):

$$V_{ref} = V_{1stroder} + \Delta V_{GS} + V_{NL1-2} + V_{os1}\frac{R_3 + R_4 + R_5}{R_1} + V_{os2}\frac{R_3 + R_4 + R_5}{R_2} \quad (28)$$

where V_{os1-2} are the offset voltage of A_{1-2} described by (27). Voltages V_{os1-2} are amplified by the resistor ratio, thus increasing the changes at the output voltage. Besides applying the chopping technique, a high DC gain and large input transistors have been employed to minimize random offset voltages. While a very symmetrical and compact layout can reduce the systematic offset.

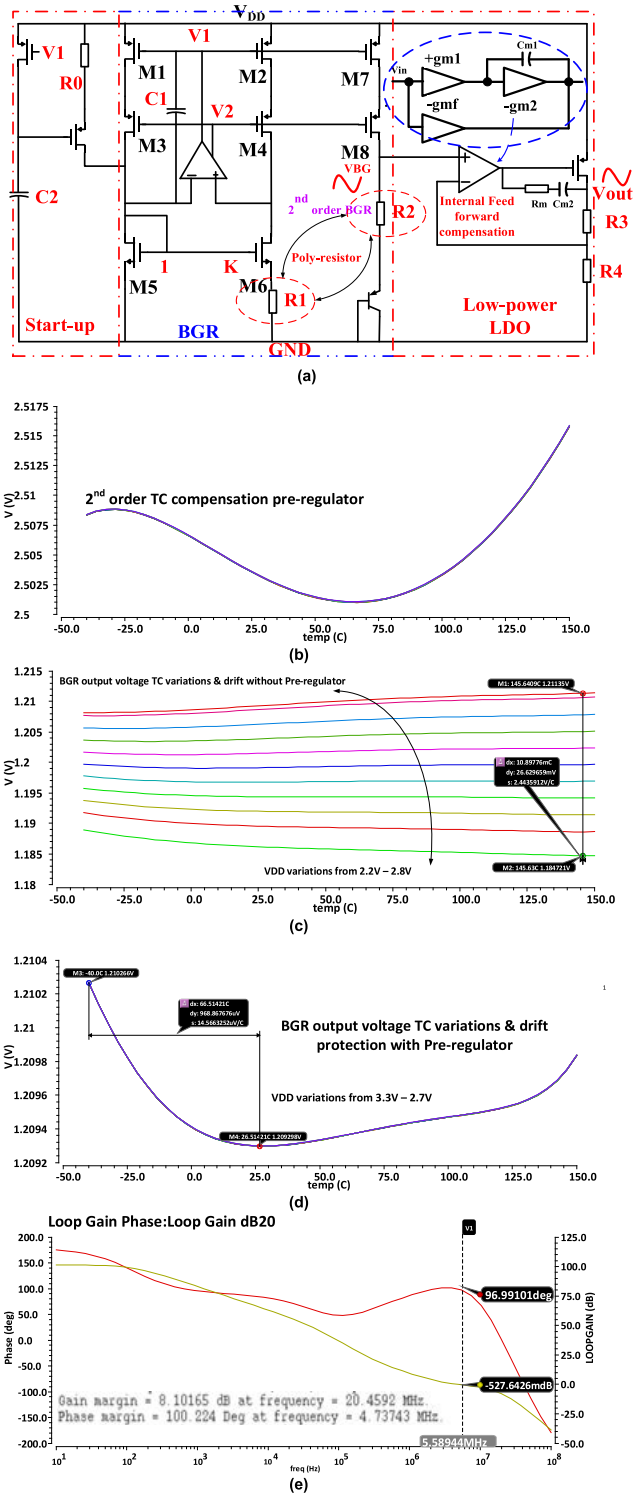
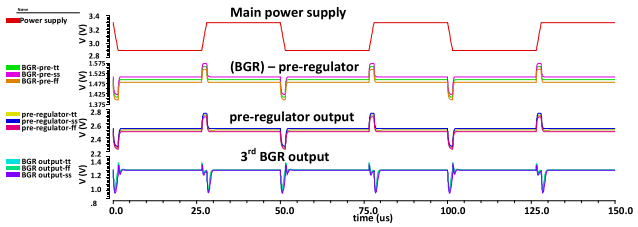


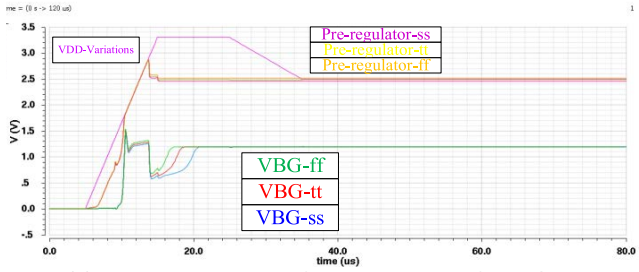
FIGURE 9. **(a). The proposed pre-regulator. (b) the 2nd order TC compensated pre-regulator output voltage (c) BGR output voltage drift & T.C. variations without pre-regulator assistance (d) BGR output T.C. variations & drift protections with pre-regulator assistance (e) LDO loop stability simulation.**

D. CHOPPING RIPPLE REDUCTION USING SWITCHED R.C. FILTER & OUTPUT BUFFER

To reduce the ripple at the output voltage caused by the chopping technique, a switched capacitor (S.C.) notch filter



(a). Transient simulation of line regulation enhancement of the BGR



(b). Transient simulation of start-up process of the BGR

FIGURE 10. (a) Transient simulation of line regulation enhancement of the BGR. (b) Transient simulation of start-up process of the BGR.

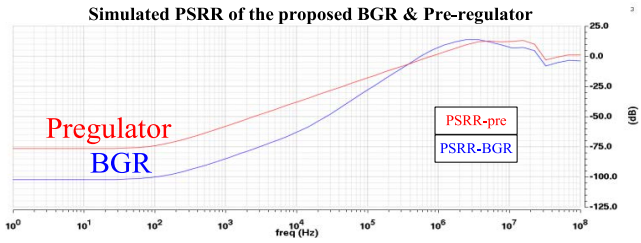


FIGURE 11. Simulated PSRR enhancement of the proposed BGR with pre-regulator protection.

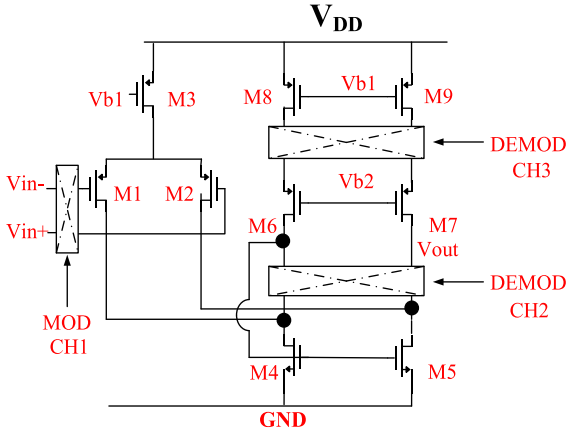


FIGURE 12. The Chopping Error Opamp (A_{1_2}) used in the proposed BGR.

was included at the input node of the output buffer. The notch filter is shown in Fig. 14 (c) and comprises a switched capacitor resistor shown in Fig. 14 (a).

The two transmission gates (S1 and S2) are controlled by non-overlapping clock signals, Φ1 and Φ2 (Fig. 14(b)). During phase Φ1, the input voltage is sampled onto C1,

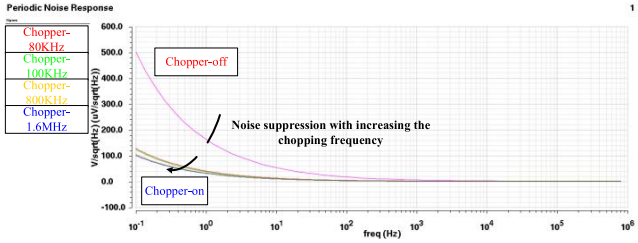


FIGURE 13. Analysis of the noise spectrum of the BGR before and after chopper & notch filters were activated.

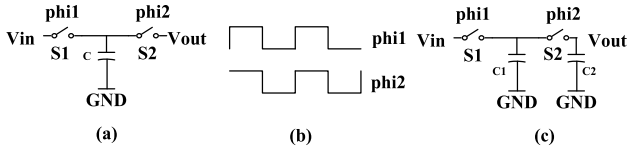


FIGURE 14. (a) Switched capacitor resistor; (b) non-overlapping clock; (c) low-pass notch filter.

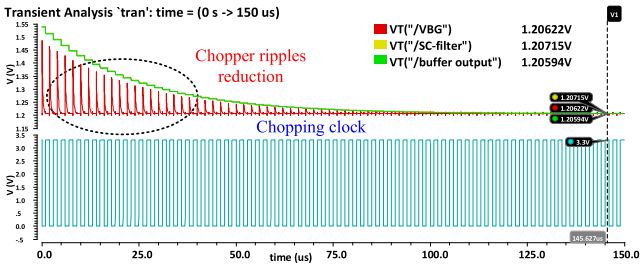


FIGURE 15. Sample and hold SC-filter for BGR output voltage ripples reduction.

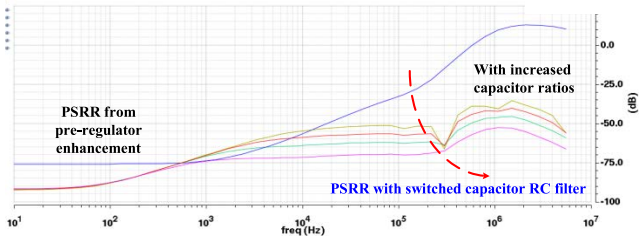


FIGURE 16. PSRR enhancement by adding output SC-low pass filtering.

while during phase Φ2, this ripple-free sampled voltage is transferred to C2. The advantage of the S.C. filter compared with the R.C. filter is that the frequency domain response of the first will introduce distinct notches at f_{chop}. Moreover, the harmonics of the S.C. filter can also improve the order of the LPF, saving a significant amount of area and achieving higher-order filtering and process-independent cut-off frequency. For an input x(t), the time-domain response y(t) for S.C. low-pass filter can be described as:

$$y(t) = \sum_{k=0}^{\infty} x(kT) * [u(t - kT) - u(t - (k + 1)T)] \quad (29)$$

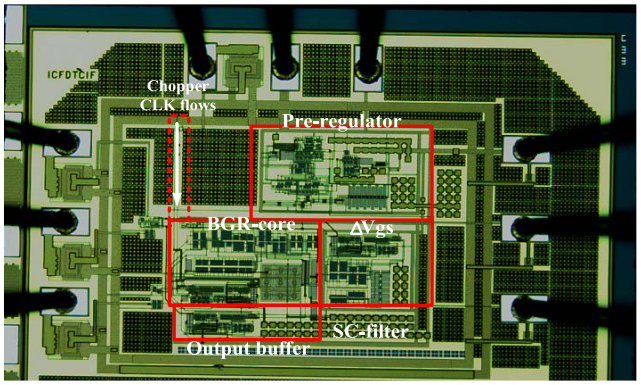


FIGURE 17. The microchip of the proposed bandgap.

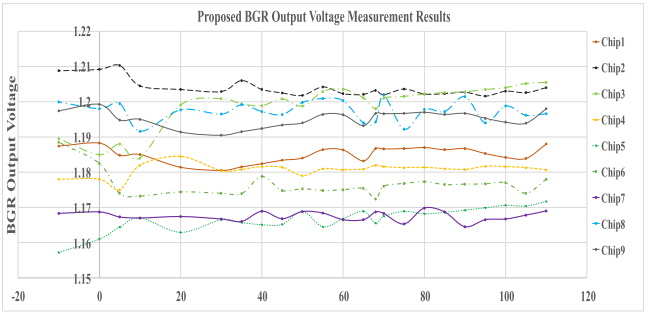


FIGURE 18. The proposed bandgap reference output voltage with temperature variations.

where $T = \frac{1}{f_{ch}}$ In the frequency (s) domain, (29) becomes:

$$Y(s) = \sum_{k=0}^{\infty} x(kT) * \left[\frac{exp^{-skT} - exp^{-s(k+1)T}}{s}\right] = \frac{1 - exp^{-sT}}{s}\left[\sum_{k=0}^{\infty} x(kT) exp^{-skT}\right] \quad (30)$$

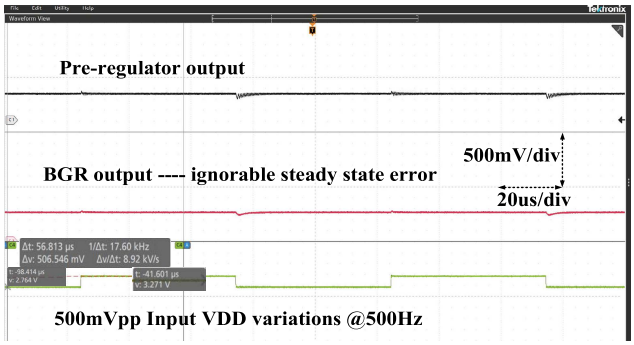
Thus, rewriting for the transfer function of the filter $H(s)$ from (30), we get:

$$H(s) = \frac{1 - exp^{-sT}}{s} \quad (31)$$

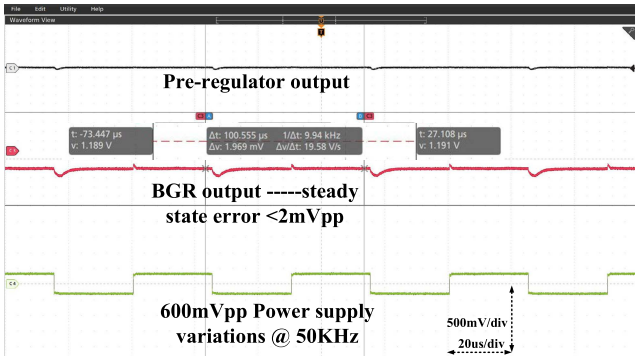
The filter loop bandwidth can also be calculated as the following:

$$\omega_{eq} = \frac{1}{R_{ch}C} = f_{ch}\frac{C_1}{C_2} \quad (32)$$

The transient response of the BGR output voltage before and after activating the SC filter is shown in Fig. 15. We can see that a considerable portion of ripples due to the chopper technique is reduced, showing the importance of the output SC-filter without much area penalty. Fig. 16 shows the PSRR simulation results of the proposed BGR. The high-frequency PSRR performance is improved by applying an output S.C. low pass filter, while the pre-regulator mainly protects the low-frequency PSRR.



(a). 500mVpp VDD voltage under with clock variations @ 500Hz



(b). 600mVpp VDD voltage under with clock variations @ 50KHz

FIGURE 19. (a) 500mVpp VDD voltage under with clock variations @ 500Hz. (b) 600mVpp VDD voltage under with clock variations @ 50KHz.

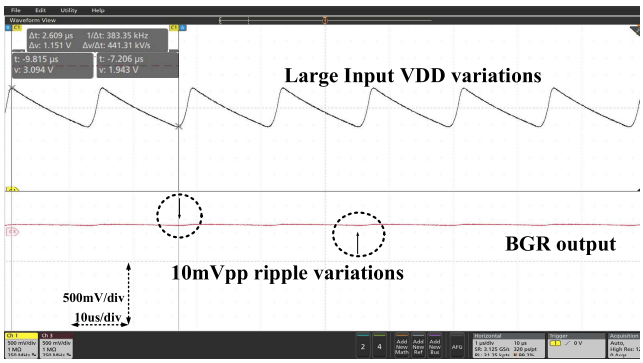


FIGURE 20. Transient VDD voltage variations with ramp variations.

E. FABRICATED CHIP AND SILICON AREA

Fig. 17 depicts a microphotograph of the proposed BGR implemented in 0.18 μm standard CMOS technology. The entire chip area is 0.56*0.8 mm^2.

VI. EXPERIMENTAL RESULTS

A. OUTPUT VOLTAGE AS A FUNCTION OF TEMPERATURE

For assessments of proposed BGRs, several specific non-ideal effects, such as thermal electromotive forces (EMFs), need to be considered. Therefore, it is essential to consider the equipment's errors as well. By alternating probes during each measurement at a given temperature point, each measurement is repeated ten times in order to reduce systematic error,

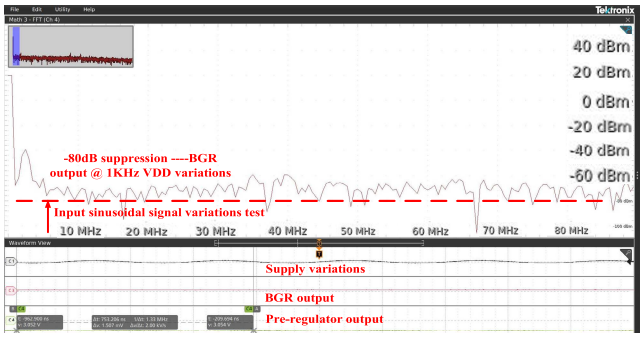
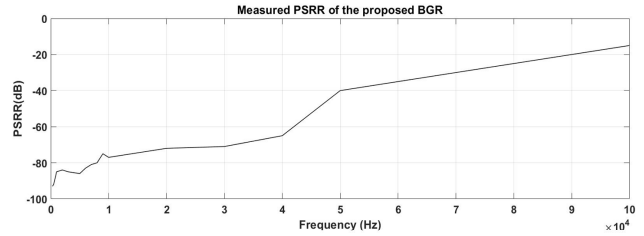
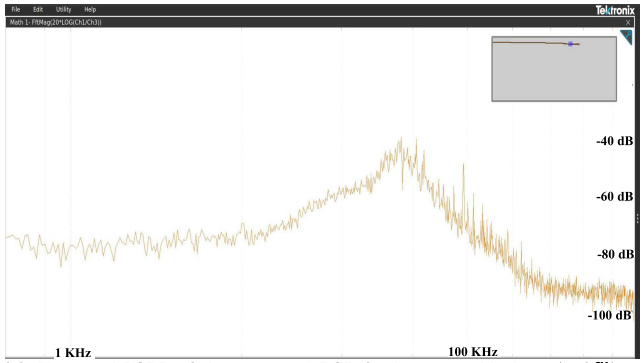


FIGURE 21. BGR output spectrum and its power supply noise rejection capability.



(a). Measured low-frequency PSRR of the proposed BGR without output filter



(b). Measured PSRR of the proposed BGR final output with the output filter

FIGURE 22. (a) Measured low-frequency PSRR of the proposed BGR without output filter. (b) Measured PSRR of the proposed BGR final output with the output filter.

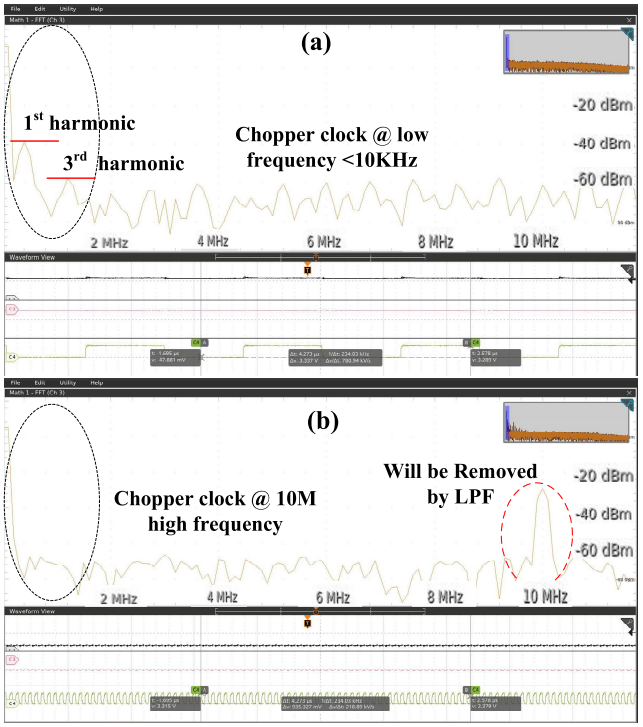
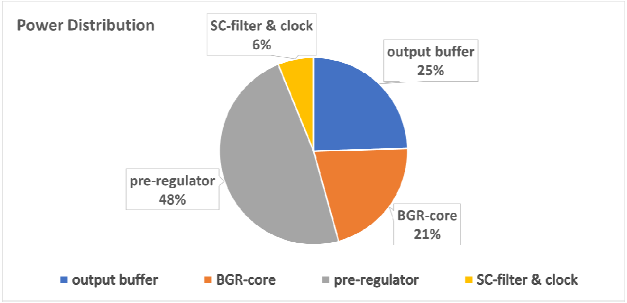
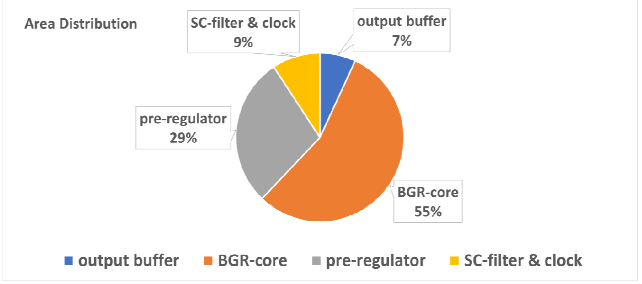


FIGURE 23. Measured functionality of chopper technique for flicker & D.C. offset the reduction.



(a)



(b)

FIGURE 24. (a) The proposed BGR power distribution, (b) The proposed BGR area distribution.

including several sources of systematic error, such as random offsets, mismatched BJTs, mismatched current mirrors, and mismatched resistors. Wires leading from the temperature chamber to V_{BG} are twisted together as differential wires in order to reduce spur and other common mode noise. (EMFs) can be reduced by using wires that are made from the same material and of the same length. The average value is then calculated from these ten measurements. Fig.18 illustrates the temperature behavior of the output voltage of the proposed BGR for nine samples extracted from varying in temperature from $-10°C$ to $110°C$ without trimming. The measured temperature coefficient is 5-15 ppm/°C, which is more precise than conventional 1st order BJT-BGR with concave-down parabola T.C. (e.g., usually 50-80 ppm).

Note that although the circuit presents some sample-to-sample variation, high-order temperature compensation is guaranteed without any trimming technique, which is the most important. The voltage variations are caused by the mismatch of the output resistor. If a very accurate output voltage is desirable, a simple trimming circuit can be added. However, two-point temperature calibration is not needed, and as a consequence, the trimming procedure is significantly simplified.

B. OUTPUT VOLTAGE AS A FUNCTION OF VDD VARIATIONS

The output response as a function of supply voltage variations was also measured and shown in Fig. 19-20. The power supply voltage was configured to operate as a periodical signal with 500 Hz and 50 kHz frequencies with amplitude variation of 2.7 V to 3.3V. The output variation under these conditions is less than 1%.

Fig. 20 shows a considerable V_{DD} variation (sawtooth variation), and its effect on the BGR output is still minimal. Therefore, the proposed BGR circuits can have strong immunity to power supply variations.

C. OUTPUT SPECTRUM AND PSRR PERFORMANCE

The measured BGR output spectrum and the PSRR performance are shown in Fig.21 and Fig.22, respectively. The V_{DD} voltage was measured at 3.3 V, and the PSRR value at DC and 1kHz frequency is −80 dB. The worst PSRR is −40.5 dB at 90 kHz.

D. OUTPUT NOISE AND POWER/AREA BREAKDOWN

Fig. 23 shows the measured noise PSD of the BGR for different chopping frequencies ($fchop = 10$KHz, $fchop = 10$MHz) at room temperature (27°C) with all noise sources considered. As can be seen, the chopping technique significantly mitigates the error amplifier's 1/f noise, which is dominant from 10 Hz to about 100kHz. The high chopping frequency ($f_{chop} = 10$MHz) shows a very effective chopping ripple reduction in the frequency domain. The ripple at 1st and 3rd harmonics is also reduced from −40dB to below −60dB, respectively.

Fig. 24 shows the breakdown of power and area for the proposed BGR. The pre-regulator, SC filter, and output buffer will significantly improve circuit performance at the cost of increased power consumption and area consumption.

Table 1 compares this proposed bandgap voltage reference with other prior-art curvature-compensation bandgap voltage references.

VII. CONCLUSION

This paper presents a novel high PSRR, low noise, and high-order curvature-compensated bandgap voltage reference with a measured temperature coefficient of 5-15 ppm/°C, and supply current consumption of 150 μA under a 3.3V power supply. The output buffer with a switched RC LPF is used to reduce the BGR noise further, save area and increase BGR PSRR. The chopping technique is applied in the error amplifier to significantly reduce the BGR output noise and input offset to allow the proposed BGR to work in low-noise applications. Finally, several silicon tests have been conducted to demonstrate the feasibility of the proposed curvature-compensated bandgap voltage reference.

REFERENCES

[1] Y. P. Tsividis and R. W. Ulmer, "A CMOS voltage reference," *IEEE J. Solid-State Circuits*, vol. SSC-13, no. 6, pp. 774–778, Dec. 1978.

[2] A. P. Brokaw, "A simple three-terminal IC bandgap reference," *IEEE J. Solid-State Circuits*, vol. SSC-9, no. 6, pp. 388–393, Dec. 1974.

[3] P. B. Basyurt and D. Y. Aksin, "Design of a curvature-corrected bandgap reference with 7.5 ppm/C temperature coefficient in 0.35 μm CMOS process," in *Proc. IEEE Int. Symp. Circuits Syst.*, Seoul, South Korea, May 2012, pp. 3142–3145.

[4] B. Ma and F. Yu, "A novel 1.2–V 4.5-ppm/°C curvature-compensated CMOS bandgap reference," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 61, no. 4, pp. 1026–1035, Apr. 2014.

[5] Q. Duan and J. Roh, "A 1.2–V 4.2-ppm/°C high-order curvature compensated CMOS bandgap reference," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 62, no. 3, pp. 662–670, Mar. 2015.

[6] J.-H. Li, X. Zhang, and M. Yu, "A 1.2-V piecewise curvature-corrected bandgap reference in 0.5 μm CMOS process," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 19, no. 6, pp. 1118–1122, Jun. 2011.

[7] P. Malcovati, F. Maloberti, C. Fiocchi, and M. Pruzzi, "Curvature-compensated BiCMOS bandgap with 1-V supply voltage," *IEEE J. Solid-State Circuits*, vol. 36, no. 7, pp. 1076–1081, Jul. 2001.

[8] Z.-K. Zhou, Y. Shi, Z. Huang, P.-S. Zhu, Y.-Q. Ma, Y.-C. Wang, Z. Chen, X. Ming, and B. Zhang, "A 1.6-V 25-μ A 5-ppm/° C curvature-compensated bandgap reference," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 59, no. 4, pp. 677–684, Apr. 2012.

[9] B.-S. Song and P. R. Gray, "A precision curvature-compensated CMOS bandgap voltage reference," *IEEE J. Solid-State Circuits*, vol. SSC-18, no. 6, pp. 634–643, Dec. 1983.

[10] T. Cao, Y. Han, X. Liu, H. Luo, L. Liao, and H. Zhang, "A 0.9-V high-PSRR bandgap with self-cascode current mirror," in *Proc. IEEE Int. Conf. Circuits Syst. (ICCAS)*, Kuala Lumpur, Malaysia, Oct. 2012, pp. 267–271.

[11] G. Rincon-Mora and P. E. Allen, "A 1.1-V current-mode and piecewise-linear curvature-corrected bandgap reference," *IEEE J. Solid-State Circuits*, vol. 33, no. 10, pp. 1551–1554, Oct. 1998.

[12] Y. Huang, L. Zhu, F. Kong, C. Cheung, and L. Najafizadeh, "BiCMOS-based compensation: Toward fully curvature-corrected bandgap reference circuits," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 65, no. 4, pp. 1210–1223, Apr. 2018.

[13] M. Gunawan, G. C. M. Meijer, J. Fonderie, and J. H. Huijsing, "A curvature-corrected low-voltage bandgap reference," *IEEE J. Solid-State Circuits*, vol. 28, no. 6, pp. 667–670, Jun. 1993.

[14] S. R. Lewis and A. P. Brokaw, "Curvature correction of bipolar bandgap voltage reference," U.S. Patent 4 808 908, Feb. 28, 1989.

[15] L. Liu, X. Liao, and J. Mu, "A 3.6 μV_{rms} noise, 3 ppm/°C TC bandgap reference with offset/noise suppression and five-piece linear compensation," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 66, no. 10, pp. 3786–3796, Oct. 2019, doi: 10.1109/TCSI.2019.2922652.

[16] R. Wang, W. Lu, M. Zhao, Y. Niu, Z. Liu, Y. Zhang, and Z. Chen, "A sub-1 ppm/°C current-mode CMOS bandgap reference with piecewise curvature compensation," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 65, no. 3, pp. 904–913, Mar. 2018.

[17] H.-M. Chen, C.-C. Lee, S.-H. Jheng, W.-C. Chen, and B.-Y. Lee, "A sub-1 ppm/°C precision bandgap reference with adjusted-temperature-curvature compensation," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 64, no. 6, pp. 1308–1317, Jun. 2017.

[18] K. Chen, L. Petruzzi, R. Hulfachor, and M. Onabajo, "A 1.16-V 5.8-to-13.5-ppm/°C curvature-compensated CMOS bandgap reference circuit with a shared offset-cancellation method for internal amplifiers," *IEEE J. Solid-State Circuits*, vol. 56, no. 1, pp. 267–276, Jan. 2021.

[19] J. Jiang, W. Shu, and J. S. Chang, "A 5.6 ppm/°C temperature coefficient, 87-dB PSRR, sub-1-V voltage reference in 65-nm CMOS exploiting the zero-temperature-coefficient point," *IEEE J. Solid-State Circuits*, vol. 52, no. 3, pp. 623–633, Mar. 2017.

[20] U. Kamath, E. Cullen, J. Jennings, I. Cical, D. Walsh, P. Lim, B. Farley, and R. B. Staszewski, "A 1 V bandgap reference in 7-nm FinFET with a programmable temperature coefficient and an inaccuracy of ±0.2% from −45°C to 125°C," in *Proc. IEEE 44th Eur. Solid State Circuits Conf. (ESSCIRC)*, Sep. 2018, pp. 78–81, doi: 10.1109/ESSCIRC.2018.8494284.

[21] S. Mehrmanesh, M. B. Vahidfar, H. A. Aslanzadeh, and M. Atarodi, "A 1-volt, high PSRR, CMOS bandgap voltage reference," in *Proc. Int. Symp. Circuits Syst.*, vol. 1, May 2003, pp. I-381–I-384.

[22] Y. Shi, S. Li, J. Cao, Z. Zhou, and W. Ling, "A 180 nm self-biased bandgap reference with high PSRR enhancement," *Nanosc. Res. Lett.*, vol. 15, no. 1, p. 104, Dec. 2020.

[23] H. Zhang, P. K. Chan, and M. T. Tan, "A high PSR voltage reference for DC-to-DC converter applications," in *Proc. IEEE Int. Symp. Circuits Syst.*, May 2009, pp. 816–819.
[24] A. Dey and T. K. Bhattacharyya, "A CMOS bandgap reference with high PSRR and improved temperature stability for system-on-chip applications," in *Proc. Int. Conf. Electron Devices Solid-State Circuits (EDSSC)*, Tianjin, China, Nov. 2011, pp. 1–2.
[25] R. Burt and J. Zhang, "A micropower chopper-stabilized operational amplifier using a SC notch filter with synchronous integration inside the continuous-time signal path," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2729–2736, Dec. 2006.
[26] Y. P. Tsividis, "Accurate analysis of temperature effects in I_c–V_{BE} characteristics with application to bandgap reference sources," *IEEE J. Solid-State Circuits*, vol. SSC-15, no. 6, pp. 1076–1084, Dec. 1980, doi: 10.1109/JSSC.1980.1051519.

XIMING FU was born in Lanzhou, China. He received the bachelor's and Master of Applied Science degrees in electrical engineering from Dalhousie University. He is currently pursuing the Ph.D. degree with the VLSI Research Group, Dalhousie University. He is also working in analog and RF mixed-signal IC design with the VLSI Research Group, Dalhousie University. His research interests include ultra-low power, low noise receiver design, such as SRO-RX, power management ICs, and high-performance PLL design.

DALTON MARTINI COLOMBO (Member, IEEE) received the B.Sc. degree in computer engineering from the Federal University of Itajuba, Brazil, in 2005, and the M.Sc. and Ph.D. degrees in microelectronics from the Federal University of Rio Grande do Sul, Brazil, in 2008 and 2015, respectively. In 2012, he was a Visiting Researcher with the SPICE Modeling Group, Texas Instruments, Dallas, TX, USA. He worked as an Analog and Mixed-Signal Integrated Circuit Designer with CEITEC-SA, Porto Alegre, Brazil, from 2013 to 2016. Since 2018, he has been a Professor with the Federal University of Minas Gerais, Brazil.

YADONG YIN received the B.S. degree in electrical engineering from Beijing Jiaotong University, Beijing, China, in 2003, and the Ph.D. degree in microelectronics from the Institute of Microelectronics, Chinese Academy of Sciences, Beijing, in 2009. He worked with the Institute of Microelectronics, Chinese Academy of Sciences, from 2009 to 2014. In 2015, he joined the School of Physics and Information Engineering, Fuzhou University, Fuzhou, China, where he is currently an Associate Research Fellow. His current research interests include CMOS RF/mixed-signal integrated circuit, wireless power transfer systems, and ultralow power wireless communication systems.

KAMAL EL-SANKARY (Senior Member, IEEE) received the B.Eng. degree from Lebanese University, Tripoli, Lebanon, in 1997, the M.A.Sc. degree in electrical engineering from the University of Quebec, Montreal, QC, Canada, in 2002, and the Ph.D. degree in electrical engineering from the Ecole Polytechnique, University of Montreal, Montreal, in 2006. He joined the Department of Electrical and Computer Engineering, Dalhousie University, Halifax, NS, Canada, in 2006, where he is currently a Professor. His current research interests include mixed-signal, analog, digital and RF integrated circuits design, and embedded systems.