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RESEARCH ARTICLE

A CMOS SoC for Wireless Ultrasonic Power/Data Transfer and SHM Measurements on Structures

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ABSTRACT This paper describes a highly-integrated CMOS system-on-chip (SoC) for active structural health monitoring (SHM). The chip integrates ultrasonic power and bidirectional half-duplex data transfer, a power management unit (PMU), and an ultrasound transceiver to enable wireless ultrasonically-coupled sensor SHM networks on structures. The PMU includes an active bias-flip rectifier with off-delay compensation, a high-efficiency dual-path DC-DC converter with inductor time-sharing, and five switched-capacitor DC-DC converters to generate multi-level spectrally band-limited pulses for guided-wave SHM. The chip was fabricated in a standard 180 nm process and has a die area of 2×2 mm^2. Test results show power conversion efficiency (PCE) $>$ 85% for the active rectifier, $>$ 70% for the inductive DC-DC converter, and $>$ 60% for the switched-capacitor DC-DC converters. Output pulses have a peak-to-sidelobe ratio (PSL) $>$ 30 dB and worst-case out-of-band emissions < -30 dB, respectively. The SoC was integrated with a low-power microcontroller and passive components to realize miniaturized (15 mm $\times$ 30 mm) wireless SHM nodes. A set of nodes was deployed on an SHM test-bed (carbon fiber reinforced polymer sheet) representing an airframe panel. Tests on this wireless network confirm both long-range ultrasound power/data transfer and the ability to detect structural damage.

INDEX TERMS Energy harvesting, structural health monitoring (SHM), ultrasound power/data transfer.

I. INTRODUCTION

Much of the world's critical civil infrastructure, including bridges, pipelines, and transportation, is in increasingly poor condition due to the effects of ageing and deferred maintenance [1]. Structural health monitoring (SHM) is fast becoming an important component of any integrated strategy for managing the associated risks [2], [3], [4].

Broadly speaking, SHM sensors can be divided into two categories: *passive* (sensing-only) and *active* (both actuation and sensing). Scalable SHM systems of both types require small, lightweight, inexpensive, unobtrusive, and minimally invasive sensor networks [5]. Traditional wired SHM networks use individual wires for power and data transfer to each sensor node. The large number of wires required to support a large-scale wired network of this type presents installation and maintenance challenges. In addition, the weight of these wires is often unacceptable for high-value structures, such as airframes. Replacing point-to-point wired links with a single wired bus can reduce the weight of the wires, but introduces significant reliability challenges since a single-point bus failure can now disable the entire network. Using a RF-based wireless network can eliminate the wires [6], but at the expense of significantly higher power consumption (and hence lower operating lifetime). These networking issues are particularly challenging for active SHM nodes, which provide greater measurement flexibility (since actuation waveforms can be arbitrarily selected) but also have higher power consumption. Thus, while self-powered passive SHM nodes (typically using vibration energy harvesting) have been demonstrated [7], [8], [9], similar progress on wireless active SHM nodes is lacking.

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These fundamental issues can be addressed by exploiting the high efficiency of directional ultrasound links for power/data transfer, as already demonstrated for biomedical implants [10], [11]. In fact, one can envision using guided acoustic waves propagating through the structure for both sensing and power/data transfer to the SHM nodes, thus enabling methods for jointly optimizing all three processes [12], [13]. We refer to such through-structure wireless networks for active SHM as being ultrasonically-coupled [14].

This paper describes the design and testing of a custom CMOS IC that enables miniaturized wireless sensor nodes for ultrasonically-coupled active SHM networks. Each autonomous node relies on this IC for wireless acoustic power and data transfer, power management, and making SHM measurements. The rest of this paper is organized as follows. Wireless SHM networks are introduced in Section II. The design of the IC is presented in Section III. Electrical characterization results from the IC are discussed in Section IV, while Section V presents measurement results obtained from an SHM test bed. Finally, Section VI concludes the paper.

II. INTRODUCTION TO WIRELESS SHM NETWORKS

A. SHM MEASUREMENTS

Guided ultrasound waves are popular for SHM of thin-walled structures such as airframes, submarine hulls, storage tanks, and pipes. These "Lamb waves" can propagate relatively long distances with little loss, thus allowing a few sensors to monitor large areas of the structure using transmission (pitch-catch), reflection (pulse-echo), or passive (impact/acoustic emission detection) measurements [15], [16].

Multiple Lamb waves modes - either symmetric (denoted S_i where $i \geq 0$), or asymmetric (denoted A_i) - can propagate in thin-walled structures, as shown in Fig. 1(a). Moreover, the figure shows that they are generally dispersive, i.e., have frequency-dependent group velocities. To simplify subsequent signal processing and damage detection algorithms, most applications assume that only one or two wave modes (typically A_0 and S_0) have been excited. A band-limited excitation signal can be used for this purpose, as shown in the figure. Note that the required center frequency is material- and structure-dependent: it scales as v_s/d where v_s is the shear wave velocity in the material and d is the thickness.

Thin piezoelectric transducers, which are also known as piezoelectric wafer active sensors (PWAS), are popular for generating and receiving Lamb waves due to their low profile, broadband characteristics, and low cost [17]. Their lateral (i.e., in-plane) vibrations excite Lamb wave modes in a frequency-dependent manner, as shown in Fig. 1(b). For example, in this case, operating around 300 kHz ensures that only the S_0 mode is excited. Thus, the spectral properties (center frequency, bandwidth, and side-lobe levels) of SHM transmitters must be precisely controlled to obtain the best monitoring results.

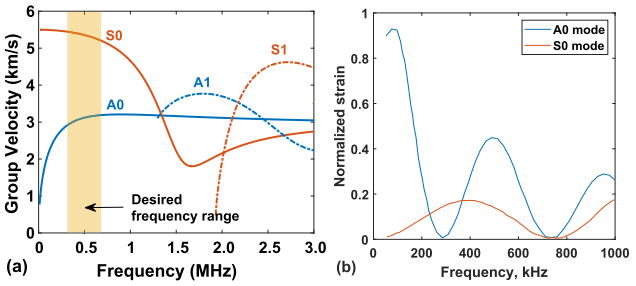

FIGURE 1. Active SHM using PWAS on a 1.5 mm-thick aluminum plate: (a) dispersion of Lamb waves; and (b) expected amplitudes of S_0 and A_0 modes versus frequency for a 7 mm-square PWAS (figure adapted from [17]).

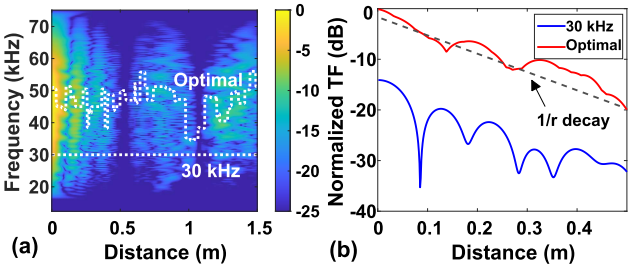

FIGURE 2. Measured power transmission in a 2 mm-thick stainless steel plate using Lamb waves: (a) power attenuation over long distances (0-1.5 m) in the 20-70 kHz range; (b) attenuation versus distance r for both a randomly-selected frequency (30 kHz) and the distance-dependent optimal frequency.

Both transmission- and reflection-type SHM measurements require pulsed waveforms to obtain spatial resolution. However, simple "on-off" pulses with rectangular amplitude profiles are undesirable because of their poor spectral side-lobe levels (worst-case of -13 dB). Thus, windowed pulses should be used instead. For example, one can use cosine-sum or raised cosine window functions, which are defined as

$$w[n] = a_0 + (1 - a_0) \cdot \cos\left(\frac{2\pi n}{N}\right), \quad 0 \leq n \leq N, \quad (1)$$

where a_0 is a constant. The choice $a_0 = 25/46 \approx 0.54$ results in the Hamming window, which is favored for active SHM due its low worst-case side-lobe level (approximately -41 dB).

B. ULTRASOUND POWER TRANSFER ON STRUCTURES

Guided ultrasound waves are also suitable for long-range wireless power and data transfer within structures [14]. The resulting ultrasound channels are highly frequency-selective due to multi-path propagation, which generates patterns of constructive and destructive interference (known as "slow fading"). For example, the measurements in Fig. 2(a) show complex frequency- and distance-dependent power transmission patterns even in a simple structure (a uniform metal plate). Fig. 2(b) shows that operating at the distance-dependent optimum frequency $f_{opt}(r)$ can significantly increase the available power (by $>$ 15 dB in this case). Also, the available power decays slowly with distance

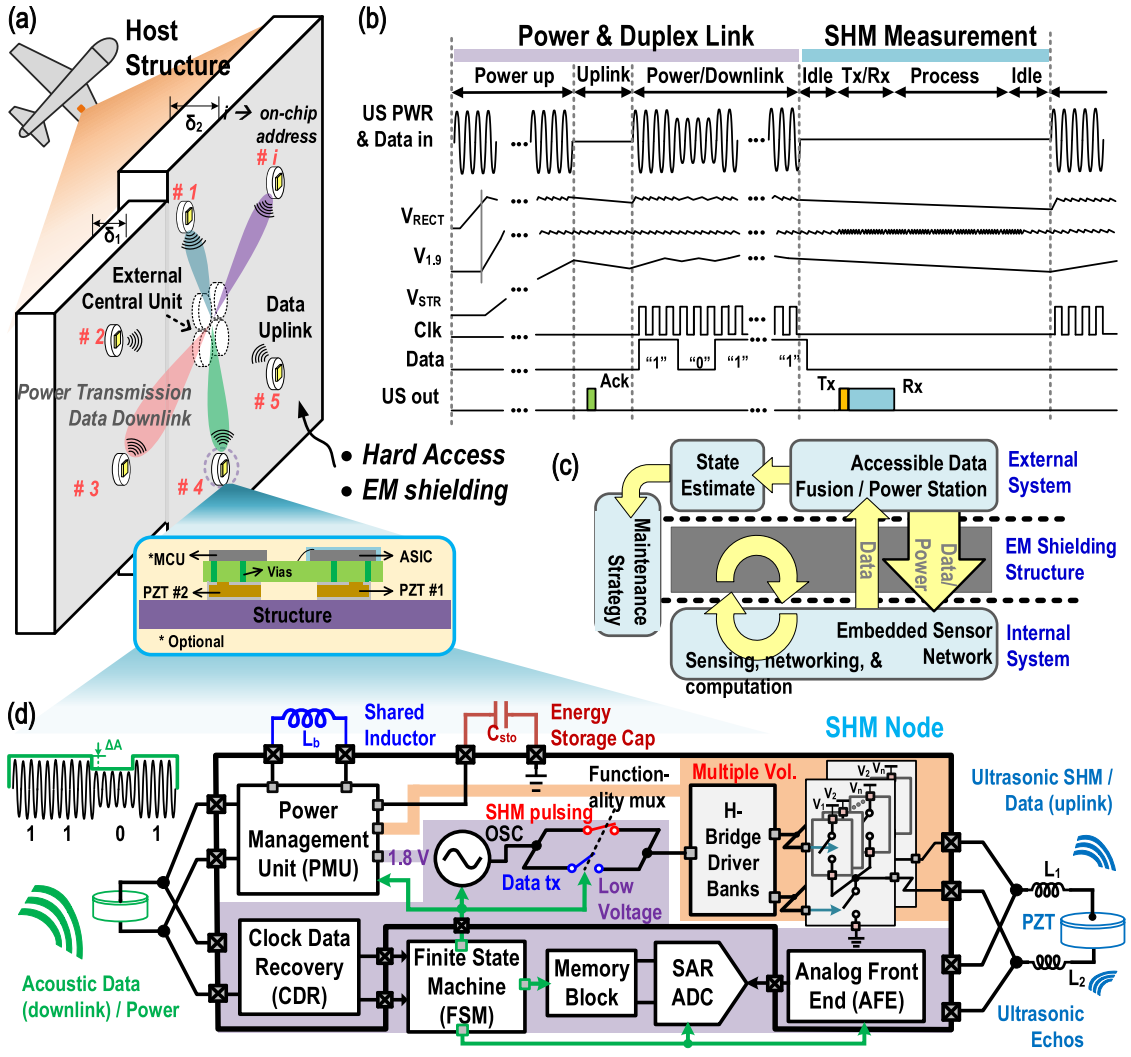

FIGURE 3. (a) Overview of the proposed ultrasonically-coupled wireless network for structural health monitoring (SHM). (b) High-level timing sequence of the combined ultrasonic power/data transfer and measurement cycle. (c) Block diagram of a closed-loop maintenance strategy enabled by a wireless SHM network deployed within a hard-to-access internal region. (d) Block diagram of the proposed miniature wireless SHM node. All the blocks shown inside the solid black line are integrated within the custom IC, while the others are implemented within an off-the-shelf MCU.

($\propto 1/r$), as expected for guided waves in 2-D, thus enabling efficient long-distance power and (low-speed) data transfer. However, $f_{opt}(r)$ can change with time due to both environmental and structural changes (bending, temperature fluctuations, etc.). In earlier work, we addressed this challenge by developing a near-maximum power point tracking (nMPPT) algorithm that allows each node to track its own optimal transmission frequency [14].

C. ULTRASONICALLY-COUPLED NETWORK ARCHITECTURE

The overall design of a self-optimizing ultrasonically-coupled network for an emerging SHM application, namely monitoring hard-to-access areas of a structure, is shown in Fig. 3(a). A wired central unit (known as the hub) provides access to the external world. The hub delivers ultrasonic power to a distributed set of sensor nodes, and also maintains bidirectional data links with them. Each node contains a custom ASIC and microcontroller (MCU) for making local SHM measurements and transferring the results back to the hub for further processing. Fig. 3(b) shows important waveforms during a typical measurement cycle. During the first part of the cycle, nMPPT is used to find $f_{opt}(r)$ and enough power is delivered to power up the node. Next, the node sends an acknowledge (ACK) signal via the data uplink (node to hub). On receiving ACK, the hub sends instructions to the node via the data downlink (hub to node), for which bits are modulated on the power carrier. The node then uses these instructions to set its parameters (e.g., operating frequency, pulse length, etc.) and carries out either a transmission- or reflection-type SHM measurement. Finally, it uses the uplink to transmit acquired data back to the hub and returns to an idle (or sleep)

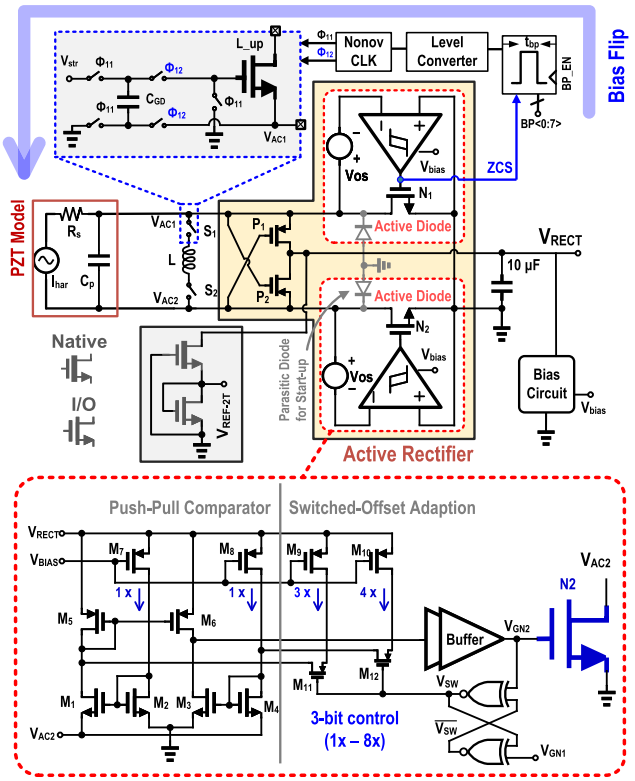

FIGURE 4. Block diagram of the AC-DC converter (active bias-flip rectifier) showing the push-pull hysteretic comparator with switched-offset delay compensation used within the rectifier.

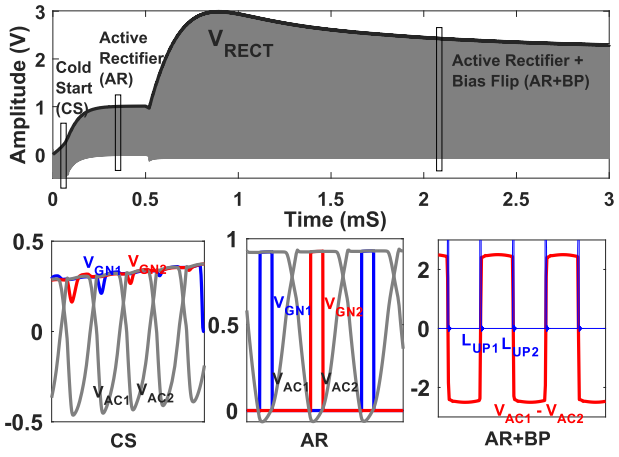

FIGURE 5. Transient simulation results for the AC-DC module: (1) cold start (CS) using passive diodes; (2) active rectifier (AR); (3) active rectifier + bias flip (AR+BP).

state. The hub integrates data from multiple nodes to develop estimates of the current state of the structure (e.g., maps of stress distribution or damage locations). Such estimates can then be used by human operators and/or AI algorithms to drive maintenance decisions, as shown in Fig. 3(c).

III. CHIP DESIGN

A highly-integrated ASIC is key for miniaturizing the proposed ultrasonically-coupled SHM sensor nodes (thus enabling deployment on non-planar surfaces) and also reducing their power consumption (thus enabling sparse sensor networks coupled via long-range links). Fig. 3(d) shows a block diagram of the proposed custom SHM IC, which is integrated together with an off-the-shelf ultra-low-power MCU to realize autonomous ultrasonically-coupled SHM sensor nodes. The chip is interfaced to two PWAS: the first (shown on the left) is used for acoustic power and data downlink from the central hub, while the second (shown on the right) is used for SHM measurements and also data uplink to the hub. Both links are designed to operate at programmable frequencies within the 0.1-1 MHz range to ensure single- or dual-mode Lamb wave propagation within a variety of structures (e.g., metal or carbon-fiber composite plates of different thicknesses).

The main components of the chip include the power management unit (PMU), clock and data recovery (CDR), SHM transmitter, load-shift keying (LSK)-based data transmitter, and the analog front-end (AFE) of the SHM receiver. The MCU contains the clock generator (which determines the operating frequency), a finite state machine (FSM) for sequencing the measurement, an ADC for digitizing the output of the SHM receiver, and on-chip memory (SRAM) for storing the results. In the next few sub-sections, we describe the major building blocks of the proposed IC in more detail.

A. ACTIVE BIAS-FLIP RECTIFIER

Power management is a major function of the proposed ultrasonically-coupled SHM IC. The first component of the PMU is an AC-DC converter (rectifier) that converts the AC voltage across transducer (i.e., PWAS) #1 into a DC voltage for recharging an energy storage capacitor. Fig. 4 shows the block diagram of the proposed bias-flip rectifier. The core of the design is an active rectifier consisting of two PMOS switches (P_1 and P_2) and two NMOS switches (N_1 and N_2). The former are directly driven by the AC voltage across the transducer ($v_{AC1} - v_{AC2}$), while the latter are driven by hysteretic push-pull comparators to minimize i) voltage drop during the ON period; and ii) reverse current flow during the OFF period. Each comparator internally generates an adaptive offset voltage V_{OS} to compensate for its own turn-OFF time delay, thus minimizing reverse current flow [18]. Note that only OFF-time delay compensation is implemented since reverse current directly degrades voltage and power conversion efficiency (VCE and PCE, respectively). On the other hand, the ON-time delay only affects the conduction time of the switches, which is not considered in this design.

Fig. 4 (zoomed-in view) shows one of the comparators in more detail. The design compares V_{AC2} (or V_{AC1}) with ground to generate the gate control signal V_{GN2} (or V_{GN1}). The input current mirrors M_1-M_4 are biased at $I_{BIAS} \approx$ 200 nA (denoted 1× in the figure) by V_{BIAS}, which is generated by a PTAT current reference as shown in Fig. 6(a). Two offset currents (with nominal values of 3× and 4×) generate the required offset V_{OS}. Specifically, M_1 sinks more current

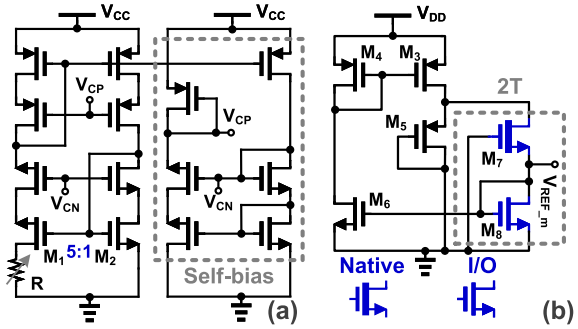

FIGURE 6. Schematics of the on-chip current and voltage reference circuits: (a) constant-G_m current reference with self-bias circuit; (b) modified 2T voltage reference with improved supply regulation.

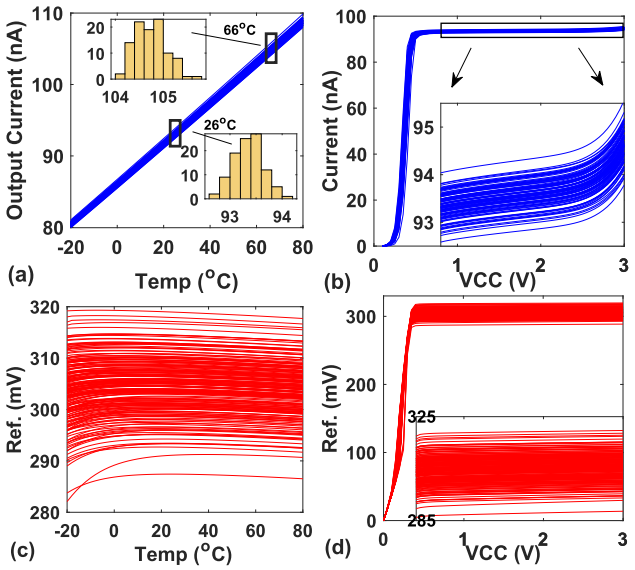

FIGURE 7. Monte Carlo simulation results for the PTAT current reference and modified 2T voltage reference.

than M_2 when V_{AC2} is below ground, thus causing M_6 to source more current than M_3 can sink, driving V_{GN2} high and turning on the active switch $N2$ to charge the filtering cap (10 μF). The offset current switches, M_{11} & M_{12}, are off initially since V_{SW} has been high (V_{GN1} was high and V_{GN2} was low during the $N1$ switch operation). They turn on when V_{GN2} goes high and V_{GN1} stays low. The latch provides de-glitching and also ensures that the offset currents turn off when the complementary gate signal V_{GN1} goes high. The optimal value of V_{OS} is load-dependent, and can be optimized via 3-bit control of the offset currents. The size of two pass-transistors ($N1$ and $N2$) can also be tuned via 3-bit control to achieve the optimal power conversion efficiency under different load conditions.

Since the comparators are powered by the rectified output V_{RECT}, they are not available during "cold-start" conditions when the output capacitor is completely discharged. In this case, the parasitic drain-substrate diodes of N_1 and N_2 provide rectification (with lower efficiency), as shown in Fig. 4.

In a conventional full-bridge rectifier, each diode contributes a forward voltage drop $V_D \approx 0.7$ V, such that the output DC voltage $V_{RECT} \leq V_P - 2V_D$ where V_P is the amplitude of the AC voltage across the transducer. Moreover, the transducer has to charge its internal capacitance C_P on every cycle, which wastes power. Fundamentally, this is because v_P is out of phase with the transducer current i_P due to the capacitive nature of the transducer impedance. The proposed rectifier uses "bias-flip" switches[1] to improve the output power available from the transducer [19] by more than 200%. Specifically, switches S_1 and S_2 are placed in series with an off-chip shunt inductor L and turned on when i_P crosses zero. Therefore, C_P and L instantaneously constitute a resonance tank and the inductive voltage $v = L(di/dt)$ then quickly flips the polarity of v_P, which reduces the energy loss caused by charging/discharging C_P. The resulting transducer voltage and current (v_P and i_P) are nearly in phase (resembling a resistive impedance), which maximizes the available power. A bootstrap driver (shown in the inset of Fig. 4) is used to create a floating gate-source voltage for controlling S_1 and S_2 through the AC cycle. During phase ϕ_{11}, the DC voltage on the storage capacitor (V_{STOR}) is stored on C_{GS} and $V_{GS1,2}$ is reset to zero. During phase ϕ_{12}, the stored voltage is added to V_{AC} to set the gate voltage. The necessary switches use dynamic body biasing to ensure that their parasitic diodes remain OFF. Switch timing ($t_{on} = \pi\sqrt{LC_P}/2$) for the proposed bias-flip circuit is controlled by a feedback loop that digitally adjusts the pulse width t_{bp} (8-bit control BP<0:7> with a timing step of 2.2 ns) to ensure zero-current switching (ZCS). The delayed line uses 4-bits ($\mathbf{CO} < \mathbf{0} : \mathbf{3} >$) for coarse control and the other 4-bits ($\mathbf{FN} < \mathbf{0} : \mathbf{3} >$) for fine control. The delays are generated using weak inverters charging up capacitors. A range of 0.56 μs is used to accommodate a wide change in PZT sizes (various C_P values) and CMOS process variations. The $\mathbf{BP} < \mathbf{0} : \mathbf{7} >$ signals are fed in externally (e.g., pull-up/down resistors) and tuned via a one-time calibration. Unlike [19], we integrate active diode into the bias-flip rectifier, which significantly improves the conversion efficiency. Also the ZCS signals ($V_{GN1,2}$) generated from the push-pull comparators are implemented for synchronized switching on an inductor.

Fig. 5 illustrates a transient simulation for the active bias-flip rectifier circuit, initially from cold start (CS) using parasitic bulk diodes when the rectified output V_{RECT} is 0 V, then transiting to the active rectification (AR) stage once when V_{RECT} is grater than ~1 V, and finally into the active bias-flip rectification (AR+BP) stage, during which the V_{RECT} is boosted up by more than 200%.

The unregulated output DC voltage V_{RECT} is used to power two bias generator circuits. The first is a fully-cascoded constant-G_m reference with a nominal output current of $I_{BIAS} = 100$ nA, shown in Fig. 6(a). Figs. 7(a) and (b) show the simulated output currents versus the ambient temperature

[1]This approach is also known as parallel-SSHI, where SSHI stands for "synchronized switch harvesting on inductor".

and the supply voltage. The standard deviations in current due to process variation are typically <0.3 nA. The second uses a two-transistor (2T) reference [20] to generate a PVT-robust voltage. A basic 2T reference using native and I/O transistors is shown in Fig. 6(b) (dashed box). We modified this design to improve power supply regulation, as shown in Fig. 6(b). The reference current I_{REF} through M_8 is mirrored to M_6 and then M_3 with a ratio $1 : m$, $m > 1$. The diode-connected device M_5 then carries a current $(m-1)I_{REF}$, ensuring that V_{DS} of M_7 becomes nearly independent of V_{DD}. The typical output voltage is $V_{REF\_2T} \approx 325$ mV with a temperature coefficient of 17.1 ppm/°C when V_{DD} is 3 V and with a line sensitivity of 0.014%/V when V_{DD} varies from 0.5 to 3 V, as shown in Figs. 7(c) and (d). The two bias generator circuits can operate down to 0.5 V and 0.35 V, respectively.

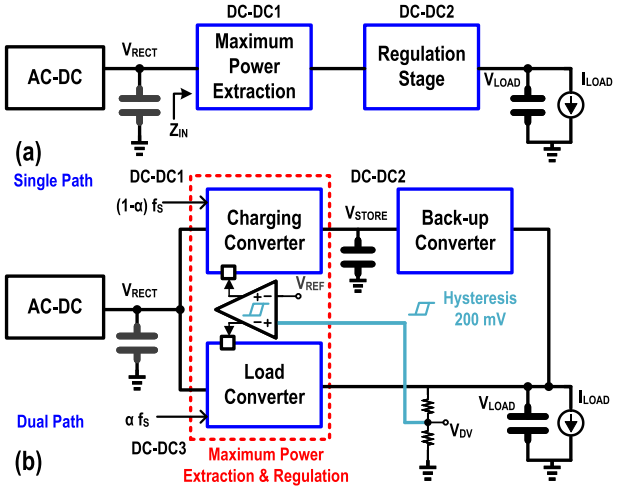

FIGURE 8. Architecture of the DC-DC converter: (a) conventional, and (b) proposed. The load is represented by a current source I_{LOAD}.

B. DC-DC CONVERTER

The DC-DC converter transforms the unregulated rectifier output V_{RECT} into two regulated outputs: V_{STOR} (nominally 3.3 V) and V_{LOAD} (nominally 2.0 V). The former is stored on a large energy reservoir C_{STOR} (a super-capacitor in this case), while the latter powers the rest of the sensor node. Conventionally, these voltages are generated by two DC-DC converters in series, as shown in Fig. 8(a). The first converter ensures maximum power point tracking (MPPT) by adjusting its input impedance to ensure maximum power transfer from the rectifier (and ultimately the ultrasound transducer), while the latter regulates the load voltage V_{LOAD}. Unfortunately, this series configuration suffers from reduced power efficiency, since the PCE of the cascaded converters is the product of the individual efficiencies, i.e., $\eta_{tot} = \eta_1\eta_2$.

By contrast, here we propose a dual-path architecture [21] in which two boost converters - the charging converter (CC) and the load converter (LC) - are placed in parallel and adaptively selected by the current value of V_{LOAD}, as shown in Fig. 8(b). The LC delivers power to the load, while the CC

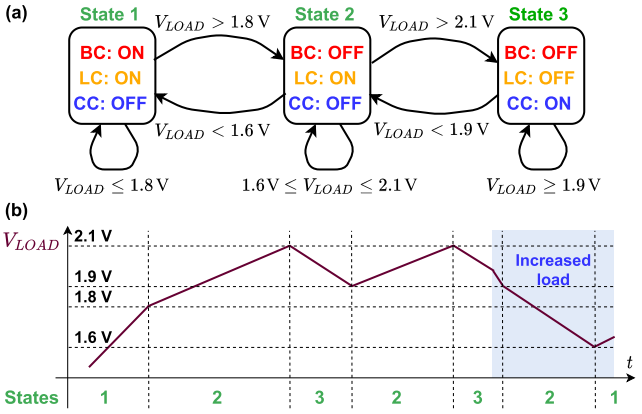

FIGURE 9. (a) State transition diagram of the proposed dual-path DC-DC converter; and (b) typical load voltage V_{LOAD} for a typical load (unshaded region) and a heavy load (shaded region).

allows excess power from the rectifier to be stored in C_{STOR} for later use. In addition, a back-up buck converter (BC) is used to charge the load from V_{STOR} if the latter requires more power than is currently available from the rectifier. The system can transition between these states on every switching cycle based on the current value of V_{LOAD}. For this purpose, several resistively-divided versions of V_{LOAD} (denoted by V_{DV}) are compared with a reference voltage V_{REF} from the modified 2T circuit.

The resulting state transition diagram for the DC-DC converter can be summarized as shown in Fig. 9(a). Under normal conditions, the system cycles between states 2 and 3, resulting in a peak-to-peak ripple of $V_H = 200$ mV around the nominal load voltage of 2.0 V as shown in Fig. 9(b); here V_H is the amount of hysteresis between the switching thresholds for states 2 and 3 (2.1 V and 1.9 V, respectively). However, when the harvested power is insufficient for the load and V_{LOAD} drops below 1.6 V, the system transitions to state 1 (see Fig. 9(b)), where both the BC and LC are turned on to rapidly recharge C_{LOAD}. The switching thresholds for states 1 and 2 (1.8 V and 1.6 V, respectively) are also offset by $V_H = 200$ mV. The resulting fluctuations in V_{LOAD} are acceptable for this application, but can be reduced by using a higher-resolution divider to set a smaller value for V_H.

Let us denote the probability that the system is in state 2 by $p(2) = \alpha$ $(0 < \alpha < 1)$. Clearly, the probability that the system is in either of the other two states is $p(1)+p(3) = (1-\alpha)$. Also, let us denote the PCE of the LC and CC (assumed to be equal for simplicity) as η_1, and the PCE of the BC as η_2. The PCE during state 2 is simply η_1 since only the LC is operating. On the other hand, states 1 and 3 together transfer energy to the load in two steps ($V_{RECT} \rightarrow V_{STOR} \rightarrow V_{LOAD}$), resulting in a effective PCE of $\eta_1\eta_2$. Thus, the average end-to-end PCE of the proposed DC-DC converter is given by

$$\eta_{tot} = \eta_1 \times \alpha + \eta_1\eta_2 \times (1-\alpha). \quad (2)$$

The availability of an upload data link (node to hub) allows the hub to regulate its output power level such that the

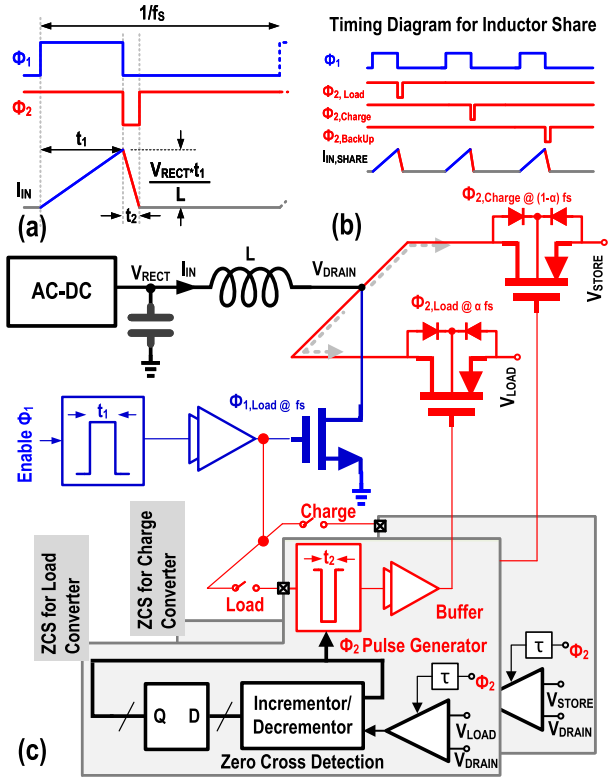

FIGURE 10. (a) Current waveform in DCM mode for the DC-DC converter. (b) Timing diagram used for inductor sharing. (c) Block diagram for zero current switching (ZCS) in the load and charging converters.

harvested power is approximately equal to that consumed by the load. In this case the CC and BC are mostly inactive, i.e., $\alpha \approx 1$. As a result, (2) simplifies to $\eta_{tot} \approx \eta_1$, which is likely to be significantly higher than the cascaded converter architecture. More generally, the system may receive more harvest more power than needed by the load, in which case it cycles between states 2 and 3 as described earlier. In this case, $p(1) \approx 0$, such that $p(3) = (1-\alpha)$ and the effective duty cycles of the LC and CC are α and $(1-\alpha)$, respectively.

All three converters operate in discontinuous conduction mode (DCM), which allows them to use a single time-shared off-chip inductor L_{DC}. The input impedance R_{IN} (as seen by the rectifier) for a single boost converter can be found by estimating the average inductor current $\overline{I_{IN}}$ per cycle. Given the pulse widths t_1 and t_2 for the two switches (as controlled by the clock phases Φ_1 and Φ_2, see Fig. 10(a)), the result is

$$\overline{I_{IN}} = \frac{1}{2}(t_1+t_2)\frac{V_{RECT}\cdot t_1}{L_{DC}}f_s \text{ and} \quad (3)$$

$$R_{IN} \equiv \frac{V_{RECT}}{\overline{I_{IN}}} = \frac{2L_{DC}}{t_1^2 f_s}\left(1+\frac{t_2}{t_1}\right)^{-1} \approx \frac{2L_{DC}}{t_1^2 f_s}, \quad (4)$$

where f_s is the switching frequency (fixed at 50 kHz in our design) and the approximation is valid when $t_2 \ll t_1$. Thus, t_1 can be controlled to adjust R_{IN} and thus ensure MPPT.

The switch configuration used for inductor time-sharing is shown in Fig. 10(c). There are a total of five switches: two series switches for the CC and LC, respectively; one shunt switch shared by them; one series switch for the BC; and one series switch for implementing both MPPT and rectifier under-voltage protection. Under normal circumstances when $p(1) \approx 0$, either the LC or CC is always on (with duty cycles of α and $(1-\alpha)$, respectively). As a result, the average value of R_{IN} is unchanged, which allows MPPT to be maintained:

$$R_{IN,av} \approx \left[\alpha R_{IN,LC}^{-1} + (1-\alpha)R_{IN,CC}^{-1}\right]^{-1} = \frac{2L_{DC}}{t_1^2 f_s}. \quad (5)$$

Fig. 11 shows a simplified view of how the DC-DC architecture was implemented on-chip. Two feedback loops are used to adapt the switch timings, as shown by the green and blue arrows in Fig. 11. The green MPPT loop turns off the first series switch when the signal MPPT_SMP goes high, thus disconnecting the DC-DC converter from the rectifier. A sample-and-hold (S/H) within the "MPPT" block then measures the open-circuit voltage $V_{RECT,0}$ of the rectifier. Low leakage (typically 10-aA leakage) low charge injection switches [22] are used in the S/H circuit to store the reference and ensure MPPT accuracy. Note that a hysteretic comparator also turns off this switch when the loaded rectifier voltage V_{RECT} drops below a pre-set threshold, thus providing under-voltage protection. During normal operation, the loop ensures MPPT by adjusting the duration of Φ_1 (denoted by t_1), and thus R_{IN}, such that the loaded value of $V_{RECT} = 0.5 \times V_{RECT,0}$; this is generally a good approximation to the maximum power point. Adjustment is performed digitally using an 6-bit accumulator, and can be disabled by a control signal MPPT_EN as shown in Fig. 11. The dashed box in this figure shows one of the comparators in more detail. A dynamic two-stage design [23] is used in which the first stage provides energy-efficient amplification and the second stage contains both a simple voltage amplifier and a positive-feedback amplifier to obtain rail-to-rail digital outputs.

The second feedback mechanism consists of independent zero current switching (ZCS) loops for the LC and CC. These blue loops are shown in more detail in Fig. 10(c). They use similar 6-bit digital control circuits to adjust the individual durations of Φ_2 (denoted by t_2) such that ZCS is obtained for the inductor current waveform, thus maximizing power efficiency. Finally, the present value of V_{LOAD} is used to switch between the LC and CC as described earlier, thus ensuring load voltage regulation. Fig. 12(a) shows typical transient simulations for the DC-DC converters. The top plot shows the MPPT process, which typically includes a 20 ms sample-and-hold stage and a t_1 tuning stage, during which V_{CAP} is regulated to half of the open-circuit voltage by tuning t_1 timing. The bottom plot shows the regulated voltage on V_{DD} and V_{STOR}. Figs. 12(b) and (c) shows the ZCS process for the load and charging converters, where both achieve zero current switching (i.e., synchronous operation) by tuning the t_2 timing (see the red curves in the sub-figures).

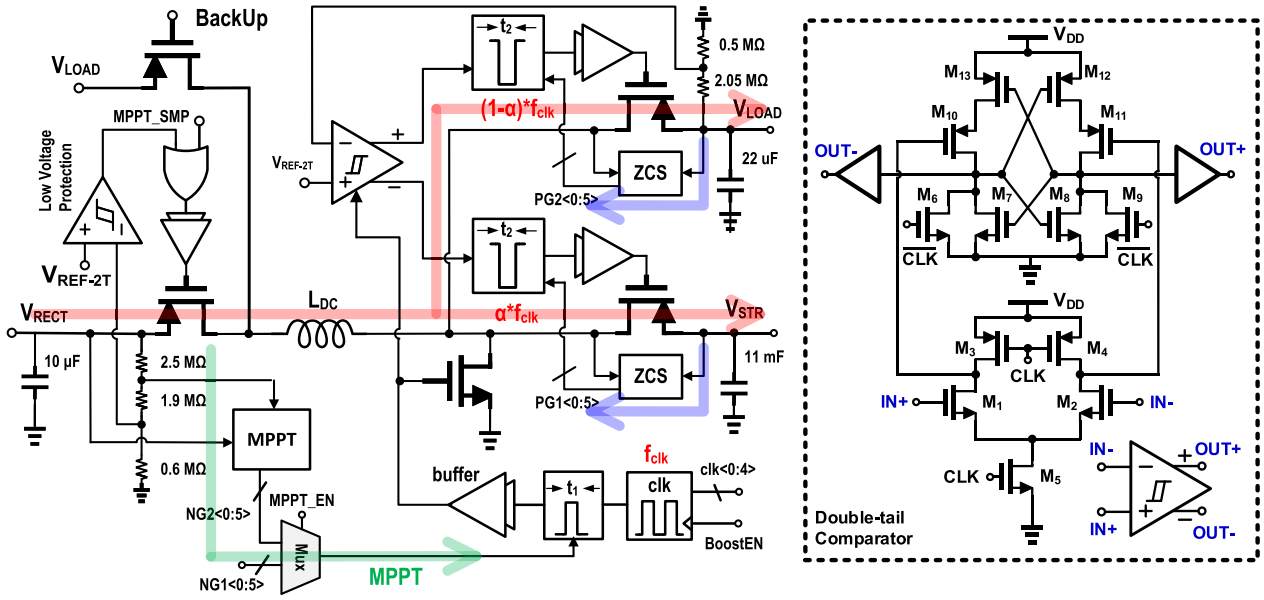

FIGURE 11. Block diagram of the DC-DC converter circuit, including the power flow path (orange), MPPT control loop (green), and ZCS control loops (blue). An energy-efficient dynamic two-stage comparator is implemented in our design (dashed box).

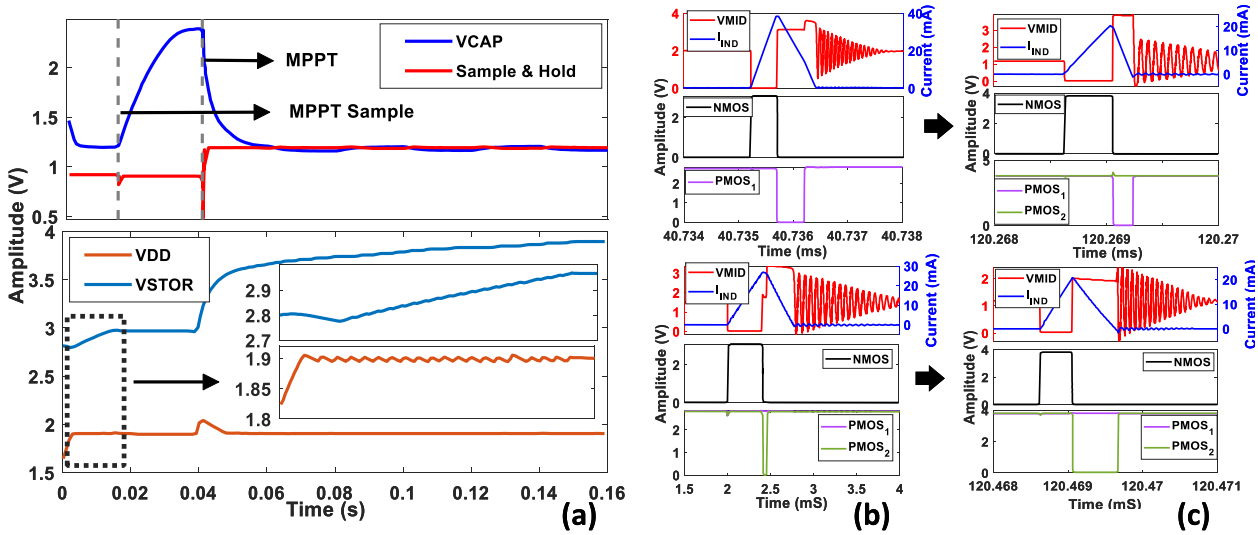

FIGURE 12. DC-DC simulation results: (a) MPPT process with an MPPT clock of 1 kHz (top), voltage regulation to 2.0 V for storage cap voltage <4.0 V (see zoom-in view); (b) initial asynchronous LC/CC converters; (c) synchronous LC/CC converters with ZCS.

C. SHM TRANSMITTER

Fig. 13 (left) shows a block diagram of the transmitter (TX) used for SHM measurements. The Tx generates pulses across PWAS #2 with shapes that approximate a Hamming-windowed tone burst, as shown in the figure. As described in Section II, windowing ensures that the pulse is localized in the frequency domain (i.e., does not have significant side-lobes), which improves the accuracy of SHM measurements by avoiding the excitation of multiple propagating Lamb wave modes. The earlier (wired) SHM transceiver IC described in [24] used pulse-width modulation (PWM) to generate a close approximation to a Hamming-windowed pulse. However, PWM requires the use of a high-frequency clock (in the earlier design, 16× higher than the operating frequency) to generate narrow pulses, which significantly increases overall power consumption of the IC. The new design eliminates this problem by dynamically switching between multiple power supply voltages during the pulse, thus directly controlling its amplitude on a cycle-by-cycle basis. The cycle period, and thus the center frequency f_0 of the pulse, is externally programmable via the clock frequency, resulting in a −3 dB excitation bandwidth of $1.30 \times f_0/5 \approx f_0/4$ for a five-cycle pulse, where the factor of 1.30 arises from the Hamming window.

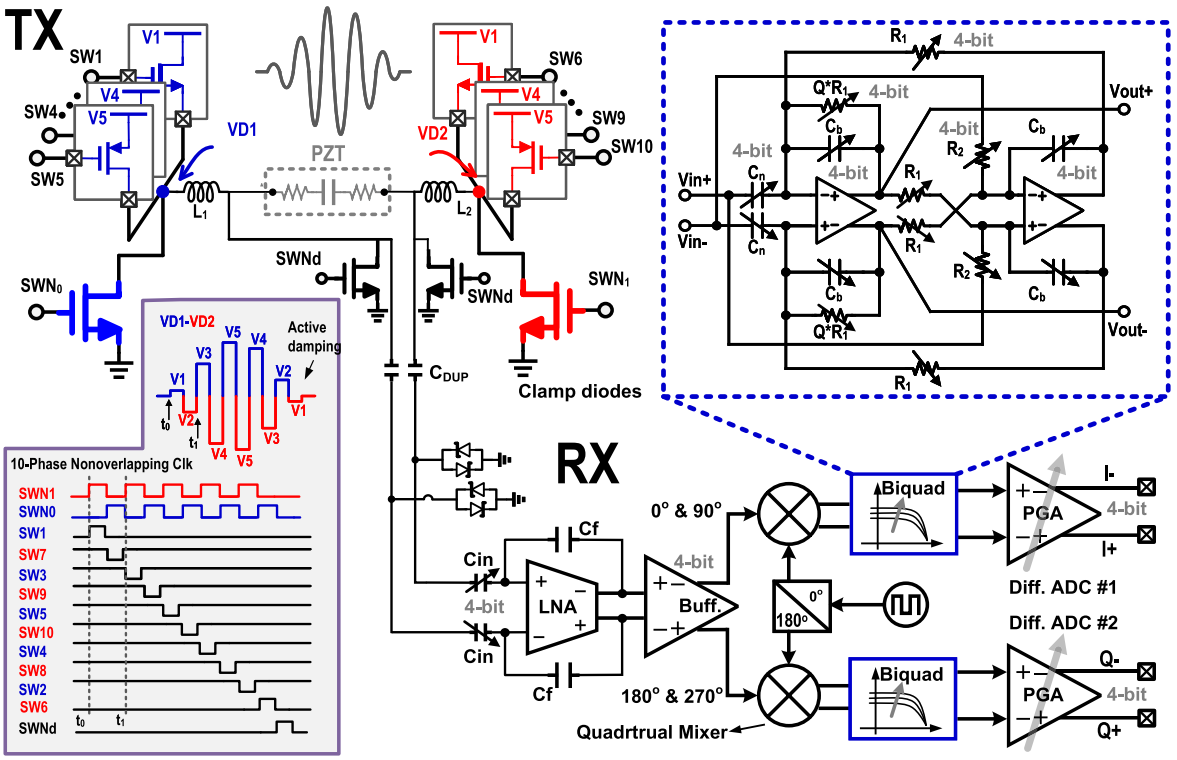

FIGURE 13. Block diagram of the SHM transmitter and receiver, including the off-chip blocking caps (C_{DUP}) used as a passive duplexer.

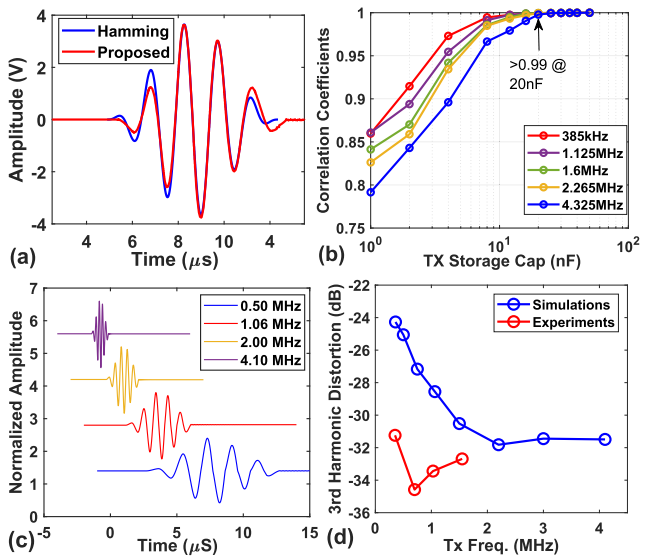

FIGURE 14. Transmitter simulation results: (a) optimized multilevel (i.e., 5 levels) transmit excitation waveform (red) after LPF; (b) minimum storage capacitance, C_L, required for each voltage level to ensure low waveform distortion while remaining energy efficient at different center frequencies; (c) excitation waveform at different center frequencies; (d) third-harmonic suppression versus center frequency (simulated and measured).

The transmitter circuit uses a H-bridge topology to ensure high power-efficiency and maximize the output signal swing (up to $\pm V_{DD}$), as shown in Fig. 13. Small off-chip inductors L_1 and L_2 are placed in series with the load (i.e., the ultrasound transducer) to create a series LRC circuit with quality factor Q, which suppresses harmonics and further boosts the steady-state voltage across the transducer by a factor of up to Q. The high-side switches of the H-bridge are split into five pairs ($SW1$–$SW10$). Each pair is supplied by a different DC supply voltage (denoted V_1–V_5), thus enabling the pulse envelope to be dynamically controlled using the switching sequence shown in the figure, which is generated on-chip from a single external trigger pulse. We use NMOS devices for switches $SW1$ and $SW6$ due to the low voltage level ($V_1 \approx 0.3$ V), while the others are implemented using PMOS devices. The necessary DC voltages are generated by on-chip switched-capacitor DC-DC converters, as described in the next section.

Fig. 14(a) illustrates the simulated excitation waveform (red) and the reference Hamming-windowed waveform (blue). The spectra of these waveforms indicates that our proposed scheme provides a good approximation to the desired frequency response, with only ~6-dB degradation in side-lobe suppression (discussed further in the next section). Also note that the proposed transmitter is fully digital and can typically operate up to several MHz (as shown in Fig. 14(c)).

D. SWITCHED-CAPACITOR DC-DC CONVERTERS

A set of five parallel switched-capacitor converters use pulse-frequency modulation (PFM) [25] to efficiently generate the five regulated output voltages required by the transmitter, namely $V_1 = 0.36$ V, $V_2 = 0.89$ V, $V_3 = 1.9$ V, $V_4 = 2.87$ V,

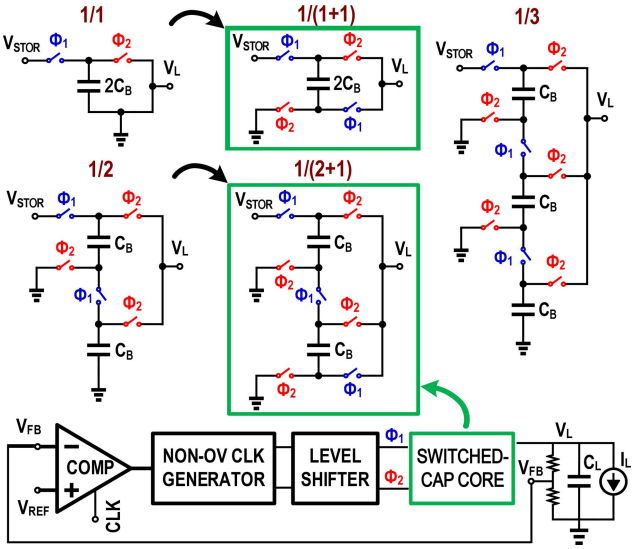

FIGURE 15. Block diagram of the switch configurations (top) and PFM feedback loop (bottom) used by the switched-capacitor DC-DC converters. Only the highlighted switch configurations were utilized in the final design. The 1/1 configuration (a single switch) is not shown for simplicity.

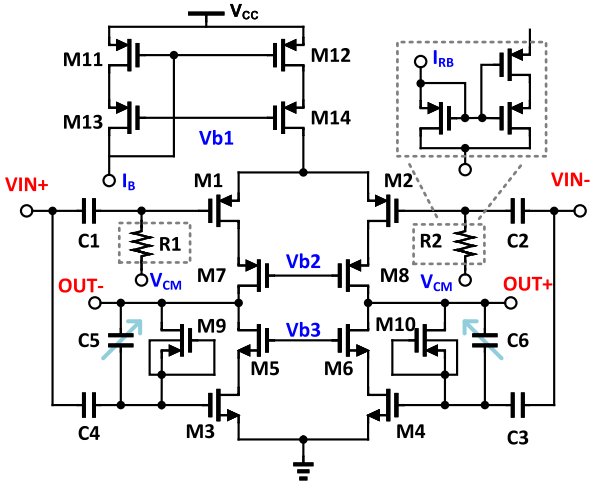

FIGURE 16. Transistor-level schematic of the low-noise amplifier (LNA).

and $V_5 = 3.3$ V. These values were obtained by numerical optimization (as shown in Fig. 14 (a)), with the target being the best possible five-level approximation to the desired SHM transmit pulse waveform (five cycles long, Hamming-windowed). Simulations show that the five-level pulse has 20 dB lower worst-case sidelobe level than a simple "on-off" tone burst, resulting in a peak-to-sidelobe ratio (PSL) of approximately −32 dB. Fig. 14 (d) shows the simulated side-lobe suppression for different excitation frequencies. The experimental results (discussed later) show more than 30 dB suppression.

Three of the five required DC levels were generated by 1/1 ratio converters: i) $V_{STOR} > 3.3$ V $\rightarrow 3.3$ V and 2.87 V; and ii) $V_{LOAD} > 1.9$ V $\rightarrow 1.9$ V. The two remaining voltage levels were obtained as follows: i) a 1/3 ratio converter to generate 0.89 V from V_{STOR}, and ii) a 1/2 ratio converter to generate 0.36 V from 0.89 V. The necessary switched-capacitor configurations are shown in Fig. 15. The 1/1 converters consist of a single switch between the input (V_{STOR} in the figure) and output (V_L), and are not shown for simplicity. For the 1/2 and 1/3 converters, we used the configurations highlighted in Fig. 15 ("1/(1+1)"and "1/(2+1)", respectively) rather than the alternative designs also shown in the figure, which require more switches and thus have lower efficiency. The "1/(1+1)"and "1/(2+1)" configurations can be derived from basic 1/1 and 1/2 converter designs by adding a single pair of switches, as indicated by the arrows.

A similar PFM-based voltage-regulation loop is used for each converter, as shown in Fig. 15. The loop feeds back a divided version of the output voltage V_L (denoted by V_{FB}) to a hysteretic comparator, which then enables/disables the local non-overlapping clock generator. A relatively low value of hysteresis (50 mV) was used to ensure low output voltage ripple, and thus accurately-shaped pulses. The on-chip capacitance used by the 1/2 and 1/3 converters was set to a relatively large value ($C_B = 25$ pF) to ensure low output impedance. Finally, voltage droop during the pulse was minimized by using off-chip capacitors (C_L) to store enough charge at each output node. The value of C_L was optimized in simulations to ensure both high-fidelity waveforms (which favors large C_L values) and high energy efficiency (i.e., low transmit energy per pulse, which favors small C_L values). The results, which are shown in Fig. 14(b), suggest that $C_L = 20$ nF provides a good compromise between these factors. Note that the waveform correlation coefficients in this figure are referenced to the maximal-fidelity waveforms obtained using a large load capacitance ($C_L = 100$ nF).

E. TRANSMIT-RECEIVE SWITCH

Since the PWAS voltage can significantly exceed V_{DD} (due to the voltage amplification provided by the resonant *LRC* load), a simple off-chip transmit-receive switch (duplexer) was used to protect the input terminals of the SHM receiver. This circuit consists of small series capacitors C_{DUP} and two sets of back-to-back diode clamps, as shown in Fig. 13 (middle). In transmit mode, the diodes turn on (behaving as a short circuit), thus placing an effective capacitance $C_{DUP}/2$ in parallel with the PWAS and limiting the voltage across the receiver terminals to one diode drop (approximately ±0.7 V). The value of C_{DUP} is chosen to be significantly smaller than the transducer capacitance C_P to ensure that the added capacitance does not significantly degrade transmitter efficiency. In receive mode, the diodes turn off (behaving as an open circuit), thus allowing the received signals to pass into the receiver through C_{DUP}.

F. RECEIVER

The receiver design is shown in Fig. 13 (right). The first stage is a fully-differential low-noise amplifier (LNA) based on a current-reused folded-cascode OTA topology, as shown in

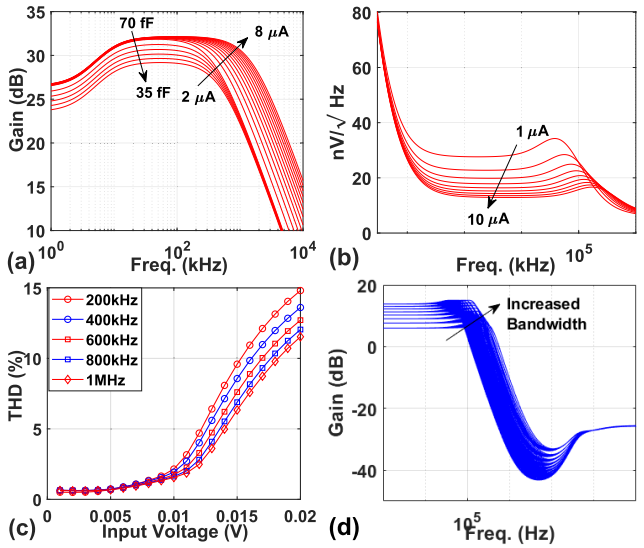

FIGURE 17. Simulation results for the receiver: (a) gain and bandwidth of the LNA as a function of bias current and feedback capacitance C_f; (b) LNA input-referred noise as a function of bias current; (c) total harmonic distortion (THD) of the LNA as a function of input amplitude; (d) gain and bandwidth of the proposed biquad (2nd-order active RC filter).

Fig. 16. The gain of the LNA is set by capacitive feedback to $A_v = C_{in}/C_f$; here C_{in} is fixed at $\sim 2pF$ and C_f is digitally programmable via a 4-bit capacitor DAC. The presence of C_{DUP} causes the gain to decrease to $A_v = C_{in,eff}/C_f$ where $C_{in,eff} = C_{in}C_{DUP}/(C_{in} + C_{DUP})$, thus degrading the input-referred noise from its design value of ~ 12 nV/Hz$^{1/2}$, as shown in Fig. 17(b). To minimize such degradation, we set $C_{DUP} \gg C_{in,max}$. Thus, the condition $C_P \gg C_{DUP} \gg C_{in,max}$ is required for the proposed passive duplexer to work as intended. In our design $C_P \approx 100$ pF and $C_{in,max} = 2$ pF, so we used $C_{DUP} = 10$ pF to approximate $\sqrt{C_P C_{in,max}}$, which is a suitable value. Note that we have ignored the off-state capacitance C_d of the diodes (which further attenuates the received signal) for simplicity; low-capacitance diodes ($C_d < 1$ pF) were used to minimize additional signal attenuation.

Fig. 17(a) shows how the gain and bandwidth of the LNA changes when configured with different values of C_f and bias currents. The LNA has a simulated 2% THD of 10 mV at a bias current of 4 μA, which results in around 114 dB of dynamic range (DR).

The rest of the receiver uses a standard super-heterodyne topology with fully-differential signal path to minimize even-order distortion and common-mode noise. Quadrature down-conversion (using passive double-balanced mixers) is used to down-convert received SHM signals to baseband, thus minimizing the sampling rate required by the MCU's ADC. The LNA output is buffered by a fully-differential folded-cascode op-amp (shown in Fig. 18) before driving the mixers. The op-amp uses a nominal bias current of $I_B = 2$ μA derived from a 1 μA constant-G_m reference. It has a unity-gain bandwidth product of 15.5 MHz and in-band integrated noise of 107 μV_{rms} with a power consumption of 88 μW. The constant-G_m reference also generates the other op-amp bias voltages (V_{b2}–V_{b5}). The op-amp uses a continuous-time CMFB loop for simplicity, as shown in Fig. 18 (right).

The quadrature outputs (I and Q) of the mixer are low-pass filtered by a second-order biquad [26] (shown within the dashed box in Fig. 13) before being amplified by a differential programmable-gain amplifier (PGA). Both the biquad and the PGA use the same op-amp as in the mixer buffer. The biquad transfer function (TF) can be found in [26]. It has a Chebyshev-type response with programmable DC gain ($H(0)$), stop-band rejection ($H(\infty)$), cut-off frequency (ω_c), and notch frequency (ω_n). We fixed $H(0) = 1$ and programmed the other biquad parameters (and thus the frequency response of the receiver) using 4-bit resistor and capacitor DACs interfaced to a standard 3-wire on-chip SPI port. Fig. 17 (d) shows the simulated gain and bandwidth of the biquad under different resistor/cap settings. The goal is to match the excitation bandwidth of $\approx f_0/4$ while minimizing out-of-band noise and clock feedthrough.

G. ULTRASOUND DATA TRANSCEIVER

The ultrasonic downlink and uplink reuse the two PWAS used for power delivery and SHM measurements (#1 and #2, respectively), as shown in Fig. 3(d). The hub uses binary frequency shift keying (BFSK) to modulate downlink data on the power carrier [14]. The strongly frequency-selective ultrasound channel converts such frequency modulation into amplitude modulation, as indicated on the figure. The on-chip clock and data recovery (CDR) block uses an envelope detector (ED) and hysteretic comparator to extract the amplitude-modulated bits, as shown in Fig. 19. Typical SHM measurement cycles are slow (<1 measurement/hour), so relatively low downlink data rates (10-200 bits/sec) are generally used.

Uplink data is transmitted on PWAS #2 by reusing the SHM transmitter shown in Fig. 13 (left). For this purpose, the switches connected to voltages V_1–V_4 ($SW1$–$SW4$ and $SW6$–$SW9$) are disabled, with only $SW5$ and $SW10$ (connected to $V_5 = 3.3$ V) remaining active. Thus, the transmitter output reduces to a single-cycle pulse. Data is encoded using on-off keying (OOK) to minimize energy consumption: the presence of a pulse within a symbol period represents '1', while its absence represents '0'.

IV. ELECTRICAL CHARACTERIZATION RESULTS

A. SHM NODE DESIGN

The SHM chip was designed in the TSMC 180 nm standard CMOS process and fabricated through Muse Semiconductor. Fig. 20 (right) shows a labeled die photograph of the IC, which measures 2 mm × 2 mm. All on-chip bias voltages and currents were internally generated using on-chip constant-G_m current references and 2T-type voltage references.

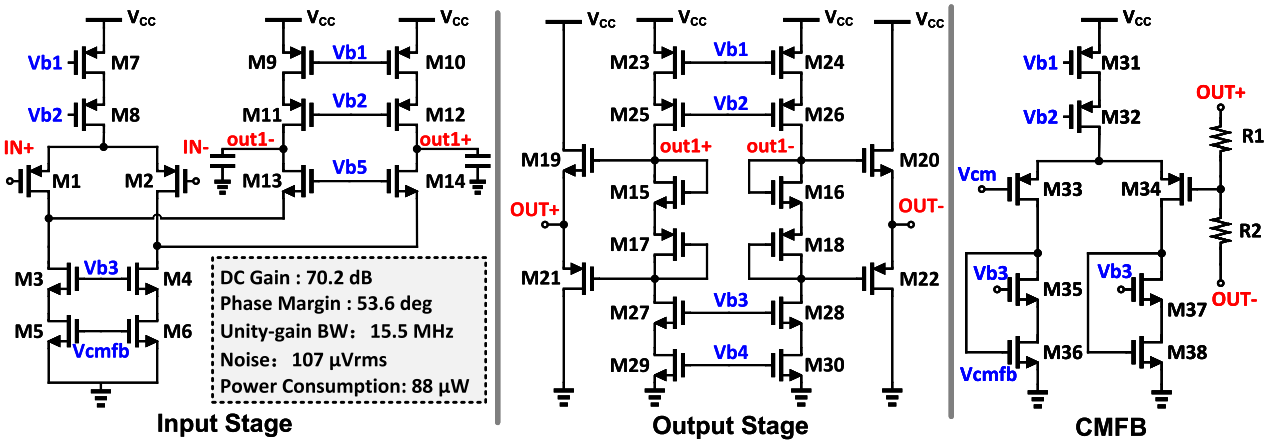

FIGURE 18. Schematic of the fully-differential op-amp used in the SHM receiver: (a) first stage, (b) second stage, (c) common-mode feedback (CMFB) circuit.

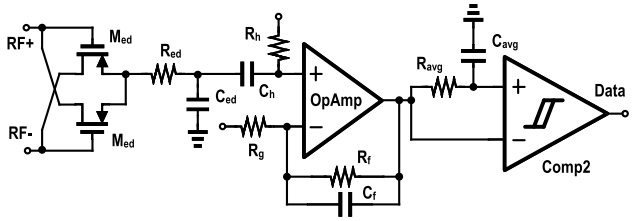

FIGURE 19. Schematic of the receiver for the ultrasonic downlink, where C_{ED} and C_{AVG} are off-chip capacitors.

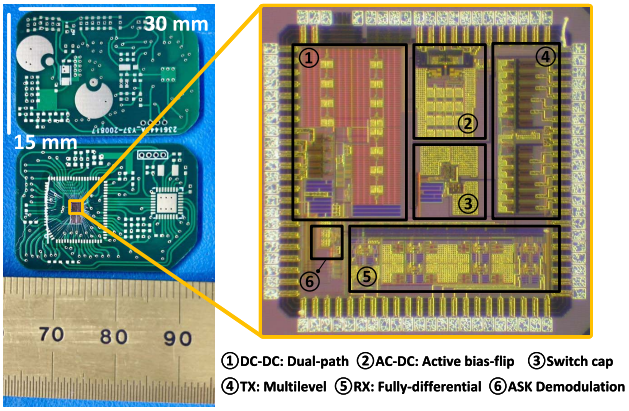

FIGURE 20. Die photograph of the proposed SHM IC.

The custom SoC was integrated with an off-the-shelf ultra-low-power MCU (MSP430FR2476, Texas Instruments), two low-profile lead zirconate titanate (PZT) ultrasound transducers (diameter of 5 mm), and passive components (including $C_{RECT} = 10\ \mu$F, $C_{LOAD} = 22\ \mu$F, and $C_{STOR} = 11$ mF) to realize miniaturized and fully-autonomous wireless SHM sensor nodes, as shown in Fig. 20 (left). Bare dies were assembled using a chip-on-board method to minimize node size (currently, 15 mm × 30 mm). This section describes electrical test results from the sensor node, while the next section presents SHM results from a test-bed.

B. ACTIVE RECTIFIER

An experimental setup was used for measuring the VCE and PCE of the active rectifier. The input AC voltage and current were monitored using two differential probes, with the second connected across a 120 Ω sense resistor. The output DC voltage V_{RECT} at various loads R_L was monitored using a Keithley 2450 source meter unit (SMU).

Fig. 21 shows measured results from the proposed active bias-flip rectifier. Figs. 21(a) and (b) show the PCE and VCR, respectively, as a function of input frequency f_{in} for three different values of load resistance (R_L). Both PCE and VCR decrease with frequency due to increased dynamic loss in the switches and comparators. Also, PCE decreases with increased load (i.e., lower values of R_L) at low frequencies due to increased conduction loss in the switches, but the trend is reversed at high frequencies where dynamic loss (which is largely load-independent) is dominant. Excellent performance (PCE > 85%, VCR > 90%) is obtained over the expected operating range ($R_L = 5 - 15$ kΩ, $f_{in} < 400$ kHz). Figs.21(c) and (d) show the PCE and VCR, respectively, as a function of load resistance R_L for three different values of input frequency. Fig. 21(e) shows that the measured PCE and VCR are nearly independent of AC input amplitude over the typical operating range ($V_{AC} = 1.1 - 1.9$ V) at $f_{in} = 300$ kHz. This result again suggests that conduction loss (which decreases with V_{AC}) is small compared to dynamic loss. Fig. 21(f) shows the measured transient voltage/current waveform under various loading conditions in two cases: i) without switch-off delay compensation (top); ii) with switch-off delay compensation (bottom). Note that compensation eliminates reverse curent flow, as expected. Fig. 21(h) shows the output power as a function of R_L in two cases: i) using the active rectifier (AR) alone, and ii) combining the AR with a small off-chip inductor ($L = 8.2\ \mu$H) and the bias-flip circuit. The latter increases the maximum

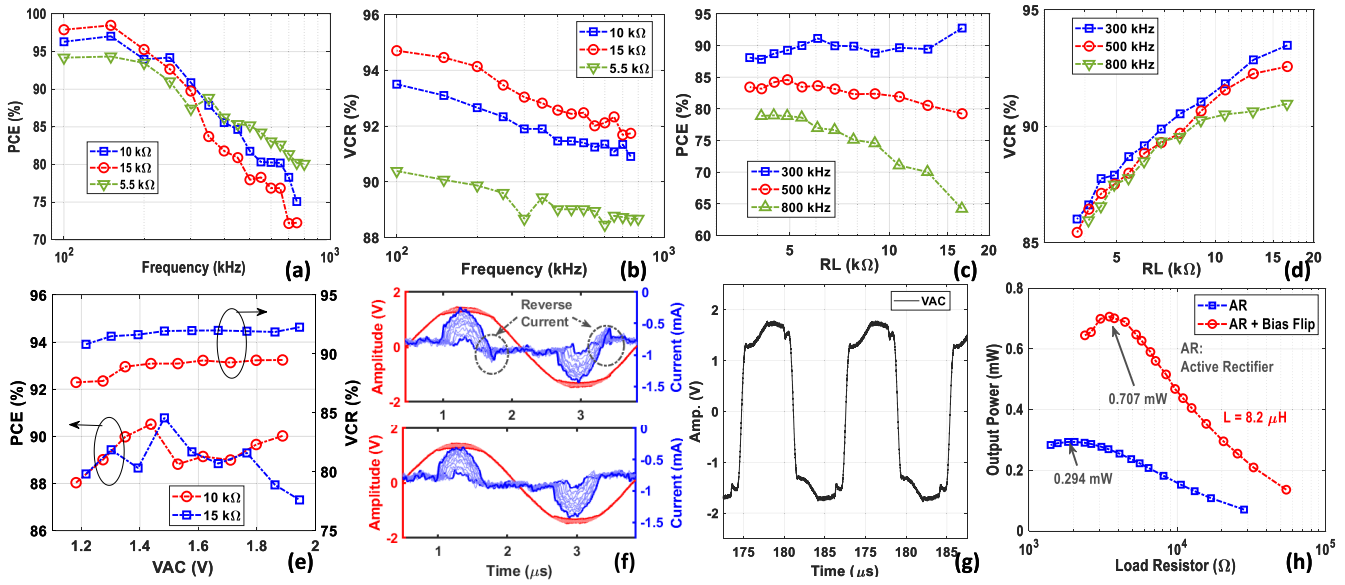

FIGURE 21. AC-DC experimental results: (a) and (b) PCE and VCR versus carrier frequency when loaded with 5.5 $k\Omega$, 10 $k\Omega$, and 15 $k\Omega$ resistors; (c) and (d) PCE and VCR versus different load resistors when using carrier frequencies of 300 kHz, 500 kHz, and 800 kHz; (e) Measured PCE and VCR of the rectifier versus AC voltage amplitude for two values of load (R_L). (f) transient voltage/current waveform with/without switch-off delay compensation: compensation off (top) and compensation on (bottom); (g) boosted bias-flip voltage waveform across the transducer; (h) Output DC power versus R_L with and without the bias flip circuit. All results were obtained at f_{in} = 300 kHz unless otherwise specified.

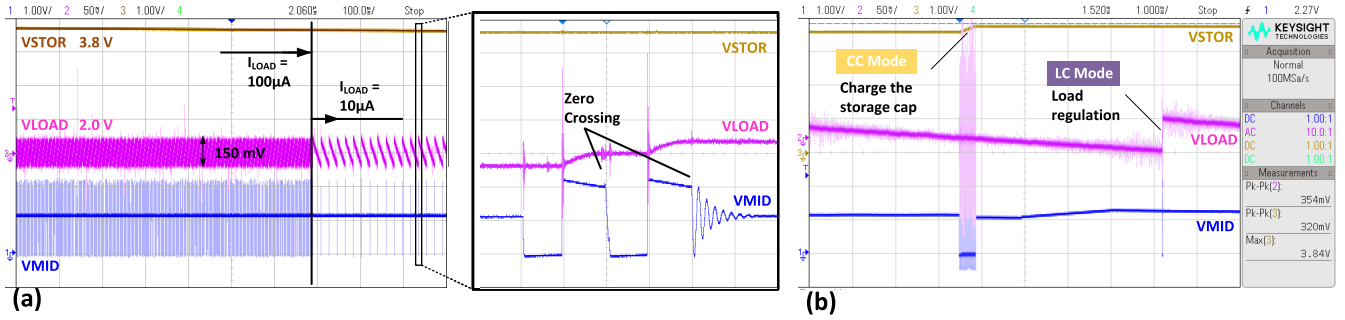

FIGURE 22. Typical measured waveforms for the DC-DC converter: (a) load regulation on 2 V power supply when the load current steps from 100 μA to 10 μA; (b) zoom-in views for the CC and LC modes, illustrating time sharing of the inductor.

available power by 2.4×, as expected. The corresponding transient waveform across the transducer can be observed in Fig. 21(g).

C. DC-DC CONVERTER

Typical measured waveforms for the DC-DC converter are shown in Fig. 22(a). The figure on the left shows a zoomed-out view (100 ms/division), highlighting the response to a load step. The figure on the right shows a zoomed-in view (2 ms/division), highlighting the zero current switching (ZCS) waveform for the load converter. Fig. 22(b) shows a zoomed-in view (1 ms/division) for cases where the CC and the LC modes are ON, respectively. As expected, the voltage of the common drain node (V_{DRAIN}) equals V_{STOR} when the CC is ON, while it equals V_{LOAD} when the LC is ON. After either converter turns off, the parasitic capacitance at V_{DRAIN} (which is now floating) results in high-frequency ringing. However, this does not affect the regulated voltages.

Fig. 23 summarizes the measured PCE of the DC-DC converter versus load current. Fig. 23(a) shows the PCE for the time-shared boost converters (CC and LC) under normal conditions, with the system cycling between states 2 and 3 such that $\alpha > 0$. The figure shows that PCE > 70% is maintained over the typical range of V_{RECT} for load currents >30 μA. Fig. 23(b) shows the PCE for the back-up buck converter (BC), which is only active in state 1. In this case, PCE >78% is maintained over a wide range of load currents.

D. SWITCHED-CAPACITOR DC-DC CONVERTERS

Fig. 23(c) compares measured and simulated PCE of the 1/2 and 1/3 ratio switched-capacitor (SC) DC-DC converters (used by the SHM transmitter) versus output power for various conversion ratios and clock frequencies f_{clk}. PCE improves with f_{clk}, as expected; this is because the output resistance R_{out} of a SC converter is a strongly-decreasing

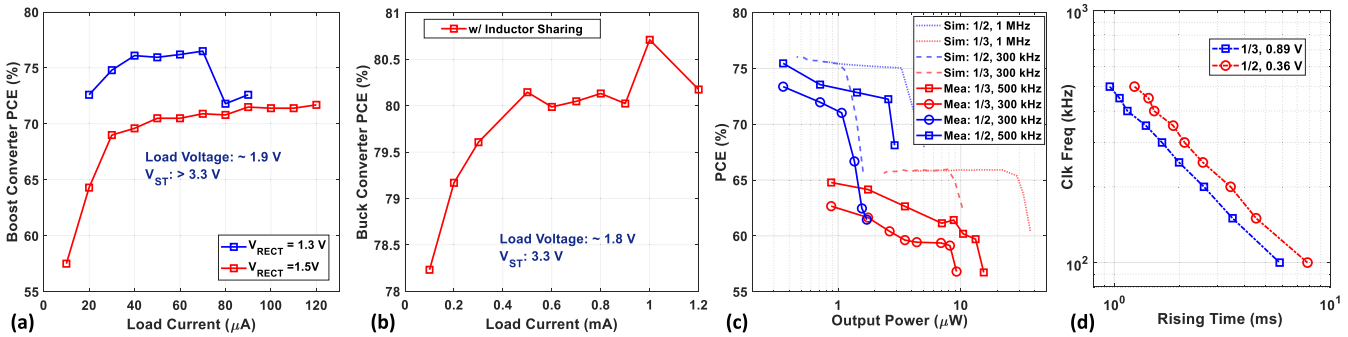

FIGURE 23. (a)-(b) Measured PCE for the DC-DC converters versus load current: (a) the boost converters (CC and LC, operating simultaneously with $\alpha > 0$) for different values of V_{RECT}; (b) the back-up buck converter (BC). (c)-(d) Measured performance of the 1/3 and 1/2 ratio switched-capacitor DC-DC converters used to power the SHM transmitter: (c) PCE versus output power for various clock frequencies and conversion ratios, compared with simulations; and (d) voltage rise time versus clock frequency.

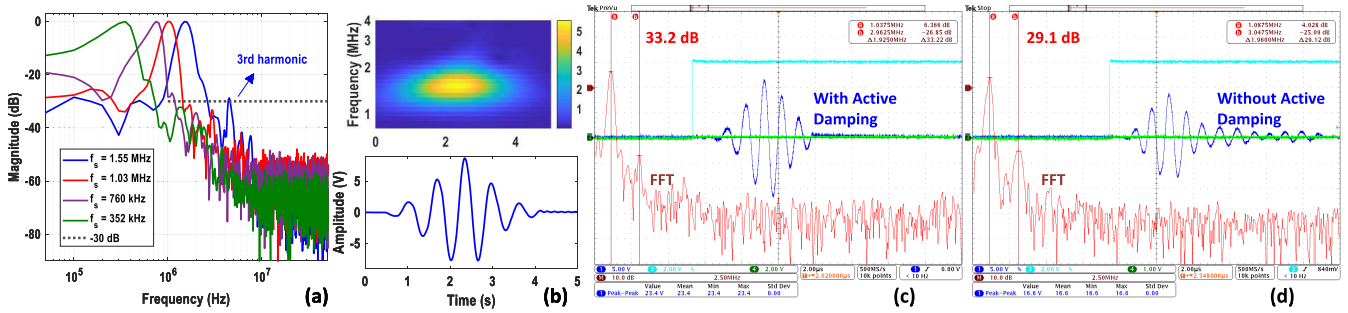

FIGURE 24. Measured results of the SHM transmitter: (a) output spectrum of the transmitter at various operating frequencies. The worst-case amplitude of the third harmonic is < -30 dBc.(b) typical output pulse across the transducer in the time-frequency plane (top) and time-domain (bottom). (c) and (d) Measured excitation waveforms with/without active damping, respectively.

function of switching frequency. In particular, theoretical models predict $R_{out} \propto 1/f_{clk}$ when f_{clk} is relatively low (known as the slow-switching limit) [27]. In addition, the measured PCE is slightly higher than the simulations, probably due to higher-than-expected switching losses due to parasitic capacitance. The 1/1 converters do not contribute significantly to power loss since they use a single switch, which results in significantly higher PCE; thus, their performance is not shown here. Fig. 22(d) plots the rise time of the 1/2 and 1/3 converters versus f_{clk}. The figure shows that rise time is inversely proportional to f_{clk}, which suggests that $R_{out} \propto 1/f_{clk}$ in agreement with theoretical models.

E. SHM TRANSMITTER

Fig. 24 shows electrical test results for the SHM transmitter. Fig. 24(b) shows a typical output pulse across the transducer in the time-frequency plane (top) and the time-domain (bottom). The waveform closely resembles a Hamming-windowed tone burst, as desired. Note that passive amplification by the tuned *LRC* load significantly increases the peak voltage amplitude compared to that generated by the chip ($\pm$3.3 V).

The resulting frequency spectra (at different operating frequencies) are shown in Fig. 24(a). In each case, the off-chip series inductors (L_1 and L_2) were adjusted to match the desired operating frequency. The smooth envelope of the pulse strongly suppresses side-bands; the worst-case PSL is $\sim$30 dB, in agreement with simulations. Similarly, the tuned circuit suppresses harmonics, with worst-case out-of-band emissions (caused by the third harmonic) being smaller than -30 dBc. However, it also results in significant pulse ringdown, i.e., relatively slow decay of residual energy in the transducer after the pulse. Such ringdown is suppressed using active damping, i.e., by using shunt switches (designed to be large turn-on resistance to avoid the off-chip damping resistor) connected at each PZT terminal (denoted by SWNd in Fig. 13) that are turned on after the end of each pulse. Fig. 24(c) shows a typical measured excitation waveform when using active damping for ringdown suppression; a PSL of 33.2 dB is observed. On the other hand, Fig. 24(d) shows the excitation waveform with active damping disabled. In the latter case, pulse ringdown degrades the PSL by $\sim$4 dB (to 29.1 dB).

F. SHM RECEIVER

Fig. 25(a) shows measured small-signal transfer functions for the receiver at different gain and bandwidth settings; these results are in good agreement with simulations. The maximum available -3 dB bandwidth is $\sim$100 kHz,

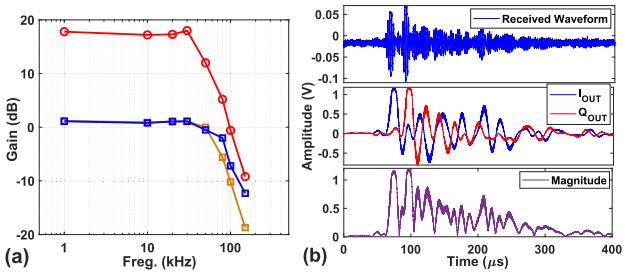

FIGURE 25. (a) Measured small-signal transfer functions of the SHM receiver at different gain and bandwidth settings. (b) Typical measured input waveform in SHM mode (top) and the resulting differential outputs of the receiver chain: I and Q components (middle) and magnitude (bottom).

which is adequate over the desired range of center frequencies for SHM measurements ($f_0 < 400$ kHz) given that the excitation bandwidth is $\approx f_0/4$. Similarly, the gain range of ~10 to 50 dB is adequate for SHM applications, since received signal amplitudes of 1-30 mV are typical in both transmission and reflection mode as shown in Fig. 25(b).

G. PERFORMANCE SUMMARY AND COMPARISON

Table 1 compares the performance of this chip with other SHM ICs in the literature, including our own earlier work [24], [28]. The chip described in this paper is power-efficient and achieves excellent spectral localization of the transmit waveform (−30 dB to −36 dB) over a broad frequency range (0.05-2.5 MHz) compared to previous work by suppressing both sidelobes and harmonics. It is also the first to integrate ultrasonic power and half-duplex data transfer capabilities within the same chip, thus enabling ultrasonically-coupled and remotely-powered SHM sensor nodes.

V. ACTIVE SHM MEASUREMENTS

The functionality of the chip was verified by carrying out SHM measurements out on a test-bed representing an airframe panel. For this purpose, six wireless sensor nodes (#1–#6) were attached on one side of a carbon fiber reinforced polymer (CFRP) sheet (0.3 m × 0.3 m in size, 2 mm thick).

A. POWER TRANSFER

Using the bias-flip circuit, a peak output power of ~75 μW was obtained at a distance of ~17 cm (from node #3 to node #4) for a transmit waveform of 30 V_{pp} at the optimal excitation frequency of $f_{in} = 409$ kHz, as shown in Fig. 27(a). Similar measurements for a slightly shorter link (distance ~12 cm, from node #2 to node #5) and closely-spaced excitation frequencies ($f_{in} = 376$ kHz and 377 kHz) are shown in Fig. 27(b) for a transmit waveform of 20 ~ 30 V_{pp}. These results show that available power decreases significantly (by ~25%) when f_{in} increases by only 1 kHz from its optimum value, which highlights the frequency-selective nature of the acoustic channel and the need to adaptively

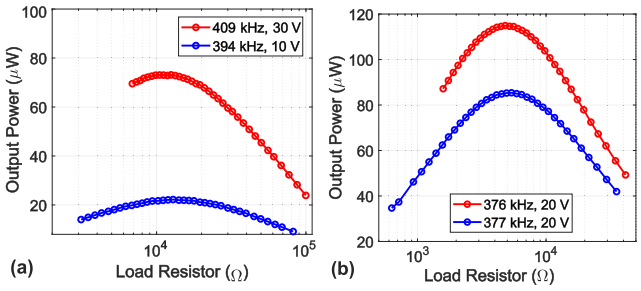

FIGURE 26. (a) #3-#4 pair power transfer; (b) #2-#5 pair power transfer.

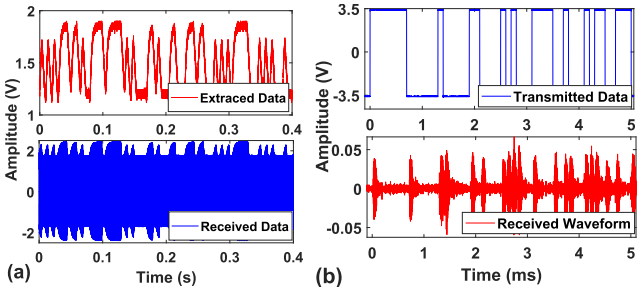

FIGURE 27. (Typical waveforms measured for the ultrasound data link: (a) BPSK downlink at a bit rate of 200 bits/sec; (b) uplink at a bit rate of 10 kbits/sec.

set f_{in} for each node using nMPPT methods. It is also interesting to note that available power levels are significantly lower (by about 3×) than earlier experiments over similar distances using thin aluminum plates [14], either because of worse acoustic impedance matching with the PZT transducers or the anisotropic mechanical properties of the CFRP sheet.

B. DATA TRANSFER

Fig. 27 shows typical downlink data transmission waveforms at 200 bits/sec and a distance of ~10 cm (from node #7 to node #3). The frequency-selective ultrasound channel converts the BFSK-modulated waveform generated by the hub (node #7) into amplitude shift-keying (ASK), as expected. The measured bit error rate (BER) is $<10^{-4}$ (no bit errors were detected within 10^4 bits). Finally, OOK-based uplink data transmission with BER $< 10^{-4}$ was achieved for distances up to ~20 cm and rates up to 15 kbits/s.

C. LOCALIZATION OF STRUCTURAL DAMAGE

A variety of damage detection and localization algorithms have been proposed for SHM using guided ultrasound waves [16], [32], [33]. The general approach relies on comparing the current observation with one or more previous baselines recorded from undamaged structures, thus generating differential features that quantify changes from the baselines. These features generally include time-varying changes in the baselines due to environmental fluctuations (e.g., in temperature), which must be removed using various compensation methods [34]. Finally, anomalies are detected when

TABLE 1. Comparison with prior work on integrated SHM ICs. Major performance improvements are highlighted.

Parameter	This Work	CICC 2018 [24]	NEWCAS 2016 [28]	JSSC 2014 [29]	JSSC 2014 [30]	TBCAS 2018 [31]
Technology	0.18 μm	0.5 μm	0.5 μm	0.25 μm BCD	0.13 μm, LAE [a]	0.18 μm BCD
# of Tx	1	1	1	4	N/A	1[b]
# of Rx	1	1	1	0	1	1[c]
Tx windowing performance	**−30-36 dB**	−30 dB	−25 dB[d]	−40 dB	N/A	N/A
Tx output (maximum)	±16 V	±6.3 V	±15 V	±36 V	N/A	15 V
Tx frequency range	**0.05-2.5 MHz**	0.1-2.2 MHz	0.55-1 MHz	780 kHz	N/A	60 Hz[e]
Remotely-powered	**Yes**	No	No	No	Yes	Yes
Communications	**Ultrasound half-duplex**	I^2C	No	No	Inductive half-duplex	Ultrasound downlink
Downlink (rate & BER)	80 bps @ 10^{-4}	400 kbps[f]	N/A	N/A	2 Mbs @ 10^{-5}	11 kps @ 10^{-5}
Uplink (rate & BER)	10 kbps @ 10^{-4}	400 kbps	N/A	N/A	2 Mbs @ 10^{-5}	N/A
Tx power consumption	**13.2 μJ / 5 μs TX**	875 μW	325-575 μW	28 μJ / 5 μs TX	N/A	N/A
Die size	2 × 2 mm^2	1.1 × 2.2 mm^2	0.55 × 1.1 mm^2	3.6 × 3.6 mm^2	2 × 2 mm^2	1.48 × 2.42 mm^2

a: Large-area electronics (LAE) using a-Si on 50 μm polyimide @ 180°C; b: Current/optical stimulation; c: Strain sensing; d: theoretical value for triangular-windowed waveform; e: 22 to 5000 μA/8bit; f: I^2C standard BER.

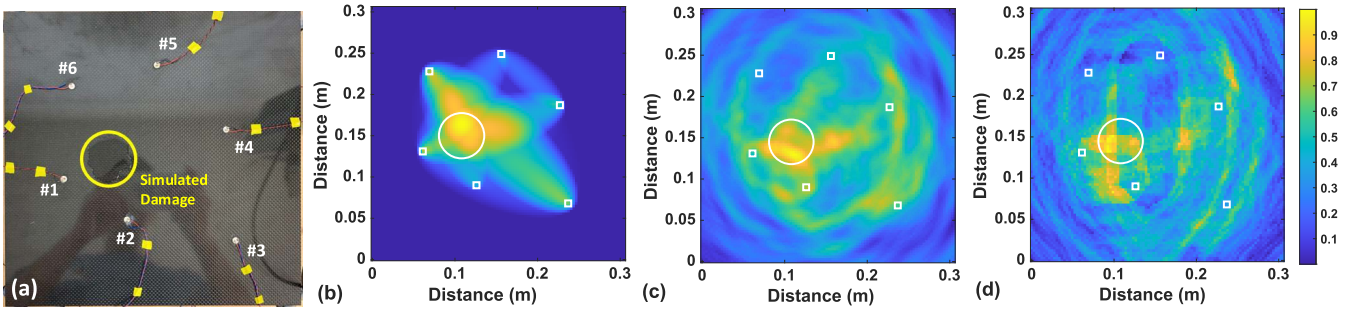

FIGURE 28. (a) Photograph of the SHM test-bed, which uses six wireless sensor nodes placed on on side of a 2-mm-thick CFRP sheet (size = 0.3 × 0.3 m). Structural damage was simulated by placing a drop of water on the sheet (as indicated by the yellow circle). (b)-(d) Damage localization maps obtained using: (b) RAPID, (c) delay-and-sum (DAS), and (d) group velocity compensated DAS algorithms, respectively.

the compensated differential features exceed certain predefined threshold values.

The set of six sensor nodes described above was considered to be a simple example of a wireless SHM network and used for initial damage localization experiments on the CFRP test-bed. For this purpose, a drop of water was placed on the surface of the CFRP sheet to locally perturb the Lamb wave velocity and thus simulate structural damage, as shown in Fig. 28(a). During the active SHM experiments, we wirelessly precharged the SHM nodes (e.g., $V_{STOR} > 3$ V) to ensure both structural fault sensing and communications. The central node was fixed in the center of the CFRP sheet (on the other side). Data for a single measurement was acquired by transmitting from one node and receiving from all the nodes. For this purpose, each SHM node was configured to transmit (TX) or receive (RX) via predefined codes during downlink. The RX nodes turn on after initialization while waiting for the TX to send out the excitation pulse through the structure. The central node (after a predefined measurement time window, typically, 1 min) then selects each SHM node sequentially as the TX and acquires the resulting measurement data. In other words, the process is repeated with each of the 6 sensor nodes serving as the transmitter, thus resulting in a 6 × 6 data matrix.

Data matrices obtained with and without the simulated damage were processed off-line using two well-known SHM algorithms, namely RAPID (Reconstruction Algorithm for Probabilistic Inspection of Damage) [32] and delay-and-sum (DAS) [35], to extract damage localization maps. The resulting maps, which are shown in Figs. 28(b)-(c), encode the probability that damage is present at each spatial point (x, y) on the test-bed. The results show that both RAPID and DAS algorithms can successfully localize the simulated damage. However, the RAPID algorithm relies on combining pairwise measurements and thus has poor sensitivity to points outside the convex hull of sensor node positions, which reduces its usefulness for large-area SHM. While the DAS algorithm does not suffer from this problem, a close examination of the resulting damage map (Fig. 28(c)) shows relatively poor spatial resolution and several unwanted maxima outside the damage region. These issues can be addressed by using a more accurate Lamb wave propagation model. Due to the anisotropic mechanical properties of the CFRP sheet, the group velocity acquires a non-uniform angular

dependence $v_g(\theta)$ that affects the DAS results. This dependence was experimentally characterized for the test-bed by using pair-wise propagation measurements and then included in the DAS algorithm. The resulting group velocity compensated damage map is shown in Fig. 28(d); it has significantly improved spatial resolution, as expected.

VI. CONCLUSION

This paper has described a highly-integrated SoC that enables ultrasonically-coupled wireless SHM networks on structures. Electrical test results confirm the functionality of all major on-chip blocks, including the PMU, SHM transceiver, and ultrasound data transceiver. The chip was used to realize autonomous sensor nodes that were successfully deployed on an SHM test-bed (CFRP panel). Future work will focus on further miniaturization of the sensor nodes by integrating a two-channel ADC, clock generator, FSM, and SRAM on the chip, thus eliminating the external MCU.

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