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RESEARCH ARTICLE

A 6.3-ppm/°C, 100-nA Current Reference With Active Trimming in 28-nm Bulk CMOS Technology

ANDREA BALLO, (Member, IEEE), ALFIO DARIO GRASSO, (Senior Member, IEEE), AND MARCO PRIVITERA, (Member, IEEE)

Dipartimento di Ingegneria Elettrica Elettronica e Informatica, University of Catania, 95125 Catania, Italy

Corresponding author: Alfio Dario Grasso (agrasso@dieei.unict.it)

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ABSTRACT This paper introduces a current reference based on ΔV_{GS} generation principle and adopts integrated poly-p+ resistors and a nW-power OTA to reduce the line sensitivity. Implemented in a 28-nm standard CMOS technology, the circuit provides a nominal current equal to 100nA and operates down to 0.6 V with a line sensitivity equal to 1.2 %/V in the range [0.8-1.8] V and a temperature coefficient equal to 6.3 ppm/°C in the range [10-90]°C. Comparison with the state-of-the-art confirms the validity of the proposed solution and its suitability to be exploited in ultra-low-power and area-constrained applications.

INDEX TERMS Current reference, low voltage, low power, area-efficient, Internet of Things, sensor nodes, implanted biomedical devices.

NOMENCLATURE

- q = $1.602 \cdot 10^{-19}$ C, elementary charge of electrons.
- k_B = $1.38 \cdot 10^{-23}$ J/K, Boltzman constant.
- I_D = drain current.
- S_i = W_i/L_i aspect ratio of the i-th transistor.
- μ = mobility of carriers in the channel.
- V_{TH} = threshold voltage.
- K_T = temperature coefficient for threshold voltage.
- b_R = 1^{st}-order temperature coefficient of resistors.
- c_R = 2^{nd}-order temperature coefficient of resistors.
- β_R = b_R/R relative temperature coefficient of resistors.
- V_T = $k_B T/q$, thermal voltage.
- T_0 = room temperature, T = 300 K.
- ϵ_{OX} = electrical permittivity of the oxide, SiO_2.
- t_{OX} = thickness of the oxide.
- C_{OX} = ϵ_{OX}/t_{OX}, gate-oxide specific capacitance.
- N_{CH} = channel doping concentration.
- n_i = intrinsic carrier concentration.
- N_C = density of state in the conduction band at T = 300 K.
- N_V = density of state in the valence band at T = 300 K.
- E_g = energy band-gap of silicon.
- n = $1 + C_d/C_{OX}$ sub-threshold slope factor.

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I. INTRODUCTION

The last decade technological improvements in the fabrication of nanometer-scale integrated active devices is doubtless the key factor that has given birth to the paradigm of the Internet-of-Things (IoT). The reduction of cost per transistors has paved the way, for sub-mm^2 electronic devices, to their pervasive use in smartphones, cars, houses, industrial tools and, more recently, implantable medical devices (IMDs) [1], [2], [3].

These lasts, more specifically than the others, are dominated by low invasiveness as main feature. Since most of the area of an electronic device is occupied by its battery, the always growing demand of battery-less and energy-autonomous IoT nodes has led to the concept of Energy Harvesting for IMDs [3], [4]. This concept is intended as the ability of scavenge energy from the external environment (i.e., light, heat and vibrations) and/or from externally coupled energy sources as electromagnetic fields or acoustic ultrasonic pressure waves [3]. In addition, being the harvested

energy limited in terms of power density and being the maximum overall power budget lower than few mW, the ultra-low power (ULP) consumption (i.e., μW or, better, nW-power level [5], [6], [7], [8]) is the second key-factor that enables to disseminate complex electronic systems in human bodies.

The ability to collect data and measurements of vital signs with long-term monitoring wireless sensors networks (WSNs) in implanted or wearable devices requires high accuracy in both analog and digital circuits against variations of temperature and supply voltages [9], [10]. Current references (CRs) ([11], [12], [13], [14], [15], [16], [17], [18], [19], [20], [21], [22], [23], [24], [25], [26], [27], [28], [29], [30], [31], [32], [33], [34]) belong to these high-precision analog circuits and are mainly adopted for digital-to-analog converters (DACs) ([35], [36]), current-starved ring-oscillators (CSROs) ([37], [38], [39]), biasing block for amplifiers and filters ([40], [41], [42], [43], [44]), current-mode analog-to-digital converters (ADCs) ([45], [46]) and, more recently, they have been adopted to control the output voltage of integrated DC/DC converters (i.e., charge-pumps [47]) or as auxiliary circuits in communication sub-systems (i.e., BPSK demodulators [48], [49]).

Similarly to the review in [34], it is possible to classify the literature on the generation of constant-with-temperature (CWT) currents into four categories:

1) *β-multipliers*: starting from the results of the Widlar current generator reported in [50], it is possible to divide a proportional-to-absolute-temperature (PTAT)-voltage with a poly resistance with the same temperature coefficient (TC), obtaining thus a CWT current as in [11], [16], [20], [21], [22], [23], [25], [26], [28], and [30].
2) *ZTC*: since all the transistors show a zero-temperature-coefficient (ZTC) gate-to-source voltage bias point, these temperature unsensitive currents are generate through a $V_{GS}(T)$. Indeed, when working in strong-inversion transistors a slightly PTAT bias is required to obtain a ZTC-working transistor, while when in weak-inversion, a complementary-to-absolute-temperature (CTAT) bias point is needed for the same purpose [13], [17], [18], [51]. Also 2T-based current reference belong to this methods, since they generate CTAT (or PTAT) bias voltage by exploiting the 2T-voltage reference structure [29], [33].
3) *PTAT+CTAT*: they exploit the weighted sum between PTAT and CTAT current generators. The principle of the PTAT generation relies on $\Delta V_{BE}/R$ (using BJTs); on the other hand, the CTAT temperature dependency is obtained by using the ratio between ΔV_{GS} (or a V_{BE} of a BJT) of NMOS transistors and a resistor [12], [14], [15], [19], [24], [27], [31], [32].

This work aims to present a novel current reference implemented in the 28-nm Bulk CMOS technology provided by TSMC. It is based on ΔV_{GS} generation principle and adopts integrated poly-p+ resistors and a nW-power, self-biased, single-stage OTA to reduce the line sensitivity of the circuit that provides a reference current, $I_{REF} = 100$ nA. Moreover, it is well-suitable to work down-to 0.6-V supply voltage, revealing very-low TC comparable to that of a Bandgap Current reference (BGCR), while the overall power consumption can be reduced down to 180 nW, when $V_{DD} = 0.6$ V and 230 nW with $V_{DD} = 0.8$ V. Furthermore, an active trimming network is added to reduce the PVT variation and compensate for the TC in all the five simulated process corners.

The current reference is designed for an implanted biomedical device, where the average operating temperature is [20-50]°C. However, it is capable of working with better performance as compared to the state-of-the-art in the range [0-100]°C. The paper is organized as follows. Section II illustrates the working principle of the proposed current reference. Section III explains the proposed current reference with the active trimming network, while Section IV reports the layout and the post-layout simulations of the circuit. Section V presents the comparison of the proposed CR with the previous arts and, finally, in Section VI concluding remarks and comments are reported.

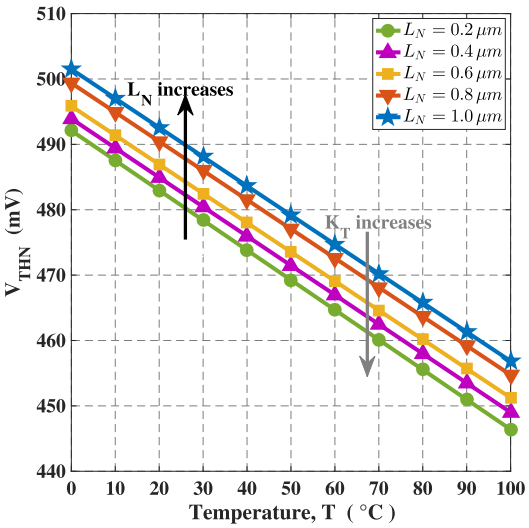

FIGURE 1. Threshold voltage of SVT09 thin-oxide n-type transistors operating in sub-threshold region with fixed aspect ratios, $S_N = 10$. The Figure refers to a 28-nm Bulk CMOS technology provided by TSMC and adopted in this work.

II. WORKING PRINCIPLE

A. BEHAVIOUR OF V_{TH} IN SUB-THRESHOLD SHORT-CHANNEL DEVICES

The working principle of the proposed CMOS CR and its temperature stability is explained starting from two main considerations on the variations of the threshold voltage of transistors and with the support of Fig. 1, where the threshold voltage variation of thin-oxide n-type transistors operating in sub-threshold region is reported. The first variation relies on V_{TH} vs. temperature, when transistors work in sub-threshold region. Indeed, as explained in [13] and [52], the behaviour of V_{TH} as function of the temperature is identified and

approximated with the following linear equation

$$V_{TH}(T) = V_{TH0} - K_T \Delta T \tag{1}$$

where V_{TH0} is the threshold voltage at room temperature and K_T is positive when working in sub-threshold region, as reported in Fig. 1. Furthermore, as it can be observed in Fig. 1, while varying the channel lengths of n-type SVT09 transistors, the decreasing slopes of the curves remain almost equal each other and about $K_T \approx 446\,\mu$V/°C. In addition, after having defined the sub-threshold slope factor $n = 1 + C_d/C_{OX}$, it is possible to give out the equation for the temperature coefficient of V_{TH} as [53]

$$K_T = -(2n-1)\frac{k_B}{T}\left[\ln\left(\frac{\sqrt{N_c N_V}}{N_{CH}}\right) + \frac{3}{2}\right] + \frac{n-1}{q}\frac{dE_g}{dT} \tag{2}$$

From Eq. (2), is observed that K_T just depends on the process and does not present any significant process variations.

On the other hand, the second variation of the threshold voltage of the transistors is experimentally observed by simulation results in Fig. 1 and Fig. 2; indeed, while increasing the channel length of short-channel NMOS devices, L_N, the value of V_{THN} increases too. In conclusion, it is possible to exploit this last dependency of V_{TH} on the channel length without using devices with different threshold voltages as in Fig. 2 and as adopted by [18], [20], [22], [29], [32], [33]. This last design option leads, as main counterpart, to a more complex layout, to an increase in the number of photo-lithographic masks required for the realization and an increase to the overall cost of the chip.

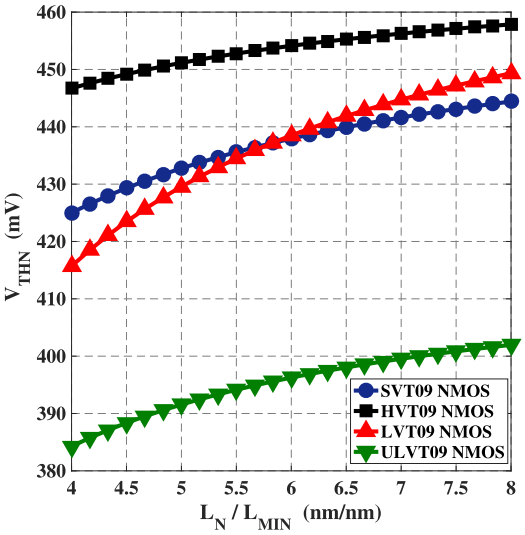

FIGURE 2. Threshold voltages of different n-type thin-oxide transistors vs. normalized channel lengths, L_N/L_{min}, where $L_{min} = 30$ nm and $W_N = 10\,\mu m$. The figure refers to a 28-nm Bulk CMOS technology provided by TSMC and adopted in this work.

B. SIMPLIFIED CIRCUIT CONFIGURATION AND ANALYSIS

The simplified circuit for the proposed CR is shown in Fig. 3. It is a 4-transistors (4T), ΔV_{GS}-based, sub-threshold and

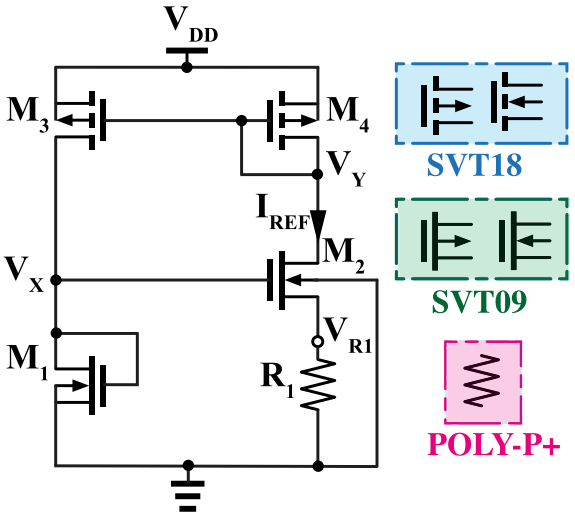

FIGURE 3. Simplified schematic of the proposed CR.

self-biased current reference, as the one proposed by [22] with the main difference, for the simplified schematic, of the use of the same type of transistors for M_1 and M_2.

The circuit is essentially made-up by a PMOS current mirror, with thick-oxide (SVT18) transistors, M_3 and M_4. The analysis of the CR is based on the Kirchhoff's Voltage Law (KVL) inside of the loop made by R_1, V_{GS2} and V_X. Indeed, by using KVL it is possible to carry-out the following equation

$$V_{R1} = R_1 I_{REF} = V_{GS1} - V_{GS2} \tag{3}$$

Suppose that both M_1 and M_2 are working in sub-threshold region and that their drain currents are given by

$$I_{D1} = I_{D0} S_1 e^{\left(\frac{V_{GS1}-V_{TH1}}{nV_T}\right)}\left[1 - e^{\left(-\frac{V_{DS1}}{V_T}\right)}\right] \tag{4a}$$

$$I_{D1} = I_{D0} S_2 e^{\left(\frac{V_{GS2}-V_{TH2}}{nV_T}\right)}\left[1 - e^{\left(-\frac{V_{DS2}}{V_T}\right)}\right] \tag{4b}$$

where $I_{D0} = \mu_n C_{OX}(n-1)V_T^2$. Moreover, by supposing that $V_{DS1} = V_X > 4V_T$ and $V_{DS2} > 4V_T$ it is possible to simplify the previous equations neglecting the channel length modulation effect as follows

$$I_{D1} \approx I_{D0} S_1 e^{\left(\frac{V_{GS1}-V_{TH1}}{nV_T}\right)} \tag{5a}$$

$$I_{D1} \approx I_{D0} S_2 e^{\left(\frac{V_{GS2}-V_{TH2}}{nV_T}\right)} \tag{5b}$$

In addition, taking into account that both M_1 and M_2 are implemented using the same type of transistors (SVT09), it was supposed, in Eq.(4a) and Eq.(5a), that $n_1 = n_2 = n$ and $C_{OX1} = C_{OX2} = C_{OX}$.

By solving Eq. (5a) and Eq. (5b) for the gate-source voltages of M_1 and M_2 and substituting these in Eq. (3) it is found out that

$$I_{REF} = \frac{1}{R_1}\left[(V_{TH1} - V_{TH2}) + nV_T \ln\left(\frac{S_2}{S_1}\cdot\frac{S_3}{S_4}\right)\right] \tag{6}$$

Since M_1 and M_2 are selected of the same type of transistors (SVT09), in order to obtain a positive quantity for $V_{TH1} - V_{TH2}$, to simplify Eq. (6), it was chosen $S_1 = W_1/L_1 = \frac{\alpha \cdot W_2}{\alpha \cdot L_2} = S_2$, with α a positive multiplicative factor. As a result, Eq. (6) becomes the following

$$I_{REF} = \frac{1}{R_1}\left[(V_{TH1} - V_{TH2}) + nV_T \ln\left(\frac{S_3}{S_4}\right)\right] \tag{7}$$

where I_{REF} just depends on design choices as the value of the resistance, R_1, the difference $V_{TH1} - V_{TH2}$ and the ratio S_3/S_4. Moreover, it is important to underline that also the integrated resistor, R_1, varies with temperature with the following expression

$$R_1(T) = R_{10} + b_R T + c_R T^2 \tag{8}$$

where R_{10} is the value of R_1 at T = 0 K and b_R and c_R are positive coefficients. In addition, for a sake of conciseness, it is possible to neglect the 2^{nd}-order term in Eq. (8), leading to a 1^{st}-order linear approximation.

The temperature stability of a CR is measured by its temperature coefficient, TC with the equation

$$TC = \frac{1}{I_{REF}} \cdot \frac{\partial I_{REF}(T)}{\partial T} = \frac{1}{I_{REF}} \frac{I_{REF,max} - I_{REF,min}}{\Delta T} \tag{9}$$

where I_{REF} is the nominal value of the DC reference current at T_0, while $I_{REF,max}$ and $I_{REF,min}$ are the maximum and the minimum value, respectively, of the reference current within the temperature range, ΔT. Then, by using the following equation is possible to carry-out the minimum value for TC

$$\frac{\partial I_{REF}(T)}{\partial T} = 0 \tag{10}$$

While R_1 and $V_{TH1} - V_{TH2}$ are chosen to obtain the desired nominal value of I_{REF}, on the other hand, by applying the definition of Eq. (10) to Eq. (7), it is possible to find out the optimum ratio, $(S_3/S_4)_{opt}$, to minimize the TC. The math passages are here summarized

$$\frac{\partial V_{R1}(T)}{\partial T} \cdot R_1 - \frac{\partial R_1(T)}{\partial T} \cdot V_{R1} = 0$$
$$\left[\Delta K_{T2,1} + n\frac{k_B}{q}\ln\left(\frac{S_3}{S_4}\right)\right] \cdot R_1 - (V_{R1} \cdot b_R) = 0 \tag{11}$$

where $\Delta K_{T2,1} = K_{T2} - K_{T1}$ (for a sake of brevity) and V_{R1} is derived out from Eq. (3) and Eq. (7). By expanding the intermediate passages reported in Eq. (11) it results that

$$\left(\frac{S_3}{S_4}\right)_{opt} = \exp\left[\frac{q}{nk_B}\left(\frac{\beta_R \Delta V_{TH1,2} - \Delta K_{T2,1}}{1 - \beta_R T_0}\right)\right] \tag{12}$$

where, for a sake of conciseness, it was indicated $\Delta V_{TH1,2} = V_{TH1} - V_{TH2}$. In a more intuitive way, Eq. (7) suggests that an increase in $\Delta V_{TH1,2}$ leads to an increase in the CTAT behaviour of the CR, while an increase in the ratio S_3/S_4 increases the PTAT component of I_{REF}. Furthermore, as can be appreciated from Fig. 1, $\Delta K_{T2,1} = K_{T2} - K_{T1}$ could be neglected in Eq. (12) when using the same type of transistors for both M_1 and M_2. Finally, by substituting the result of Eq. (12) into Eq. (7) is found out the optimum nominal value of the reference current, $I_{REF,opt}$ that minimize the TC

$$I_{REF,opt} = \frac{1}{R_1}\left[\Delta V_{TH1,2} + T_0\left(\frac{\beta_R \Delta V_{TH1,2} - \Delta K_{T2,1}}{1 - \beta_R T_0}\right)\right] \tag{13}$$

Moreover, by evaluating $\beta_R T_0 \ll 1$ and $\Delta K_{T2,1} \simeq 0$, Eq. (13) is approximated as follows

$$I_{REF,opt} \approx \frac{\Delta V_{TH1,2}}{R_1} \tag{14}$$

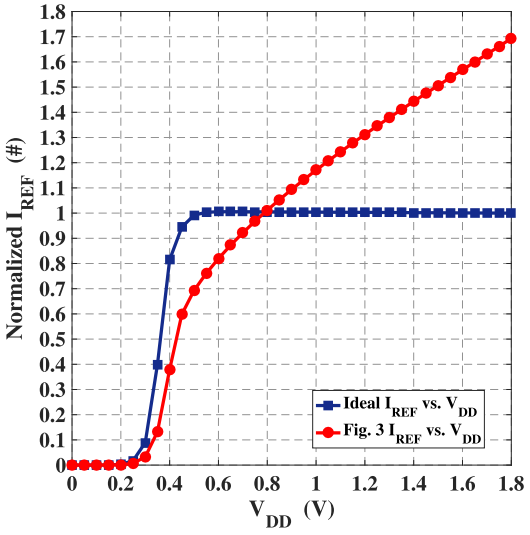

FIGURE 4. Normalized I_{REF} vs. V_{DD} for the simulated simplified schematic of the proposed CR in Fig. 3 and the ideal case.

C. LINE SENSITIVITY

The Line Sensitivity (LS) quantifies the static sensitivity of the output on the DC variations of the power supply line voltage, namely V_{DD}. The equation that allows to evaluate the LS is the following

$$LS = \frac{1}{I_{REF}} \frac{\partial I_{REF}}{\partial V_{DD}} = \frac{1}{I_{REF}} \frac{I_{REF,max} - I_{REF,min}}{V_{DD,max} - V_{DD,min}} \tag{15}$$

This quantity is a useful tool for characterizing the robustness of the CR in the presence of variations of V_{DD} as in the case battery discharge or various regulated power supply voltages ($V_{DD,L}$ and $V_{DD,H}$) inside the same SoC [54]. Since, the reference current in the simplified CR in Fig. 3 depends on the current ratio of I_{D3}/I_{D4} provided by the linear current mirror M_3-M_4, it is important to investigate on this ratio when varying V_{DD}.

$$\frac{I_{D3}}{I_{D4}} = \frac{S_3}{S_4} \cdot \frac{\left[1 - \exp\left(-\frac{V_{SD3}}{V_T}\right)\right]}{\left[1 - \exp\left(-\frac{V_{SD4}}{V_T}\right)\right]}$$
$$= \frac{S_3}{S_4} \cdot \frac{\left[1 - \exp\left(\frac{V_X - V_{DD}}{V_T}\right)\right]}{\left[1 - \exp\left(\frac{V_Y - V_{DD}}{V_T}\right)\right]}$$

$$= \frac{S_3}{S_4} \cdot \frac{\left[\exp\left(\frac{V_X - V_{DD}}{V_T}\right) - 1\right]}{\left[\exp\left(\frac{V_Y - V_{DD}}{V_T}\right) - 1\right]} \tag{16}$$

Since $V_{X,Y} < V_{DD}$ it is possible to approximate Eq. (16) as follows

$$\frac{I_{D3}}{I_{D4}} \approx \frac{S_3}{S_4} \cdot \frac{V_X - V_{DD}}{V_Y - V_{DD}} \tag{17}$$

From Eq. (17) is possible to understand that just if $V_X = V_Y$ it is true that $I_{D3}/I_{D4} = S_3/S_4$; otherwise, this above mentioned current ratio will vary with V_{DD} as reported in Fig. 4 with the red curve. Indeed, while V_{DD} increases, the drain current of M_3 increases too, leading to an increase of $V_{GS1} = V_X$, but also I_{REF} increases lowering the voltage on node V_Y.

III. THE ACTIVE TRIMMING NETWORK

The schematic in Fig. 5 shows the complete circuit of the proposed CR without the trimming network. It takes into account the advantages of the solution depicted with Fig. 3 in the previous section with the addition of a self-biased single-stage OTA (shown in Fig. 6) to improved the line sensitivity and a start-up circuit to avoid any zero bias point. The used technology is the 28-nm Bulk CMOS provided by TSMC and the simulation environment is Cadence Virtuoso.

The nominal value of the reference current is set equal to $I_{REF} = 100\,\text{nA}$. It was realized making a $\Delta V_{TH1,2} \sim 18\,\text{mV}$ drops on a nominal $R_1 = 180\,k\Omega$. This last integrated resistor was realized in poly-p+ and presents a specific resistance-over-square equals to $R_s = 576\,\Omega/\square$, while $\beta_R \approx 0.0275\,\%/°\text{C}$. The theoretical value for $(S_3/S_4)_{th}$ kept from Eq. (12) was about 1.1, while the simulated one is $(S_3/S_4)_s = 1.185$. The other components' values are summarized in Tab. 2.

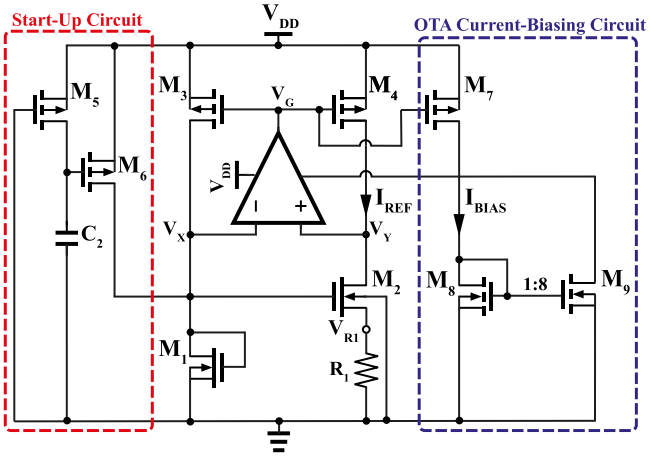

FIGURE 5. Complete schematic of the proposed CR.

The addition of the OTA provides a negative feedback control on the voltage V_G and allows keeping $V_X = V_Y \simeq 330\,mV$ whatever it will be the variation on V_{DD}. Moreover, since it does not require any stringent specification in terms

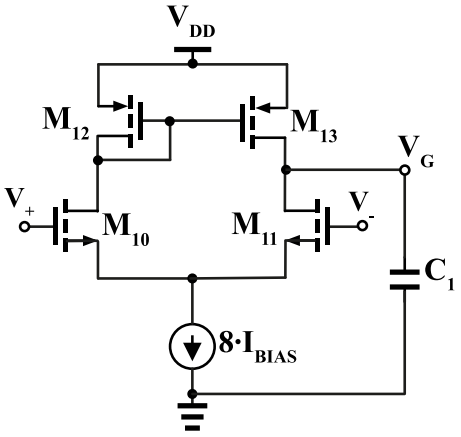

FIGURE 6. Single-stage OTA for the CR in Fig. 5. NMOS Bulks are connected to GND node and PMOS Bulks to V_{DD}.

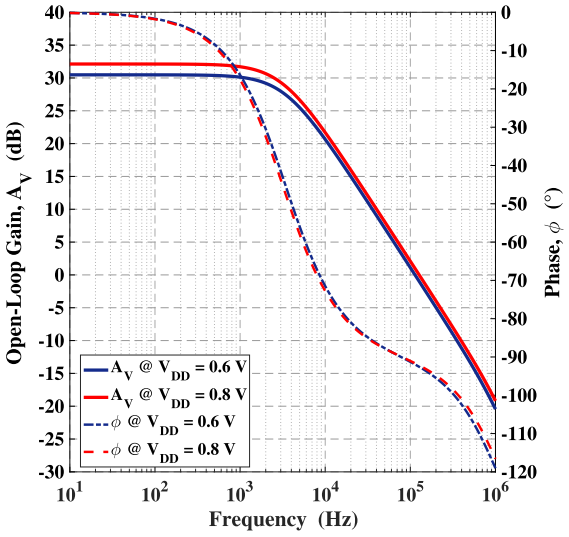

FIGURE 7. Open-Loop Gain and Phase AC simulation results for the self-biased single-stage OTA in Fig. 5 and Fig. 6, with $I_{BIAS} = 10\,\text{nA}$ and $C_1 = 1.5\,\text{pF}$.

of bandwidth and gain, it was implemented with a simple differential pair, as shown in Fig. 6. The OTA is biased by the reference current itself, by exploiting transistor M_7 and the 1:8 current mirror made up by M_8-M_9, leading to a static current consumption of about $I_{DD,OTA} = 90\,\text{nA}$. The transconductance efficiency $g_m/I_D \sim 29\,V^{-1}$ since all the transistors are working in weak-inversion region. Finally, a MOM-capacitor, $C_1 = 1.5\,\text{pF}$, was added on the output node, V_G, to provide stability to the entire CR. The AC simulations results show a DC open-loop gain, $A_V \sim 30\,\text{dB}$ and a bandwidth $f_{GBW} \sim 120\,kHz$.

Corner analysis reported in Fig. 8 and Tab. 1 shows that without any trimming sub-circuit the variations around the reference current are in the order of ±40%. Although this high inaccuracy, the minimum TC results about 10-50 ppm/°C for $V_{DD} \sim 0.8\,\text{V}$ in the temperature range $T \in [0 - 100]\,°\text{C}$.

TABLE 1. Summarizing Table for pre-layout simulation of the proposed CR without the trimming network.

Corner	SS	SF	TT	FS	FF
$I_{REF}(nA)$	70	84	100	117	140
TC^{a}_{min} (ppm/°C)	30	36	14	20	13.5
LS (%/V)^{c}	0.44	0.5	0.39	0.31	0.34

^{a}:TC_{min} @ $V_{DD} = 0.8$ V and $T \in [0-100]$ °C
^{c} evaluated in the range $V_{DD} \in [0.8-1.8]$ V.

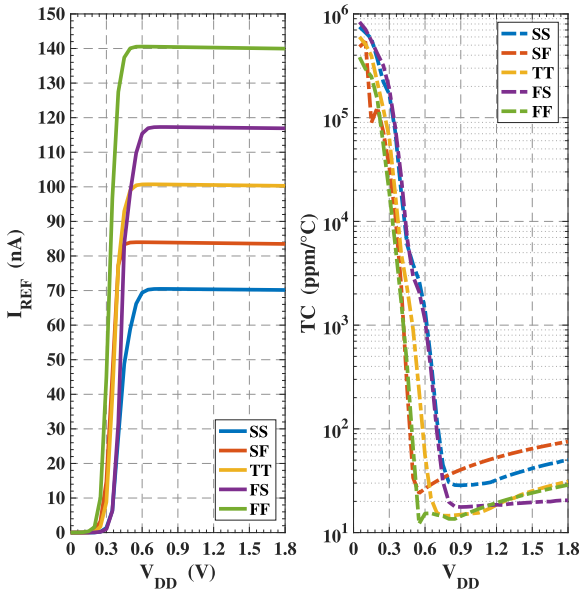

FIGURE 8. I_{REF} vs V_{DD} on the right and TC vs V_{DD} on the left for the untrimmed CR shown in Fig. 5.

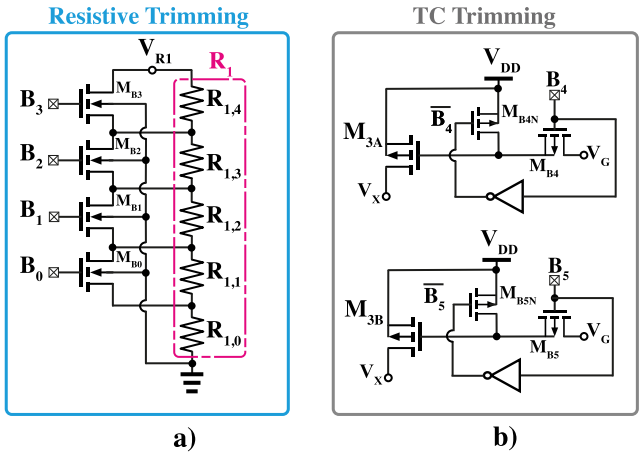

FIGURE 9. Trimming network for the proposed CR in Fig. 5. a) Correction of the nominal value of I_{REF}; b) Correction of the TC.

The schematic shown in Fig. 9a) and b) depicts the adopted trimming network for the proposed CR. The sub-circuit in Fig. 9a) allows to reduce the variations of the nominal value of I_{REF} under the simulated corners. Indeed, by using NMOS switches ($M_{B0} \dots M_{B3}$) it modifies the value of the resistance R_1 by properly adding series integrated poly-p+ resistances as a function of the measured corner (e.g., in the SS corner, all the switches are closed, in the FF corner, all the switches are open). It is also worth noticing that ON-resistances of switches, R_{ON}, have been taken into account. On the other side, the sub-circuit in Fig. 9b) compensates for the TC by properly modifying the ratio S_3/S_4 (see Eq. (12)). After post-layout simulations, it was found out that just two bits are required for this purpose. When $B_{4(5)}$ is high ($\overline{B_{4(5)}}$ is low), $M_{3A(3B)}$ is connected in parallel with M_3 increasing its aspect ratio; on the contrary, when $B_{4(5)}$ is low ($\overline{B_{4(5)}}$ is high), thanks to switches $M_{B4N(B5N)}$ the gate of $M_{3A(3B)}$ is short-circuited to V_{DD} and no current (expect from leakage one) passes through it. In addition, the trimming circuit is driven by $B_0 \dots B_5$ signals in the range of [0; V_{DD}] and the negated ones are internally generated by exploiting minimum sized inverters.

TABLE 2. Aspect ratios and component dimensions for the proposed CR in Fig. 5, Fig. 6 and Fig. 9.

Component	Size	Unit
M_1	4/1	μm/μm
M_2	2/0.5	-
M_3, M_4	5/0.5	-
M_5, M_6	5/0.3	μm/μm
C_2	18	fF
M_7	1.2/1.8	μm/μm
M_8	2.5/0.5	-
M_9	20/0.5	-
$M_{10,11}$	33.75/0.5	μm/μm
$M_{12,13}$	10/2	-
C_1	1.5	pF
$M_{B0,B1,B2,B3}$	1.5/0.3	μm/μm
M_{3A}	0.925/0.5	-
M_{3B}	0.91/0.5	-
$M_{B4,B4N}$	3/0.3	-
$M_{B5,B5N}$	3/0.3	-
$R_{1,0}$	112.5	kΩ
$R_{1,1}$	27.0	-
$R_{1,2}$	32.5	-
$R_{1,3}$	32.5	-
$R_{1,4}$	37.5	-

TABLE 3. 6-Bit Binary words used in post-layout simulations for the trimming circuit in Fig. 9a),b).

Corner	Binary Word ($B_5 \dots B_0$)	R_1 [kΩ]	Ratio (S_3/S_4)
SS	011111	112.5	1.185
SF	011110	139.5	1.185
TT	101100	172	1.182
FS	011000	204.5	1.185
FF	010000	242	1.185

IV. POST-LAYOUT SIMULATIONS

The layout of the circuit is shown in Fig. 10, where different areas have been enclosed in yellow boxes. It is important to underline that the CR Core area includes also the start-up circuit and the Active Trimming embeds the minimum size inverters for the generation of negated trimming signals, $\overline{B_4}$ and $\overline{B_5}$.

Fig. 11a) reports the power breakdown of the proposed CR circuit, referring to the static power consumption of the OTA,

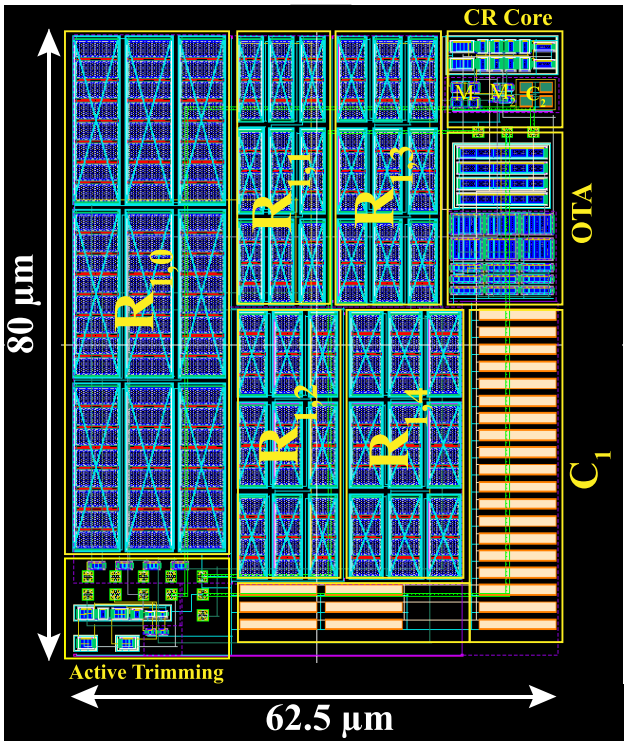

FIGURE 10. Layout of the proposed CR. The occupied area is equal to 5000 μm^2.

the reference current, I_{REF} and the left branch of the CR, namely I_{D1}, since it depends on the current passing through transistor M_1 (see Fig. 5). On the other side, Fig. 11b) shows the area breakdown of circuit referring to the layout reported in Fig. 10. As regard the post-layout simulations, they can be divided in two sets, since they mainly concentrate on the the temperature stability and on the line sensitivity.

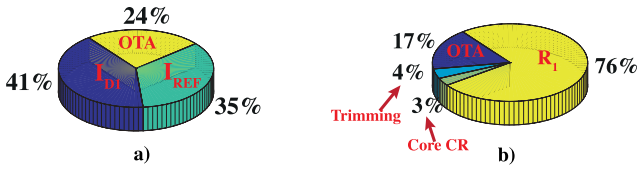

FIGURE 11. a) Power breakdown of the proposed CR. b) Area breakdown of the proposed CR.

A. CORNER ANALYSIS

As it possible to observe from Fig. 12, the TT-corner manifests a $TC_{TT} = 13$ ppm/°C over the temperature range $T \in [0 - 100]$ °C, while it reduces down to $TC^*_{TT} = 6.3$ ppm/°C over the temperature range $T^* \in [10 - 90]$ °C; in both this cases, the power supply is $V_{DD} = 0.8$ V, but, as can be appreciated from Fig. 12, when $V_{DD} = 0.6$ V, $TC_{TT} = 250$ ppm/°C for $T \in [0 - 100]$ °C. Hence, for the higher nominal power supply, the temperature behaviour of the CR meets the typical specification of the more power-wasting BGCRs with 2^{nd}-order temperature compensation.

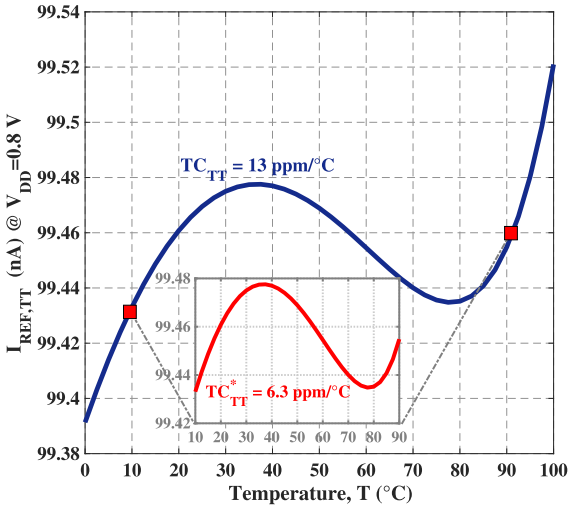

FIGURE 12. Temperature coefficient, *TC* of the proposed CR around the TT-corner in two different temperature ranges, $T \in [0 - 100]$ °C and $T^* \in [10 - 90]$ °C; $TC_{TT} = 13$ ppm/°C for the former and $TC^*_{TT} = 6.3$ ppm/°C for the latter.

Fig. 13 reports the behaviour of the proposed CR around all the five corners, when $V_{DD} = 0.8$ V, in terms of TC. This last parameters spans from 87 ppm/°C for the SF corner to 13 ppm/°C for the TT corner. In a more restricted temperature range, namely $T^* \in [10 - 90]$ °C, it could be seen that the TC is reduced in all the corners, as summarized in Tab. 4.

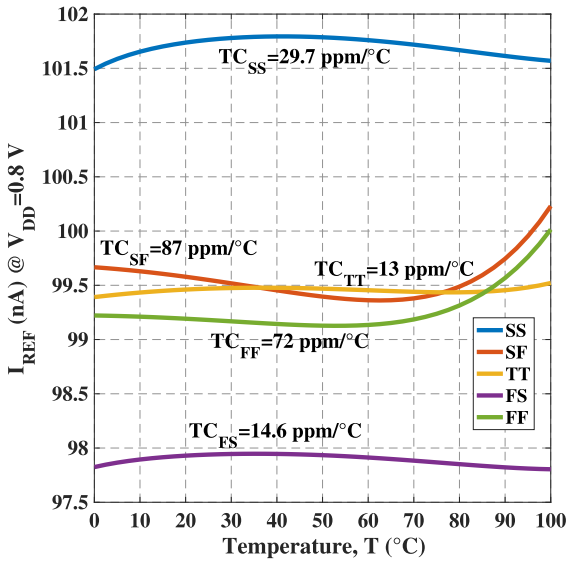

FIGURE 13. Temperature coefficients, *TC*s of the proposed CR around all the corners when $V_{DD} = 0.8$ V. The temperature range is $T \in [0 - 100]$ °C. Results are obtained after trimming.

Finally, Fig. 14 reports the transient step-response of the proposed CR in the temperature range $T \in [0 - 100]$ °C. It was simulated by applying a V_{DD} step-signal from 0 V to 0.8 V to emulate the start-up phase of the CR, for four different temperatures within the indicated range. The rise/fall time of the supply are supposed equal to 1 ms, since they

are typically provided by LDOs with this time delays. The simulated settling time for $I_{REF,TT}$ is around 200 μs.

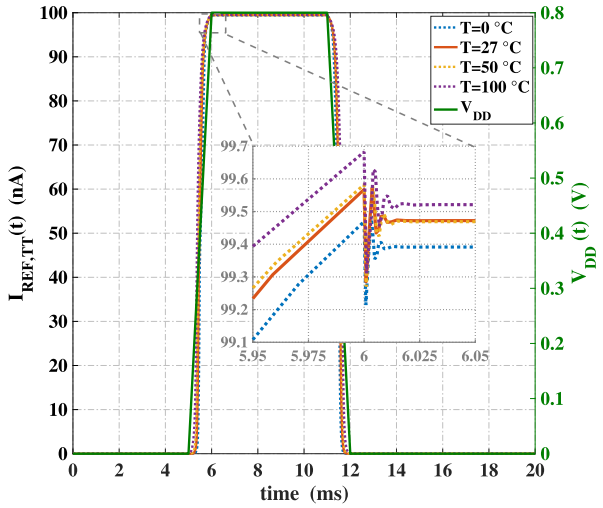

FIGURE 14. Step-response in time-domain results for the TT corner in the temperature range $T \in [0 - 100]$ °C.

B. LINE SENSITIVITY

The second set of results concentrates on the variation of the power-supply V_{DD}. Indeed, Fig. 15 shows that the minimum temperature coefficient for all the five corners is obtained around $V_{DD} = 0.8$ V, so it is possible to take this last value as the optimum one to guarantee the maximum temperature stability of the proposed CR.

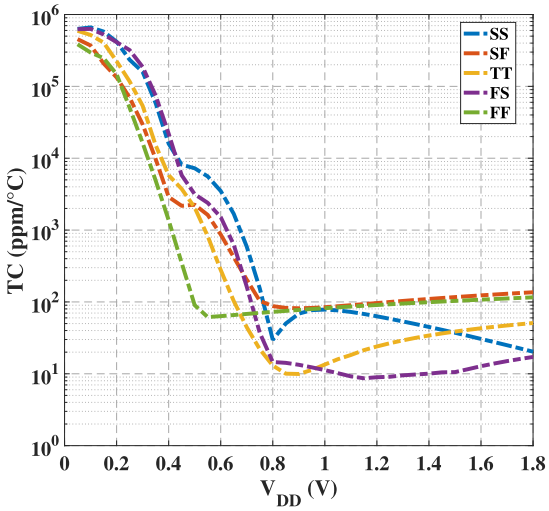

FIGURE 15. Temperature coefficients, *TC*s evaluated in $T \in [0 - 100]$ °C of the proposed CR vs power-supply voltage, $V_{DD} \in [0 - 1.8]$ V around the 5 corners after the trimming.

As concern the results shown in Fig. 16, they manifest an overall variation of the reference current at room temperature about equal to 4 nA, that is extremely low if compared to Fig. 8, where the variation of I_{REF} (w.o. the trimming circuit)

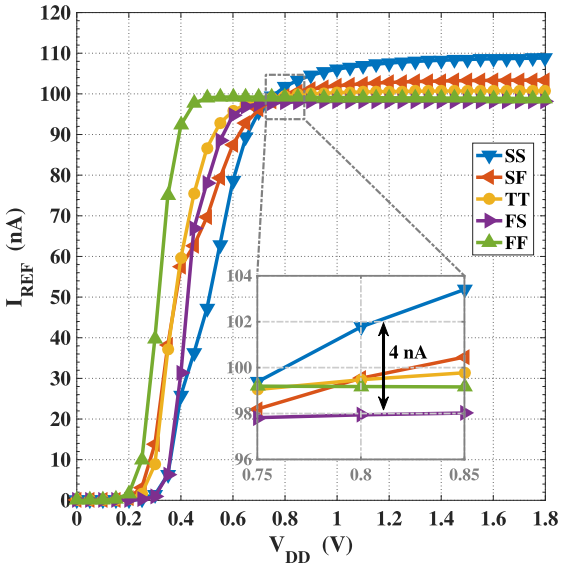

FIGURE 16. I_{REF} of the proposed CR around the five corners vs. V_{DD} at T_0 after the application of the trimming circuit with binary word configuration shown in Tab. 3.

was around 70 nA, from the SS to the FF corner. In addition, it is possible to notice that the line sensitivity for the SS and the SF corner is higher than other cases; this is due to the active trimming circuit, since, in these corners, all the switches are closed, but they are driven by V_{DD}-amplitude signals. By increasing V_{DD}, it will reduce the R_{ON} of switches and, thus, the nominal value of R_1. This will lead to an increase of the reference current. Nevertheless, it is also possible to change the binary word used for the trimming in Tab. 3 to increase the overall R_1 value.

TABLE 4. Summarizing table for post-layout simulation of the proposed CR with the trimming network @ $V_{DD} = 0.8$ V.

Corner	SS	SF	TT	FS	FF
$I_{REF}(nA)$	101.7	99.5	**99.5**	97.8	99.2
TC^*_{min} (ppm/°C)[a]	24.5	44.7	**6.3**	16.6	55.4
TC_{min} (ppm/°C)[b]	29.7	87	**13**	14	72
LS (%/V)[c]	6.9	3.86	**1.2**	0.2	0.32

[a] evaluated in the range $T^* \in [10 - 90]$ °C.
[b] evaluated in the range $T \in [0 - 100]$ °C.
[c] evaluated in the range $V_{DD} \in [0.8 - 1.8]$ V.

C. MONTE CARLO SIMULATIONS

Monte Carlo simulations have been executed on the proposed CR to demonstrate the robustness of the implemented system. The results of 200 simulations taking into account global and local variations around TT corner are summarized in Fig. 17. In particular, Fig. 17(left) reports the DC value of the reference current, I_{REF}. The mean value is $\mu = 99.8$ nA, while the standard deviation is $\sigma = 5.12$ nA, leading to a relative percentage variation of $\sigma/\mu \approx 5\,\%$. Fig. 17(right) shows the TC evaluated in the range $T \in [0 - 100]$ °C. The mean value is equal to $\mu = 24.7$ ppm/°C, while it not possible

TABLE 5. State-of-the-art comparison table; this work (T.W. (a);(b), first column of the table) compared with other CRs in the range [7.5-100] nA.

Parameters	T.W. (a);(b)	[11]	[12]	[13]	[14]	[15]	[16]	[17]	[18]	[19]	[20]	[21]	[22]	[23]
Type of Work	Sim.	Meas.	Meas.	Meas.	Meas	Sim.	Meas.	Meas.	Sim.	Meas.	Meas.	Sim.	Sim.	Meas.
# of sampl.	-	20	15	9	23	-	10	32	-	8	16	-	-	30
Year	2022	2007	2010	2010	2013	2015	2016	2017	2017	2019	2019	2019	2020	2021
Techn. (nm)	28	350	350	350	180	180	180	180	180	500	180	180	180	180
V_{DD} (V)	0.6-1.8	1.5-4.0	1.3-3.0	1.8-3.0	0.8-2.0	1.0-1.8	1.25-1.8	1.5-2.4	0.9-1.8	3.0	0.7-2.0	1.4-3.6	0.8-2.0	2.0-5.0
I_{REF} (nA)	99.5	9.14	9.95	96	54.1	14	92.3	35.02	10.86	90	9.97	50	7.5	51
I_{DD}/I_{REF}	2.89	4	6.84	5.78	5.32	10.7	4.03	1.02	3.12	8.51	4.01	4.0	2	1.92
Power (nW)	230[c]	54.84	88.53	1000	288	270	670	53.53 [e]	30.5	2300	28	300	12	192
Area (mm^2)	0.005	0.035	0.128	0.015	0.245	0.010	0.0013	0.017	0.018	0.0217	0.055	0.009	0.31	0.063
T. Range (°C)	10-90;0-100	0-80	-20-80	0-80	0-80	0-70	-40-85	-40-120	-20-120	-30-85	-40-125	-55-125	-40-125	-45-125
TC (ppm/°C)	6.3;13	44	1190	520	63	10	177	282	108	361.6	150	11.6	44.52	89
LS (%/V)	1.2 [d]	0.056	0.046	0.2	0.21	0.05	7.5	3.0	0.86	4.67	0.6	0.05	0.35	1.76
FOM^a	0.22; 0.37	2.20	81.4	37.57	4.19	1.53	5.70	1.8	2.40	26.76	3.64	0.26	0.54	1.00
Proc. Var. (%)	5.0	2.16	14.1	n.d.	1.4	2.33	6.12	1.6	3.83	-	1.6	n.d.	n.d.	1.15
Trimm.	Yes	No	Yes	No	No	No	No	No	No	No	Yes	Yes	No	Yes
Complexity[b]	M-L	M-H	H	M-L	H	M	L	L	M	M	M	H	L	H
Special Comp.	Res.	No	No	No	Res.	No	No	No	ZVT Res.	BJT, Res.	HVT, Res.	Res.	HVT, Res.	BJT, Res.

[a]: $FOM = \frac{TC}{\text{T.Range}} \cdot \frac{I_{DD}}{I_{REF}}$ (ppm/°C^2); [b]: L=Low, M=Middle, H=High. [c]: @ $V_{DD} = 0.8$ V; [d]: Evaluated within the range $V_{DD} \in [0.8 - 1.8]$ V.
[e]:Overall static power consumption not indicated in [17].

TABLE 6. State-of-the-art comparison table; this work (T.W. (a);(b), first column of the table) compared with other CRs in the range [100-1000] nA.

Parameters	T.W. (a);(b)	[24]	[25]	[26]	[27]	[28]	[29]	[30]	[31]	[32]	[33]	[34]
Type of Work	Sim.	Sim.	Sim.	Sim.	Sim.	Meas.	Meas.	Meas.	Sim.	Sim.	Meas.	Meas.
# of sampl.	-	-	-	-	-	10	45	10	-	-	15	10
Year	2022	2009	2013	2014	2017	2017	2018	2019	2019	2019	2021	2022
Techn. (nm)	28	180	180	180	180	350	180	350	180	180	180	180
V_{DD} (V)	0.6-1.8	0.7	1.0-3.3	1.2-3.0	1.7-1.9	2.0-3.6	0.45-1.8	1.35-3.6	1.2-2.0	1.35-3.0	0.6-1.8	0.65-1.8
I_{REF} (nA)	99.5	941	1000	500	1000	1000	338	230	142.5	100	190.8	990
I_{DD}/I_{REF}	2.89	8.44	2.0	3.3	50	2.05	1.4	2.02	4.8	4.0	1.0	1.0
Power (nW)	230[c]	5300	2000	1980	85000	4100	213	630	820.8	540	114.6	640
Area (mm^2)	0.005	0.02	0.01	n.d.	0.05	0.057	0.00075	0.036	0.02	0.0012	0.004	0.034
T. Range (°C)	10-90;0-100	-25-75	-40-120	-40-120	-40-140	-40-120	0-80	-45-125	-40-85	0-100	0-100	-40-85
TC (ppm/°C)	6.3;13	29	153	119	29.6	143	578	221	40	335	1480	38
LS (%/V)	1.2 [d]	n.d.	0.67	0.69	n.d.	2.73	3.9	3.8	1.4	0.03	1.4	0.20
FOM^a	0.22; 0.37	2.44	1.91	2.45	8.22	1.83	10.11	2.62	1.53	13.40	14.80	0.30
Proc. Var. (%)	5.0	0.3	n.d.	0.43	3.0	3.7	2.7	5.3	3.13	2.1	3.93	33.3
Trimm.	Yes	No	No	Yes	No	No	Yes	No	No	No	No	Yes
Complexity[b]	M-L	M	L	H	H	L	L-M	L-M	M	M	Low	Low
Special Comp.	Res.	Res.	Res.	Res.	BJT, Res.	Res.	ZVT	Res.		HVT	ZVT	Res

[a]: $FOM = \frac{TC}{\text{T.Range}} \cdot \frac{I_{DD}}{I_{REF}}$ (ppm/°C^2); [b]: L=Low, M=Middle, H=High. [c]: @ $V_{DD} = 0.8$ V;
[d]: Evaluated within the range $V_{DD} \in [0.8 - 1.8]$ V.

to evaluate a standard deviation, since the distribution is not a Gaussian one. On the other hand, it is possible to observe that the minimum and maximum TC value is equal to to 7.6 ppm/°C and 152.3 ppm/°C, respectively.

V. COMPARISON

The state-of-the-art comparison is proposed in Tab. 5 and Tab. 6. The first table summarizes the works in literature regarding CRs with $I_{REF} \in [7.5 - 100]$ nA, while the second one shows the solutions with $I_{REF} \in [100 - 1000]$ nA. In both tables the best parameters are highlighted in cyan, while the worst ones are reported in red. It is possible to observe that the proposed CR presents the most scaled technology and the lowest TC, in particular in the restricted temperature range [10-90] °C. Indeed, the proposed solution shows a TC 1.58X lower than the minimum in Tab. 5 and 4.6X lower than the minimum in Tab. 6. The Figure-of-Merit

$$FOM = \frac{TC}{\text{T. Range}} \cdot \frac{I_{DD}}{I_{REF}} \quad (ppm/°C^2) \tag{18}$$

proposed in [31] is also included in Tab. 5 and Tab. 6 which takes into account the TC and the temperature range, but also the ratio I_{DD}/I_{REF}, where I_{DD} is the overall static current consumption of the CR. The proposed CR shows the lowest FOM (1.2X lower than the best one in the state-of-the-art comparison tables), while maintaining one of the lowest area occupation. Note, however, that the temperature range of the proposed CR it is not the widest one, since it was designed to be used in IMD or in IoT wearable nodes, where the usual temperature is in the range of [0-100] °C (or [10-90] °C). For these properties, it is seen from that the proposed solution is

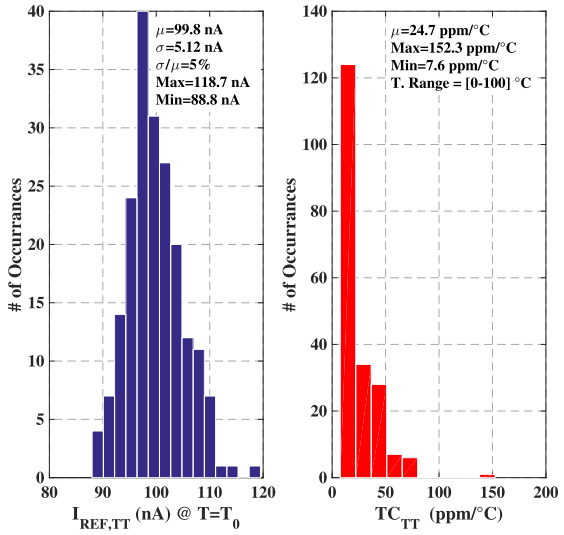

FIGURE 17. Monte Carlo simulations for the proposed CR (200 iterations and 15 bins) On the left the reference current, on the right the temperature coefficient.

the best trade-off in terms of area and TC and area and FOM as can be appreciated from Fig. 18.[1]

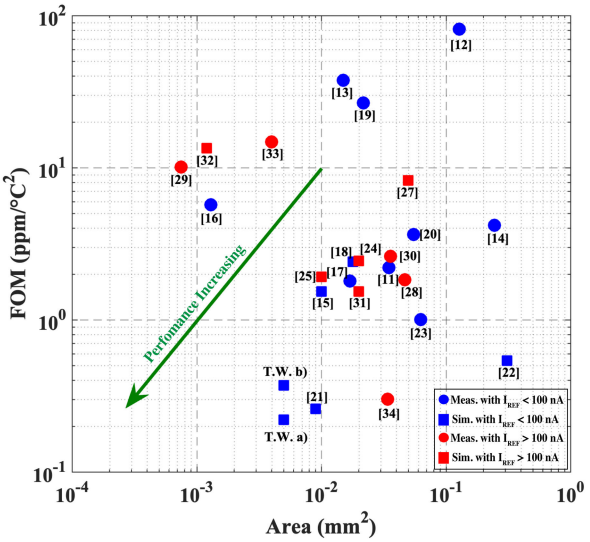

FIGURE 18. FOM vs. Area comparison of the solutions reported in both Tab. 5 and Tab. 6.

VI. CONCLUSION

A novel current reference has been introduced in this work. The reference current is generated exploiting the voltage difference of the threshold voltage of MOS transistors operating in weak inversion. Designed in a standard 28-nm CMOS technology, post-layout simulations shows high stability over process, corner and voltage variations thanks to the adoption of an embedded trimming circuit. As highlighted by comparison with the state-of-the-art, the proposed solution is a good candidate for area- and power-constrained applications, such as IoT sensor nodes and IMDs.

As compared to other solutions exploiting the same principle of operation, the main innovations of the proposed circuit and the contribution of the work can be summarized as follows:

1) the same kind of transistor is exploited in the CR and the adopted technology is the most scaled compared to previous works;
2) the adoption of an OTA in the reference core increases the performance in terms of line sensitivity;
3) a theoretical analysis of the line sensitivity is carried out providing design guidelines to increase the performance;
4) an active trimming circuit is introduced, for the first time in the literature, to simultaneously reduce the effects of process variations on the nominal reference current and the temperature variations leading to a very low TC within the five process corners.

[1] It was excluded [26] since it was not declared the area occupation of the proposed circuit.

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ANDREA BALLO (Member, IEEE) was born in Catania, Italy, in 1990. He received the Laurea *(summa cum laude)* and Ph.D. degrees in electronic engineering from the University of Catania, Catania, in 2016 and 2020, respectively. Since 2021, he has been a Research Fellow and an Adjunct Professor of electronic devices at the University of Catania. His current research interests include low-voltage low-power analog circuit design and analog and mixed electronics for energy harvesting applications. He is a Member of the Editorial Board of *Journal of Electronics and Electrical Engineering* (JEEE) (UWP) and a member of the topical advisory panel of different journals of MDPI, like *Applied Sciences and Electronics*.

ALFIO DARIO GRASSO (Senior Member, IEEE) was born in Catania, Italy, in 1978. He received the Laurea *(summa cum laude)* and Ph.D. degrees in electronic engineering from the University of Catania, Catania, in 2003 and 2006, respectively. From 2006 to 2011, he worked as a Freelance Engineer in the field of electronic systems. From 2009 to 2010, he was an Adjunct Professor of electronics at the Kore University of Enna, Italy. In 2011, he became a Researcher (Assistant Professor) and in 2015, he was appointed as an Associate Professor at the University of Catania. He teaches graduate courses on advanced VLSI digital design, microelectronics and basic electronics. He has coauthored more than 100 papers on refereed international journals and conference proceedings. His current research interests include low-voltage low-power analog circuit design and analog and mixed signal processing for energy harvesting applications. In 2017, he received the Italian National Scientific Qualification for the position of a Full Professor. He is an Associate Editor of *IET Electronics Letters*, *International Journal of Circuits Theory and Applications* (Wiley), and *Journal of Circuits, Systems and Computers*, and is a Member of the Editorial Board of *Sensors* (MDPI).

MARCO PRIVITERA (Member, IEEE) was born in Piazza Armerina, Italy, in 1997. He received the bachelor's and master's degrees *(summa cum laude)* in electronic engineering from the University of Catania, Italy, in 2019 and 2021, respectively, where he is currently pursuing the Ph.D. degree in electronic engineering with the University of Catania. His current research interests include power management integrated circuits, data communication sub-systems, and ultra-low power analog blocks for energy harvesting applications.

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