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RESEARCH ARTICLE

Design, Implementation, and Deployment of Modular Battery Management System for IIoT-Based Applications

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ABSTRACT This paper proposes design and implementation of a battery management system (BMS) for the industrial internet of things (IIoT) enabled applications. The hardware and software development of this BMS is briefly presented in this paper. In terms of hardware development, the presented BMS have modular topology and has 1) high fault tolerance and 2) has exceptionally flexible deployment owing to its topology having multiple local management units (LMUs) connected to a central management unit (CMU). This hardware design approach aims to address the overall design efficiency and cost trade-off of BMS deployment. The hardware design efficiency is tested using actual deployment. In terms of fault tolerance using 1 – 3 LMUs at fault, the voltage monitoring accuracy is maintained for each LMUs. An average of 0.00017 V, 0.0008 V and 0.001 V voltage difference is yielded for 1, 2, and 3 modules at fault respectively. Additionally, core BMS sub-circuit is tested to verify hardware design efficiency such as the DC-to-DC converter which yielded 92.74%. Furthermore, the CMU is integrated with a wireless communication circuit that enables IIoT-based applications such as the emerging edge-based, and a plethora of intelligent deployment. In terms of software, the presented BMS aims to realize state-of-the-art processing through IIoT based approach. For software testing and verification, the BMS is deployed to an unmanned ground vehicle (UGV). The signal stability is tested for UGV based application at a 3500s deployment time whereas an average of 0.0010V voltage difference is yielded. This is verified using time markers which is further analyzed using software-based signal processing and acquisition simulation. Concisely, the proposed BMS aims to converge IIoT applications to its actual deployment. The proposed BMS is designed, implemented, and successfully deployed to test its viability both in the simulation platform and actual deployment.

INDEX TERMS Battery management system, edge processing, industrial IoT, lithium-ion, modular architecture.

I. INTRODUCTION

The demand for battery management systems (BMSs) is forecasted to have a compound annual growth rate of 10% from 2021 to 2026, as reported in 2020. This is in line with the estimated global demand for batteries, specifically lithium-ion batteries. The rapidly increasing battery utilization and innovation play a key role toward a better economic and environmental future [1], [2]. It is estimated that between 2020 and 2030, the global demand for batteries, specifically lithium-ion batteries, will increase elevenfold from 185 GWh to 2,000 GWh. This global demand corresponds to 91.9 billion US dollars of market growth projected for 2030 from 40.5 billion dollars in 2020. The majority of this demand will be from the transportation sector, which, as of 2021, is worth 725 billion USD. It is estimated that 8 out of 10 cars

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TABLE 1. BMS topologies and design approach.

Reference	Topology	Balancing	Fault Tolerance	Wireless Communication Capability	Edge AI Capability
[9]	Centralized	Active	No	No	No
[10]	Centralized	Passive	No	No	No
[11]	Centralized	Passive	No	No	No
[12]	Centralized	Active	Yes	No	No
[13]	Centralized	Passive	No	No	No
[14]	Centralized	Passive	No	No	No
[15]	Centralized	Passive	No	No	No
[16]	Centralized	Passive	No	Yes	No
[17]	Distributed	Active	Yes	No	No
[18]	Distributed	Active	No	No	No
[19]	Distributed	Active	Yes	No	No
[20]	Distributed	Active	Yes	Yes	No
[21]	Modular	Active	No	No	No
[22]	Modular	Active	No	No	No
[23]	Modular	Passive	No	No	No
Proposed [8]	**Modular**	**Passive**	**Yes**	**Yes**	**Yes**

in the market would be electric vehicles (EVs) by 2050. The growth of the electric transportation sector [3] and this increasing demand gear toward the development of industrial Internet-of-Things (IIoT)-based vehicles known as Internet-of-Vehicles (IoV) [4]. The European Patent Office (EPO) and International Energy Agency (IEA) have emphasized that aside from mitigating the effects of climate change, batteries are a source of renewable energy. This rapidly growing global battery market is a sustainable way to recover the economy, which was impacted as a result of the COVID-19 crisis. In line with this, the World Health Organization (WHO) considers extended batteries as an innovative key technology for saving lives in connection with the pandemic. Additionally, with the inevitable global economic recession due to the COVID-19 pandemic, batteries will play a major role in the green energy and renewables sector, which is projected to have one of the highest investments returns in the future owing to the rapid shift in renewable energy resources and energy conservation in both commercial and industrial applications. This proves the research relevance and consequently highlights the urgency for the rapid development of BMSs, considering that battery life efficiency is directly proportional to the efficiency of its management system.

A. RELATED WORK

The majority of existing BMSs are designed for lithium-ion batteries (LIBs), also known as Li-ion batteries, because of their notable merits, such as high energy density and power with comparatively long-life spans [5], [6], [7]. However, LIBs have performance inconsistencies, which lead to performance instability caused by the extrinsic and intrinsic factors of the LIB. These factors result in an early aging effect or cell degradation. All BMSs aim to monitor, control, and protect cells in a pack for efficient, state-of-the-art, and safe applications, as highlighted in our previous paper [8]. There are three topologies for conventional BMS: 1) centralized, 2) distributed, and 3) modular; these topologies can be used in combination as hybrid topology. Currently, the majority of conventional BMSs utilize centralized topology because, it is the most economical though also, least expandable and requires numerous wiring connections [9], [10], [11], [12], [13], [14], [15], [16]. Distributed BMS [17], [18], [19], [20], however, is considered to be the most expensive; it is expandable and requires the least number of wiring connections. The modular topology compromises both the centralized and distributed topologies. This is because modular topology enables controller-to-controller communication among all local management modules and central management modules [21], [22], [23]. A hybrid topology is any combination of these three topologies for a specific application. Table 1 lists the related works on BMS with their corresponding topologies. It can be observed that all the topologies have various balancing approaches and design considerations. The design approaches vary on the basis of the target application.

The rapidly increasing demand for the BMS is constrained by the trade-off between the design cost and its functionality. It is a well-known problem in this field, particularly for EV applications, which mostly uses LIBs. However, an optimized structure design can minimize the cost and operational losses of a BMS [24]. Many researchers have focused on improving the existing BMSs when considering their overall cost [11], [20], [25], [26], [27], [28]. While the average price of a BMS ranges from 300 USD to 10,000 USD, the price itself is directly proportional to the application, such as the nominal voltage of the battery stack.

Conventional BMS has the economic advantage of extending the battery life, thereby increasing the overall accuracy of the BMS, and lowering its design and implementation cost. BMS performs various key functions in batteries, such as monitoring, protection, charging/discharging management, communication, diagnosis, and data management [29]. These conventional functions are widely applied in current BMS

design approaches; however, the majority of the existing BMSs do not consider the hardware required for software implementation of intelligent applications. In [30], an adaptive switching algorithm deployed to an energy management system (EMS) is highlighted, which makes the EMS intelligent. In [31], an intelligent BMS was proposed, wherein intelligent control was used. Another logical approach for energy management in battery applications is the use of fuzzy logic [32]. This paper also presents an intelligent software approach. In [33], a predictive intelligent BMS was proposed for accurate and state-of-the-art state-of-charge (SoC) estimation. In [34], authors proposed an intelligent BMS which could transmit data through the Internet in coordination with the algorithm. This approach is communication dependent for its application efficiency and reliability. In summary, there are various studies that aim to make conventional BMS intelligent for reliable and state-of-the-art applications. However, the majority of the existing studies mainly focus on the optimized software algorithm to enhance the current BMS by deploying intelligent algorithms to demonstration and evaluation boards. Despite these developments to improve the efficiency and deployment capability of existing BMS, there is still a research gap in addressing issues such as its 1) flexible deployment, 2) fault tolerance, and 3) intelligent and 4) state-of-the-art BMS deployment.

B. MOTIVATION AND CONTRIBUTION

The trend of using the modular BMS topology is gaining attention because of its advantages such as deployment flexibility and scalability [21], [22], [23]. Using modular BMS topology enhances the performance efficiency of battery-based applications because of its flexibility and scalability whereas it can be reconfigured to meet the system demand and can be easily modified to address evolving deployment requirements. In battery-based applications, deployment flexibility, efficiency, and maintenance, fault tolerance is already a crucial concern. Furthermore, integrating a BMS for intelligent and state-of-the-art deployment is another crucial factor to consider to address the technological advancement; especially in this industry 4.0 era which is lacking [9], [10], [11], [12], [13], [14], [15], [16], [17], [18], [19], [20], [21], [22], [23].

Driven by the preceding study and as the BMS deployment advances towards state-of-the-art deployment, we proposed a design, implementation, and deployment of Modular BMS for IIoT-based applications. The following are the principal contributions of this paper:

- Design of a modular BMS which realizes a fault-tolerant deployment via the isolation channel designed for the CMU to LMU communication.
- A modular BMS capable of intelligent and state-of-the-art deployment.
- Detailed hardware and software design analysis which includes design standards, considerations, and actual application parameters.
- Actual implementation and deployment for the proposed modular BMS which includes performance metrics, i.e., deployment flexibility and fault tolerance, voltage, current, temperature monitoring accuracy for local processing and IIoT-based processing.

IIoT-based BMS deployment is the motivation of this paper. This approach is the design advancement of the circuit design approach we presented in [8].

II. PROPOSED MODULAR BMS

An overview of the proposed methodology to achieve the proposed modular BMS is presented in Fig. 1. The actual developed modular BMS prototype is presented in Fig. 1(a). The software part is used for the deployment of the algorithm to the proposed BMS hardware for actual deployment. The software part and actual implementation testing is presented in Fig. 1(b); it is composed of: 1) algorithm deployment, 2) BMS software platform and 3) real-time results validation which adheres to the BMS hardware and software development. The hardware section highlights actual deployment which is also presented in Fig. 1(c) includes the 1) modular BMS application for the design approach, 2) battery pack rating and battery type, and 3) hardware testing, all of which are for the actual circuit design of the modular BMS. The implementation of the battery packs for the deployment of BMS is the common node for Fig. 1(a), Fig. 1(b) and Fig 1(c). The proposed modular BMS is designed for up to four local management units (LMUs) connected to a central management unit (CMU). The LMU independently monitors, controls and protect all the lithium-ion cells in each module. The CMU is the common node for all LMUs; it receives data for monitoring, control, and protection of the whole LIB pack. The CMU also have the battery current measurement IC.

Fig. 2 shows an overview of the proposed modular BMS. This BMS is capable of local processing and wireless real-time data processing and acquisition which realizes intelligent and state-of-the-art deployment. Furthermore, The proposed modular BMS enables the application of a cloud-computing platform through an integrated wireless communication module. The communication module paves the way for a plethora of intelligent applications for the designed modular BMS. The proposed modular BMS is also designed to withstand faulty modules through module isolation, thus realizing a fault-tolerant system that is adaptive to faulty situations. Overall, the designed modular BMS realizes a framework for a fault tolerant deployment with convergence to intelligent and state-of-the-art applications; which is the core focus of this BMS prototype version. In cases of faulty and degraded or depleted battery cells, it would result to a degraded battery pack which BMS aims to address in advance. The degraded battery cells can be monitored and detected by each of the LMUs connected to the CMU. This monitoring can help reduce further damage to the battery pack through the protection algorithm. As for the balancing, this would end the balancing cycle and would trigger the signal to activate the protection algorithm for each LMUs independently.

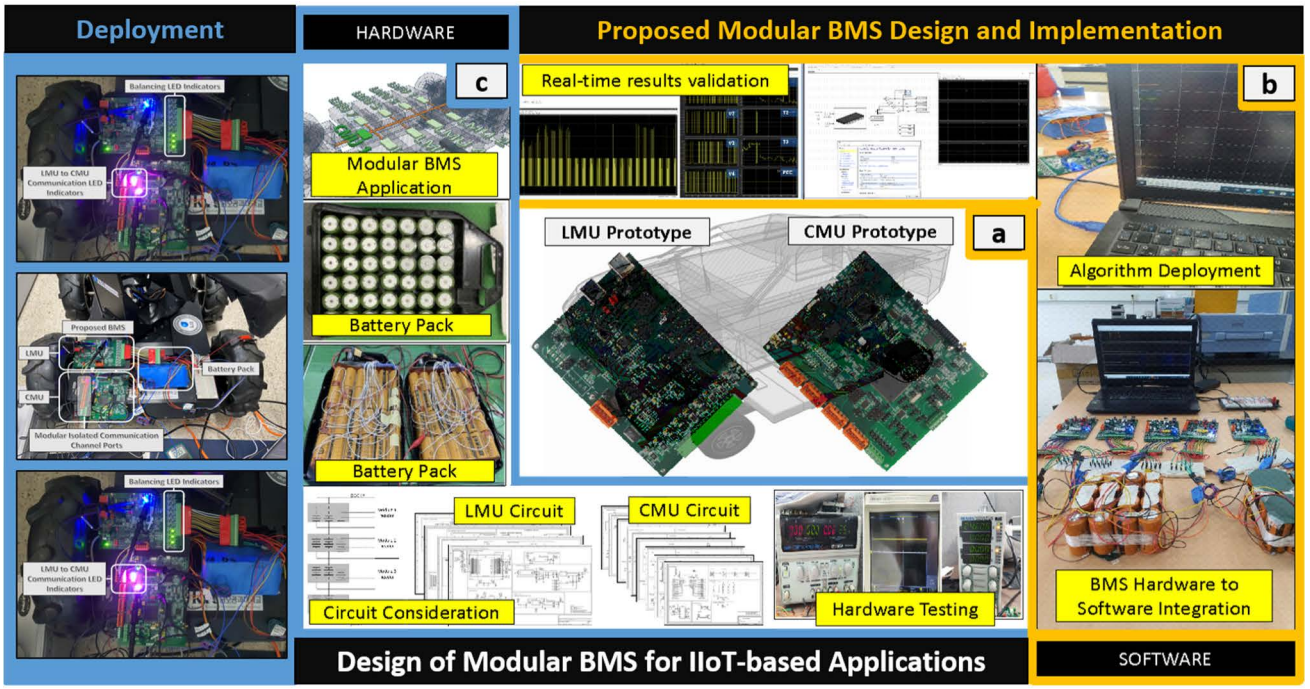

FIGURE 1. Overview of the proposed methodology modular BMS (a) actual LMU and CMU prototype design, (b) implementation testing (c) deployment.

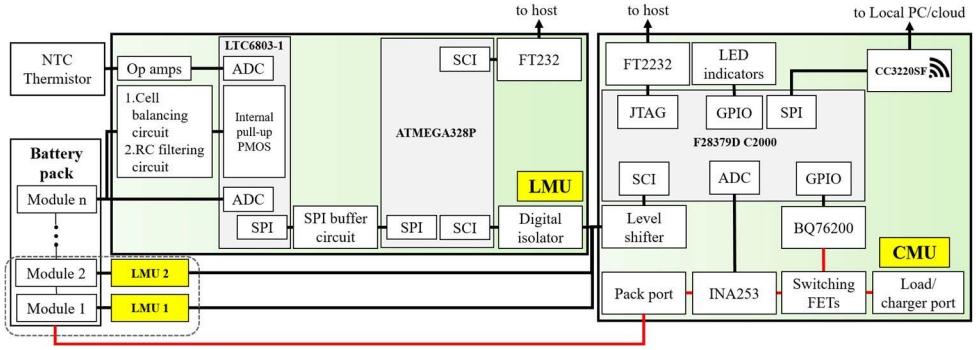

FIGURE 2. Overview of the proposed modular BMS structure.

A. HARDWARE DESIGN CONSIDERATION

The design of the modular BMS hardware is based on simulation, theoretical, and prototype analysis. In this section, the principle theoretical analysis of the proposed BMS is briefly discussed. The development of the hardware adheres to the specifications of the designated BMS application, such as deployment application. Battery is one of the core aspects of BMS deployment, and theoretical analysis is the first step in the design.

An equivalent circuit model (ECM) to analyze the dynamic behavior of the battery pack integrated into the hardware is shown in Fig. 3, which is the battery cell equivalent circuit model.

Fig. 3. shows the ECM used for the battery cell which is crucial for the BMS design. The ECM is divided into

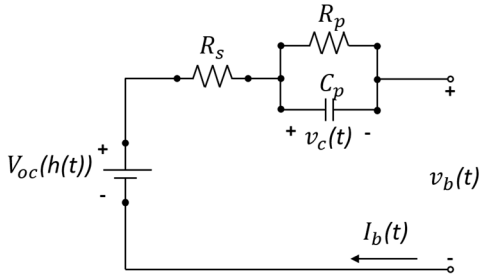

FIGURE 3. Overview of the proposed modular BMS structure.

three parts consisting of passive components: 1) the equivalent internal resistance in ohms (Ω), represented by R_s, 2) the parallel resistor-capacitor (RC) circuit $C_p//R_p$, where

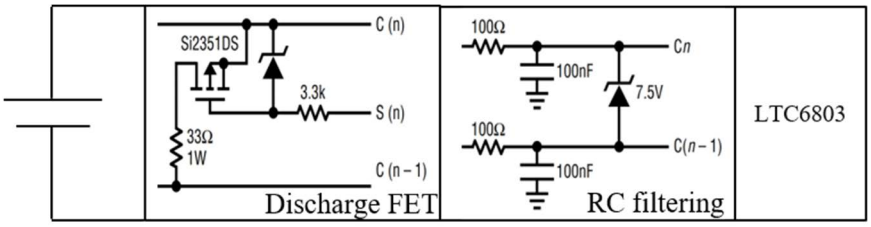

FIGURE 4. Proposed BMS voltage monitoring circuit.

R_p represents the polarization equivalent resistance and C_p represents the polarization equivalent capacitance; this RC circuit is used for the simulation of transient response of the battery cells during charging or discharging; and 3) the open-circuit voltage (OCV), $V_{oc}(h(t))$, is a nonlinear function of SoC$h(t)$. The threshold value of R_s can be calculated using ohms law. The calculation in terms of ohms law is with respect to the load voltage (V_L) and the load resistance (R_L) value. The nominal value of the reference current (I_{ref}) is calculated using V_L and R_L. Going further, I_{ref} is used to calculate the voltage across the internal resistor. The OCV and the V_L is then used to derive the voltage across the internal resistor (V_{ir}). The value of the OCV is the summation of V_L and the V_{ir}. Finally, the R_s of the battery cell is calculated by dividing the V_{ir} and the I_{ref}. For the R_s threshold value, the implementation and hardware design considered varies from 120 mΩ to 320 mΩ which is dependent on the operating parameters which includes V_L, R_L, I_{ref} and V_{ir}. This value is considered for each lithium-ion battery cell. The equivalent circuit model (ECM) considers current as the control input and the measured terminal voltage as the output.

$$V_{oc}(h\,(t)) = V_b(t) - I_b\,(t)\,R_s \tag{1}$$

Based on Fig. 3, the transient and steady state behavior of a battery cell is simulated. In Eq. (1), V_{oc} is the input voltage of the battery in volts (V), V_b is the output voltage of the battery in volts (V), $I_b\,(t)$ is the internal dynamic current of the battery in amperes (A) and R_s is the dynamic ohmic resistance in ohms (Ω). This analysis enabled the design consideration and theoretical analysis of the circuit for both hardware and software development.

■ **Local Management Unit (LMU)** – In this section, the development and theoretical discussion of the LMU module is briefly discussed.

The voltage-monitoring-circuit block diagram of the LMU is shown in Fig. 4. A set of two different circuits, specifically, a discharge field-effect transistor (FET) circuit and an RC filtering circuit are directly connected to the cells of the module of the battery pack. The discharge FET discharges the cells with a higher voltage compared with other cells. The discharge FET is integrated with a high-impedance discrete p-type metal-oxide semiconductor field-effect transistor (P-MOSFET) device with a discharge resistor. The RC filtering, filters out transient voltages and unwanted signal distortions, which leads to reduced error in the analog to digital conversion process. In this circuit design for the RC filtering circuit, a 16 kHz RC filtering is the optimal design consideration for the current BMS design approach, which consists of a 100 Ω resistance and a 0.1 μF capacitance. The integrated resistance is 100 Ω, adhering to the overall operating temperature of the BMS and its overall operational power loss due to impedance and heat dissipation. This complete battery monitoring integrated circuit (IC) of the proposed modular BMS implements a sampling system for the execution of analog to digital conversion. An average 0.5 ms conversion window is yielded, provided that all signals are distinguishable, adhering to the sigma-delta modulator rate of 512 kHz. An internal 8 parts-per-million per degree Celsius (ppm/°C) voltage reference combined with the analog to digital converter (ADC) gives LTC6803 its outstanding measurement accuracy. LTC6803 is the battery monitoring IC of LMUs. The sigma-delta ADC in this design outputs a 12-bit code with an offset of 0×200 (512 in decimal system). The input voltage is expressed in Eq. (2) as

$$V_{INPUT} = (D_{OUT} - -512) \times V_{LSB}. \tag{2}$$

DOUT is the digital output with a decimal integer value. VLSB is the least significant bit voltage of 1.5 mV. The RC filtering circuit is composed of a series resistor and a shunt capacitor with 30 dB attenuation.

The RC filtering circuit design considerations led to the use of the Si2351DS cell balancing MOSFET. The Si2351DS cell balancing MOSFET or the discharge FET has a small transient during the switch-on-and-off condition, which is the basis for the RC filter circuit design, which is optimal for this specific application. Setting the cut-off frequency of these RC filters reasonably high permits adequate settling before analog-to-digital conversion. The ADC timing delay is 0.5 ms; thus, a 16 kHz RC filter is optimal.

In terms of the RC filter power loss, heat dissipation is the key metric to be considered for the RC filter circuit. The maximum power loss of the RC filtering is limited by the heat that the battery monitoring IC LTC6803 can withstand. The 100 Ω resistor used in this design has an operating temperature of −55 to 155 °C, which adheres to the maximum overall operating temperature of the LTC6803, which is 125 °C. This 100 Ω resistor was specifically chosen for this application.

The balancing approach used for this BMS circuit is passive balancing. Passive balancing is cost-efficient compared to active balancing. This cost is inline with the components

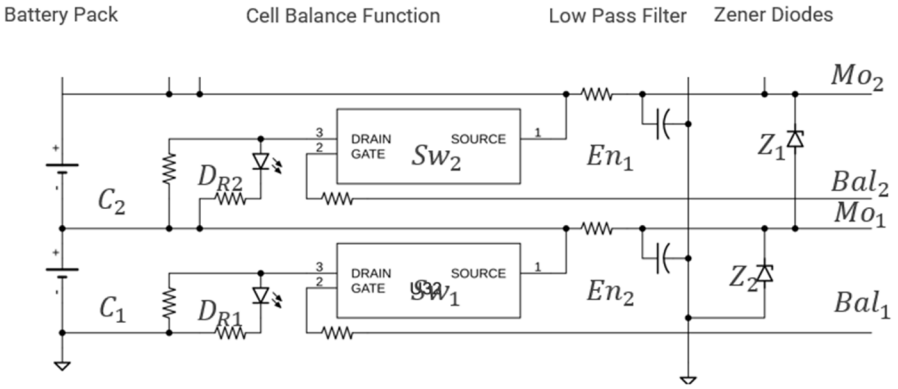

FIGURE 5. Theoretical analysis for the passive balancing circuit of the proposed modular BMS.

needed to realize an active cell balancing approach whereas passive balancing requires only a filter circuit and a bleeder also known as discharge resistor to actuate cell balancing as highlighted in [8]. The proposed approach in [8] which is the extension of this paper proves that passive balancing has high implementation viability and have high balancing implementation accuracy. Moreover, it can correct the long-term discrepancy of self-discharge current on a cell-to-cell basis. Fig. 5 shows the actual theoretical circuit analysis for passive balancing of the designed BMS. Cell 1 (C_1) can be discharged through resistor D_{R1} and switch 1 (Sw_1). Cell 2 (C_2) can be discharged through resistor D_{R2} and switch (Sw_2), and so on. Should the cell-voltage measurements determine that a cell is in need of being discharged, each cell has a corresponding discharge resistor $D_{R1}, D_{R2} \ldots, D_{RN}$. Switches Sw_1, Sw_2...are implemented using a transistor, specifically an N-type MOSFET, but they could also be implemented using other types of MOSFETs, bipolar or other types of transistors, a relay, a mechanical switch, or other type of switch. Control voltages, illustrated as Enable 1–2 (En_1, En_2 ...) signals, for the N type MOSFET switches should have appropriate levels to turn the switches on and off. Control signals for other types of switches are readily devised. The charge equalization currents could be of the same order of magnitude. In this balancing approach, heat is generated. The power dissipated as heat is expressed in Eq. (3) as follows:

$$\mathrm{p} \approx V_{NOM} \times I_{balance}. \tag{3}$$

where V_{NOM} is the nominal voltage and $I_{balance}$ is the balancing current. For fast dissipative balancing, more heat is generated than for slower balancing. This generally imposes a high-wattage requirement on the balancing resistors. This high-wattage requirement is the design consideration on the approach used for the discharge FET of this proposed modular BMS. A 33 Ω, 1 W bleeder resistor is used for the passive balancing circuit as highlighted in Figure 4 discharge FET figure. This bleeder resistor value considers the parameter of the connected battery cell which have a minimum, nominal and maximum voltage range of +3.2V, +3.6V and +4.2V respectively. The bleeder resistor is used to limit the power dissipated to the normal operating voltage of the LTC6803. The specific resistor integrated in the proposed modular BMS can handle up to –40°C to + 125°C which directly adheres to the temperature parameters of the passive balancing circuit IC (LTC6803). The bleeder resistor limits the power dissipated by the Si2351DS MOSFETs with respect to the connected UC cells and the pre-defined threshold voltage. The MOSFETS connected to the bleeder resistor is also dependent on the heat tolerance of the LTC6803 which is –40°C to + 125°C. With this configuration of addressing the passive balancing circuit heat tolerance, fast and slower balancing such as 20 mV can be accommodated by the proposed BMS passive balancing circuit. Concisely, the passive cell balancing threshold, regardless of its iteration and value is limited by the operating temperature of the discharge FET. The 20 mV is the used cased scenario for the implementation in this paper.

The heat generated by balancing can be similar to that generated by normal cell operation. Therefore, dissipative balancing may increase the cooling requirements for the battery-pack thermal-management system, which is a significant expense. A Zener diode is placed in parallel to the measuring resistor to protect the following measurement circuits against overvoltage. Because the voltage divider is designed to be highly resistive to keep the losses low, the voltage tap of the measuring resistor should have a significantly high resistance so as not to load the voltage divider. For this reason, an impedance converter that is followed by the filter circuit and the ADC should be used to tap the voltage. Fig. 3 and Eq. (1) enabled the theoretical analysis calculation for the circuit simulations.

In addition to the voltage of the cells in the module, the battery monitoring IC also measures the module temperature using a 12-bit delta-sigma ADC. The ADC outputs a digital (decimal) value of the measured analog temperature and stores it in the temperature register group as a digital (binary) value. The battery-monitoring IC has two temperature channels for the circuit design approach. Both the channels can

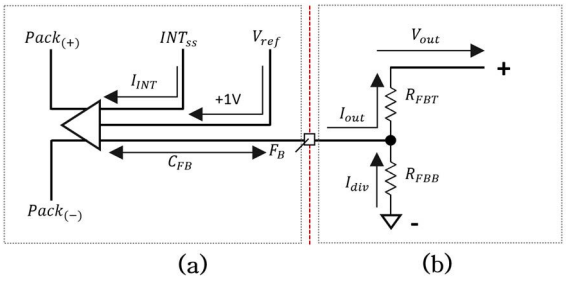

FIGURE 6. Proposed BMS LMU DC-DC converter circuit design approach (a) internal circuit (b) external circuit.

measure the temperature at one point of the battery module. The digital (decimal) is converted to an analog equivalent voltage using Eq. (4).

$$V_{T-a} = ETMPx_{10} \times 1.5mV \tag{4}$$

where V_{T-a} is the analog equivalent voltage of the temperature, and $ETMPx_{10}$ is the digital (decimal) temperature at channel x. The analog voltage equivalent is converted to the analog temperature (°C) using Eq. (5).

$$(\mathrm{C}^{\circ}) = \frac{298.15 \times 3988}{-298.15\, ln\, ln\left(\frac{3.0585}{V_{T-a}} - 1\right) + 3988} - 273.15 \tag{5}$$

The LMU monitoring, balancing, and losses, such as the heat dissipation of the LMU module are considered in the proposed BMS circuit design and development. To maintain the overall efficiency and accuracy of the BMS, another pivotal sub-circuit is the integrated DC-to-DC buck converter. The design considerations include the losses, actual implementation, and deployment. The proposed DC-to-DC converter (buck; step-down) is presented in Fig. 6, which is directly connected to the battery pack positive ($Pack_{(+)}$) and negative ($Pack_{(-)}$) terminals. Fig. 6(a) and Fig. 6(b) depict the internal and external circuits of the DC-to-DC converter. The efficiency of the DC-to-DC converter is directly proportional to the efficiency and losses of the battery pack, which makes it a sub-circuit of the proposed BMS circuit design approach. Another factor that makes this sub-circuit pivotal is that it is a power source for the BMS system that enables an independent supply of power when connected to a battery pack.

The DC-to-DC converter integrated into the LMU module has a +1 V voltage reference (V_{ref}), which is used as a reference to precisely regulate the output voltage considering the operating temperature range, such as the losses similar to the concept of Eq. (3). The output voltage (V_{out}) is regulated by a resistor divider circuit toward the bidirectional feedback (F_B) pin of the DC-to-DC converter. In the resistor divider circuit, the tolerance of the resistor is 1%, and it has a minimal temperature coefficient. The lower resistance value of the divider circuit is R_{FBB}, which represents the lower-side resistor. The divider current adheres to the value of R_{FBB}. After calculating the divider current (I_{div}) value for the DC-to-DC converter application, the value of the top-side resistor, denoted as R_{FBT}, for circuit design application is computed using Eq. (6).

$$R_{FBT} = \frac{V_{out} - V_{ref}}{V_{ref}} \times R_{FBB}. \tag{6}$$

For this application, as shown in Fig. 7, the value of R_{FBB} and R_{FBT} were 22.1 kΩ and 88.7 kΩ, respectively, which adheres to the specific recommended value of R_{FBT} in an efficient range of 10–100 kΩ. A lower value of R_{FBT} reduces the overall efficiency of the DC-to-DC converter under a light load (high output resistance; low current). However, under a heavy load (low output resistance and high current), a higher value of R_{FBT} leads to a minimal static current, which is also an optimized factor to be considered when light-load efficiency is critical. Although this is the case, a higher value of R_{FBT} ($R_{FBT} \geq 1\,M\Omega$) leads to a noisy feedback signal. Overall, the tolerance and temperature variation of the applied resistor in the divider circuit directly affect the output voltage regulation of the external DC-to-DC converter of the LMU module.

The internal logic circuit of the DC-to-DC converter utilizes an internal soft start (INT_{ss}) approach, where the amount of voltage and current passing towards the converter is regulated, such as the internal soft start current (I_{INT}) itself. This is a protection approach for the LMU-module circuit. This protection approach of the DC-to-DC converter is the core protection circuit for the LMU module with respect to its direct connection to the battery pack.

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Fig. 7 shows the actual-LMU DC-to-DC converter, which incorporates a peak and valley inductor current limitation as a means of protection. The DC-to-DC converter design approach protects the LMU from overloading and short circuits and limits the maximum output current (I_{out}), as shown in Fig. 6b. The formula for overcurrent protection and short-circuits protection for the LMU is shown in Eq. (7):

$$I_{out|max} = \frac{I_{LSLIM} + I_{HSMAX}}{2} \tag{7}$$

where $I_{out|max}$ is the maximum current threshold with respect to the valley (I_{LSLIM}) and peak (I_{HSMAX}) currents of the DC-to-DC converter. I_{LSLIM} is the low-side current limit, while I_{HSMAX} is the high-side maximum (peak) current. The feedback voltage is then calculated with respect to the $I_{out|max}$, and if the yielded voltage value is lower than 40% of the actual V_{ref}, the DC-to-DC converter activates the hiccup mode. The hiccup mode is activated for 256 consecutive cycles via the trigger switch of the I_{LSLIM}. This shuts the converter down for a period of hiccup time (T_{HICCUP}). In the cases where overcurrent and short-circuit faults are still

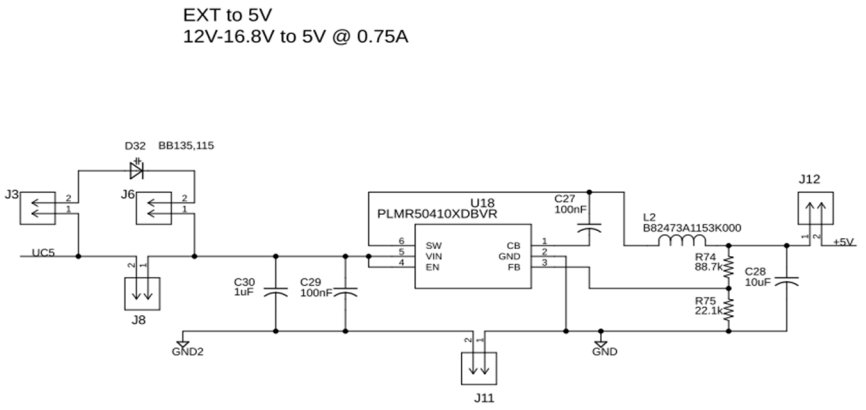

FIGURE 7. Actual LMU DC-DC converter circuit design.

evident in the LMU system, T_{HICCUP} simultaneously occurs until the fault condition is not evident on the DC-to-DC converter circuit. Hiccup have the advantage of reducing losses through power dissipation in faulty conditions, whereas the overall accumulated heat of the LMU is managed which leads its deployment safety.

■ **Central Management Unit (CMU)** – The central management unit acquires and processes the data from the connected LMU. In this section, a brief hardware design for IIoT-based development and consideration is highlighted, which paved the way for intelligent and state-of-the-art deployment such as for IIoT capable BMS. The overall battery pack monitoring is performed by the CMU. It includes: 1) pack voltage monitoring, and 2) pack current measurement. In the hardware discussion of this paper, presented in section II overview, the CMU consists of battery current measurement IC and central MCU. The battery-pack voltage is monitored by summing all the module voltages from the LMU. The battery-pack current is measured using the battery current measurement IC. The current measurement IC converts the current to an equivalent voltage reading. The voltage reading is sent to the CMU by directly connecting the voltage output from the current measurement IC to the 12-bit ADC of the central MCU. Two steps are necessary to obtain the actual current measurement: 1) convert digital to analog equivalent voltage, 2) convert analog equivalent voltage to current value. The digital equivalent voltage is converter to its equivalent analog value using Eq. (8).

$$V_a = \frac{V_{ref}}{2^n - 1} V_d \tag{8}$$

where V_a is the equivalent analog voltage; V_d is the equivalent digital voltage; V_{ref} is the reference voltage, which is equal to 2.5 V; and n is the resolution of the central MCU, which is equal to 12. For example, an equivalent digital voltage of 4259 is converted to its equivalent analog voltage using Eq. (8) as 2.6 V. The analog equivalent voltage is converted to the current value using Eq. (9).

$$I\ (A) = \frac{V_a - 2.5}{100mV} \tag{9}$$

where I(A) is the pack current and V_a is the equivalent analog voltage. The equivalent analog voltage in the above-mentioned example is converted to a pack current value of 1 A using Eq. (9).

Fig. 8 shows the wireless communication channel of the proposed modular BMS. The wireless communication channel is directly connected to the MCU of the CMUs, which is TMS28379D. The wireless communication channel is connected to the CMU via SPI GPIO pins, including CS, SCLK, MOSI, and MISO, for communication. This realizes an edge-efficient and IIoT-based modular BMS.

The antenna has a frequency synthesizer that generated varying output frequencies as diversified values of the reference frequency. X_1 and X_2 represent the crystal oscillators of the wireless communication channel. The equivalent circuit model (ECM) of the crystal oscillators is emphasized, where C_0 is the shunt capacitance, L_M is the motional inductance, R_M is the motional resistance, and C_M is the motional capacitance. These passive components (L_M, R_M, *and* C_M) represent the equivalent impedance of the subjected X_1 and X_2 oscillators at the natural resonant frequency. The parameter for selecting an oscillator tolerance for the wireless communication circuit module is presented in Eq. (10) in ppm units as under:

$$Tol_{total} = Tol_{initial} + Tol_{temp} + Tol_{age} + Tol_{pull}. \tag{10}$$

Tol_{total} is the total tolerance, $Tol_{initial}$ is the production tolerance basis from the technical documentation, Tol_{temp} is the temperature tolerance, Tol_{age} is the component aging effect and Tol_{pull} is the frequency pulling pertaining to the mismatched loading capacitance. The unit of ppm stands for the accuracy of a frequency. Specifically, for this BMS design consideration, ppm stands for the part of a whole number in units of 100 ppm = 0.01% from 1/1000000. For this application, the wireless communication channel circuit integrated

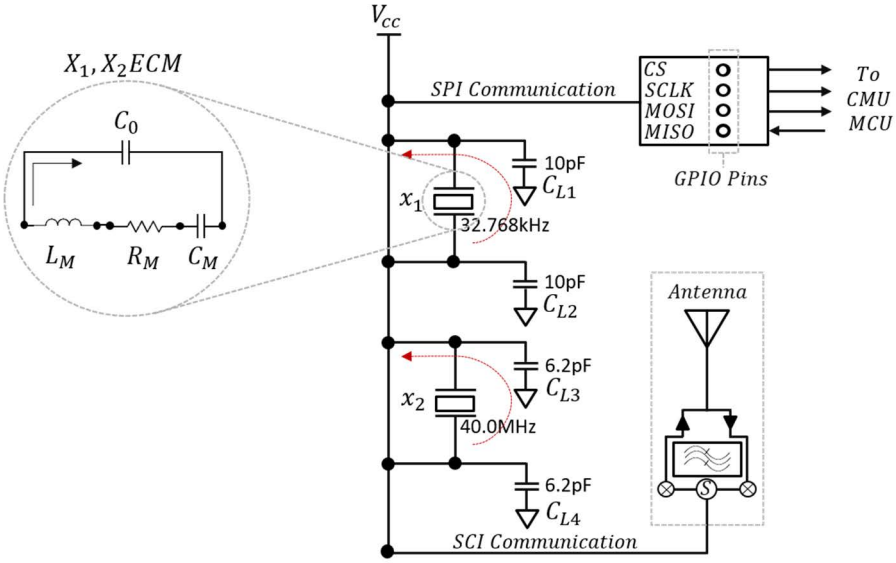

FIGURE 8. Actual communication channel circuit design.

to the BMS utilizes a crystal oscillator with a corresponding value of 32.768 kHz and 40.0 MHz frequency with a specific accuracy of ±150 and ±25 ppm accordingly.

All these theoretical analyses of the wireless communication channels pertain to the crystal oscillator tuning. For this specific application, two clocks are used for the actual operation. The slow clock, which is used as a real-time clock (RTC) with a frequency of 32.768 kHz. A fast clock is used for internal processing and wireless local area network (WLAN) with a frequency of 40 MHz. The standard error for 802.11 b/g requires the error to be in the range of ±25 ppm; if the design does not adhere to this requirement, the BMS wireless communication interface may have access difficulty and interruption owing to multiple access points. The frequency error for the 40 MHz clock should adhere to the standard or minimum at all costs or should be centered at an average frequency error of 0 ppm.

In the realization of this circuit integrated with the proposed modular BMS, $C_{L1} - C_{L4}$ represents the load capacitance, which is the net capacitance of the oscillator feedback loop. This capacitance is pivotal for maintaining the frequency range of the oscillator. For the theoretical analysis and computation of the total load capacitance, Eq. (11) is used.

$$C_L = \frac{C_{L1} \times C_{L2}}{C_{L1} + C_{L2}} + C_{PIN} + C_{STRAY} \tag{11}$$

where C_L is the total load capacitance, $C_{L1}\&C_{L2}$ are discrete load capacitances, C_{PIN} is the capacitance of the device pin, and C_{STRAY} is the stray capacitance of the board. Fig. 8 shows the actual capacitance values used in the feedback loop of the circuit oscillators.

■ **LMU to CMU communication channel** – The communication channel between the LMU and CMU circuit module is designed with a fault-tolerant integration approach. The LMU has a digital isolator, whereas the CMU has level shifters to process input logic signals with varying reference voltages, known as voltage differences.

Fig. 9 shows the actual isolated LMU to CMU communication channel. The highlighted circuit in red shows the common node for this communication channel. This particular communication channel is isolated with respect to the CMU and LMU communication. The isolation keeps the system stable even when one LMU fails. This approach keeps the BMS performance stable despite having faulty modules. On the other hand, the CMU has a communication architecture that allows bidirectional communication without the need for a direction-control signal. This means that the LMU output to the CMU input and LMU input to the CMU output simultaneously communicates throughout the entire processing time. This communication continues even if one of the LMUs fails.

In the direct current (DC) state, the output of the CMU can manage to operate at a high or low state, but this output can vary to allow an external driver to override its data flow when the LMU sends in a return. The circuit logic for this implementation includes two PMOS transistors (represented "P" on the circuit) and two NMOS transistors (represented "N" on the circuit) per channel. The transistors adhere to the monoflap in this circuit, by which it controls the transition speed of the MOSFET. The conditions for this monoflap are as follows. During the low-to-high signal transition, the PMOS transistors are switched on. On the other hand, during high-to-low signal transitions, the NMOS transistors are switched on.

B. SOFTWARE DESIGN CONSIDERATION

The development of the software for this IIoT-based modular BMS hardware design adheres to the theoretical analysis of the hardware design. As shown in Fig. 3, the software

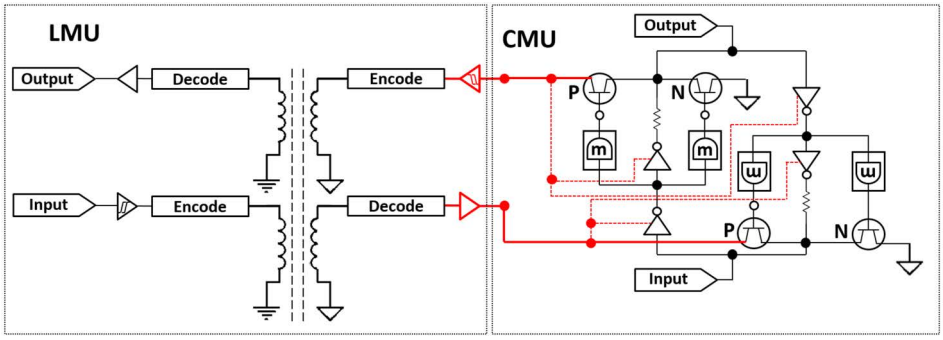

FIGURE 9. LMU to CMU isolated communication channel.

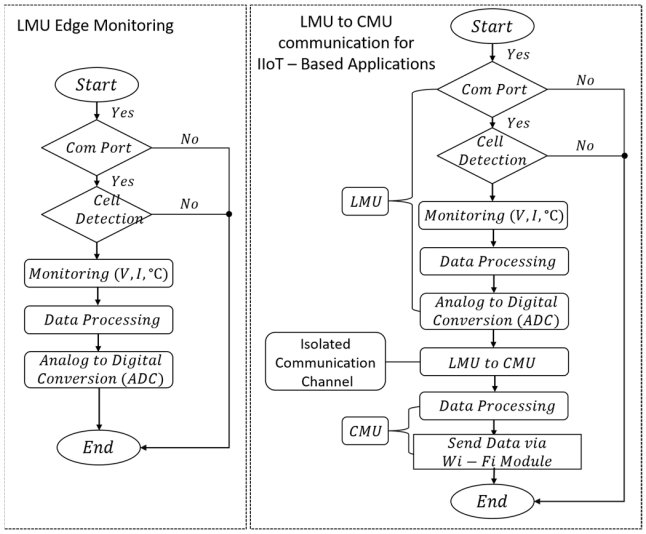

FIGURE 10. LMU to CMU isolated communication channel (a) local processing (b) IIoT – based application processing.

design approach considers the dynamic characteristics of a lithium-ion battery cell in a pack.

■ **Deployed Monitoring Algorithm –** Fig. 10 depicts the monitoring algorithm of the proposed modular BMS. Figure 10(a) shows the LMU monitoring locally paving way for intelligent processing at the edge, whereas the LTC6803 manages the connected battery pack via the uploaded algorithm on the local MCU of the LMU which is the ATMEGA. Figure 10(b) shows the monitoring and data transmission from the local processing in LMU to cloud processing via the CMU module. This realizes the proposed IIoT – based BMS applications. The LMU locally processes the data transmitted to the CMU via the LMU to the CMU isolated communication channel. The CMU wireless communication module allows the wireless data transmission of the locally processed data. The co-processing of data can thus occur locally, at the edge, and with the cloud which in turn facilitates the critical development of the proposed modular BMS for soft real-time and hard real-time applications.

■ **Deployed Balancing Algorithm –** The cell balancing of the BMS adheres to passive cell balancing; it actuates

Algorithm A Cell Balancing

1 Measure all cell voltages V_{cell1}, V_{cell2}, V_{cell3}, *and* V_{cell4}
2 Get minimum voltage,
$V_{min} = min\,(V_{cell1}, V_{cell2}, V_{cell3},\ and\ V_{cell4})$
3 Get difference of each cell voltage with V_{min},
$V_{diff-n} = V_{celln} - V_{min}, n = 1, 2, 3, 4$
4 if $V_{diff-n} > 20$ mV:
5 set *DCCn* to 1
6 Back to 1

through a bleeder resistor that dissipates excess cell charge in the form of heat. The cell balancing algorithm is presented as Algorithm A. First, all cell voltages are measured. Then, the minimum voltage among all the cell voltages is obtained. Subsequently, all the cell voltages are subtracted from this minimum voltage. If the difference between the cell voltage and the minimum voltage is greater than 20 mV, the discharge resistor that cell is connected by setting DCCn bit to 1, where n is the number of cells. The DCC bits are set to zero by default. V_{diff-n} represents the $V_{reference}$ which is the threshold value for the passive balancing circuit actuation.

Fig. 11 shows the summary of the cell balancing for all the cells in a module of the battery pack. This figure summarizes the theoretical analysis of the implemented cell-balancing algorithm. $V_{B(1,2,3,4)} = V_{reference}$ corresponds to the set voltage reference or threshold for the voltage of batteries 1, 2, 3 and 4. PB_{On} corresponds to the passive balancing actuation based on the conditions of each battery cell pertaining to their voltage. If the voltage of $V_{B(1,2,3,4)} \neq V_{reference}$ with the conditions of $V_{B(1,2,3,4)} > V_{reference}$ and $V_{B(1,2,3,4)} < V_{reference}$, the passive balancing actuation is turned on. On the other hand, if $V_{B(1,2,3,4)} = V_{reference}$, the passive balancing achieves its final goal, and the process terminates.

■ **Deployed Protection Algorithm –** The protection algorithm of all the LMUs connected to the CMU is controlled by the central MCU. Fig. 12 shows the overall protection algorithm deployed to the BMS. $V_{BPack} = V_{threshold}$ indicates that the voltage threshold is set with respect to the equivalent voltage of the battery pack. $V_{Monitoring}$ is the voltage monitoring function of the BMS. The monitoring function pertains to the

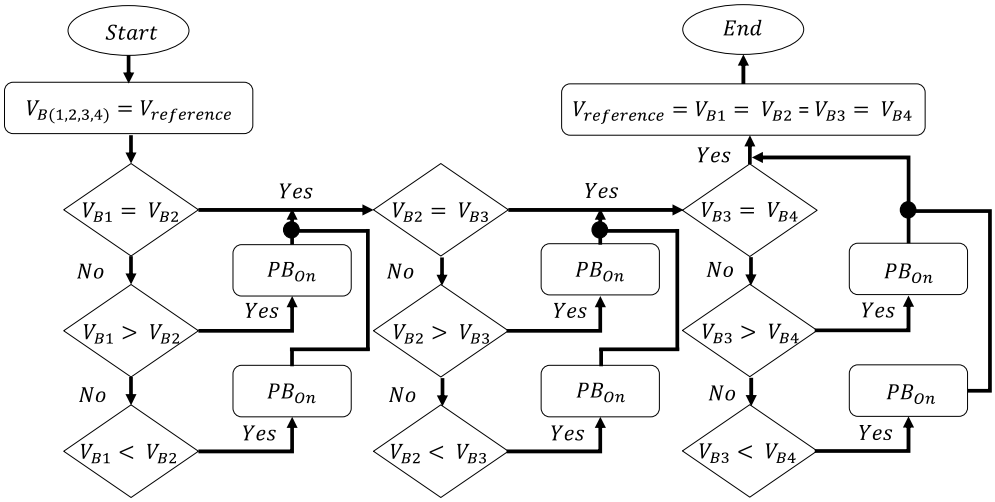

FIGURE 11. Deployed BMS balancing algorithm flowchart.

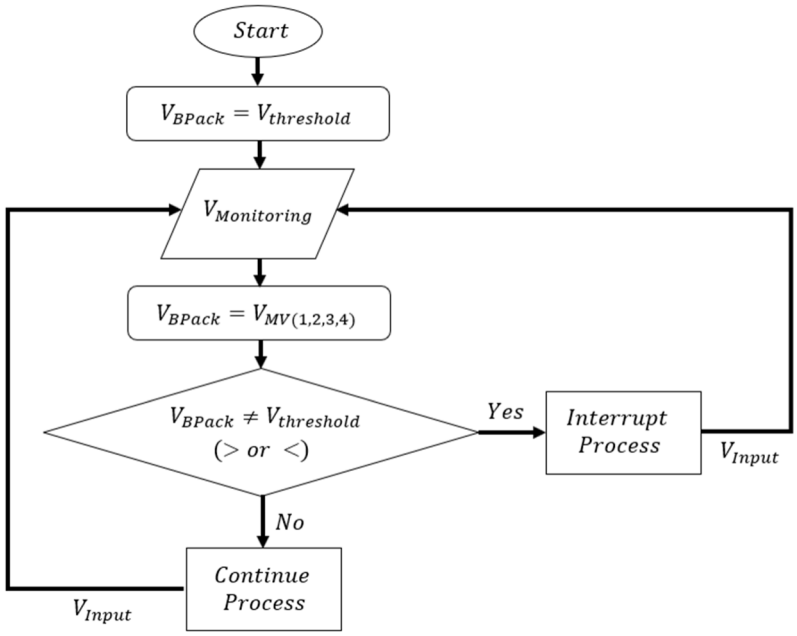

FIGURE 12. Deployed BMS protection algorithm flowchart.

V_{BPack} that is the summation of the voltage from modules 1, 2, 3, and 4 represented by $V_{MV(1,2,3,4)}$. The condition is set to hold a threshold for undervoltage and overvoltage protection of the BMS If $V_{BPack} \neq V_{threshold}$ the BMS will actuate to stop the process, thereby stopping the voltage input to the system. $V_{BPack} \neq V_{threshold}$ have two specific conditions which are as follows:

- $V_{BPack} > V_{threshold}$ stands for overvoltage state which will trigger the V_{BPack} voltage flow stoppage of the BMS.
- $V_{BPack} < V_{threshold}$ stands for the undervoltage which state which will trigger the V_{BPack} voltage flow stoppage of the BMS.

$V_{BPack} = V_{threshold}$ is the normal state of the BMS whereas the nominal operation voltage of the BMS is flowing to the system. This condition enables the flow of the V_{BPack} voltage to the system.

■ **Deployed Algorithm for IIoT Applications –** Fig. 13 highlights the IIoT-based processing capability of the proposed modular BMS realizing intelligent and state-of-the-art processing. In deploying an algorithm, the computing power of the MCU should be considered. This is due to the constraints between the algorithm size and the computing capability or power of the MCU. For this implementation, the computing power of the TMS28379D. The BMS signal acquisition sensors for both the LMUs and CMU are

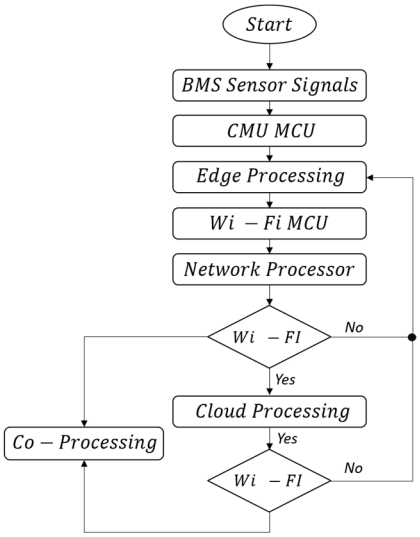

FIGURE 13. BMS for IIoT based applications processing flowchart.

represented by the BMS sensor signal block. The CMU MCU processes the signal acquired from the LMU sensors and CMU sensors. This BMS is capable of IIoT-based processing, wherein a machine-learning model for edge AI applications is deployed on the CMU MCU for battery state estimation and processing. The Wi-Fi module of the CMU enables wireless network processing. When wireless communication is available, the proposed BMS transmits and processes data to the cloud for processing. This paves the way for the co-processing capability of the BMS. The edge processing of the BMS is independent of the co-processing; this capability paves the way for a plethora of intelligent applications, such as for IIoT-based modular BMS deployment.

III. RESULTS AND DISCUSSIONS

Fig. 14(a) shows the actual battery pack for deployment, and Fig. 14(b) shows the battery modules with the actual cell. Fig. 14 shows the actual modular BMS, which was theoretically discussed in the methodology section. Fig. 15(a) and 15(b) show the actual LMU and CMU modules of the BMS, respectively. As measured, the actual sizes of the LMU and CMU are 100 × 150 mm and 120 × 150 mm, respectively. Fig. 14(a) and Fig. 14(b) shows the actual battery pack used for testing the proposed BMS. The battery cells were manufactured and provided by BEXEL Co. Ltd. South Korea. The battery cell is LIB34600 with a 6.55 Ah rating. Each cell has a minimum, nominal, and maximum rated voltage of 3.2 V, 3.6 V, and 4.2 V, respectively. Each LMU module has a minimum, nominal, and maximum rated voltage of 12.8 V, 14.4 V, and 16.8 V, respectively. One battery pack with 4 modules has a minimum, nominal and maximum rated voltage of 51.2 V, 57.6 V, and 67.2 V, respectively. In our previous study [8], the proposed BMS was tested using a DC power supply. Fig. 16 shows the comparative advantage of the proposed modular BMS monitoring accuracy compared with

TABLE 2. Average relative error comparison of the BMS voltage monitoring.

Relative Error (%)	[32]	[33]	[34]	Proposed Method [8]
Cell 1	0.028	0.55	0.08	0.028
Cell 2	0.056	0.81	0.12	0.034
Cell 3	0	0.27	0.093	0.051
Cell 4	0.139	-	0.23	0.030
Average	0.058	0.54	0.1308	0.03575

other studies, as presented in Table 2. In summary for the DC power supply-based testing, the total simulated terminal voltage values for this modular BMS are 51.2V (total minimum), 57.6V (total nominal), 59.2V, and 67.2V (total maximum). Cells 1-4 of the battery module connected to LMUs 1-4 have yielded an impressive result in terms of accuracy. Table 2 presents the actual voltage applied to the proposed modular BMS and LMUs 1-4 average voltage measurement for each cell with respect to the simulation time.

The RMSE voltage measured for each cell 1-4 in LMUs 1-4 module is 0.0013, 0.0018, 0.00282 and 0.001625 respectively. This yields a mean RMSE of 0.0018895. The voltages of each LMUs' cells 1, 2, 3, and 4 are stable throughout the test, as plotted in Fig. 16. Fig. 16 plots the actual voltage with respect to the BMS measured voltage results. The deployment of the proposed modular BMS circuit to the simulation platform proves the successful integration of the BMS hardware to the simulation platform for real-time practical applications. In Fig. 16, the rectangular box highlights the transition of measured cell voltage from 3.7 V to 4.2 V. The figure depicts a magnified view of the voltage measurement of LMUs 1–4 for each cell at simulation time of 1340–1415 s. The measured voltage yielded a stable relation with the actual voltage in each cell, indicating high voltage measurement accuracy.

Table 3 shows the LMU voltage measurement cross-performance analysis using a DC power supply as the source. This cross-performance analysis demonstrates the advantage of this modular BMS design, that is, fault tolerance. This analysis highlights real-time cell voltage measurement with faulty LMUs in the system. The designed modular BMS showed a comparable advantage to the existing implementations in terms of voltage measurement accuracy. This accuracy is maintained even when a faulty LMU is introduced to the system. Table 3 presents the modular BMS cross-performance analysis. This table demonstrates the advantage of the proposed BMS by presenting the simulation results with faulty LMU modules. For this simulation analysis, the 3.6 V nominal voltage for each lithium-ion cell was used as the reference voltage. This gives a total of 14.4 V, which is the nominal voltage for each LMU. Fig. 17 shows the actual CMU and LMUs of the modular BMS, wherein the fault condition is highlighted. The isolated communication channel of the proposed modular BMS utilizes a serial communication interface (SCI). This isolation approach is highlighted in Fig. 9; this fault tolerance makes the system adaptive to

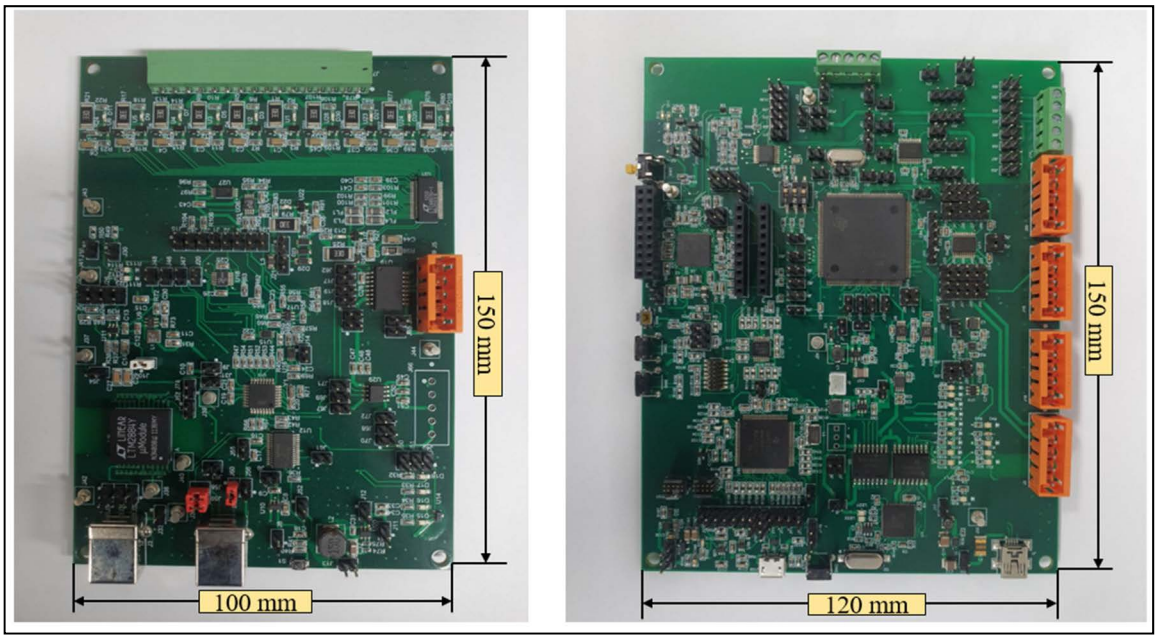

FIGURE 14. Actual modular battery management system PCB (a) LMU and (b) CMU module.

TABLE 3. LMU voltage cross-performance fault analysis. (DC power supply.)

Actual Voltage Input : 14.4V (Nominal)	**1 Faulty LMU**											
Fault	LMU 1			LMU 2			LMU 3			LMU 4		
Active Module	LMU 2	LMU 3	LMU 4	LMU 1	LMU 3	LMU 4	LMU 1	LMU 2	LMU 4	LMU 1	LMU 2	LMU 3
Average (V)	3.602	3.6001	3.601	3.602	3.6	3.602	3.603	3.601	3.603	3.603	3.602	3.604
RMSE (%)	**0.002**	**0.002**	**0.002**	**0.003**	**0.002**	**0.003**	**0.003**	**0.003**	**0.003**	**0.005**	**0.003**	**0.004**
2 Faulty LMUs												
Fault	LMU 1 and LMU 2			LMU 1 and LMU 3			LMU 1 and LMU 4			LMU 2 and LMU 4		
Active Module	LMU 3	LMU 4		LMU 2	LMU 4		LMU 2	LMU 3		LMU 1	LMU 3	
Average (V)	3.604	3.605		3.602	3.604		3.603	3.598		3.603	3.602	
RMSE (%)	**0.004**	**0.0056**		**0.003**	**0.0045**		**0.003**	**0.005**		**0.004**	**0.002**	
3 Faulty LMUs												
Fault	LMU 1 , LMU 2 and LMU 3			LMU 1 , LMU 3 and LMU 4			LMU 1 , LMU 2 and LMU 4			LMU 2 , LMU 3 and LMU 4		
Active Module	LMU 4			LMU 2			LMU 3			LMU 1		
Average (V)	3.603			3.602			3.603			3.602		
RMSE (%)	**0.003**			**0.003**			**0.003**			**0.002**		

faulty situations. Fault adaptivity increases not only the overall BMS-deployment safety, but also minimizes the maintenance cost and the overall operational cost. In terms of fault, the faulty LMU does not affect the performance of other LMUs; hence, the system operation is not interrupted. Maintenance and BMS failure are costly, which directly affect the trade-off between the design cost and functionality. The proposed modular BMS design approach and isolation realize cost-effective and operationally efficient BMS deployment. This isolation approach adheres to the ISO26262 design standards for ''Road vehicles – Functional safety'' emphasizing the safety standards of deploying BMS to the rapidly growing electric-based transportation industry. After simulating with a controlled DC power supply, the proposed modular BMS was deployed with an actual battery pack. This integrates the dynamic characteristics of battery cells to the proposed modular BMS. Table 4 lists the average RMSE of each module when subjected to battery pack monitoring. For this test, two modules were tested with cells 1–8. Cells 1–4 were the subjects for the voltage monitoring for LMU 1 and LMU 3; for LMU 2 and LMU 4, cells 5–8 were used for voltage monitoring. Overall, the accuracy of the average voltage monitoring has a negligible RMSE for a total voltage monitoring time of 1800 s. LMUs 1 – 4 have an average RMSE of 0.00083, 0.00178, 0.00083 and 0.00085 respectively. This shows the voltage measurement accuracy of the designed modular BMS, which is comparatively lower compared with the test using a DC power supply.

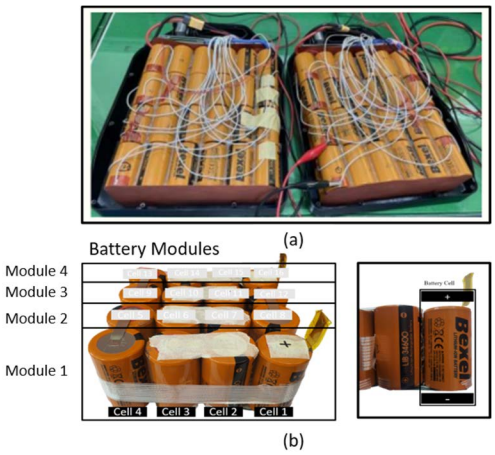

FIGURE 15. Actual and (a) battery pack enclosure (b) battery modules.

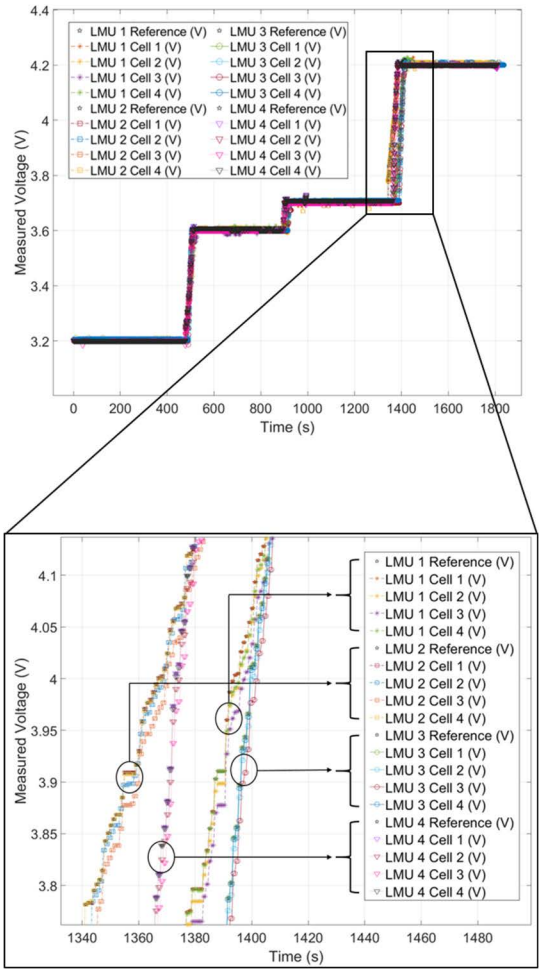

FIGURE 16. BMS test with power supply as a source.

This proves the monitoring accuracy of the proposed modular BMS considering the dynamic behavior of the battery, which is pivotal to the battery state estimation such as state-of-health (SoH), state-of-charge (SoC) and remaining useful life (RuL).

TABLE 4. Average RMSE (%) of each LMU module. (Battery pack source.)

LMU 1	Cell 1	Cell 2	Cell 3	Cell 4	Testing time (s)
Actual Voltage (V)	3.355	3.678	3.678	3.665	
Average Voltage Reading (V)	3.356	3.678	3.678	3.667	1800s
RMSE (%)	**0.001**	**0.0002**	**0.0001**	**0.002**	
LMU 2	Cell 5	Cell 6	Cell 7	Cell 8	Testing time (s)
Actual Voltage (V)	3.357	3.679	3.675	3.676	
Average Voltage Reading (V)	3.357	3.678	3.678	3.679	1800s
RMSE (%)	**0.0001**	**0.001**	**0.003**	**0.003**	
LMU 3	Cell 1	Cell 2	Cell 3	Cell 4	Testing time (s)
Actual Voltage (V)	3.355	3.678	3.678	3.665	
Average Voltage Reading (V)	3.357	3.679	3.678	3.665	1800s
RMSE (%)	**0.002**	**0.001**	**0.0001**	**0.0002**	
LMU 4	Cell 5	Cell 6	Cell 7	Cell 8	Testing time (s)
Actual Voltage (V)	3.357	3.679	3.675	3.676	
Average Voltage Reading (V)	3.358	3.681	3.675	3.676	1800s
RMSE (%)	**0.001**	**0.002**	**0.0001**	**0.0003**	

Table 5 lists the voltage monitoring accuracy test results of multiple LMUs connected to the CMU when subjected to a fault and a battery pack as the source. To simplify the tables, each LMU is connected to a battery module operating at the nominal voltage of 14.4 V. The sum of individual cell voltages is the module voltage, which is the reference voltage for this test and is named as the actual module voltage in Table 5. In this test, the BMS system is subjected to faulty LMUs whereas it started with 4 LMUs with 1 at fault until all 4 LMUs is at fault. Throughout the test, the voltage monitoring accuracy was stable, and the process of the modular BMS was not interrupted even when the LMU module or modules were at fault. As shown in Table 5, when one module was at fault, the voltage differences yielded were 0.0008, 0.003, 0.001, and 0.002, respectively, with an average voltage difference of 0.00017 V. When two LMU modules were at fault, the voltage differences yielded were 0.001, 0.002, 0.00018, and 0.00011, respectively, with an average voltage difference of 0.0008 V. Lastly, when three LMUs were at fault, the voltage differences yielded were 0.00011, 0.002, 0.002, and 0.00012, respectively, with an average voltage difference of 0.001 V. All of these errors are minimum and could be caused by the initial voltage reading and the dynamic behavior of the battery itself from the time the voltage was first measured to the time it was monitored by the BMS. This modular BMS topology with fault isolation communication realizes an adaptable architecture that is flexible and expandable in terms of actual deployment.

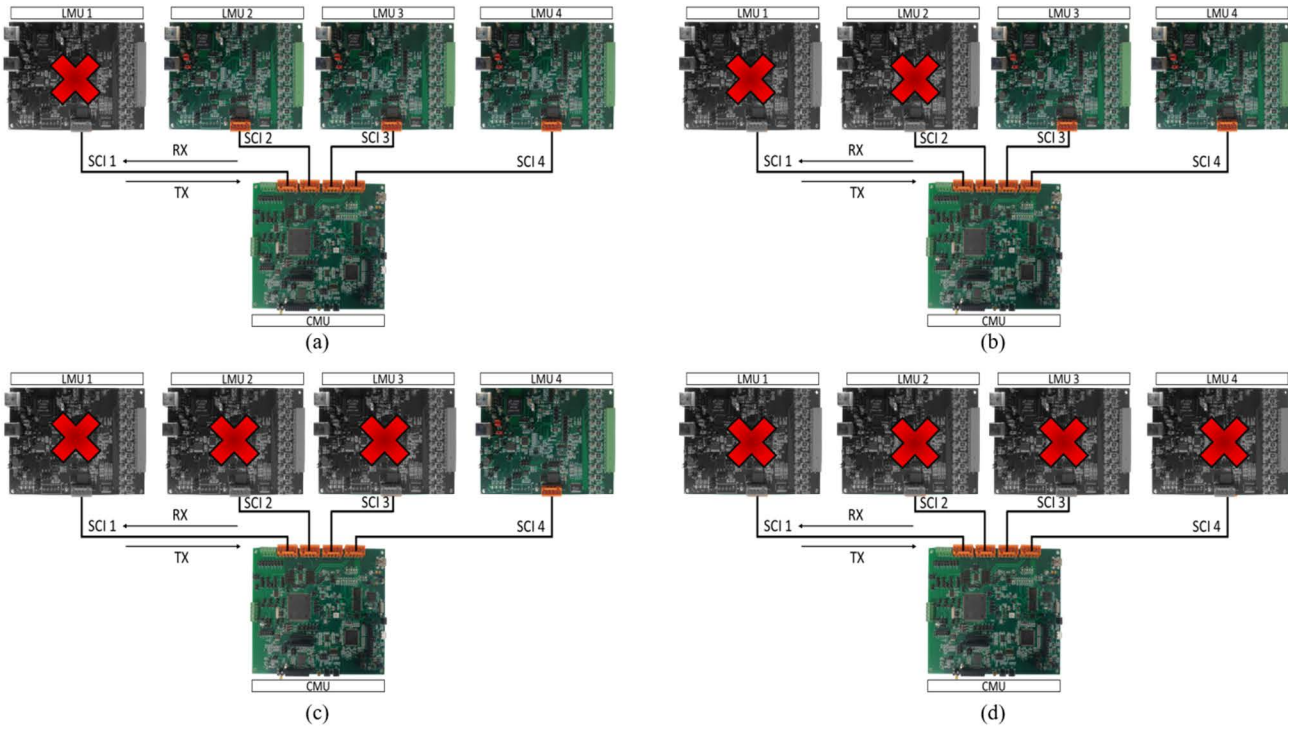

FIGURE 17. Modular BMS fault tolerance analysis (a) 1 LMU at fault (b) 2 LMUs at fault (c) 3 LMUs at fault and (d) 4 LMUs at fault.

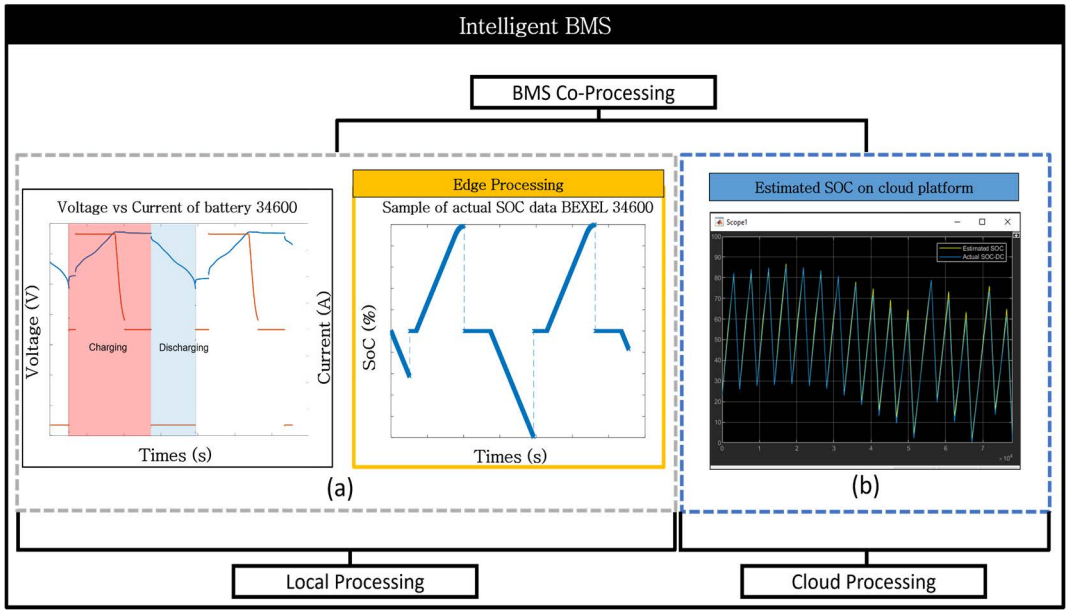

FIGURE 18. Actual modular BMS IIoT-based capability using actual battery for deployment.

The main aim of this modular BMS is to efficiently deploy IIoT-based applications such as shown in Fig. 18. To prove the implementation viability of the proposed modular BMS in this study, it is deployed to an unmanned ground vehicle (UGV) for military applications, which is controlled wirelessly via a 2.4 GHz ISM band control signal. This is to test the proposed BMS in actual applications with its IoT capability for industrial-scale applications. The UGV has a battery pack of maximum voltage rating of 67.2 V and a maximum speed of 10 km/h with 30 kg load. The average running time of this UGV is 600 min.

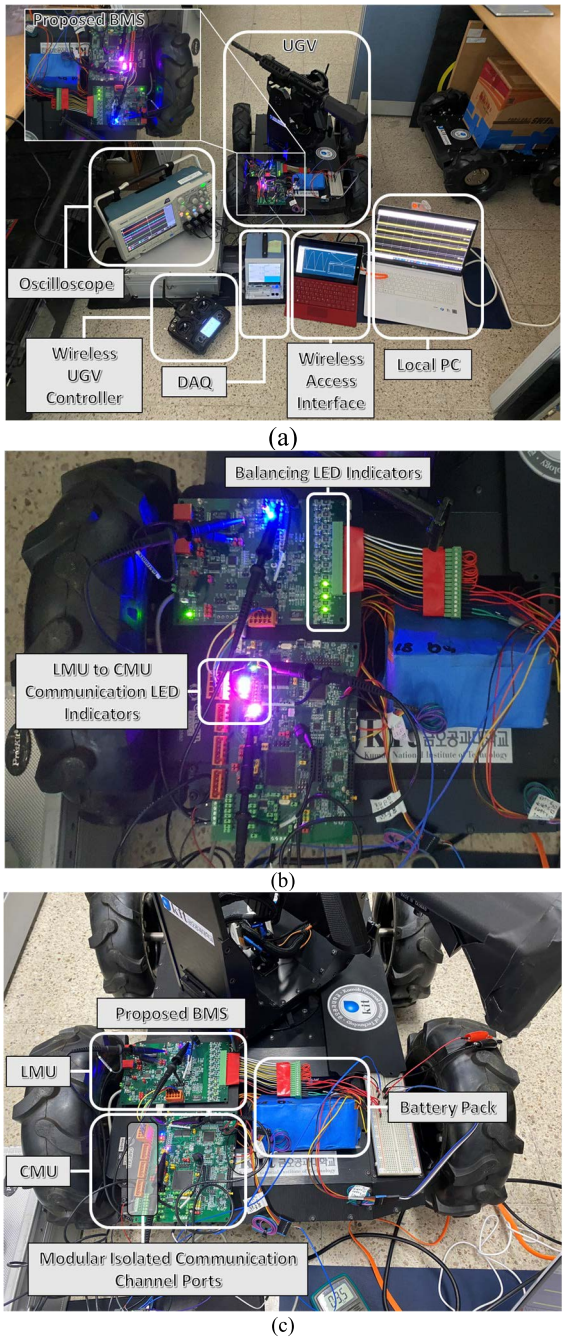

FIGURE 19. Proposed modular BMS (a) Actual modular BMS UGV deployment overview (b) Magnified view of the proposed and deployed BMS (c) Detailed overview of the modular BMS IIoT -based application.

Fig. 18 shows the implementation of local processing (edge-based), IIoT based processing using the BEXEL rechargeable battery pack in the UGV with LIB34600 cells. In Fig. 18(a), the acquired battery parameters from the LTC6803 of the LMUs, such as the voltage and current are pre-processed through a locally deployed model. The locally deployed model for battery parameter acquisition is realized through the LMU MCU which is the ATMEGA. These processed parameters are then acquired by the CMU from all the LMUs which the CMU is capable of processing locally. The capability of the CMU to process the parameters locally through a deployed model realizes edge efficient deployment and design approach.

The acquired pre-processed parameters would also be the input for cloud-based processing of the CMU. This cloud-based processing also takes place at the CMU MCU which is the TMS28379D. By integrating a wireless external communication sub-circuit to the CMU MCU, as shown in Fig. 8, the proposed modular BMS realizes BMS co-processing capability. This makes the CMU capable of co-processing the data locally at the edge and using the cloud computing paradigm with the integration of wireless communication, such as for battery state prediction or estimation, as shown in Fig. 18(b). Fig. 19 depicts the actual deployment and testing for the proposed modular BMS. Fig. 19(a) depicts the UGV deployment of the BMS. The proposed BMS is deployed to the battery-pack power source of the UGV via the battery dock compartment. For emphasis, the battery dock compartment is opened, and the battery pack and the BMS is taken outside, as shown in Fig. 19(b). Devices are used to measure the raw signal and the actual signal processed by the BMS to verify its efficiency and implementation accuracy as shown in Fig. 19(a). Detailed deployment of the proposed BMS is shown in Fig. 19(c). Tektronics MDDO3034 mixed-domain oscilloscope (350 MHz, 2.5 GS/s) and Tektronix TPP0500B 500 MHz Probe (300V CAT II, 3.9 pF/10 MΩ) were used to test and analyze the stability of the sensor input signals being processed by the BMS. The raw signal data were acquired by OpreX GP10 data acquisition (DAQ) module with the universal analog input GX90XA for real-time signal visualization and storage for the analysis of the results. Two local connections directly communicate with the deployed BMS. The local PC is used to deploy the machine learning algorithm to the applied BMS IIoT applications. The overall algorithm with the machine learning block for the battery state estimation is presented in Fig. 20. The figure demonstrates the importance of the measured battery-cell parameter accuracy. Fig. 20(a) depicts the battery cell data acquisition, which is locally processed by the LMU and then monitored by the CMU module. Fig. 20(b) shows the acquired battery cell parameters. Fig. 20(c) shows the processing of the acquired battery cell data for state estimation via the SOC estimation block. This state estimation, as shown in Fig. 20(d), relies on the acquired battery cell parameters by which the proposed modular BMS is capable of transmitting wirelessly to the cloud using the CMU module via the CC3220SF block. The local PC also enables real-time signal analysis and visual representation via the simulation platform in MATLAB- Simulink. The local PC, similar to the wireless access interface, can access the proposed GUI, as presented in Fig. 21 for this modular BMS; however, the wireless access interface is a device particularly enabled by the IIoT-based application capability of the BMS. This wireless access interface can access the deployed BMS wirelessly in real time with and without the Internet. This is made possible by the co – processing capability of the proposed

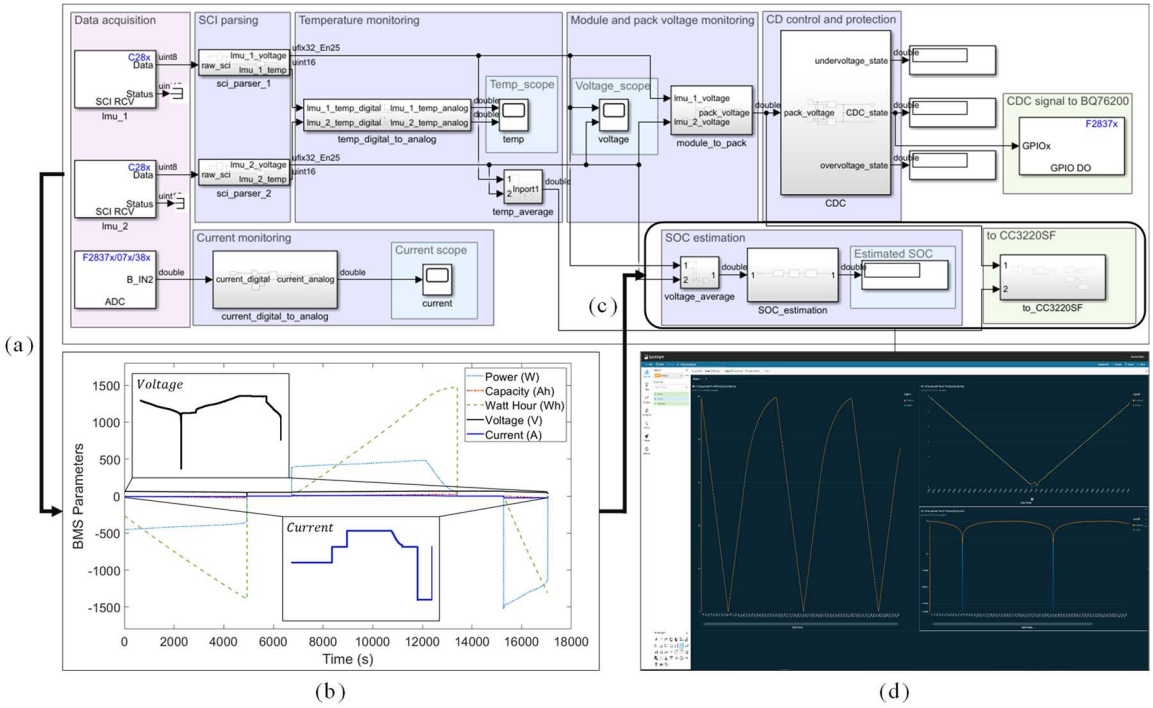

FIGURE 20. Overall overview and actual results of the intelligent data processing (a) battery cell data acquisition (b) acquired battery cell parameters (c) local processing for the battery(d) IIoT processing capability of the proposed BMS.

FIGURE 21. Proposed GUI for the BMS access nodes (a) local PC (b) wireless access interface.

modular BMS. The edge device can locally process data when the internet communication is not accessible. This allows soft and hard real-time deployment of the proposed modular BMS.

Fig. 22 shows the monitoring voltage at a 3500 s deployment time or almost an hour using a battery pack with modules that represent the minimum, nominal and maximum value of each cell. The measurement validates the voltage monitoring of the BMS at minimum (3.2 V), nominal (3.6 V), and maximum (4.2 V) voltage values of the battery pack. It can be seen in the figure that although there are minimal fluctuations in the voltage monitoring, the overall monitoring accuracy is stable. This is proved by the cell average reference voltage coinciding with the actual measured voltage. Furthermore, to concretely analyze these results, the acquired voltage signal of the oscilloscope on the BMS local processing remains stable for both the temperature and temperature measurement capability of the BMS. Fig. 23(a) and Fig. 23(b) shows the analog-to-digital conversion of the voltage monitoring. Fig. 24 shows the analog reading of the BMS prototype deployed to the UGV on an oscilloscope, which is visualized as a digital signal in a local PC, as shown in Fig. 23(b). It is known that in any prototype hardware development, the signal acquisition is pivotal to the performance efficiency of the proposed design approach. The voltage monitoring signal stability of cells 1–4 of module 1 is highlighted using Tektronics MDDO3034 mixed-domain oscilloscope. As highlighted in Fig. 23(a), the analog signals are the actual voltages for cells 1– 4. The stable signal is analyzed at a time interval of zoom factor 4kX at a specified zoom position with respect to the set time reference. Between time (a) and time (b) for all oscilloscope signal results, which is at –18.40 μs to 18.36 μs, the signal yielded is stable and accurate. The electrical signal reading for the voltage is accurate, considering the signal fluctuation. At time points (a) and (b) with respect to the reference at 4.00 μs, the signal reading for each of the cells is as follows:

Cell 1: Time (a) = 3.600 V; Time (b) = 3.640 V.
Cell 2: Time (a) = 3.560 V; Time (b) = 3.560 V.
Cell 3: Time (a) = 3.560 V; Time (b) = 3.560 V.
Cell 4: Time (a) = 3.600 V; Time (b) = 3.600 V.

These values represent accurate electrical signal measurements owing to the time interval set to highlight this result.

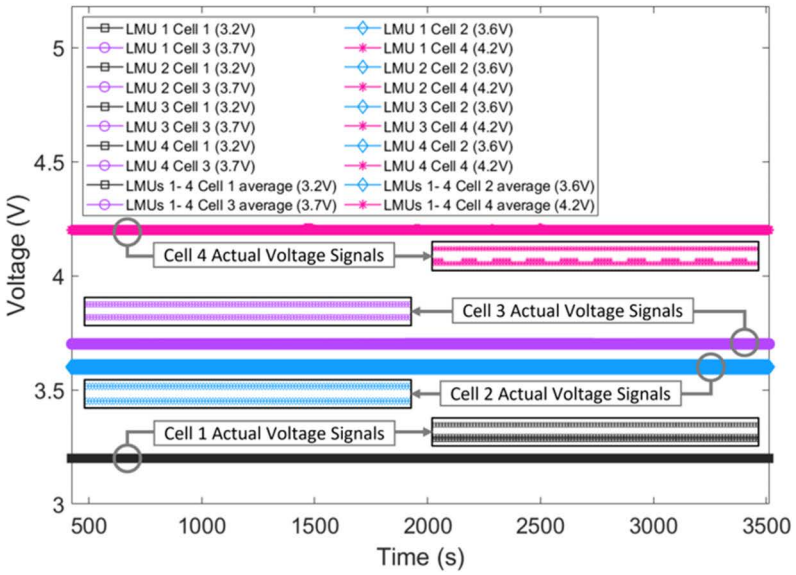

FIGURE 22. Edge and IIoT based actual co – processing capability of the proposed BMS.

TABLE 5. LMU voltage cross-performance fault analysis. (Battery pack source.)

1 Faulty LMU												
Fault	LMU 1			LMU 2			LMU 3			LMU 4		
Active LMU Module	LMU 2	LMU 3	LMU 4	LMU 1	LMU 3	LMU 4	LMU 1	LMU 2	LMU 4	LMU 1	LMU 2	LMU 3
Actual Module Voltage (V)	14.378	14.352	14.378	14.399	14.350	14.378	14.398	14.375	14.377	14.398	14.378	14.350
Monitored Module Voltage (V)	14.377	14.352	14.377	14.397	14.347	14.377	14.398	14.377	14.378	14.396	14.375	14.350
Voltage Difference	**0.001**	**0.00032**	**0.001**	**0.002**	**0.003**	**0.005**	**0.00012**	**0.002**	**0.001**	**0.002**	**0.003**	**0.00015**

2 Faulty LMUs								
Fault	LMU 1 and LMU 2		LMU 1 and LMU 3		LMU 1 and LMU 4		LMU 2 and LMU 4	
Active LMU Module	LMU 3	LMU 4	LMU 2	LMU 4	LMU 2	LMU 3	LMU 1	LMU 3
Actual Module Voltage (V)	14.351	14.379	14.378	14.378	14.378	14.353	14.399	14.350
Monitored Module Voltage (V)	14.350	14.378	14.378	14.376	14.377	14.353	14.399	14.350
Voltage Difference	**0.001**	**0.001**	**0.00012**	**0.002**	**0.001**	**0.00018**	**0.00012**	**0.00011**

3 Faulty LMUs				
Fault	LMU 1 , LMU 2 and LMU 3	LMU 1 , LMU 3 and LMU 4	LMU 1 , LMU 2 and LMU 4	LMU 2 , LMU 3 and LMU 4
Active LMU Module	LMU 4	LMU 2	LMU 3	LMU 1
Actual Module Voltage (V)	14.377	14.378	14.352	14.398
Monitored Module Voltage (V)	14.377	14.376	14.350	14.398
Voltage Difference	**0.00011**	**0.002**	**0.002**	**0.00012**

The signal stability of cells 1-4 between Time (a) and Time (b) yielded an average difference of 0.0010V. To further verify this result, these analog signals are subsequently converted to their equivalent digital signals in the LMU module, as shown in Fig. 23(b). The same test is performed to validate the temperature measurement accuracy of the proposed BMS; the results show a stable signal acquisition, as shown in Fig. 24. The acquired signal from the temperature monitoring pins and the temperature analog signal being transmitted by the LMU to the CMU when deployed to the UGV is presented in Fig. 24. As shown in the figure, in channel 3 of the oscilloscope at zoom position 8.48 μs, the sinusoidal wave is stable,

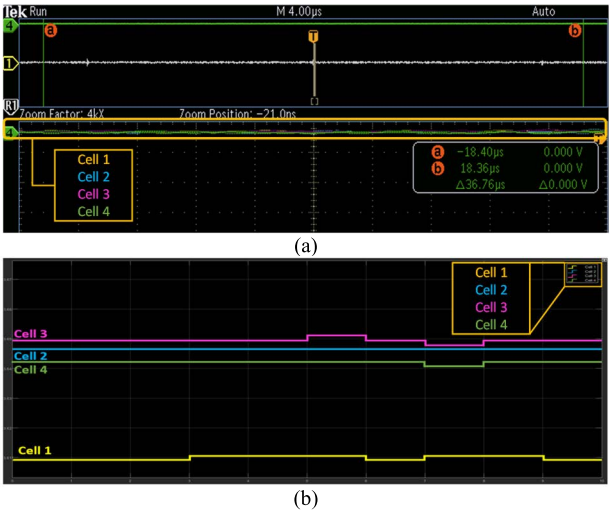

FIGURE 23. Proposed BMS input signal stability test (a) voltage monitoring analog signal (b) voltage monitoring digital signal equivalent.

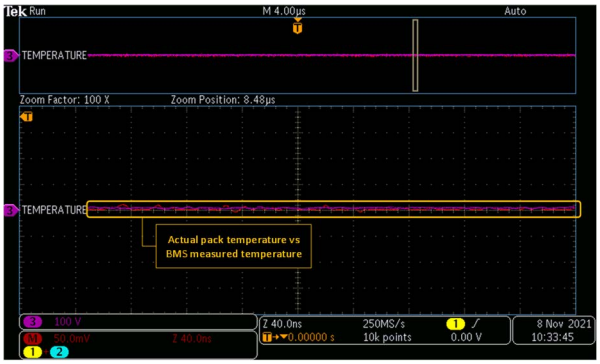

FIGURE 24. Proposed BMS input signal stability test temperature monitoring.

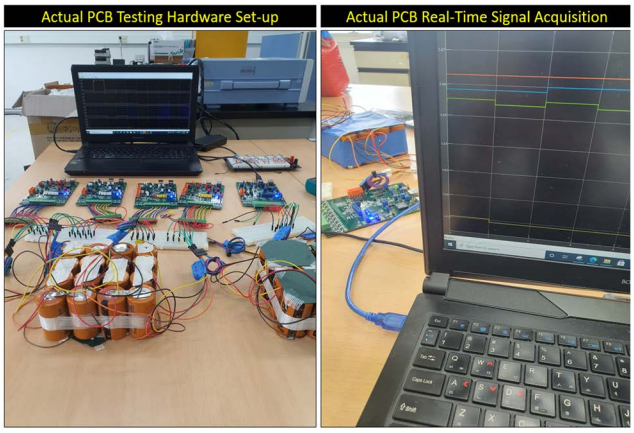

FIGURE 25. GERI south korea certification test for the proposed modular BMS.

which validates the temperature measurement accuracy of the proposed BMS.

Fig. 25 shows the actual test setup of the proposed BMS for the certification test conducted at Gumi Electronics and Information Technology Research Institute (GERI), South Korea. The results were more efficient compared to those of other BMS approaches, as shown in Table 2. In terms of voltage difference, an average of 0.001–0.007 V and 0.004 V were obtained for monitoring and balancing, respectively. In terms of the overall current demand and balancing, the average current difference was 0.102 mA, which is negligible. In terms of protection, this certification test has 10 consecutive protection tests for over-voltage and under-voltage protection, wherein the proposed BMS achieved a 100% success rate.

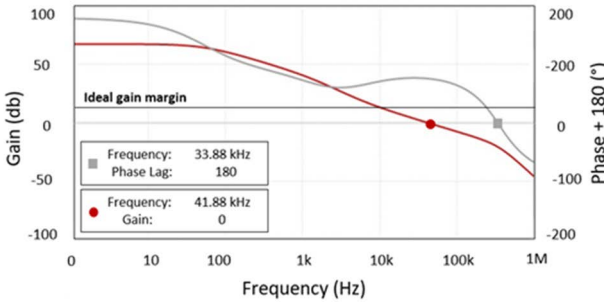

FIGURE 26. Deployed BMS DC-DC converter loop response analysis.

TABLE 6. Deployed BMS DC-DC converter loop response analysis table summary.

Frequency (kHz)	Gain (dB)
41.88	0
Frequency (kHz)	Phase lag (°)
33.88	180
	Margin
Phase (°)	76

For the BMS deployment, the efficiency of the DC–to–DC converter is directly proportional to the efficiency of the BMS because it is directly connected to the battery pack. In our previous paper [8], it was mentioned that the total efficiency of DC–to–DC converter is 92.74%; further analysis was conducted to verify this in this study. The BMS deployed to the UGV was comprehensively analyzed. Fig. 26 shows the actual results for the DC-to-DC converter considering the rating of the battery BEXEL pack modules with minimum, nominal, and maximum voltage of 12.8, 14.4 and 16.8 V, respectively. The graphical results of loop response of the LMU with the integrated isolated supply at operating voltages of 12.8 –16.8 V is presented in Fig. 26. The loop response and its parameters is listed in Table 6. The LMU DC-to-DC converter implementation response yielded a crossover frequency of 41876.97 Hz at which the control loop gain was unity (0 dB). At 180 ° lagging, the frequency yielded is 338833.358 Hz, which leads to a 75.601° phase margin and 21.898 dB gain margin. The ideal phase margin of

TABLE 7. LTC6803 temperature range.

LEAD Free Finish	Part Marking	Specified Temperature Range
LTC6803IG-1#PBF	LTC6803G-1	–40°C to 85°C
LTC6803IG-3#PBF	LTC6803G-3	–40°C to 85°C
LTC6803HG-1#PBF	LTC6803G-1	–40°C to 125°C
LTC6803HG-3#PBF	LTC6803G-3	–40°C to 125°C

the conventionally designed supply regulators adheres to is $45° < 315°$, while the ideal gain margin is above 10 dB. This validates the effectiveness and optimized design of the applied DC-to-DC converter in the LMU designed for the proposed BMS hardware prototype.

IV. CONCLUSION

In this paper, the development of IIoT-based modular BMS which can pave the way to a plethora of intelligent deployment, was briefly discussed. We implemented and evaluated our own designed modular BMS, wherein an algorithm was deployed to evaluate the deployment viability of the BMS. The deployment of the designed algorithm presented in this paper realizes design, implementation, and deployment of modular BMS for IIoT-based applications. The proposed hardware design has an integrated wireless communication sub–circuit to the central management module, by which all LMU data are collected, processed, and transmitted wirelessly. The hardware design demonstrates a comparative advantage in terms of its hardware design consideration and monitoring accuracy, as presented in Tables 1 and 2, respectively. For the hardware safety design standard, a circuit isolation approach was implemented on the modular (LMUs to CMU) communication for fault adaptivity. Furthermore, this hardware design approach realizes co-processing capability at the edge and through the IIoT computing paradigm for industrial-scale applications. This study was aimed to emphasize the design considerations for an edge-capable modular BMS, particularly its hardware and software design approach to gear towards 1) fault tolerant, 2) adaptable architecture topology, and 3) IIoT-based BMS deployment.

For future works, the hybrid integration of passive and active cell balancing in one BMS module could be explored to pave the way for a more robust and adaptive cell balancing deployment. This approach has a potential to realize a plethora of multi-configurable BMS deployment in terms of its load and cell input parameters.

APPENDIX A

LTC6803 is the battery monitoring IC used and deployed on this proposed modular battery management system. One crucial parameter is the operating temperature of the battery monitoring IC which is needed to be considered by the sub-circuits such as the RC filtering as discussed in the local management unit in the hardware design consideration section. Appendix A Table 7 shows the family of LTC6803 and the equivalent operating temperature. This information is available at the opensource datasheet of the LTC6803.

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