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RESEARCH ARTICLE

Enhanced Fault-Tolerant Robust Deadbeat Predictive Control for Nine-Level ANPC-Based Converter

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ABSTRACT Deadbeat model predictive control (DB-MPC) is one of the advanced promising control methods for power converters thanks to its simplicity, high steady-state performance and fast dynamic response. However, the high sensitivity to parameter mismatch and the difficulty of handling multiple control targets are problematic issues in DB-MPC. This work presents an improved robust DB-MPC for a new nine-level ANPC-based inverter. This inverter requires a low number of power devices compared to other single dc-source inverters. Only nine active switches and two discrete diodes are utilized to obtain a nine-level waveform. Without the need for weighting factors, the proposed DB-MPC method tackles three control goals; current control, flying capacitors (FCs) stabilization and dc-link balance, which saves the laborious effort of adjusting the weighting factors in the traditional finite control set MPC (FCS-MPC) method. Moreover, an effective dc-link balancing scheme based on power flow control is proposed and integrated into the FCs control objective. To enhance the control robustness, an EKF-based estimator is designed to identify the system parameters online. In addition, the proposed DB-MPC scheme allows the considered inverter to continue operating with the generation of five levels in the failure condition of the four-quadrant switch, improving the fault tolerance of the inverter. The developed DB-MPC method is experimentally verified in steady-state and transient operation. To demonstrate the excellent performance of the presented DB-MPC scheme, experimental comparisons with other popular MPC methods are performed.

INDEX TERMS Deadbeat MPC, multilevel inverters, capacitors balance, NP potential control, parameters estimation.

I. INTRODUCTION

Multilevel inverters (MLIs) provide attractive features over traditional two-level inverters, particularly in medium and high voltage/power applications. They have lower voltage stress on power devices, lower switching frequency, lower harmonic content, and higher efficiency [1]. Accordingly, MLIs are considered a cost-effective solution for medium and high voltage/power applications [2], [3]. There are three conventional topologies of MLIs, known as neutral point clamped (NPC), flying capacitor (FC), and cascaded H-bridge (CHB) inverters. The three-level configuration of these topologies have successfully been adopted for various applications according to the merits and demerits of each type [1], [2], [4]. However, in order to generate a higher number of levels from the conventional topologies, some challenges arise, such as the need for a large number of diodes in NPC, a large number of capacitors in FC, and multiple isolated dc sources in CHB inverters. In general, as the number of levels increases, improved waveforms with

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low harmonic content are achieved, reducing filter size and improving system efficiency. However, the required semiconductor devices and passive components are increased as well.

Hybrid MLIs offer an effective solution to produce a large number of voltage levels with a reduced number of components employed. Several hybrid structures have recently been reported in the literature [5], [6], [7], [8], [9]. Lately, an interesting MLI called nine-level split-capacitor active-neutral-point-clamped (9L-SC-ANPC) inverter was presented in [10]. The single-phase structure of this inverter employs nine power switches, two power diodes, and two FCs. Comparing with classical and recent 9L MLIs, this topology has several merits regarding the required components, conduction losses, efficiency, and overall cost as demonstrated in [10] through a comprehensive comparison. Thence, this inverter is considered in this work.

The control problem of MLIs is typically a multi-objective task, making it challenging with traditional control methods. For instance, considering FC-based MLIs, in addition to regulating the output current, the FCs and dc-link capacitors must also be balanced. Model predictive control (MPC) is considered an attractive alternative to traditional control strategies thanks to its ability to incorporate system nonlinearities and constraints with fast dynamic response [11]. One of the MPC strategies is the finite control set MPC (FCS-MPC). FCS-MPC makes use of the discrete nature of the topology by estimating the available states in a cost function considering the control goals and operational restrictions. Among MPC schemes, FCS-MPC occupies a prominent position because of its key features of being able to handle multiple goals with ease of concept, inclusion of constraints and nonlinearities, and straightforward implementation. However, variable switching frequency and, as a result, distributed harmonic spectrum, and heavy computational burden for high-level topologies are serious concerns of this method [12], [13].

Continuous control set MPC (CCS-MPC) and deadbeat MPC (DB-MPC) are two different types of MPC that offer a constant switching frequency and reduced steady-state error [14], [15]. The first method requires complex mathematical formulations and a digital platform with high computing power, and in some cases solving the control problem offline is inevitable. While DB-MPC significantly reduces the computational load by directly calculating the reference voltage that nullifies the current error at the next sample using the system-discrete model. Then, a modulation stage is used to generate the pulses for switches. DB-MPC cannot process multiple targets during the reference voltage calculation. However, handling multiple objectives is still possible during the modulation stage and is subject to the availability of the redundant states of the converter under consideration.

DB-MPC has been adopted in motor drives with conventional two-level inverters [16], [17], [18], achieving a fast dynamic performance as with FCS-MPC. In addition, compared to FCS-MPC, a much lower computational load is required for DB-MPC because there is no need for switching states evaluation, cost function optimization, or weighting factors tuning. Moreover, thanks to the presence of the modulation stage, improved steady-state behavior has been achieved with a fixed switching frequency. Despite the attractive features of DB-MPC, very few works have been reported in the literature on the application of this method to MLIs. In [19], a dual-vector MPC method based on the DB concept is presented for a CHB rectifier. In this method, the supply current regulation is targeted as a prime control objective, while the capacitors balancing is realized with available redundancies of the CHB converter. However, due to the lack of a traditional modulation stage such as carrier-based PWM (CB-PWM) or space-vector PWM (SV-PWM), fixed switching frequency operation is not realized. The authors in [14] developed a DB-MPC for controlling permanent magnet synchronous motors (PMSM) supplied by a 3L-NPC inverter. To improve the robustness of this approach, the saturation effects of the PMSM were taken into account. In [20], three DB-based MPC methods are reported for three-phase 3L-NPC to reduce the computational efforts of the traditional FCS-MPC. The three schemes depend on calculating the reference voltage using the DB concept to nullify the current error at the next sample. However, cost function optimization and weighting factor tuning are still required. In addition, the switching frequency was not constant, bringing again some of the shortcomings of the traditional FCS-MPC.

Modeling accuracy is quite significant in DB-MPC since the future decision is based solely on the calculated reference voltage, which is estimated according to the system parameters. To address the system parameters mismatch and uncertainties, several estimation approaches have been reported in the literature. In [21], a discrete-time disturbance observer is presented and incorporated into the DB-MPC for a five-phase PMSM to address the machine parameter variation issue. In [22], an online estimator based on an Extended Kalman filter is presented to estimate the filter parameters for a grid-tied modified packed U-cell MLI (MPUC-MLI). The authors in [16] investigated the performance of the traditional DB-MPC for PMSM under system parameters mismatch. Accordingly, an observer based on the sliding mode exponential law was developed to predict the stator currents and track the disturbances resulting from parameter variations.

Influenced by the challenges discussed above, an improved DB-MPC method for a new 9L-SC-ANPC inverter is proposed in this paper, addressing the issues of traditional FCS-MPC such as high computational load, variable switching frequency, weighting factors tuning, and control sensitivity to parameter mismatch. The major contributions of this paper are as follows:

1) A multi-objective low-complexity DB-MPC method is proposed to handle three goals; current control, FCs balancing and NP potential control,
2) A dc-link balancing method is developed and integrated into the FCs balancing by regulating the power transfer in the inverter. This method is suitable for MLIs with a reduced number of switches when the redundancies

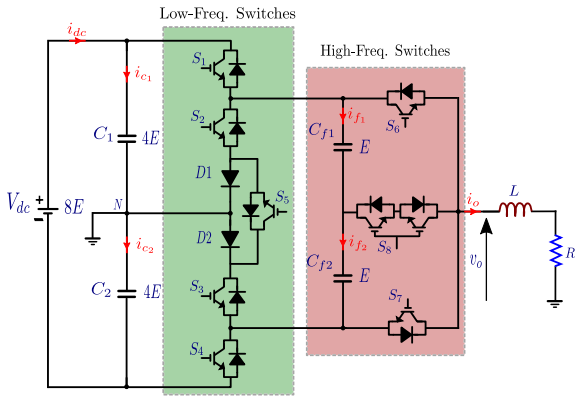

FIGURE 1. Power circuit of the 9L-SC-ANPC topology.

are insufficient to realize dc-link balancing in addition to FCs,

3) An online parameters estimator is designed based on EKF, improving the robustness of the control performance,
4) The proposed DB-MPC guarantees continuous operation of the 9L-SC-ANPC in the failure condition of four-quadrant switch, improving the reliability of the inverter,
5) The proposed DB-MPC strategy has been validated and compared with other prior-art control strategies through experimental implementation.

The rest of the paper is organized as follows. First, the operation and continuous-time model of the 9L-SC-ANPC are presented in Section II. Second, the traditional FCS-MPC is designed considering three control goals in Section III. Third, the proposed DB-MPC method is described in Section IV. Finally, the experimental implementation, results and performance evaluations are presented in Section V.

II. CONVERTER DESCRIPTION AND SYSTEM MODEL

The power circuit of the 9L-SC-ANPC topology is illustrated in Fig. 1. It consists of nine IGBTs, two diodes and two FCs supplied from a common dc-link consisting of capacitors C_1 and C_2. According to the switching frequency, this topology has two cells, a low-frequency cell consisting of switches S_1, S_2, S_3, S_4 and S_5 and a high-frequency cell consisting of switches S_6, S_7 and S_8. It is noteworthy that switches with high switching frequency have a lower standing voltage compared to other power switches, improving the power loss sharing in the inverter. According to the comprehensive comparison in [10], the 9L-SC-ANPC has a low number of power devices and FCs compared to the existing nine-level topologies. In addition, low conduction losses, high efficiency and low saturation voltage are outstanding features of this inverter as a result of the low number of on-state power devices. Based on its merits, this topology is recommended for low/medium- voltage/power high-efficiency applications.

Presuming that the dc source voltage $V_{dc} = 8E$ and the two FCs C_{f1}, C_{f2} are well stabilized at E, nine levels can be produced. The switching function s_i ($i = \{1, 2, 3, .., 8\}$) of

TABLE 1. Converter states, output voltage, and FCs charging (↑)/discharging (↓).

State	s_1	s_2	s_3	s_4	s_5	s_6	s_7	s_8	v_o	C_{f1}	C_{f2}
V_1	1	0	1	0	0	1	0	0	+4E	–	–
V_2	1	0	1	0	0	0	0	1	+3E	↑	–
V_3	1	0	1	0	0	0	1	0	+2E	↑	↑
V_4	0	0	1	0	1	1	0	0	+2E	↓	↓
V_5	0	0	1	0	1	0	0	1	+E	–	↓
V_6	0	0	1	0	1	0	1	0	0	–	–
V_7	0	1	0	0	1	1	0	0	0	–	–
V_8	0	1	0	0	1	0	0	1	-E	↓	–
V_9	0	1	0	0	1	0	1	0	-2E	↓	↓
V_{10}	0	1	0	1	0	1	0	0	-2E	↑	↑
V_{11}	0	1	0	1	0	0	0	1	-3E	–	↑
V_{12}	0	1	0	1	0	0	1	0	-4E	–	–

switch S_i can be defined as

$$s_i = \begin{cases} 1, & \text{if } S_i \text{ is ON} \\ 0, & \text{if } S_i \text{ is OFF.} \end{cases} \tag{1}$$

Table 1 illustrates ON and OFF switches for each vector with the corresponding effect on C_{f1}, C_{f2}. Note that the generated levels are labelled $\pm 4E$, $\pm 3E$, $\pm 2E$, $\pm E$ and 0.

The inverter voltage equation at the ac side is expressed according to Fig. 1 as

$$v_o = Ri_o + L\frac{di_o}{dt}, \tag{2}$$

where i_o represents the current of the 9L-SC-ANPC at the ac side. R and L are the load resistance and the filter inductance, respectively. v_o is the ac inverter voltage and is given as a function of the switches states as

$$v_o = s_1 V_{c1} - s_4 V_{c2} + s_a V_{f1} + s_b V_{f2}, \tag{3}$$

V_{c1}, V_{c2}, V_{f1} and V_{f2} are the voltages of C_1, C_2, C_{f1} and C_{f1}, respectively. s_a, and s_b are defined as

$$s_a = s_4 + s_6 - s_1 - s_2, \; s_b = s_3 + s_4 - s_1 - s_7. \tag{4}$$

The FCs model is built according to the inverter states in Table 1 as

$$\left.\begin{aligned} i_{f1} &= C_{f1}\frac{dV_{f1}}{dt} = -s_a i_o, \\ i_{f2} &= C_{f2}\frac{dV_{f2}}{dt} = -s_b i_o, \end{aligned}\right\} \tag{5}$$

i_{f1} and i_{f2} in (5) refer to the currents of C_{f1} and C_{f1}, respectively, assuming the polarity shown in Fig. 1. Similarly, the dc-link C_1 and C_2 model is given as

$$\left.\begin{aligned} i_{c1} &= C_1\frac{dV_{c1}}{dt} = i_{dc} - s_1 i_o, \\ i_{c2} &= C_2\frac{dV_{c2}}{dt} = i_{dc} + s_4 i_o, \end{aligned}\right\} \tag{6}$$

where i_{c1} and i_{c2} are the current flowing in C_1 and C_2, respectively, as depicted in Fig. 1. Suppose that C_1 and C_2 are identical and have a value of C, the relationship between the capacitors current difference $\Delta i_c = i_{c1} - i_{c2}$ and the voltage difference $\Delta V_c = V_{c1} - V_{c2}$ can be derived as

$$\Delta i_c = C\frac{d\Delta V_c}{dt}, \tag{7}$$

Δi_c can also be expressed as a function of the switches states as

$$\Delta i_c = -(s_1 + s_4) i_o. \tag{8}$$

III. TRADITIONAL FCS-MPC

The design of the traditional FCS-MPC is presented here for the 9L-SC-ANPC as a standard MPC method to be compared with the developed DB-MPC. Besides the primary current control objective, FCs balance and NP potential stabilization are included in the control design for the considered inverter. By applying Euler approach as a discretization method [22] to (2) with a sampling period T_s, the future current at $(k+1)^{th}$ sample can be obtained as

$$i_o(k+1) = (1 - \frac{RT_s}{L}) i_o(k) + \frac{T_s}{L} v_o(k), \tag{9}$$

By the same way, the voltages of C_{f1}, C_{f1} can be predicted by discretizing (5) as

$$\left.\begin{aligned} V_{f1}(k+1) &= V_{f1}(k) - \frac{T_s s_a}{C_{f1}} i_o, \\ V_{f2}(k+1) &= V_{f2}(k) - \frac{T_s s_b}{C_{f2}} i_o. \end{aligned}\right\} \tag{10}$$

Similarly, $V_c(k+1)$ is determined from (7) as

$$\Delta V_c(k+1) = \Delta V_c(k) - \frac{(s_1 + s_4) T_s}{C} i_o, \tag{11}$$

Taking into account the l_2-norm [23], the cost function g is

$$\begin{aligned} g = {} & [i_o^*(k+1) - i_o(k+1)]^2 + \lambda_1 [V_f^*(k+1) - V_{f1}(k+1)]^2 \\ & + \lambda_1 [V_f^*(k+1) - V_{f2}(k+1)]^2 + \lambda_2 [\Delta V_c(k+1)]^2, \end{aligned} \tag{12}$$

where λ_1 and λ_2 denotes to the weighting factors and are determined by trial and errors to achieve acceptable performance in terms of all goals. $i_o^*(k+1)$ in (12) is the reference value $i_o(k)$ at $(k+1)^{th}$ instant and is determined from Lagrange extrapolation [22]. As mentioned before, FCs are maintained at $V_{dc}/8$ (E), therefore, $V_f^*(k+1) = V_f^*(k) = V_{dc}/8$.

In traditional FCS-MPC, variables prediction and cost function estimation are performed each control period several times equal to the total number of converter states. Accordingly, $i_o(k+1)$, $V_{f1}(k+1)$, $V_{f2}(k+1)$, $\Delta V_c(k+1)$, and the cost function g are calculated 12 times each T_s according to (9), (10), (11) and (12), respectively, resulting in high computational burden and, therefore, the control execution is time-consuming. Additionally, adjusting the two weighting factors is a cumbersome process as there are no straightforward outlines in the literature for setting the weighting factors. Also, high steady-state error and variable switching frequency are two other major drawbacks of the traditional FCS-MPC. To address these shortcomings, a DB-MPC with the ability to handle the three control targets is developed in the next section.

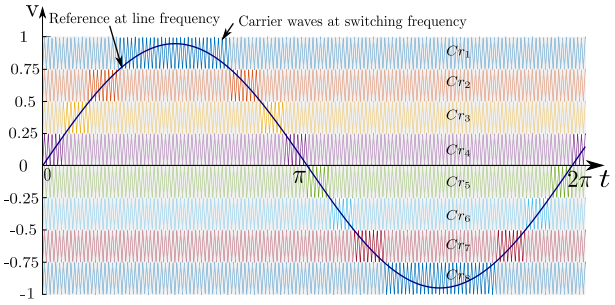

FIGURE 2. Nine-level PD-PWM waveforms.

IV. PROPOSED DB-MPC

Multiple goals handling is one of the distinct features of the traditional FCS-MPC. On the other hand, DB-MPC is usually a single-objective control method. This is an important reason for interpreting the limited application of DB-MPC to MLIs as the control problem of MLIs is typically a multi-objective task. Fortunately, handling several targets in DB-MPC is still possible in the modulation stage if there are sufficient redundancies in the inverter states. However, the MLIs with a reduced number of switches are always accompanied by a reduction in the redundant states, which limits the number of variables that can be controlled. In this regard, MLIs are divided into three types; non-redundant, semi-redundant and redundant converters [24]. Due to the significant reduction in power devices, the considered 9L-SC-ANPC can be classified as a semi-redundant topology since the redundancies are available for only $\pm 2E$ and 0. Accordingly, the available redundancies are not sufficient to balance both FCs and NP potential with the conventional concept. Thus, the prime current tracking objective is realized from the conventional DB-MPC concept and FCs balancing is realized by exploiting the redundancies. Whereas the dc-link capacitors are stabilized through the power flow control in the converter without requiring further redundancies, as described later.

By adopting Euler method, Equation (2) is written as follows:

$$v_o(k) = R i_o(k) + L \frac{i_o(k+1) - i_o(k)}{T_s}. \tag{13}$$

As discussed before, the first control objective is current tracking, which means generating the inverter voltage that causes i_o to follow i_o^* at $(k+1)^{th}$ sample. To this end, $i_o(k+1)$ in (13) is replaced by $i_o^*(k+1)$ to get the inverter reference voltage $v_o^*(k)$ as follow

$$v_o^*(k) = R i_o(k) + L \frac{i_o^*(k+1) - i_o(k)}{T_s}. \tag{14}$$

Note that $i_o^*(k+1)$ is obtained from Lagrange extrapolation as in the traditional FCS-MPC. Then, the calculated $v_o^*(k)$ is inputted to the carrier-based PD-PWM stage to generate the pulses. Fig. 2 shows the PD-PWM waveforms.

A. FLYING CAPACITORS BALANCING

As clear in Table 1, there are redundant states for levels $\pm 2E$ and 0. The zero-level redundancy does not affect the

FCs and is therefore used to reduce the number of power device commutations. While the redundancies of $\pm 2E$ can be utilized to realize the FCs balancing. As can be noticed from Table 1, for $\pm 2E$-level states (V_3, V_4, V_9 and V_{10}), the effect on C_{f1} and C_{f2} is the same (charging or discharging). Therefore, based on the voltage deviation of each capacitor, the priority should be first identified. In doing so, the priority P is determined as

$$P = \begin{cases} 1, & \text{if } |\Delta V_{f1}(k)| > |\Delta V_{f2}(k)|, \\ 0, & \text{if } |\Delta V_{f1}(k)| < |\Delta V_{f2}(k)|, \end{cases} \tag{15}$$

where $\Delta V_{f1}(k)$ and $\Delta V_{f2}(k)$ are the voltage deviations of C_{f1} and C_{f2}, respectively, and are calculated as

$$\Delta V_{f1}(k) = V_f^*(k) - V_{f1}(k), \quad \Delta V_{f2}(k) = V_f^*(k) - V_{f2}(k). \tag{16}$$

Assuming that C_{f1} has priority (P=1) and the inverter is generating voltage level $+2E$, switching state V_3 or V_4 should be applied based on the polarity of the $\Delta V_{f1}(k)$ and $i_o(k)$. For example, if $V_{f1}(k)$ is lower than its reference V_f^* ($\Delta V_{f1}(k) > 0$), V_3 is applied for $i_o(k) \geq 0$ and V_4 is applied for $i_o(k) < 0$ to charge the capacitor and increase its voltage. To this end, a Heaviside function $H(y)$ is defined as

$$H(y) = \begin{cases} 1, & \text{if } y \geq 0 \\ 0, & \text{if } y<0. \end{cases} \tag{17}$$

According to (17), $f(\Delta V_{fi})$ is given as

$$H(\Delta V_{fi}) = \begin{cases} 1, & \text{if } \Delta V_{fi}(k) \geq 0 \\ 0, & \text{if } \Delta V_{fi}(k)<0, \end{cases} \tag{18}$$

where $i = \{1, 2\}$ represent the FC number. Similarly, $f(i_o)$ is written as

$$H(i_o) = \begin{cases} 1, & \text{if } i_o(k) \geq 0 \\ 0, & \text{if } i_o(k)<0. \end{cases} \tag{19}$$

Hence, the state of $\pm 2E$ to be applied is selected as

$$\left.\begin{aligned} V_{2E} = P\{V_4[H(\Delta V_{f1}) \oplus H(i_o)] + V_3[H(\Delta V_{f1}) \odot H(i_o)]\} \\ +\bar{P}\{V_4[H(\Delta V_{f2}) \oplus H(i_o)] + V_3[H(\Delta V_{f2}) \odot H(i_o)]\}, \\ V_{-2E} = P\{V_{10}[H(\Delta V_{f1}) \oplus H(i_o)] + V_9[H(\Delta V_{f1}) \odot H(i_o)]\} \\ +\bar{P}\{V_{10}[H(\Delta V_{f2}) \oplus H(i_o)] + V_9[H(\Delta V_{f2}) \odot H(i_o)]\}. \end{aligned}\right\} \tag{20}$$

where $\oplus$ and $\odot$ represent the logical operations XOR and XNOR, respectively. Equation (20) defines the appropriate switching state that reduces the voltage deviation of the FCs based on the direction of i_o and the actual FCs voltages. First, after sensing $V_{f1}(k)$ and $V_{f2}(k)$, the priority is determined based on $\Delta V_{f1}(k)$ and $\Delta V_{f2}(k)$ according to (15). Then, taking $+2E$ as an example and assume that the FC with the priority has a voltage lower than its reference ($\Delta V_{fi} > 0$), V_3 is applied if $i_o(k) \geq 0$ and V_4 is applied if $i_o(k) < 0$ to charge this FC, as shown in Table 1. The same concept is valid for $-2E$.

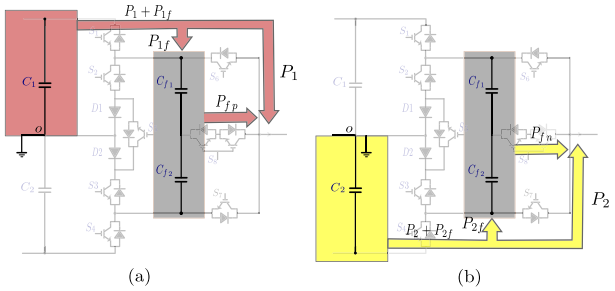

FIGURE 3. Power interchange (a) in positive half-cycle, (b) in negative half-cycle.

B. DC-LINK BALANCING

Since the 9L-SC-ANPC inverter has a limited number of redundant states due to the significant reduction in the used components and is classified as a semi-redundant topology, the available redundancies are not sufficient to achieve NP potential control in addition to balancing the FCs in the single-phase operation. Therefore, inspired by the concept presented in [10] for traditional CB-PWM, the NP balance is realized in this work by regulating the power transfer in the topology. The NP balance is integrated into the designed DB-MPC method. This approach can be applied to any FC-based MLI.

Fig. 3 shows the power supplied from the dc-link to FCs and the ac side (ac load) during an entire sinusoidal cycle. According to the power flow analysis, it is clear that during the positive half-cycle, the upper capacitor C_1 provides power P_{1f} to the FCs and P_1 to the ac load, whereas C_2 takes over the power feed task in the negative half-cycle with providing powers P_{1f} and P_{1f}, as shown in Fig. 3b. Accordingly, the total power supplied by the dc-link is the summation of the power P_{c1} from C_1 and the power P_{c2} from C_2. P_{c1} and P_{c1} can be expressed as

$$P_{c1} = P_1 + P_{1f}, \quad P_{c2} = P_2 + P_{2f}. \tag{21}$$

From (21), it is clear that the energy provided by C_1 can be regulated by P_{1f} of the FCs. Likewise, the power P_{2f} affects the total energy provided by C_2. Note that, P_{1f} and P_{2f} can be controlled via the reference value V_f^*. Accordingly, to control the NP potential, V_f^* need to be estimated in each half-cycle based on V_{c1} and V_{c2}. For clarification, if $V_{c1} > V_{c2}$, V_f^* is increased in the positive half-cycle to increase P_{1f} and draw more energy from C_1, and is reduced in the negative part of the cycle to reduce P_{2f}. As a result, V_{c1} will decrease V_{c2} will increase. According to that, V_f^* is estimated as

$$V_f^*(k) = \begin{cases} \beta V_{c1}, & \text{if } v_o^*(k) > 0, \\ \beta V_{c2}, & \text{if } v_o^*(k) < 0, \end{cases} \tag{22}$$

where β is the ratio of the FCs voltage to the dc-link capacitor voltage in the balancing operation, $\beta = E/4E = 0.25$. The calculated value of $V_f^*(k)$ according to (22) is then used in (16) to include the NP stabilization in the FCs balancing.

TABLE 2. Converter states for the open-circuit failure condition of the bidirectional switch S_8.

State	S_1	S_2	S_3	S_4	S_5	S_6	S_7	v_o
$V1$	1	0	1	0	0	1	0	$4E$
$V2$	1	0	1	0	0	0	1	$2E$
$V3$	0	0	1	0	1	1	0	$2E$
$V4$	0	0	1	0	1	0	1	0
$V5$	0	1	0	0	1	1	0	0
$V6$	0	1	0	0	1	0	1	$-2E$
$V7$	0	1	0	1	0	1	0	$-2E$
$V8$	0	1	0	1	0	0	1	$-4E$

C. OPERATION UNDER FAULT CONDITION

One distinct feature of the 9L-SC-ANPC topology is the capability to operate with different number of levels. By exploiting this feature, the control is designed to enable the inverter to continue operating even in a failure condition of the four-quarter switch S_8. According to Table 1, there are 12 states in the normal operation allowing the generation of nine voltage levels. However, if an open circuit fault occurs in S_8, the healthy switching states will be reduced to only eight. Whereas V_2, V_5, V_8 and V_{11} in Table 1 will be faulty states. In this case, the FCs C_{f1} and C_{f2} are connected in series, forming one capacitor with a value C_f and voltage V_f, where C_f and V_f are given as

$$C_f = \frac{C_1 \cdot C_2}{C_1 + C_2}, \quad V_f = V_{f1} + V_{f2}. \tag{23}$$

with regulating C_f at $V_{dc}/4$ ($2E$), five levels ($\pm 4E, \pm 2E, 0$) can be obtained from the 9L-SC-ANPC. The switching states and produced levels in this case are shown in Table 2. To include the NP control, the reference voltage of C_f is calculated from (22) with a different value of β according to its definition, where $\beta = 2E/4E = 0.5$. It should be mentioned that the transition from the healthy operation to the faulty condition is realized by the controller with no transient time as the FC C_f is balanced at the same voltage ($2E$ assuming a balanced NP potential) in both conditions. Since there is only one FC, no priority check according to (15) is required. After calculating the new $V_f^*(k)$ by (22) with $\beta = 0.5$, ΔV_f^* is calculated as

$$\Delta V_f(k) = V_f^*(k) - V_f(k). \tag{24}$$

Subsequently, the redundant states of $\pm 2E$ in Table 2 can be identified as

$$\left.\begin{aligned} V_{2E} &= V_3[f(\Delta V_f) \oplus f(i_o)] + V_2[f(\Delta V_f) \odot f(i_o)] \\ V_{-2E} &= V_7[f(\Delta V_f) \oplus f(i_o)] + V_6[f(\Delta V_f) \odot f(i_o)]. \end{aligned}\right\} \tag{25}$$

D. MODEL PARAMETERS ESTIMATOR DESIGN

Since the future decision in the DB-MPC depends only on the calculated reference voltage, the modeling accuracy is considered quite significant. A slight variation in the model parameters due to ageing or thermal effects can lead to a deterioration of the system performance. To deal with this matter, an EKF-based estimator is developed to identify the filter and load parameters (R, L).

To design the EKF-based estimator, the state-space model should be first established in the discrete-time form. The continuous-time state-space model including disturbances is represented as

$$\begin{aligned} \dot{x} &= Ax + Bu + w, \\ y &= Cx + Du + v, \end{aligned} \tag{26}$$

where $x = (i_o,\ R,\ L)^T$ is the state vector, $u = v_o$ is the system input, and $y = i_o$ is the output. A, B, C, and D represent the system matrices. While w and v refer to the model uncertainties and noises related to measurements, respectively. w and v have covariance matrices represented by Q and R, respectively. The entries of Q and R are determined using the particle swarm optimization (PSO) method [25] as they have a crucial influence on the estimation accuracy. For the considered system in Fig. 1, A, B, C, and D are defined as [22]

$$A = \begin{bmatrix} -\frac{R}{L} & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix}, \ B = \begin{bmatrix} \frac{1}{L} \\ 0 \\ 0 \end{bmatrix}, \ C = \begin{bmatrix} 1 & 0 & 0 \end{bmatrix}, D = 0. \tag{27}$$

For discretization, forward Euler approach is applied to (26), which results in

$$\begin{aligned} x(k+1) &= A_d x(k) + B_d u(k) + w(k), \\ y(k) &= C_d x(k) + D_d u(k) + v(k), \end{aligned} \tag{28}$$

A_d, B_d, C_d, and D_d in (28) are defined as

$$\begin{aligned} A_d &= \begin{bmatrix} 1 - \frac{T_s R_t}{L_t} & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix}, \quad B_d = \begin{bmatrix} \frac{T_s}{L_t} \\ 0 \\ 0 \end{bmatrix}, \\ C_d &= \begin{bmatrix} 1 & 0 & 0 \end{bmatrix}, \quad D_d = 0. \end{aligned} \tag{29}$$

The implementation of the EKF algorithm is depicted in Fig. 4 and can be summarized in steps as follows

1) Initialization of state vector $x_0 = x(0)$ and covariance matrices Q and R.
2) Prediction phase
   a) State prediction $\hat{x}^-(k)$,

$$\hat{x}^-(k) = A_d \hat{x}(k-1) + B_d u(k-1), \tag{30}$$

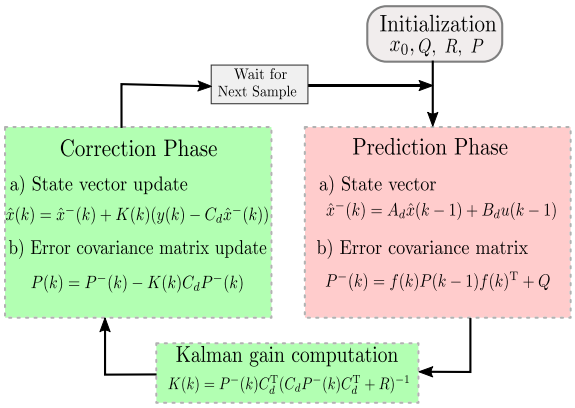

FIGURE 4. Flowchart of the EKF-based parameters estimator.

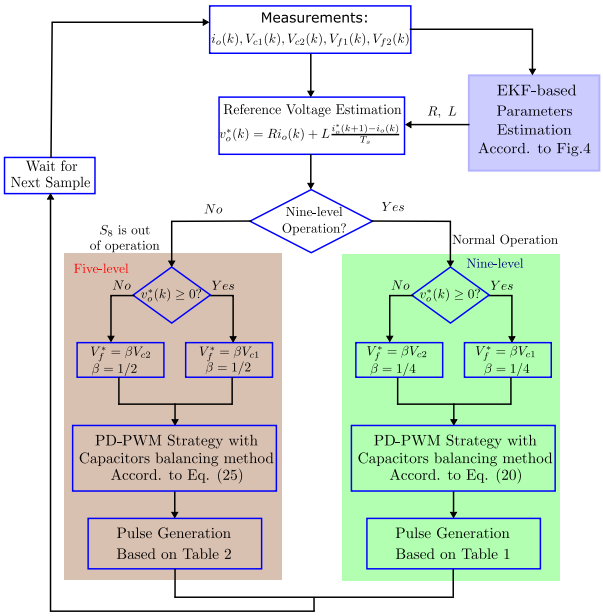

FIGURE 5. Flowchart of the proposed DB-MPC method.

b) Error covariance matrix prediction $P^-(k)$,

$$P^-(k) = J(k)P(k-1)f(k)^T + Q, \quad (31)$$

where $J(k)$ is the Jacobian matrix and written as

$$J(k) = \frac{\partial}{\partial x}(A_d x(k) + B_d u(k))|_{\hat{x}^-(k)}. \quad (32)$$

According to the system model, $J(k)$ is expressed as

$$J(x) = \begin{bmatrix} 1 - \frac{T_s R}{L} & \frac{-T_s}{L} i_o & \frac{T_s R}{L^2} i_o - \frac{T_s}{L^2} v_o \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} \quad (33)$$

3) Kalman gain $K(k)$ computation,

$$K(k) = P^-(k)C_d^T(C_d P^-(k)C_d^T + R)^{-1}. \quad (34)$$

4) Correction phase using measurements

a) State vector update,

$$\hat{x}(k) = \hat{x}^-(k) + K(k)(y(k) - C_d\hat{x}^-(k)), \quad (35)$$

b) Error covariance matrix,

$$P(k) = P^-(k) - K(k)C_d P^-(k). \quad (36)$$

5) Go to step 2.

The flowchart of the proposed DB-MPC method is shown in Fig. 5. Since the FCs balancing is realized using the available redundancies in PWM-based schemes, the operation at low line frequencies is limited with the proposed DB-MPC method due to the low number of redundant vectors in the 9L-SC-ANPC inverter. Accordingly, this inverter is recommended for grid-connected applications, where operation at low line frequencies is not required, as discussed in [10].

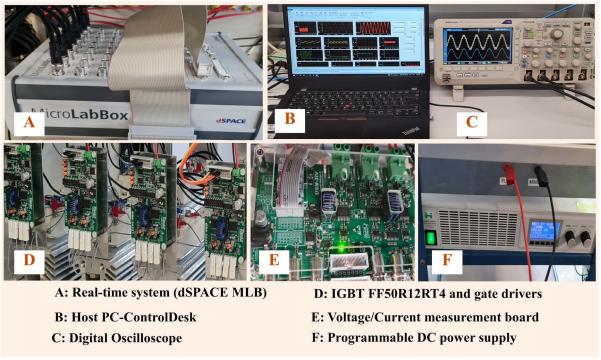

FIGURE 6. Experimental setup.

TABLE 3. Converter parameters used in experiments.

Parameter	Value
Input voltage, V_{dc}	400 V
Carrier frequency, f_c	5 kHz
Resistance (load), R	22 Ω
Inductance (filter), L	6 mH
dc-link, C_1 and C_2	3.3 mF
FCs, C_{f1} and C_{f2}	4 mF
Dead time	2 μs

V. EXPERIMENTAL RESULTS

For the experimental validation, three distinct MPC methods are experimentally implemented and compared under the same operating conditions, which are defined as follows. The first method is the traditional FCS-MPC algorithm, detailed in Section III. The second method is the single-predictive FCS-MPC. This method is first proposed in [26] for the conventional two-level converter and the 3L-NPC converter to eliminate the computational load required for the current prediction in FCS-MPC. Due to its high performance and low computational load, this concept is then applied to various converter topologies such as the 5L-ANPC inverter in [12] and the 3L T-type converter in [27]. To eliminate the calculation efforts required for the current prediction in this approach, the reference voltage that obliges i_o to follow i_o^* at $(k+1)^{th}$ sample is estimated by (14). Then, the current tracking objective is expressed in terms of voltage instead of current. Accordingly, the cost function in (12) of the traditional FCS-MPC is modified as follows:

$$g = [v_o^*(k) - v_o(k)]^2 + \lambda_{v1}[V_f^*(k+1) - V_{f1}(k+1)]^2 \\ \lambda_{v1}[V_f^*(k+1) - V_{f2}(k+1)]^2 + \lambda_{v2}[\Delta V_c(k+1)]^2, \quad (37)$$

where λ_{v1} and λ_{v2} are two weighting factors. Note that instead of 12 × current predictions in traditional FCS-MPC, this method estimates the reference voltage only once per sample, so it is called single-predictive FCS-MPC. However, it is still required to perform 12 × predictions for the FCs and dc-link voltages and 12 × cost function evaluation. The third implemented method is the DB-MPC proposed in this paper.

Fig. 6 shows the experimental setup used in the validation. A dSPACE Microlabbox is used as a digital controller to implement the two control methods. The parameters of the experimental implementation are provided in Table 3. The

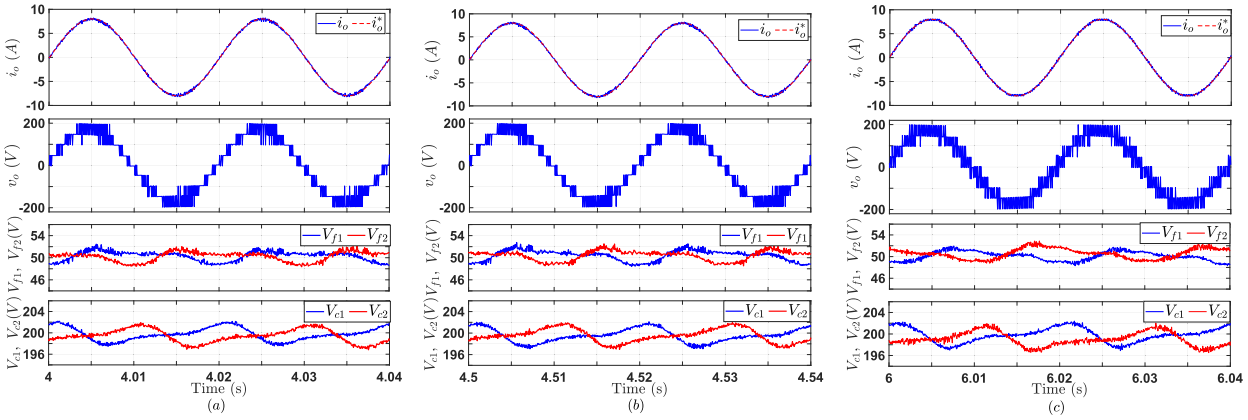

FIGURE 7. Experimental waveforms: (a) Traditional FCS-MPC, (b) Single-predictive FCS-MPC, and (c) Proposed DB-MPC.

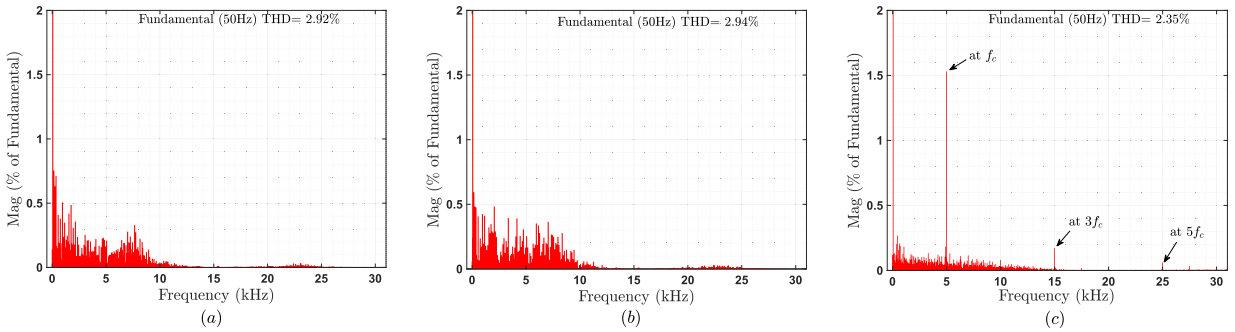

FIGURE 8. Harmonic spectrum of output current: (a) Traditional FCS-MPC, (b) Single-predictive FCS-MPC, and (c) Proposed DB-MPC.

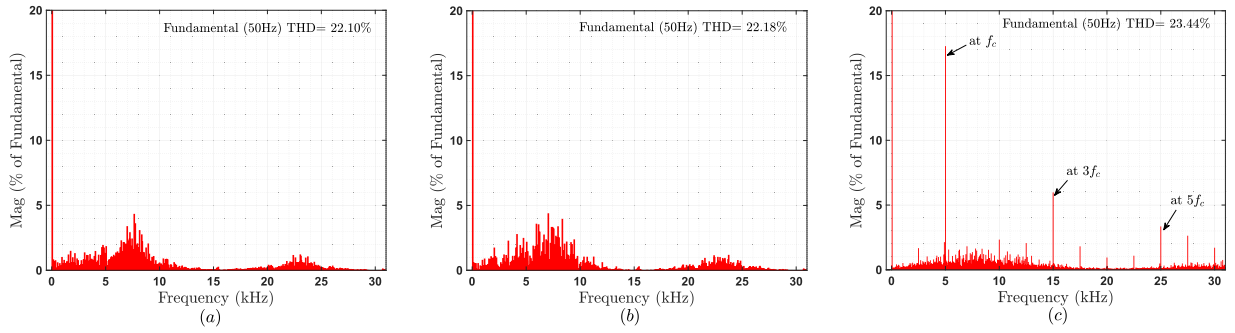

FIGURE 9. Harmonic spectrum of output voltage: (a) Traditional FCS-MPC, (b) Single-predictive FCS-MPC, and (c) Proposed DB-MPC.

delay compensation method presented in [28] is adopted in the validation.

As previously discussed, the weighting factors λ_1 and λ_2 in traditional FCS-MPC and λ_{v1} and λ_{v2} in single-predictive FCS-MPC should be first tuned. For a fair and meaningful comparison with multiple control objectives, λ_1, λ_2, λ_{v1}, and λ_{v2} are tuned to give the same voltage ripples in the FCs and dc-link as in the DB-MPC method. Subsequently, the comparison can be assessed in terms of the current tracking as a prime control target. Considering the experimental parameters in Table 3 and i_o^*=8 A, λ_1, λ_2, λ_{v1}, and λ_{v2} are determined by trial and errors and found to be 0.25, 0.06, 2700, and 450, respectively. Under these values, the three MPC methods have voltage tolerances of 3.5 V and 5 V in FCs and dc-link capacitors, respectively.

A. STEADY-STATE AND DYNAMIC OPERATION AT NOMINAL SYSTEM PARAMETERS

For a fair comparison, the same average switching frequency f_s should be adopted for the MPC methods under consideration [29]. f_s of the 9L-SC-ANPC converter is calculated as

$$f_s = \frac{\sum_{i=1}^{8} f_{si}}{8}, \tag{38}$$

where f_{si} is the average switching frequency of switch S_i, with $i \in \{1, 2, 3, 4, 5, 6, 7, 8\}$, and is calculated based on the number of commutations n_{si} in the period T_c as $f_{si} = n_{si}/T_c$ [27]. The proposed DB-MPC method is validated experimentally at $T_s = 50$ μs and carrier frequency $f_c = 5$ kHz. According to (38), f_s of the DB-MPC is found to be 2 kHz. For the traditional and single-predictive FCS-MPC methods, a sampling period T_s of 65 μs is chosen to result in the same average

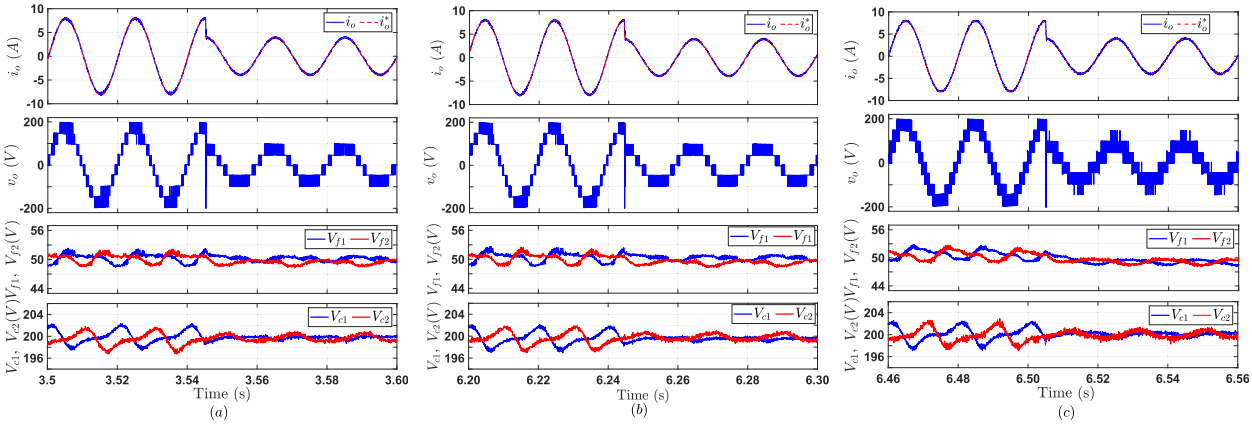

FIGURE 10. Experimental results for current step-change (8 A to 4 A): (a) Traditional FCS-MPC, (b) Single-predictive FCS-MPC, and (c) Proposed DB-MPC.

TABLE 4. Performance comparison at steady-state operation with nominal system parameters *R* and *L*.

Method	e_i	THD_i	THD_v	f_s
Traditional FCS-MPC	1.86%	2.92%	22.10%	2 kHz
Single-predictive FCS-MPC	1.88%	2.94%	22.05%	2 kHz
Proposed DB-MPC	1.61%	2.35%	23.44%	2 kHz

switching frequency, $f_s = 2$ kHz. Fig. 7 shows the experimental steady-state waveforms for the three methods at $i_o^* = 8$ A. The plotted waveforms, from top to bottom, are reference i_o^* and measured i_o currents, inverter voltage v_o, FCs measured voltages V_{f1} and V_{f2}, and dc-link measured voltages V_{c1} and V_{c2}. As it is clear for the three MPC schemes, i_o tracks i_o^* with high performance. v_o has nine steps in the fundamental cycle, reducing the voltage harmonic contents. The three MPC methods have balanced FCs with voltage ripples of 3.5 V. In addition, the capacitors of the dc-link are balanced with voltage ripples of 5 V. The spectrum of the current harmonics is shown in Fig. 8. As can be seen, all MPC methods have very low THDs, valued at 2.92%, 2.94%, and 2.35% for the traditional, single-predictive FCS-MPC, and the proposed DB-MPC, respectively. However, the harmonics in the traditional and single-predictive FCS-MPC methods are distributed over a wide frequency range, making filter design for grid-tied applications a challenging task. In contrast, for the DB-MPC method, the harmonics are concentrated at the carrier switching frequency and its multiples (f_c, $3f_c$, $5f_c$). Fig. 9 depicts the harmonics spectrum of v_o. Although the THD_v of the DB-MPC is slightly higher than that of FCS-MPC, it is concentrated at f_c and its multiples, which can be easily filtered, in contrast to the FCS-MPC. For a clear and supported performance assessment, Table 4 lists three performance indicators for all methods, which are the mean absolute current error e_i [29] and the total harmonic distortion THD_i and THD_v of i_o and v_o, respectively. According to Table 4, the developed DB-MPC method has better values in terms of e_i and THD_i. To examine the transient operation, Fig. 10 depicts the waveforms for a sudden change in i_o^* (from 8 A, 50 Hz to 4 A, 50 Hz). From the results, all MPC schemes have a fast dynamic response and a very effective FCs and NP balancing.

A 5-kW single-phase model of the considered inverter is built in the PLECS software tool to evaluate the efficiency and investigate the power loss distribution among the power devices under the MPC methods. The analysis is performed with $V_{dc} = 1$ kV and $i_o^* = 20$ A. The same power switches utilized in the experimental implementation are adopted in PLECS simulation, where FF50R12RT4 IGBT and IDP30E65D1 diode manufactured by *Infineon* are utilized with the thermal and losses description provided by the manufacturer. The resulting switching P_{sw} and conduction P_{con} losses are given in Fig. 11. Note that the four-quadrant switch S_8 consists of two power devices, denoted as S_8^1 and S_8^2. From Fig. 11, one can observe that the conduction losses of the power devices are much higher than the switching losses in all MPC schemes. In addition, the three MPC schemes have a very similar loss distribution, which can be interpreted as operating at the same average switching frequency. According to the loss analysis under the same conditions, the efficiency of the traditional, single-predictive FCS-MPC, and the DB-MPC is 98.93%, 98.91%, and 98.90%, respectively. An important observation from the power loss analysis is that the four-quadrant switch has the highest power loss compared to other switches, where S_8^1 and S_8^2 have about 32% of the total losses in the 9L-SC-ANPC inverter. This confirms the feasibility of the suggested DB-MPC strategy to ensure converter operation under the failure condition of the four-quadrant switch.

B. OPERATION UNDER PARAMETER MISMATCH AND EKF-BASED ESTIMATION

In this test, the robustness and the estimating ability of the EKF-based estimator with variations in parameters R and L are investigated. For the traditional and single-predictive FCS-MPC, the system model assumes constant parameters equal to the nominal values R_n and L_n. While for the proposed DB-MPC, the model parameters used in the control algorithm are estimated using the designed EKF-based estimator and denoted as $\hat{R}$ and $\hat{L}$. The variation of model

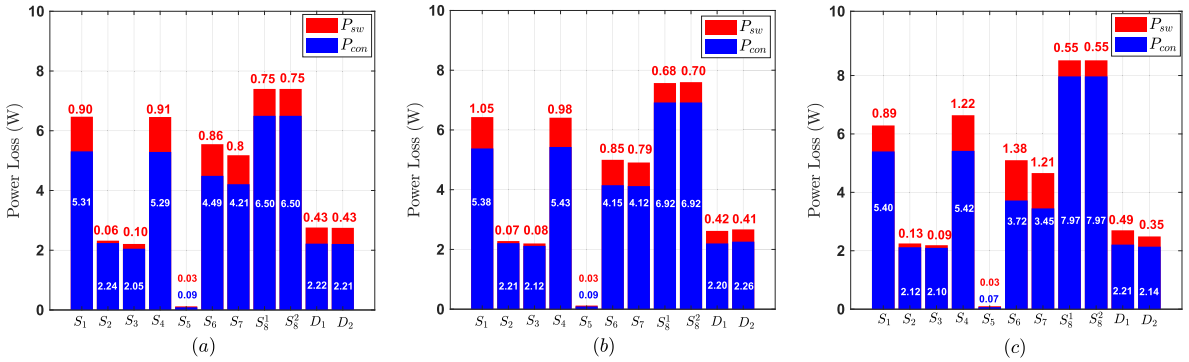

FIGURE 11. Conduction and switching losses of switches: (a) Traditional FCS-MPC, (b) Single-predictive FCS-MPC, and (c) Proposed DB-MPC.

TABLE 5. Performance comparison with a mismatch of −33.33% in R.

Method	e_i	THD_i	THD_v
Traditional FCS-MPC	3.23%	2.56%	25.50%
Single-predictive FCS-MPC	3.43%	2.67%	25.90%
Proposed DB-MPC	1.59%	2.30%	26.75%

parameters (ΔR, ΔL) is defined as

$$\Delta R = \frac{R_{act} - R_n}{R_n} \cdot 100,$$
$$\Delta L = \frac{L_{act} - L_n}{L_n} \cdot 100, \tag{39}$$

where R_{act} and L_{act} refer to the real values of the load resistance and filter inductance, respectively. Fig. 12 shows the experimental results for the change of the real system resistance between the nominal value (22 Ω) and another value (14.7 Ω), with a change percentage of 33.3%. As can be observed, for the proposed DB-MPC, the estimated resistance $\hat{R}$ follows the actual value $\hat{R}$ with a fast dynamic response and very low steady-state error. As a result, the control has high tracking quality in terms of current control despite the significant change in R_{act}. While for other FCS-MPC methods, due to the mismatch between R_{act} and R_n, a steady-state error is observed in the current. The control performance in this case in terms of e_i, THD_i and THD_v is summarized in Table 5. The control performance with filter inductance variation is depicted in Fig. 13, where L_{act} is varied from 6 mH to 2.4 mH ($\Delta L = -60\%$). As can be seen, the designed EKF-based estimator can accurately estimate the actual filter inductance, resulting in an acceptable control performance even with a −60% reduction in the filter inductance. For FCS-MPC, very high ripples are observed in the current and also the inverter voltage is highly distorted. The considered performance indicators are summarized in Table 6, which shows a clear superiority of the proposed DB-MPC over traditional and single-predictive FCS-MPC methods.

C. PERFORMANCE EVALUATION AT THE SAME CONTROL PERIOD T_S

As discussed in Section V-A, The performance of the MPC methods is compared at the same average switching frequency f_s, which necessitated the implementation of the

TABLE 6. Performance comparison with a mismatch of −60% in L.

Method	e_i	THD_i	THD_v
Traditional FCS-MPC	15.63%	28.16%	90.87%
Single-predictive FCS-MPC	17.82%	29.95%	91.87%
Proposed DB-MPC	3.92%	4.97%	20.30%

TABLE 7. Performance comparison at the same control period, $T_s = 50$ μs.

Method	Tuned Parameters	e_i	THD_i	THD_v	f_s
Traditional FCS-MPC	λ_1, λ_2	1.57%	2.42%	22.52%	2.35 kHz
Single-predictive FCS-MPC	$\lambda_{v1}, \lambda_{v2}$	1.62%	2.46%	22.18%	2.35 kHz
Proposed DB-MPC	-	1.61%	2.35%	23.44%	2 kHz

traditional and single predictive FCS-MPC methods at $T_s = 65$ μs to get $f_s = 2$ kHz as in the proposed DB-MPC method. In this section, the performance is compared at the same control period by experimentally implementing the traditional and single-predictive FCS-MPC methods at $T_s = 50$ μs. Fig. 14 shows the experimental waveforms of the FCS-MPC methods at $T_s = 50$ μs. The comparison between all MPC methods, in this case, is summarized in Table 7. Accordingly, all MPC strategies have almost similar values concerning the tracking error e_i, THD_i, and THD_v. Nevertheless, in contrast to DB-MPC, the harmonics in FCS-MPC methods are distributed over a wide frequency range, complicating the filter design, as previously discussed. In addition, the average switching frequency f_s of the two FCS-MPC methods is increased by 17.5%, 2.35 kHz compared to 2 kHz in the proposed DB-MPC method. No weighting factors are required in the proposed DB-MPC method. In contrast, two weighting factors are used in the FCS-MPC methods. Estimating the weighting factor is non-trivial and one of the ongoing research topics. Complex numerical models are usually required by performing numerous experiments and simulations under different operating conditions [30].

D. EXECUTION TIME

Computational load is one of the issues of MPC-based methods. To investigate this aspect, the execution times of traditional FCS-MPC and DB-MPC are measured on the same digital platform (dSPACE Microlabbox). The total required time for the implementation is monitored from ControlDesk by *turnaroundTime* variable. In addition, the time required to

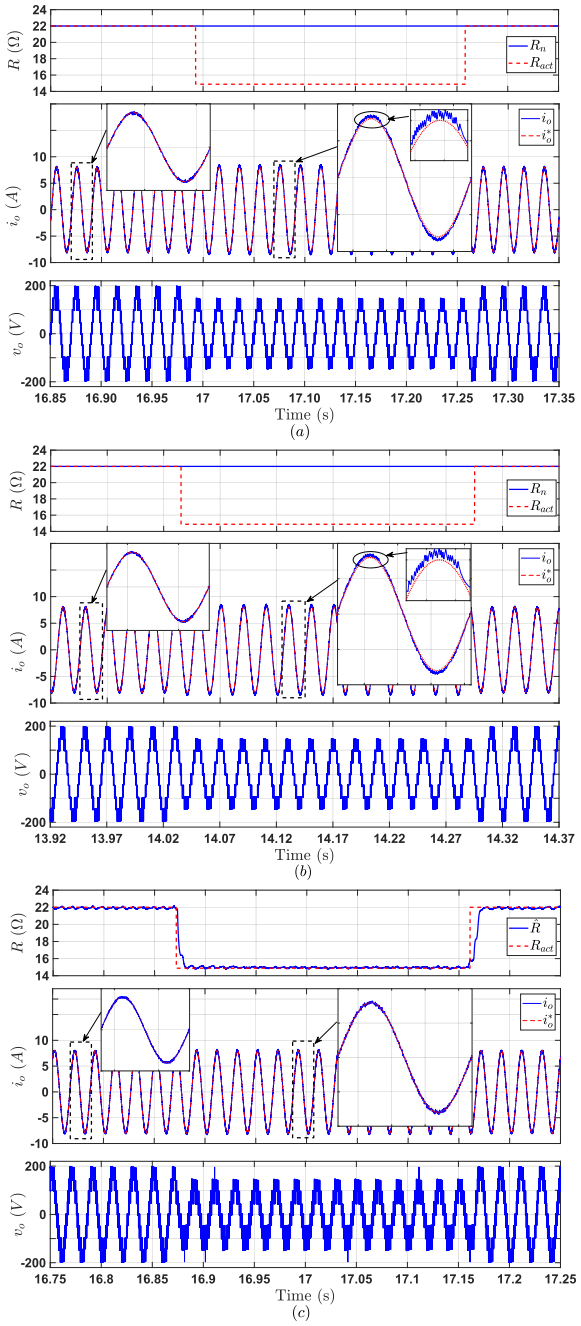

FIGURE 12. Experimental results for a mismatch in R: (a) Traditional FCS-MPC, (b) Single-predictive FCS-MPC, and (c) Proposed DB-MPC.

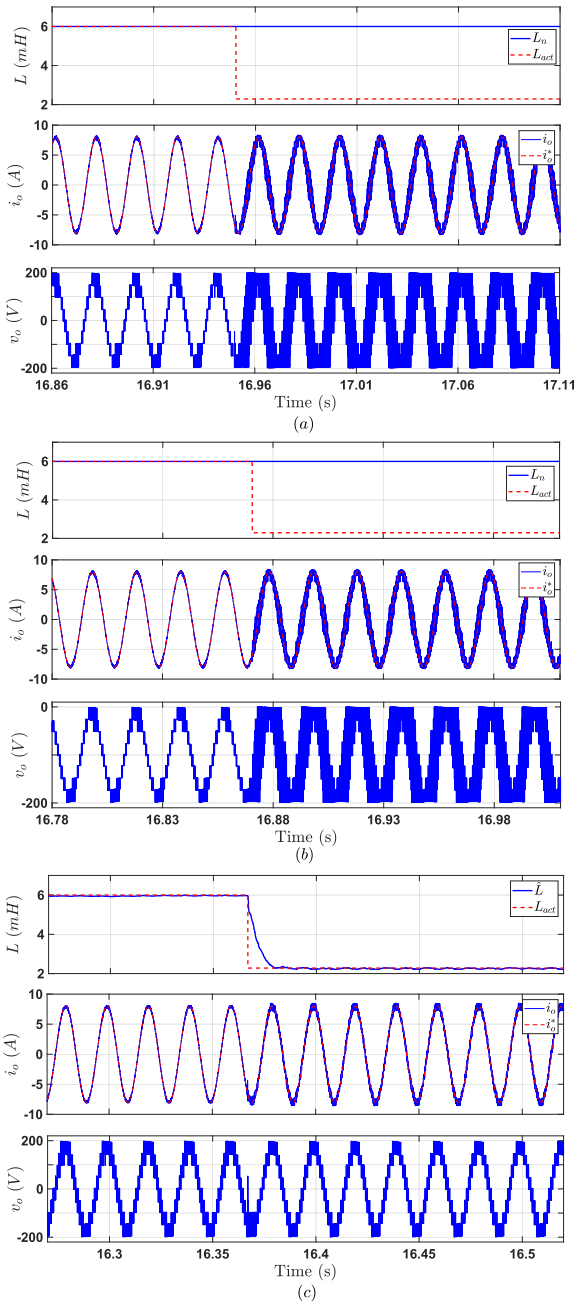

FIGURE 13. Experimental results for a mismatch in filter inductance L: (a) Traditional FCS-MPC, (b) Single-predictive FCS-MPC, and (c) Proposed DB-MPC.

execute algorithm sub-parts is also measured through *atomic subsystems*. The measured times of the three MPC methods are listed in Table 8. Accordingly, the suggested DB-MPC has a much shorter time for MPC code compared to FCS-MPC, where DB-MPC requires only 1.1 μs compared to 5.1 μs for the single-predictive FCS-MPC and 5.4 μs for traditional FCS-MPC. The reduction is achieved because, unlike FCS-MPC, neither current, FCs and dc-link voltage predictions nor cost function optimization are required. Although the designed EKF-based estimator is integrated into the proposed DB-MPC, the total execution time is still lower than the traditional method, where 11.1 μs is required for the whole developed DB-MPC method compared to 11.3 μs for traditional FCS-MPC.

E. OPERATION UNDER THE FAILURE OF THE FOUR-QUADRANT SWITCH S_8

As theoretically discussed, with the proposed DB-MPC, the 9L-SC-SNPC can continue to operate even in a failure condition of the four-quarter switch S_8. In this test, the operation is experimentally verified with an open-circuit fault in S_8. Fig. 15 shows the experimental results for this case. As can be

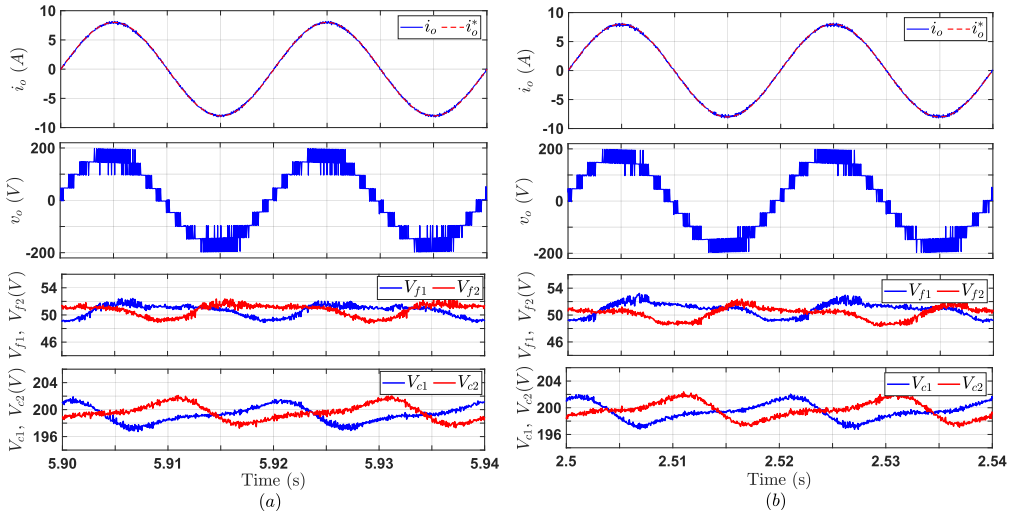

FIGURE 14. Experimental waveforms at T_S=50μs: (a) Traditional FCS-MPC, and (b) Single-predictive FCS-MPC.

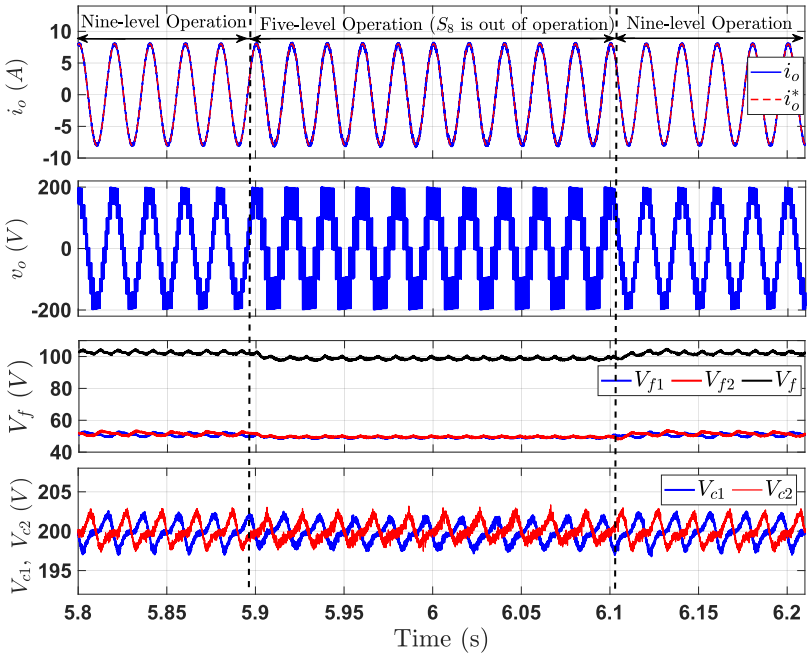

FIGURE 15. Experimental results of the proposed DB-MPC with a failure in the four-quadrant switch S_8.

seen, in normal operation, the inverter produces a nine-level voltage waveform, and when a fault occurred in S_8, the 9L-SC-ANPC was directly changed to the five-level mode with no transient time because the FCs were still stabilized at the same voltage. C_{f1} and C_{f2} are seen as on capacitor with a voltage V_f balanced at $V_{dc}/4$ (100 V). It is also clear that the dc-link capacitors are well balanced in all cases. The operation is also experimentally validated in the five-level mode with a step-change in i_o^* from 8 A to 4 A in Fig. 16. The results prove the ability of the proposed DB-MPC with the 9L-SC-ANPC topology to operate with a faulty state of S_8 in steady-state and dynamic operation. As expected, due to the reduction of the voltage levels to five, an increase is observed in the tracking errors and harmonic contents compared to the nine-level normal operation, where e_i, THD$_i$ and THD$_v$ were found to be 3.10%, 4.25% and 35.10%.

TABLE 8. Execution time of the traditional and proposed DB-MPC.

Method	Control Algorithm	EKF Algorithm	Time of Auxiliary Tasks	Total Time
Traditional FCS-MPC	5.40 μs	-	5.90 μs	11.30 μs
Single-predictive FCS-MPC	5.10 μs	-	5.90 μs	11 μs
Proposed DB-MPC	1.10 μs	4.10 μs	5.90 μs	11.10 μs

VI. CONCLUSION

In this article, an improved robust DB-MPC method was developed and applied to a recently proposed nine-level inverter. The proposed method is suitable for single-phase ANPC-based MLIs. From the theoretical investigations

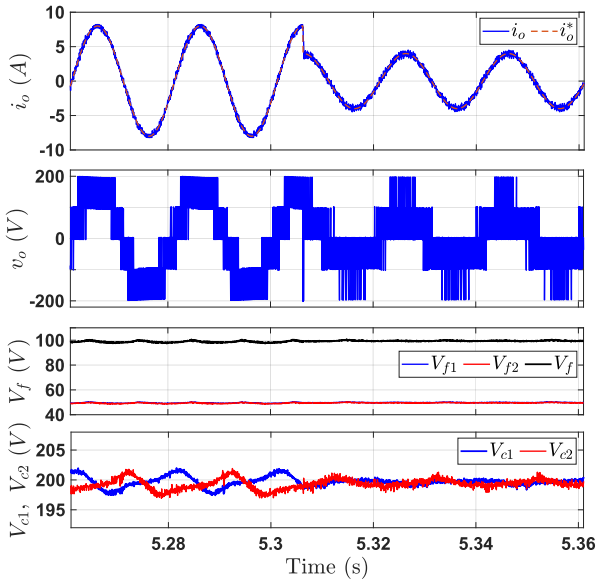

FIGURE 16. Experimental waveforms of the proposed DB-MPC in the five-level mode (open-circuit failure in S_8) with a current step-change.

and experimental results, the advantages of the proposed DB-MPC are summarized as follows:

1) Like the FCS-MPC, the proposed DB-MPC addresses multiple control goals; current control, FCs balance and NP potential control. Moreover, unlike FCS-MPC, no weighting factors are required, saving the cumbersome effort required to tune the weighting factors;
2) Thanks to the designed EKF-based estimator, the proposed method has better robustness compared to the traditional FCS-MPC;
3) Like the traditional FCS-MPC at the nominal system parameters, the proposed DB-MPC has high tracking quality and an effective balance of FCs and NP in steady-state and dynamic operation;
4) Comparing with FCS-MPC, the developed DB-MPC has a lower calculation burden;
5) The proposed DB-MPC scheme allows the 9L-SC-ANPC to continue operating with the generation of five levels in the open-circuit failure condition of the four-quadrant switch, improving the fault tolerance of the inverter.

Although the operation of the 9L-SC-ANPC is ensured under the faulty case of the four-quadrant switch S_8, it is suggested to investigate the operation under the fault conditions of other power switches in future work. In addition, the operation at low line frequencies is recommended to be considered in future work with ensuring the FCs and dc-link balance.

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