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RESEARCH ARTICLE

A Predictive Shortest-Horizon Voltage Control Algorithm for Non-Minimum Phase Three-Phase Rectifiers

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ABSTRACT Three-phase active front end rectifiers are a widely used power topology in applications such as renewable energy interfaces and motor drives, among many others. Its control is usually performed by a cascade combination of linear controllers which must be properly tuned for correct operation, and which depend on the operating point and system parameters. These family of controllers place inherent limits on the system dynamic response. On the other hand, the predictive control approach has been proposed as an alternative technique for these converters due to its fast dynamic response, simple concept, flexibility, multiple objective capability, among other desirable properties. In the case of power converter applications, short prediction horizons are usually used due to computational limitations. However, when short horizons are considered, the non-minimum phase characteristic of the rectifier voltage response can introduce stability issues, as its direct inversion is not possible without jeopardizing it. Indeed, this may lead to voltage regulation loss, and in the worst case, overcurrents that could damage the converter. To overcome such problem, this paper proposes a new concept for a predictive horizon one voltage controller for grid-connected three-phase active front end rectifiers. The proposal is based on the minimum and non-minimum phase plant factorization concept and the use of different sampling periods, to prevent the direct inversion of the non-minimum phase voltage dynamic. Simulated and experimental results are included and show its correct operation, even with a horizon one predictive voltage controller, thus ensuring the fastest response of the system for a given sampling time.

INDEX TERMS Active front end rectifier, model predictive control, non-minimum phase, voltage control.

I. INTRODUCTION

Model predictive control (MPC) can be regarded nowadays as a valid option for the control of power electronics systems [1]. Its properties such as simple concept, direct implementation in digital systems, flexibility to consider multiple control objectives and goals, and direct consideration of input constraints have made this technique an attractive alternative to conventional control techniques on these systems. In particular, Finite Control Set Model Predictive Control (FCS-MPC) [2], which exploits the discrete nature of the valid control inputs of power converters, has achieved much interest in the academic community [1].

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In spite of the many applications reported of FCS-MPC in power converters, open questions about these controllers remain. For instance, the issue of weighting factor selection [3], [4], switching frequency limitation/fixing [5], spread spectrum of electrical variables, stability issues, and computational complexity, just to name a few, are worthy of further study. In addition, the theoretical aspect of the behavior of these controllers is difficult when compared to the traditional schemes, which justifies the study of its behavior to gain intuitive understanding of their application.

Along these lines, it has been found that this control strategy poses some questions on its implementation on some power converter topologies. In fact, issues have been detected when FCS-MPC is used on systems that exhibit non-minimum phase (NMP) behavior [6], such as boost converters [7], [8], three-phase active-front-end (AFE) rectifiers [9], [10], and Z-source converters [11], in particular when short prediction horizons are considered. Due to computational constraints, most FCS-MPC applications use an horizon of one [2], i.e. they predict the behavior of the system only one sampling time ahead to generate the required control action.

On the other hand, three-phase AFE rectifiers are a widely used power conversion topology and building block [5], [12]. These converters are used in many applications such as ac drives, renewable energy interfaces, active filters, just to name a few [13], [14]. Their control is somewhat involved, due to their NMP behavior [6], which makes challenging the high performance controller design. In fact, this has led to its extensive study and many control strategies with different degrees of complexity and performance have been proposed [12] to tackle the issue. Among them, FCS-MPC appears as an interesting technique to achieve high performance control with its simple and intuitive concept.

The conventional control techniques used in AFE rectifiers can be categorized as voltage oriented control (VOC) or direct power control (DPC) schemes [12]. In VOC schemes, an inner input current loop is considered, where the converter gating signals are usually generated through a modulation scheme. In contrast, DPC schemes use an inner power loop where the switches actuation signals are directly generated. Both schemes employ an outer voltage loop to control the rectifier output voltage, usually a proportional-integral (PI) controller [12], [15], in a cascade or master-slave configuration.

At present, FCS-MPC in AFE rectifiers has resulted in at least the following methods: model predictive current control (MPCC), model predictive virtual flux control (MPVFC), model predictive direct power control (MPDPC), and model predictive virtual flux direct power control (MPVFDPC) [16]. These schemes are based on the same basic prediction concept, however each one uses different cost functions, thus resulting in different performance, particularly when operating under distorted and/or unbalanced grid voltages. In particular, FCS-MPC looks like a natural match to the DPC concept, as it allows to replace the table normally required by these controllers by using a prediction model instead.

Recent developments of FCS-MPC in AFE rectifiers include improving its switching frequency behavior [5], [13], [17], current quality [5], and the study of the system operation under unbalanced/distorted grid voltages [18], [19]. In these last two works, even sensorless operation, which do not require grid voltage sensors, has been considered. To address the variable switching frequency and improve the current quality, [5] proposes a virtual vector approach with a predictive current controller in a dq reference frame. The method uses a current-based cost function, where three additional virtual voltage vectors are evaluated, in addition to the basic and reference ones. If required, these virtual vectors are applied using a space vector modulation approach. On the other hand, [13] proposes a predictive direct duty-cycle method, where duty cycles associated to the non-zero and zero vectors for each sampling period are calculated based on the minimum value of a power error cost function. The method applies two voltage vectors each sampling period, fixing the switching frequency. Another power error based approach with duty cycle optimization is presented in [17]. A grid voltage sensorless model predictive power controller with two-vector duty cycle optimization is proposed in [18], where system operation under unbalanced and distorted grid conditions is explicitly considered. Another sensorless approach is proposed in [19], where this time a neural network estimator is used, and the gating signals are generated by a space vector modulator.

From the previous literature review, it is apparent that the NMP characteristic of the voltage control problem in three-phase AFE rectifiers is not a widely studied topic. Recently, [6] has provided a detailed study of the NMP zeros of voltage source converters when connected to a weak grid, concluding that large grid impedance and active power lead to greater importance of these zeros. Also, [20] has analyzed the effect of the voltage and current controller gains on the rectifier system stability considering the right half plane (RHP) zero of the d-axis current to output voltage transfer function. Although the conventional cascaded control approach is a simple yet effective way to naturally impose limits to the control loop gain, preventing the instability of the internal dynamics of the system due to its NMP behavior, and also to impose maximum transient current/power limits, it also reduces the achievable performance of the closed-loop system and makes controller tuning difficult.

MPC based schemes do not demand or require the use of a cascade configuration, potentially allowing to directly take into account the operating constraints and bandwidth limitations. Some previous approaches to use MPC for voltage control in AFE rectifiers are [9] and [10]. The work [9] proposes a voltage controller based on the design of a compatible power reference, where the final switching state is selected by the minimization of a power cost function. A power differential term is added to compensate possible steady state error due to losses. Meanwhile, [10] uses a dynamic power reference as well, however the generation method is different. In fact, the power reference is designed to reach the voltage one in

N steps. Then, the converter state is obtained optimizing a cost function with power and voltage terms. Recently, [15] has proposed a generalized predictive control voltage controller for fast response and disturbance rejection, noting the requirement of a long horizon for voltage control, however not much attention has been paid to the NMP behavior of the system.

On the other hand, the control literature has introduced methods to deal with NMP plants. In fact, concepts such as approximate inversion [21], [22], plant factorization [23], and sampling [24], [25], [26] have been successfully used in the control of NMP systems. However, to the author's knowledge, these methods have not been widely applied to power converters, neither in conventional or predictive controllers. Based on these concepts, this work proposes a different predictive approach to the three-phase AFE rectifier voltage control. The main contributions of this work are: (i) the origin of the inability of horizon one FCS-MPC to directly control the output voltage of the three-phase AFE rectifier is studied and intuitively explained, and (ii) a working short prediction horizon predictive voltage controller with a limited computational burden is proposed. To deal with the NMP behavior of the rectifier, the proposed MPC controller uses a minimum-phase prediction model together with exploiting consequences of the sampling process. As a result, a completely discrete and very simple control scheme is obtained, which does not use a multistep prediction, does not require a modulator, does not use an outer PI controller, and also features a good dynamic tracking performance for voltage regulation.

This paper is organized as follows: Section II shows a general introduction to FCS-MPC in power converters and the problem of using short prediction horizons in NMP plants. Section III presents the rectifier system model and applies short horizon FCS-MPC to it, illustrating the issue. Section IV presents the proposed control technique, together with its design. Section V applies the proposed technique to the system, comparing its performance to a conventional power control. Section VI experimentally verifies the proposal. The main conclusions of the work are presented in Section VII and VIII.

II. FINITE CONTROL SET MODEL PREDICTIVE CONTROL IN POWER CONVERTERS

The FCS-MPC control algorithm [1], [2] is based on the optimization of a cost function which depends on a model of the system and is designed to meet desired goals. For instance, in power electronics applications the tracking of current and/or voltage references is usually considered. These are, or directly depend on, the state variables of the power converter system. A key aspect of predictive control in power electronics applications is that the actuation depends on the on-off nature of the power valves. In turn, this means that the control input values are constrained to be in a finite or quantized set.

A. BASIC CONCEPT

The algorithm's operation in the single-input single-output (SISO) setting could be explained as follows. Starting from a continuous-time model of the system, derived from physical and circuit laws, a suitable discrete-time model is obtained which can be described in the form:

$$\mathbf{x}_{k+1} = \mathbf{f}(\mathbf{x}_k, u_k, \mathbf{p}_k), \tag{1}$$

$$y_k = h(\mathbf{x}_k, u_k, \mathbf{p}_k), \tag{2}$$

where $\mathbf{x}_k$ is the state vector, u_k the input, $\mathbf{p}_k$ the disturbance vector, and y_k the output, all at time k. Vector function $\mathbf{f}$ and function h represent the state function and output map, respectively.

The control problem is to determine at each sampling time the input value u_{k+1} that must be applied at the next sampling time to track a desired reference y^{ref}_{k+2}. In order to select the input u_{k+1} that best follows the reference, a cost function g is minimized each sampling time. A quadratic type cost function is usually used:

$$g_{k+2} = \left(y^{\text{ref}}_{k+2} - y_{k+2}\right)^2. \tag{3}$$

The aforementioned is required because the cost function g_{k+1} is already determined at current time k, since the input has already been defined at the previous sampling time. To take into account this intrinsic delay a compensation is performed [27], using the model (1)-(2) to predict the state values at $k+1$ and optimizing the cost function at time $k+2$. The input is then calculated as:

$$u_{k+1} = \arg\min_{u \in U} g_{k+2}(u), \tag{4}$$

where u is the currently evaluated input value, and U the set of valid input values. As the minimization is performed predicting the output value one sampling time ahead, this is a horizon one predictive controller. A short prediction horizon is desired in power electronics applications due to the small calculation time available, given the fast sampling times usually required.

If multiple control goals are desired, it is usual to construct an aggregate cost function as a linear combination of single ones, one for each desired control goal [3]. For instance, for two objectives:

$$g_{k+2} = k_1 g^1_{k+2} + k_2 g^2_{k+2}, \tag{5}$$

where g^1, g^2 are the cost functions associated to each goal and k_1, k_2 are positive scalar values called weighting factors. The algorithm then optimizes the value of this cost function over the available input values.

Finally, the complete algorithm can be summarized by the block diagram shown in Fig. 1. The controller requires the system states at time k in order to perform the predictions, in addition to the measurable or estimated disturbances $\mathbf{p}_k$.

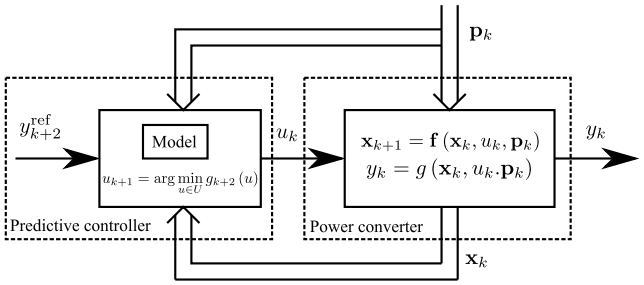

FIGURE 1. Block diagram of Finite Control Set Model Predictive Control as used in power converters.

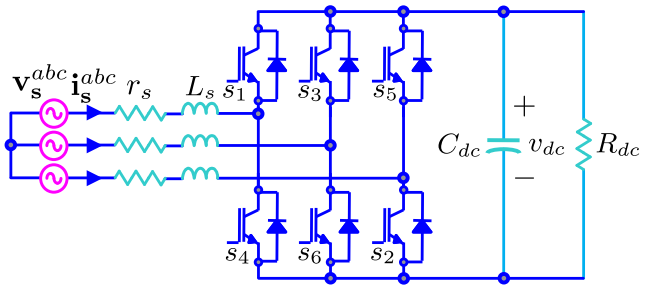

FIGURE 2. Three-phase active-front-end rectifier topology.

B. BEHAVIOR WITH NON-MINIMUM PHASE PLANTS

As previously discussed, FCS-MPC has already been used in many power converter topologies and applications with promising results. However, some power converters such as three-phase AFE rectifiers, could show non-minimum phase behavior [6] in their input-output characteristic. This is reflected as a transient undershoot in the system output, and may lead to undesired effects when closed loop control is sought. In fact, consider the following unconstrained, nonlinear and affine in the input SISO plant defined by:

$$\mathbf{x}_{k+1} = \mathbf{f}(\mathbf{x}_k) + \mathbf{g}(\mathbf{x}_k)u_k, \tag{6}$$

$$y_k = x_{2k}, \tag{7}$$

where $\mathbf{x}_k = [x_{1k}\, x_{2k}]^T$, $\mathbf{f}(\mathbf{x}_k) = [f_1(\mathbf{x}_k) f_2(\mathbf{x}_k)]^T$, and $\mathbf{g}(\mathbf{x}_k) = [g_1(\mathbf{x}_k) g_2(\mathbf{x}_k)]^T$. Predictive control minimizes each sampling time its specified cost function. Then, in the unconstrained case it can be assumed that the control input u_k completely minimizes the cost function:

$$g = \left(x_2^{\text{ref}}{}_k - x_{2k+2}\right)^2, \tag{8}$$

where $x_2^{\text{ref}}{}_k$ is the reference value for x_2 at time k. Total minimization of the cost g means that it is zero, and replacing the input value, assuming that a perfect model is available, results in the following closed loop dynamics:

$$z_{1k+1} = x_2^{\text{ref}}{}_k = y_k^{\text{ref}}, \tag{9}$$

$$x_{1k+1} = f_1(\mathbf{x}_k) - \frac{g_1(\mathbf{x}_k) f_2(\mathbf{x_k})}{g_2(\mathbf{x}_k)} + \frac{g_1(\mathbf{x}_k)}{g_2(\mathbf{x}_k)} z_{1k}, \tag{10}$$

$$x_{2k+1} = z_{1k}, \tag{11}$$

$$y_k = x_{2k}. \tag{12}$$

It can be observed that the predictive control law makes the system output $y_k = x_{2k}$ follow its reference at most two sampling times ahead as $x_{2k} = z_{1k-1} = y^{\text{ref}}_{k-2}$. Thus, the input u_k generated by this controller when applied to the system completely inverts its input-output dynamics, also adding a delay of two sampling times.

To study the implications of this plant inversion mechanism a linear SISO system can be considered. For instance, let a continuous-time system be represented in the s domain by a given transfer function $h(s)$. The relationship between its input u and its output y in the s domain is:

$$y(s) = h(s)u(s). \tag{13}$$

Then, given a desired output y_{ref}, assuming that the model $h(s)$ is known, and considering the plant inversion mechanism, the required system input $u_{req}(s)$ can be obtained as:

$$u_{req}(s) = h_{inv}(s) y_{ref}(s), \tag{14}$$

where $h_{inv}(s) = h(s)^{-1} h_f(s)$ is the inverse of transfer function $h(s)$ multiplied by a filter $h_f(s)$ to obtain a realizable implementation. From this analysis it can be concluded that if $h(s)$ has zeros in the right-hand plane (i.e. $h(s)$ is non-minimum phase), then its inverse will have unstable poles. Without loss of generality, this analysis also applies to the discrete-time case, as the continuous-time zeros can be directly mapped to a subset of the equivalent discrete-time system zeros [28]. Then, if the controller operates under this plant inversion principle, as is the case of a short-horizon predictive controller, undesirable results will be obtained. In fact, this situation leads to control issues in AFE rectifiers, as will be shown in the following.

III. FCS-MPC DIRECT VOLTAGE CONTROL PROBLEM IN AFE RECTIFIERS

Horizon one FCS-MPC has already been applied to control AFE rectifiers. Indeed, [29] presents a predictive direct power control for this topology where the output voltage is controlled by a conventional PI controller. The work only uses the predictive controller as an inner power loop, and instead uses a PI controller to generate the appropriate input power reference. However, the PI controller places limits on the dynamic behavior of the system and is usually difficult to tune. Arguably, a completely predictive controller would have a faster response and be a simpler alternative, directly controlling the voltage through the cost function. Nevertheless, issues arise with this naive horizon one FCS-MPC output voltage control strategy, which will illustrated in this section.

A. THREE-PHASE AFE RECTIFIER MODEL

The three-phase AFE rectifier topology is shown in Fig. 2, where an inductive L type filter L_s with parasitic resistance r_s is used to couple the converter to the grid. The rectifier is supplied by a stiff grid with low but unknown impedance that is assumed lumped in the voltage waveform, and thus can be neglected. A natural abc-frame continuous-time model can be obtained using the corresponding circuit laws and

input-output power balance equations [9], [10]. The model is given by:

$$\frac{d\mathbf{i}_\mathbf{s}^{abc}}{dt} = -\frac{r_s}{L_s}\mathbf{i}_\mathbf{s}^{abc} + \frac{1}{L_s}\mathbf{v}_\mathbf{s}^{abc} - \frac{1}{L_s}\mathbf{T}_\mathbf{ln}\mathbf{s}_\mathbf{r}^{abc}v_{dc}, \quad (15)$$

$$\frac{dv_{dc}}{dt} = -\frac{v_{dc}}{C_{dc}R_{dc}} + \frac{\mathbf{s}_\mathbf{r}^{abcT}\mathbf{T}_\mathbf{ln}^T\mathbf{i}_\mathbf{s}^{abc}}{C_{dc}}, \quad (16)$$

with

$$\mathbf{T}_\mathbf{ln} = \frac{1}{3}\begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix}, \quad (17)$$

and where $\mathbf{i}_\mathbf{s}^{abc}$ is the input current, $\mathbf{v}_\mathbf{s}^{abc}$ the grid voltage, $\mathbf{s}_\mathbf{r}^{abc} = [s_1\ s_3\ s_5]^T$ the rectifier switching functions vectors, all in the *abc* reference frame, and v_{dc} the rectifier output voltage. The system parameters are: L_s the rectifier's inductive filter, r_s its associated parasitic resistor, C_{dc} the dc-link capacitance, and R_{dc} a resistor which represents the converter load.

One of the input currents is linearly dependent of the other two, as it is a three-wire system, moreover, a balanced three-phase circuit is assumed. Then, it is convenient to use an $\alpha\beta 0$ reference frame. Applying the transformation defined by:

$$\mathbf{T}_{abc-\alpha\beta 0}\sqrt{\frac{2}{3}}\begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \\ 1/\sqrt{2} & 1/\sqrt{2} & 1/\sqrt{2} \end{bmatrix}, \quad (18)$$

the model in the $\alpha\beta 0$ frame is given by:

$$\frac{d\mathbf{i}_\mathbf{s}^{\alpha\beta 0}}{dt} = -\frac{r_s}{L_s}\mathbf{i}_\mathbf{s}^{\alpha\beta 0} + \frac{1}{L_s}\mathbf{v}_\mathbf{s}^{\alpha\beta 0} - \frac{1}{L_s}\mathbf{s}_\mathbf{r}^{\alpha\beta 0}v_{dc}, \quad (19)$$

$$\frac{dv_{dc}}{dt} = -\frac{v_{dc}}{C_{dc}R_{dc}} + \frac{\mathbf{s}_\mathbf{r}^{\alpha\beta 0T}\mathbf{i}_\mathbf{s}^{\alpha\beta 0}}{C_{dc}}, \quad (20)$$

where $\mathbf{i}_\mathbf{s}^{\alpha\beta 0}$, $\mathbf{v}_\mathbf{s}^{\alpha\beta 0}$, and $\mathbf{s}_\mathbf{r}^{\alpha\beta 0}$ are the transformed vectors in the $\alpha\beta 0$ frame. Given the previous assumptions, the zero components are nil, and consequently, neglected in the following analyses.

A discrete-time prediction model for predictive control purposes can be obtained by a forward Euler discretization [2] of (19)-(20), resulting in:

$$\mathbf{i}_\mathbf{s}^{\alpha\beta}{}_{k+1} = \left(1 - \frac{r_sT}{L_s}\right)\mathbf{i}_\mathbf{s}^{\alpha\beta}{}_k + \frac{T}{L_s}\mathbf{v}_\mathbf{s}^{\alpha\beta}{}_k - \frac{T}{L_s}\mathbf{s}_\mathbf{r}^{\alpha\beta}{}_k v_{dck}, \quad (21)$$

$$v_{dck+1} = \left(1 - \frac{T}{C_{dc}R_{dc}}\right)v_{dck} + \frac{T}{C_{dc}}(\mathbf{s}_\mathbf{r}^{\alpha\beta}{}_k)^T\mathbf{i}_\mathbf{s}^{\alpha\beta}{}_k, \quad (22)$$

where T is the sampling time.

B. HORIZON ONE FCS-MPC IN THE AFE RECTIFIER

The main control objectives in AFE rectifiers are the voltage regulation at the dc side, while at the same time, taking sinusoidal currents in phase with the ac mains voltage. To achieve these objectives with a predictive controller a suitable cost function must be specified, which defines the controller behavior. As previously remarked, this section will illustrate the issue that may arise when using horizon one FCS-MPC for these purposes.

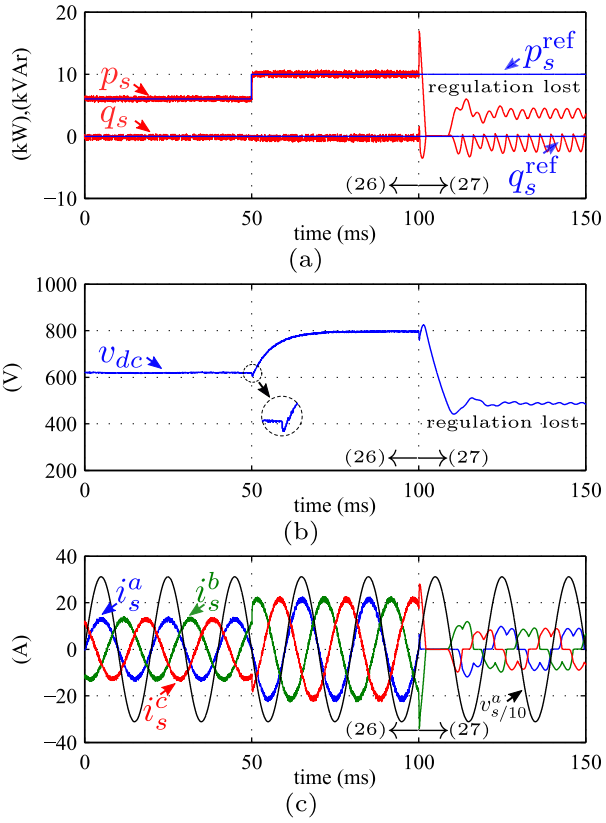

FIGURE 3. Transition from power-based cost function to the voltage-based one, eqs. (26) and (27). (a) instantaneous input active and reactive powers, p_s and q_s; (b) dc output voltage, v_{dc}; and (c) ac mains currents $\mathbf{i}_\mathbf{s}{}^{abc}$.

1) PREDICTIVE POWER CONTROL

One way to achieve the aforementioned objectives is to use a power based cost function, such as in [29]. The instantaneous active power at the rectifier ac mains side is given by:

$$p_s = v_s^\alpha i_s^\alpha + v_s^\beta i_s^\beta. \quad (23)$$

On the other hand, the instantaneous reactive power is:

$$q_s = -v_s^\beta i_s^\alpha + v_s^\alpha i_s^\beta. \quad (24)$$

A suitable cost function can be constructed from these definitions as:

$$g_{k+2} = \left(p_s^{\text{ref}}{}_{k+2} - p_{sk+2}\right)^2 + \left(q_s^{\text{ref}}{}_{k+2} - q_{sk+2}\right)^2. \quad (25)$$

Usually unitary power factor operation is desired $q_s^{\text{ref}}{}_{k+2} = 0$, hence, the cost function can be reduced to:

$$g_{k+2} = \left(p_s^{\text{ref}}{}_{k+2} - p_{sk+2}\right)^2 + \left(q_{sk+2}\right)^2. \quad (26)$$

A natural advantage of this cost function is that the active and reactive power are of the same nature and equally important, thus no weighting factors tuning is required for its correct operation.

The cost function (26) only addresses the control of the converter's active and reactive powers. To complete the scheme an outer voltage controller is required. Indeed, the reactive power is directly controlled by the cost function, but the voltage is only indirectly controlled by the active power reference. A simple solution is to use a PI voltage controller, however, this limits the output voltage dynamic response.

2) PREDICTIVE VOLTAGE CONTROL

Arguably, a more direct way to control the voltage would be to directly include it in the predictive controller cost function. For instance, to simultaneously control the output voltage and the input reactive power, the following cost function could be considered:

$$g_{k+2} = k_v \left(v_{dc\,k+2}^{\text{ref}} - v_{dck+2} \right)^2 + k_q \left(q_{sk+2} \right)^2, \qquad (27)$$

where $k_v, k_q \in \mathbb{R}^+$ are weighting factors that assign the priority of each controlled variable.

As this cost function does not directly includes a power limit in the selection of the switching state, additional logic should be included to prevent a dangerous operating condition. In the present work, it is proposed that the state minimizing the cost function (27) is selected only if it results in a input power value lower than a preset limit. Otherwise, the nearest state that minimizes the cost function and meets the power limit is selected. If there are no suitable states, i.e. every state results in a higher than the limit power value, the topology should be tripped and all gating pulses disabled.

3) SIMULATION STUDY

To illustrate the behavior of horizon one FCS-MPC in the AFE rectifier with the proposed power-based and voltage-based cost functions a simulation will be considered. The controller's cost function in the proposed test, which defines the state of the switches, will be changed from (26) to (27) while at a given operating point. The simulation is performed in PSIM using a rms ac mains phase voltage $V_s = 220$ (V) at 50 (Hz), with input filter $L_s = 10$ (mH), $r_s = 0.1$ (Ω), dc-link capacitor $C_{dc} = 200$ (μF), load resistor $R_{dc} = 64$ (Ω), and sampling time $T = 50$ (μs). A high inductance value, such as 10 (mH), is useful to emphasize the effects of the non-minimum phase phenomena in the power converter's control. The results are presented in Fig. 3.

The operation of the system depicted in Fig. 3 is as follows. From $t = 0$ to 50 (ms), the system operates under the power-based cost function (26) with a power reference of 6 (kW), which is correctly tracked, as shown in Fig. 3 (a). This results in an output voltage of approximately 620 (V), Fig. 3 (b), which is higher than the limit condition imposed by the topology. The input currents, Fig. 3 (c), are in phase with the mains voltage, as desired. At $t = 50$ (ms) the power reference is increased to 10 (kW), and the controller correctly tracks the new condition, Fig. 3 (a), which in turn increases the input current magnitude, Fig. 3 (c). The output voltage goes to 800 (V) after approximately 25 (ms), as expected with the increase of the power drawn from the grid.

Afterwards, at $t = 100$ (ms), and already operating at an output voltage of around 800(V), the system changes to the voltage cost function (27) with a reference of 800(V). A value of $k_q = 0$ is used, meaning that the controller will only try to control the output voltage, ignoring the input reactive power. It is expected that after the cost function change the input power will fluctuate around the same value, settling towards it after a brief transient. However, as shown in Fig. 3 (a), after the input power limit is reached (set at 20 (kW)), no suitable switching states are available and the protection is activated. As the gating pulses are disabled, the output capacitor discharges, Fig. 3 (b). From the results, it can be concluded that with this cost function the controller is unable to track the desired voltage reference.

IV. PROPOSED VOLTAGE CONTROL APPROACH

As illustrated in the previous section, a direct horizon one FCS-MPC voltage control does not behaves correctly in the three-phase AFE rectifier. In order to address this issue, also eliminating the conventional voltage PI controller, an alternative approach is proposed in this work. The new method, also a short horizon predictive voltage control, utilizes properties of the sampling process together with the minimum-phase system concept to enable a successful predictive voltage control. The proposed algorithm is illustrated in Fig. 4 and will be described in the following.

A. NMP BEHAVIOR OF THE POWER-VOLTAGE TRANSFER FUNCTION

From the simulation study and previous reported research, a short horizon FCS-MPC power controller allows a very fast power reference tracking. Indeed, a nearly perfect dynamic plant inversion is possible as observed in Section III. On the other hand, the simulation results show that a direct horizon one predictive voltage control is not trivial to achieve.

A first approach to a fast voltage control is to utilize a horizon one predictive controller to generate the required power reference. To achieve this objective an input power - output voltage discrete-time dynamic model is required. According to [9], the continuous-time input power - output voltage dynamic is given by:

$$p_s - \frac{L_s}{\mathbf{v_s}^{abcT}\mathbf{v_s}^{abc}} \left(p_s \frac{dp_s}{dt} + q_s \frac{dq_s}{dt} \right) - \frac{r_s}{\mathbf{v_s}^{abcT}\mathbf{v_s}^{abc}} \left(p_s^2 + q_s^2 \right) = C_{dc} v_{dc} \frac{dv_{dc}}{dt} + \frac{v_{dc}^2}{R_{dc}}, \qquad (28)$$

where for a balanced three-phase voltage set $\mathbf{v_s}^{abcT}\mathbf{v_s}^{abc} = (3/2)V_s^2$, with V_s the phase voltage amplitude. In addition, a small signal linear model can be obtained from the previous equation, which results in the following s-plane transfer function:

$$h_{vdc-ps}(s) = \frac{\Delta v_{dc}(s)}{\Delta p_s(s)} = k \frac{s + z_{vdc}}{s + p_{vdc}}, \qquad (29)$$

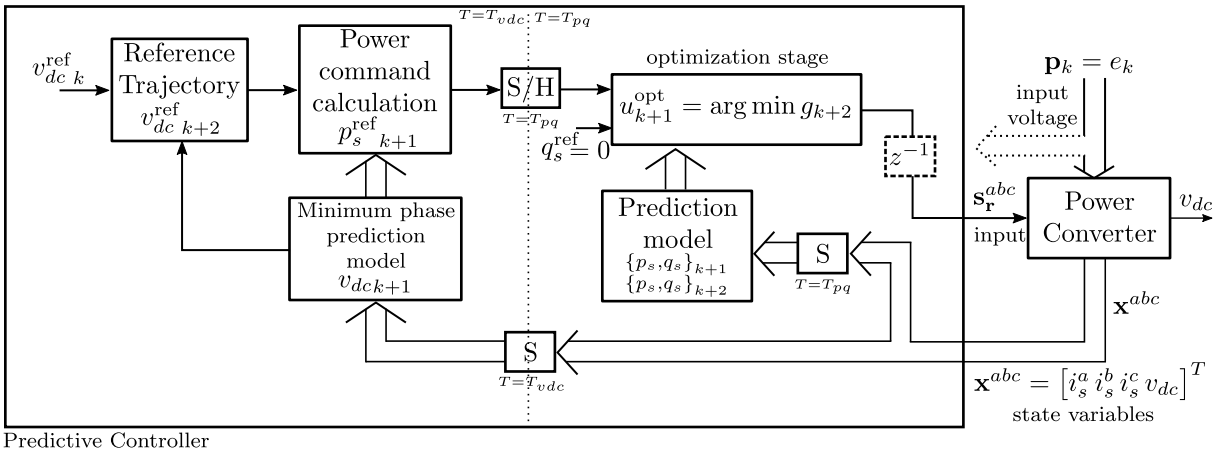

FIGURE 4. Proposed predictive controller block diagram.

where $k = -2L_sP_{so}/(3C_{dc}V_{dc}V_s^2)$, and

$$z_{vdc} = -\left(\frac{3V_s^2}{2P_{so}L_s} - \frac{2r_s}{L_s}\right), \quad p_{vdc} = \frac{2}{R_{dc}C_{dc}}, \tag{30}$$

with P_{so} is the input power at the operating point.

Transfer function (29), which locally models the dynamic relationship between the output voltage and the input power, has a RHP zero as expected from the voltage response of the horizon one FCS-MPC power controller, Fig. 3. When a step change in the power reference is commanded, a transient undershoot appears in the voltage response. As the system shows NMP behavior, a naive model inverting short horizon predictive controller involves an unstable internal dynamic, so it is not possible to implement in practice, and additional development is required.

B. MINIMUM-PHASE PREDICTION MODEL

To solve the issue and to achieve a working short horizon predictive voltage controller, the present work proposes a plant factorization approach to prevent the inversion of the non-invertible parts of the dynamics. This means that the plant is separated in invertible and non-invertible parts, i.e. minimum and non-minimum phase parts, respectively. Then, the predictive voltage controller only controls the minimum phase, invertible part.

In linear systems there are many ways in order to factor a non-minimum phase model into minimum and non-minimum phase parts [21], [22]. However, due to the fact that (28) is a nonlinear plant, they cannot be used directly. The factorization problem in nonlinear non-minimum phase systems is considerably more difficult [23]. Among the options used for linear systems is the NPZ-ignore method [21]. The key concept behind this approach is to ignore the right-half plane zero altogether in the controller design.

Based on the previous idea, a nonlinear prediction model will be generated that does not show the undesired behavior, and thus is minimum phase and invertible. Analyzing the model (28) and the transfer function (29), it can be noted that the zero is related to the power derivative, which is the input. This is a structural consequence of the need to charge the inductors to transfer the energy towards the output. A convenient approximation is to consider that the predictive power controller tracks the reference faster than the voltage loop sampling time. This enables the elimination of the power derivative from the nonlinear system equation (28), removing the undesired dynamic coupling, thus eliminating the RHP zero in the linearized model. The resulting approximate model is:

$$p_s - \frac{L_s}{\mathbf{v}_\mathbf{s}^{abcT}\mathbf{v}_\mathbf{s}^{abc}}\left(q_s\frac{dq_s}{dt}\right) - \frac{r_s}{\mathbf{v}_\mathbf{s}^{abcT}\mathbf{v}_\mathbf{s}^{abc}}\left(p_s^2 + q_s^2\right) = C_{dc}v_{dc}\frac{dv_{dc}}{dt} + \frac{v_{dc}^2}{R_{dc}}. \tag{31}$$

In addition, q_s and its derivative could be removed, as they are directly controlled by the internal predictive power controller and only act as disturbances. This means that the model can be further simplified to:

$$p_s - \frac{r_s}{\mathbf{v}_\mathbf{s}^{abcT}\mathbf{v}_\mathbf{s}^{abc}}p_s^2 = C_{dc}v_{dc}\frac{dv_{dc}}{dt} + \frac{v_{dc}^2}{R_{dc}}. \tag{32}$$

This approximate model has the same steady state behavior as the original nonlinear model, but does not have the undesired NMP behavior.

To verify the agreement of the proposed minimum-phase model with the true output voltage response a simulation study is performed. The system and the model are subjected to step changes in the input power reference. The results, presented in Fig. 5 (a), show that the approximate response has no undershoot and coincides in steady-state with the true voltage output. In addition, the approximation error is small for the proposed model. Indeed, the true response is almost indistinguishable from the approximate one without the undershoot delay.

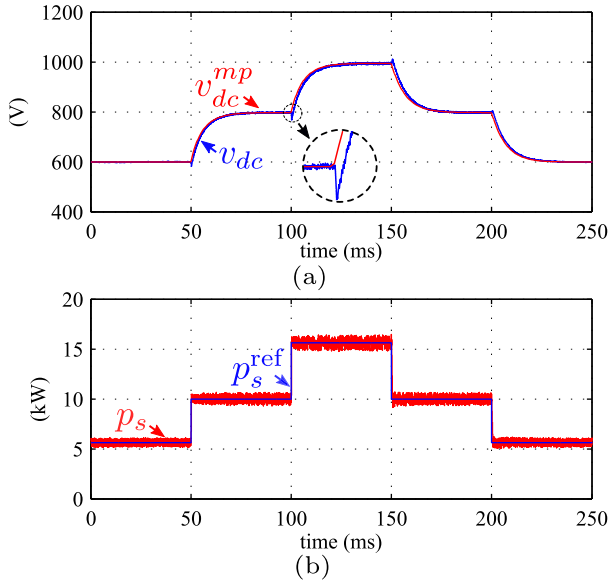

FIGURE 5. Approximate minimum-phase input power - output voltage model. (a) true output voltage v_{dc} (blue) and approximate model v_{dc}^{mp} (red); (b) converter active input power p_s (red) and command p_s^{ref} (blue).

A nonlinear discrete-time model can be obtained from (32) using the Euler approximation of the derivative:

$$\frac{dv_{dc}}{dt} \approx \frac{v_{dck+1} - v_{dck}}{T_{vdc}}, \tag{33}$$

where T_{vdc} is the voltage loop sampling time. The resulting nonlinear prediction model for the voltage v_{dc} is:

$$v_{dck+1} = \frac{T_{vdc}}{C_{dc}} \frac{1}{v_{dck}} \left(p_{sk} - \frac{2r_s}{3V_s^2}(p_{sk})^2 - \left(\frac{1}{R_{dc}} - \frac{C_{dc}}{T_{vdc}} \right) (v_{dck})^2 \right), \tag{34}$$

where the variables p_{sk} and v_{dck} are measured for the current sampling time.

C. GENERATION OF MINIMUM-PHASE OUTPUT

The proposed model only partially solves the difficulties of horizon one predictive voltage control. In particular, the dynamic response of the model is only a minimum-phase approximation of the real voltage response. This means that the predictive controller should not be directly fed back the original NMP voltage variable. If this is not the case, the RHP zero of the voltage dynamic will be fed back and considered in the model inversion, leading to internal instability. Instead, a suitable way to map the real NMP response to the minimum-phase model approximation must be found.

The aforementioned output voltage compensation is similar in concept to the Smith predictor, where the real system output is compensated by means of knowledge of the system's behavior to prevent the inversion of the non-minimum phase dynamics. The main problem is that the Smith predictor concept is difficult to apply in the context of non-linear systems, as a plant factorization is required to determine

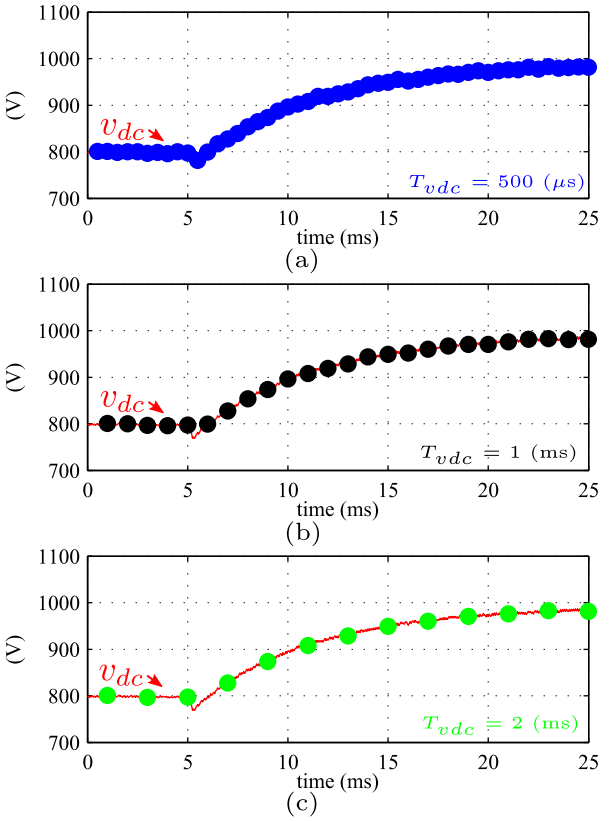

FIGURE 6. Illustration of the sampling effect on the non-minimum phase behavior of the output voltage v_{dc}. (a) sampling period $T_{vdc} = 500(\mu s)$, (b) $T_{vdc} = 1(ms)$, (c) $T_{vdc} = 2(ms)$.

the compensation term to transform the original output to a minimum phase one. To circumvent this problem, we propose to take advantage of the sampling process with a carefully selected sampling time. Previous use of this concept in the context of self-tuning control has been proposed in [26], and also in internal model control in [30]. A more recent discussion of this property is done in [25] and [24]. The present work proposes to select a sampling time which is always greater than the input power-output voltage step response undershoot. If this is the case, the undershoot will not appear in the sampled variable, making the result a minimum-phase approximation of the real output.

To illustrate the concept a simulation is performed where the continuous-time true voltage response to an input active power reference step is compared to its sampled discrete-time counterpart for different sampling periods. The results are presented in Fig. 6, for three sampling periods T_{vdc} equal to 500 (μs), 1 (ms), and 2 (ms). For $T_{vdc} = 500$ (μs), Fig. 6 (a), the sampled variable shows the undershoot as in the continuous-time response. When the sampling period is increased to 1 (ms), Fig. 6 (b), the sampled variable is in the limit of showing the NMP behavior, as the next sample after the step change is just equal to its previous value. When T_{vdc} is further increased to 2 (ms), Fig. 6 (c), the response does not show the undershoot and can be approximated as a minimum phase response, as it is monotonically increasing. As has

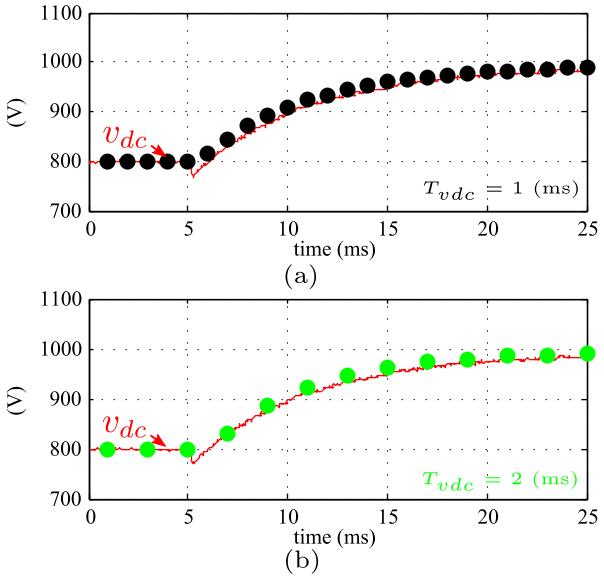

FIGURE 7. Comparison between the sampled minimum-phase approximate model response with the true non-minimum phase output. (a) sampling time $T_{vdc} = 1(ms)$; (b) $T_{vdc} = 2(ms)$.

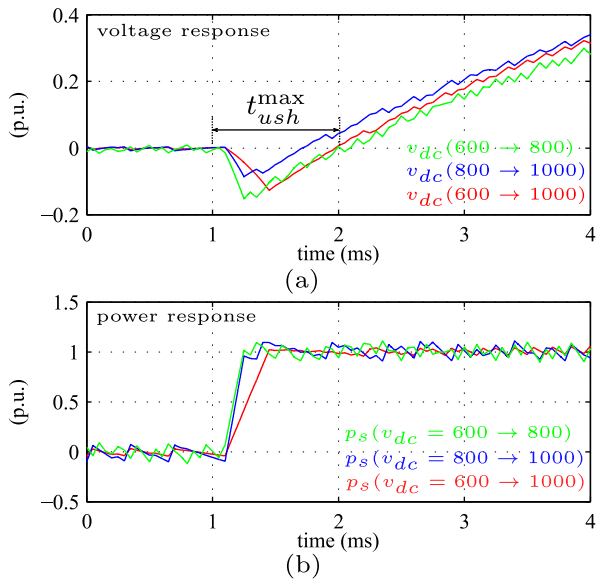

FIGURE 8. Normalized output voltage response undershoot for different active input reference steps. (a) output voltage response undershoot when moving v_{dc} from 600 to 800 (V), 800 to 1000 (V), and 600 to 1000(V); (b) normalized active power tracking for the corresponding reference step changes.

been illustrated, the sampling process can indeed remove the undesired undershoot.

To verify the accuracy of the discrete-time approximate minimum-phase model (34) with the true system output a simulation is performed. The results are presented in Fig. 7 for sampling periods of $T_{vdc} = 1$ (ms) and 2 (ms). The sampling period $T_{vdc} = 1$ (ms), Fig. 7 (a), is the critical value to generate an undershoot-less sampled output for this example parameter set. The approximate minimum-phase model accuracy in this case is limited, which is to be expected, as the minimum-phase model was designed explicitly to be free of this behavior. However, when the sampling period is increased to $T_{vdc} = 2$ (ms), Fig. 7 (b), the accuracy increases, as the model is better able to capture the true transient behavior of the system.

D. VOLTAGE CONTROLLER SAMPLING TIME SELECTION

As has been illustrated, the sampling process allows to recover an undershoot-less voltage response from the true system output. However, for this to occur, an appropriate sampling time must be used. The critical sampling time depends on the expected undershoot of the true voltage response. An analytic solution for this problem is not easy to obtain, as the power-voltage dynamic is nonlinear. However, simulation results together with some observations can be used as a practical solution.

For instance, the input power loop dynamic response to a step reference change can be used as a useful guideline to determine an appropriate sampling time. Fig. 8 shows the voltage response to step changes in the active power reference. Comparing Fig. 8 (a) and (b) it can be observed that the voltage undershoot duration is higher than the settling time of the power controller. This means that the sampling time T_{vdc} should be at least higher than this time. In addition, the undershoot time depends on the step change magnitude, being higher as the power reference increases. Then, it is proposed that the sampling time T_{vdc} should be at least two times the maximum undershoot time $t_{ush}^{\max}$:

$$T_{vdc} \geq 2\, t_{ush}^{\max}. \tag{35}$$

The $t_{ush}^{\max}$ value can be obtained from the analysis of the active power controller response to step changes in its reference. In particular, the worst case is a step change from the lowest to highest expected values, as depicted in Fig. 8 (b).

On the other hand, the linearization of model (28) could be used to obtain an approximation to the critical sampling time. For a first order plus one pole and one zero model defined by:

$$h(s) = \frac{1}{\tau_2 s + 1}\frac{\tau_3 s + 1}{\tau_1 s + 1}, \tag{36}$$

with $\tau_1, \tau_2 > 0$ and $\tau_3 < 0$ (non-minimum phase), the output is given by:

$$y(t) = 1 + \frac{\tau_1 - \tau_3}{\tau_2 - \tau_1} e^{-t/\tau_1} - \frac{\tau_2 - \tau_3}{\tau_2 - \tau_1} e^{-t/\tau_2}. \tag{37}$$

If τ_2 is very small, the output will be approximately equal to:

$$y(t) = 1 + \frac{\tau_1 - \tau_3}{-\tau_1} e^{-t/\tau_1}. \tag{38}$$

The output should be zero at the point where the undershoot has elapsed. Then, solving the equation for this instant:

$$t_z = \tau_1 \ln \frac{\tau_1 - \tau_3}{\tau_1}. \tag{39}$$

Finally, an estimation of the critical sampling time $t_{ush}^{\max}$ can be obtained by replacing the values of the linearized model (29):

$$t_z = \frac{R_{dc} C_{dc}}{2} \ln\left(1 - \frac{4P_s L_s}{R_{dc} C_{dc}} \frac{1}{4P_s r_s - 3V_s^2}\right), \tag{40}$$

where P_s is the maximum power of the converter. To have an adequate safety margin, it is proposed that the sampling time T_{vdc} should be at least two times the critical time t_z, i.e. $T_{vdc} > 2\ t_z$. This guideline can be verified considering the results of Fig. 8. Evaluating (40) for the example parameter set, the approximate critical sampling time is $t_z \approx 1$ (ms), approximately matching the simulation results. Thus, selecting $T_{vdc} = 2$ (ms) as proposed, assures that the undershoot is not present in the open loop sampled voltage response.

E. CALCULATION OF POWER COMMAND

To generate the active power command p_s^{ref} to steer the voltage v_{dc} towards its desired value, the model (34) is used by the proposed controller. As the control action is already fixed for the current sampling period an additional prediction step is required. Then, writing the model (34) for time $k+1$ gives:

$$v_{dck+2} = \left(p_{sk+1} - \frac{2r_s}{3V_s^2}(p_{sk+1})^2 - \left(\frac{1}{R_{dc}} - \frac{C_{dc}}{T}\right)(v_{dck+1})^2\right)\frac{T}{C_{dc}}\frac{1}{v_{dck+1}}. \quad (41)$$

Replacing v_{dck+2} by its desired reference $v_{dc\,k+2}^{\text{ref}}$, and p_{sk+1} by its command ${p_s^{\text{ref}}}_{k+1}$, a quadratic equation in ${p_s^{\text{ref}}}_{k+1}$ is obtained:

$$({p_s^{\text{ref}}}_{k+1})^2 + b{p_s^{\text{ref}}}_{k+1} + c = 0, \quad (42)$$

where,

$$b = -\frac{3V_s^2}{2r_s}, \quad c = \frac{3V_s^2}{2r_s}\frac{C_{dc}}{T}v_{dck+1}v_{dc\,k+2}^{\text{ref}} + \frac{3V_s^2}{2r_s}\left(\frac{1}{R_{dc}} - \frac{C_{dc}}{T}\right)(v_{dck+1})^2. \quad (43)$$

This equation has two roots given by:

$${p_s^{\text{ref}}}_{k+1} = \frac{-b + \sqrt{b^2 - 4c}}{2}, \quad (44)$$

however, the desired value ${p_s^{\text{ref}}}_{k+1}$ must verify that: (i) it is positive, (ii) it should be the lowest amount.

F. REFERENCE TRAJECTORY

Short horizon predictive controllers generally have an aggressive control response and poor robustness. In addition, in the case of output voltage control in the three-phase AFE rectifier there is a trade off between the controller bandwidth and the initial voltage undershoot. This means that a faster response usually means a greater voltage undershoot when a step command is applied. In order to improve the controller behavior to the aforementioned issues, a linear reference trajectory or set-point filter [31] will be considered. The reference trajectory for the output voltage v_{dc} will correspond to the following difference equation:

$$v_{dc\,k+2}^{\text{ref}} = v_{dc\,k}^{\text{ref}} + \alpha_r(v_{dck+1} - v_{dc\,k}^{\text{ref}}), \quad (45)$$

where α_r should be inside the unit circle to be stable, and it is assumed that $v_{dc\,k+1}^{\text{ref}} = v_{dc\,k}^{\text{ref}}$. Adjusting the value of α_r allows to tune the resulting controller dynamic, where values towards 1 imply a slower response.

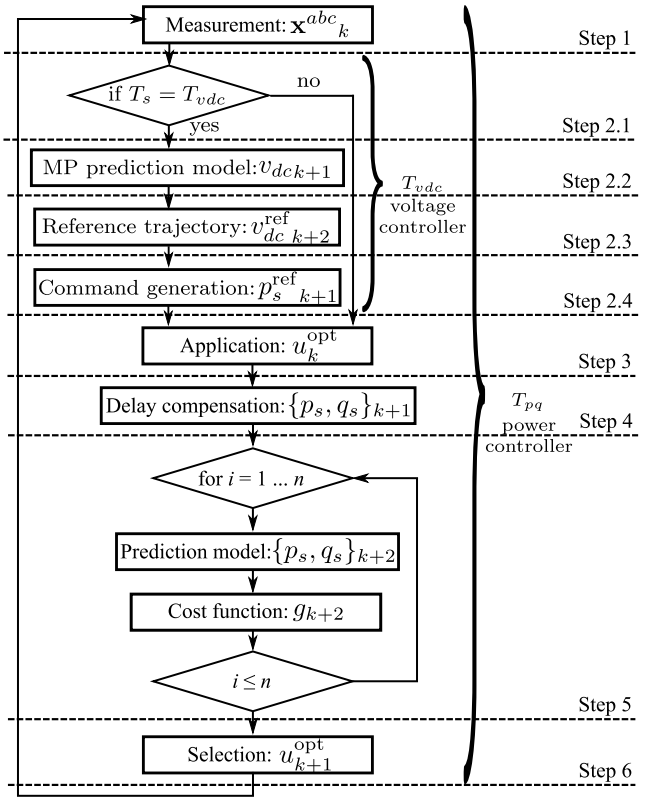

FIGURE 9. Proposed predictive controller flowchart.

G. ALGORITHM IMPLEMENTATION AND FLOWCHART

The proposed algorithm is summarized in the block diagram of Fig. 4. Its implementation and operation can be divided in the steps shown in the flowchart depicted in Fig. 9. Note that Step 2.1 up to Step 2.4 are executed with the sampling period of the voltage controller T_{vdc}, which is slower than the sampling period of the power controller T_{pq}. Herein, a detailed description will be provided.

Step 1 *Measurement*: Measure the system state variables $\mathbf{x}^{abc}$, which are the input inductors currents $\mathbf{i_s}^{abc}$ and output capacitor voltage v_{dc}, together with the disturbance $\mathbf{v_s}^{abc}$.

Step 2.1 *Voltage sampling decision*: Verify if the predictive voltage controller should be executed (updating its output), counting the number of the controller sampling periods elapsed from the previous update. If not enough sampling periods have elapsed skip to Step 3, without updating the power reference ${p_s^{\text{ref}}}_{k+1}$.

Step 2.2 *Minimum-phase prediction model*: Use the current value of the voltage v_{dck} as input to the minimum-phase model to predict the value of the voltage at time $k+1$, v_{dck+1}.

Step 2.3 *Reference trajectory*: Generate the desired voltage reference $v_{dc\,k+2}^{\text{ref}}$ used to calculate the power command ${p_s^{\text{ref}}}_{k+1}$.

Step 2.4 *Power command generation*: Use the predicted value of the voltage obtained with the minimum-phase model

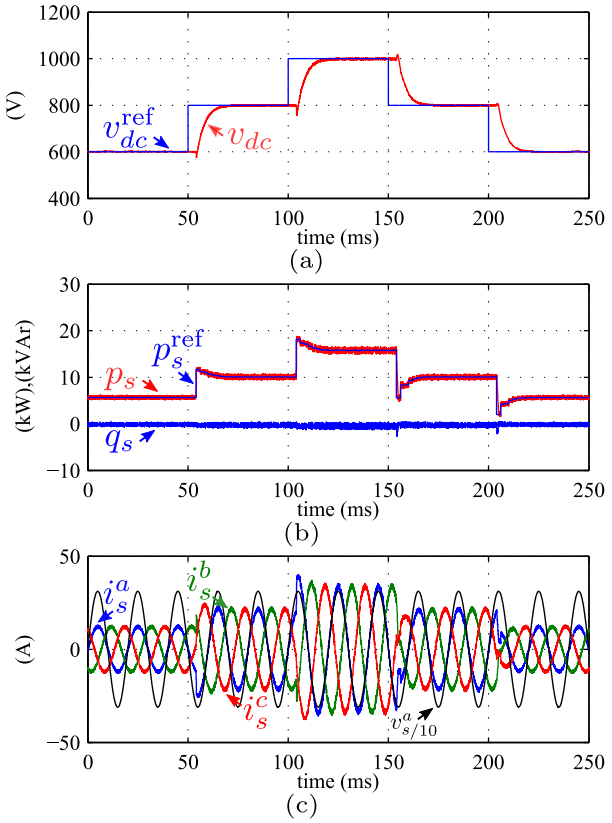

FIGURE 10. Simulation results for reference step changes with the proposed voltage controller. (a) output voltage v_{dc} and its reference v_{dc}^{ref}, (b) input active power p_s, its reference p_s^{ref}, and input reactive power q_s; (c) input currents $\mathbf{i_s}^{abc}$ and scaled phase a mains voltage $v_s^a/10$.

v_{dck+1}, and the minimum-phase model, to generate the required power command at time $k+1$, ${p_s^{ref}}_{k+1}$.

Step 3 *Application*: Apply the switching state combination $\mathbf{s_r}^{abc}$ obtained in the previous sampling time, as calculated by the controller.

Step 4 *Delay compensation*: Predict the value of both the active and reactive power at time $k+1$, p_{sk+1} and q_{sk+1}, to be used in the power prediction model.

Step 5 *Prediction*: Use the prediction model to minimize the power cost function g_{k+2} according to the references, evaluating the $n=8$ states of the power converter.

Step 6 *Selection*: Update the switching state combination $\mathbf{s_r}^{abc}$ to be applied at the next sampling time. Go to Step 1 at the next sampling period T_{pq}.

V. SIMULATION RESULTS

In order to verify the proposal feasibility simulation tests will be first considered. The parameters will be the same as the ones used before in the examples. First, the controller response to step changes in the voltage reference will be evaluated and compared with the power controlled voltage response. Afterwards, the behavior of the controller under parameters and disturbances changes will be assessed.

A. REFERENCE TRACKING TO STEP CHANGES

To study the reference tracking behavior of the proposed controller, step changes are applied to the voltage reference. The system's response to a sequence of step changes in the voltage reference is shown in Fig. 10. Fig. 10 (a) shows the reference output voltage and the actual system response. It can be observed that the reference is successfully tracked after a time delay of 2 voltage sampling periods T_{vdc}. As stated before, T_{vdc} is selected to avoid the NMP behavior of the voltage dynamic, and is bigger than the sampling period used for the power loop T_{pq}. This delay is to be expected, considering how the controller calculates the required power reference value. Indeed, as the power value at time $k+1$ is already determined in the previous sampling time, the effect on the control action -the input power command-, can only be expected at time $k+2$. After the initial delay, the controller begins the tracking of the desired reference trajectory. The characteristic undershoot behavior of the voltage response remains, meaning that the RHP zero is not canceled by the controller.

Fig. 10 (b) shows the input power of the converter and its reference, which is generated by the voltage controller. As in the voltage response, the two T_{vdc} sampling periods delay is also present in the power reference. However, this delay is transparent to the power controller, as the power controller has a much smaller sampling period T_{pq}, and is faster than the voltage one, given that it does not need to compensate the NMP behavior of the voltage. Also, the true voltage value is used inside the power controller for prediction purposes. The value of the power reference is initially higher than the steady state value, which allows the system to have a faster response than when operating in open loop. Also, the input instantaneous reactive power is regulated around its desired reference of 0 (VAr), in order to operate at unity displacement input power factor. Finally, Fig. 10 (c) shows the converter input currents, which show appropriate behavior under transient conditions, without extending too far from the steady state values.

B. COMPARISON WITH POWER CONTROLLER ONLY

To evaluate the voltage dynamic response of the proposed controller, its response is plotted in a single figure together with the ones obtained using the power controller alone and a PI voltage controller, Fig. 11. The PI voltage controller is implemented in discrete-time and has been tuned for the 800-1000V region, resulting in a gain $k_{vdc}=0.9549$ while its zero is located at $a_{vdc}=0.9$. Fig. 11 (a) shows the voltage response and Fig. 11 (b) shows the input power of the converter. It is apparent that a two T_{vdc} sampling periods delay exists in the voltage response of the proposed controller, as well as in the generated power command, as discussed before in subsection V-A. However, the delay is transparent to the power controller, which only sees the effect on its reference, due to its faster dynamics. On the other hand, it is clear from Fig. 11 (b) that the improvement in the voltage dynamic response versus the power controller alone is achieved by a transient increase in the drawn input power, even considering

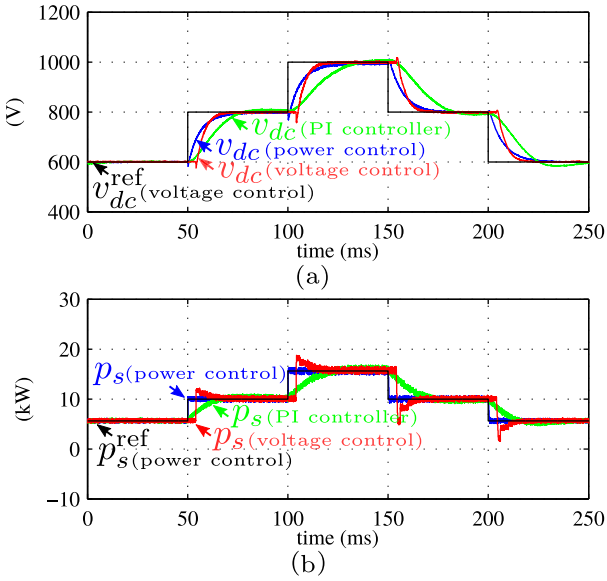

FIGURE 11. Voltage and power responses of the proposed voltage controller. (a) voltage response v_{dc} of the proposed controller (red), power controller alone (blue), PI voltage controller (green), and reference v_{dc}^{ref} (black); (b) converter active input power when using the proposed voltage controller (red), PI voltage controller (green), power controller alone (blue), and its reference p_s^{ref} (black).

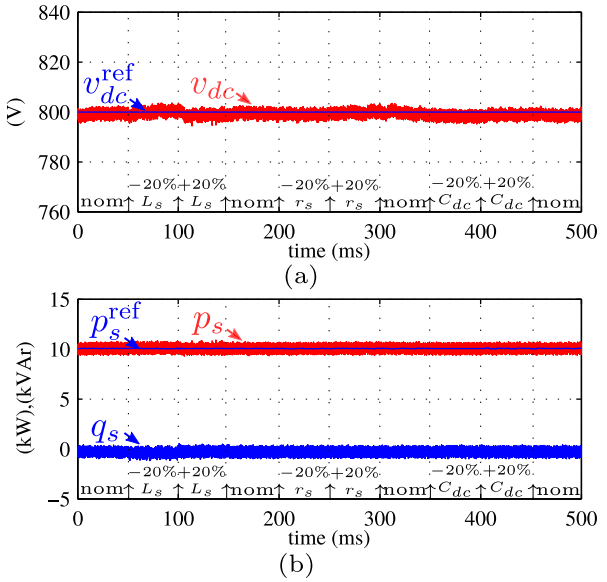

FIGURE 12. Proposed controller behavior under parameter mismatch in model parameters L_s, r_s and C_{dc}. (a) dc output voltage v_{dc} and its reference v_{dc}^{ref}; (b) instantaneous input active power p_s, its reference p_s^{ref}, and input reactive power q_s.

the delay of the closed-loop voltage controller. In contrast to the PI controller, the proposed controller shows a faster voltage response that also does not significantly change its dynamic characteristic with the operating point. A rise time of approximately 10 (ms) is obtained with the proposed controller, while the PI controller achieves 25 (ms). Also, Fig. 11 (b) shows that the input power obtained with the PI controller has a sluggish behavior when compared to the one of the proposed controller and power controller alone.

C. BEHAVIOR UNDER PARAMETER CHANGES

It is desired that the controller should have, at least, stable behavior when the model parameters do not exactly match the ones of the physical converter system as it is in most practical cases. To study the controller behavior under these conditions, a simulation is performed introducing error in the parameters of the model used by the controller. A sequence of step changes in the different model parameters is considered. The results are shown in Fig. 12.

First, during the interval 0-150 (ms), a sequence of step changes is applied to the model inductance value L_s. The value of this element depends on the component's tolerance, and the wiring used to feed the converter. Initially, the value is decreased by 20% during the interval 50-100 (ms), then it is increased by 20% from its nominal value, returning to the original condition at 150 (ms). As observed from Fig. 12, a stable behavior with very small steady state error is obtained for the controlled variables, the dc output voltage and the instantaneous input reactive power.

Afterwards, during the interval 200-300(ms), a sequence of step changes is applied to the model parasitic resistor value r_s. This parameter is defined by the filter inductor and its value depends on its losses and the supply wiring. As in the previous case, the value is decreased by 20% during 200-250(ms), and then increased by 20% from its nominal value, returning to the original condition at 300 (ms). Fig. 12 shows similar results as when the inductance value was modified, obtaining stable operation with small steady state error.

During the interval 350-450(ms), step changes in the model capacitance value C_{dc} are applied. The converter's output capacitor value depends on its aging and tolerance from nominal design values. Indeed, a tolerance of 20% is common for commercial components. For the test, the value is decreased by 20% at 350 (ms) and then increased by 20% from its nominal value at 400 (ms), returning to the initial one at 450 (ms). Fig. 12, also shows for this case that the controller remains stable and with a small steady state error, as seen before in the previous tests.

D. BEHAVIOR UNDER DISTURBANCES

The proposed control scheme should operate properly when subjected to disturbances changes, particularly in terms of stability. In the three-phase rectifier system at least two possible disturbance sources can be recognized, which are the mains voltage and the load. The first one is a common source of disturbances. Indeed, due to changes in the load conditions in the power grid, voltage sag/swell usually occurs. The controller must maintain the output voltage around the reference value, and be unaffected by these changes. The same situation is desired for variations of the load resistor, which may change depending on the connected load.

To test this situation, step changes are applied to the ac mains voltage magnitude during 0-200 (ms). Fig. 13 (a) shows the voltage response of the controller to a 20% swell

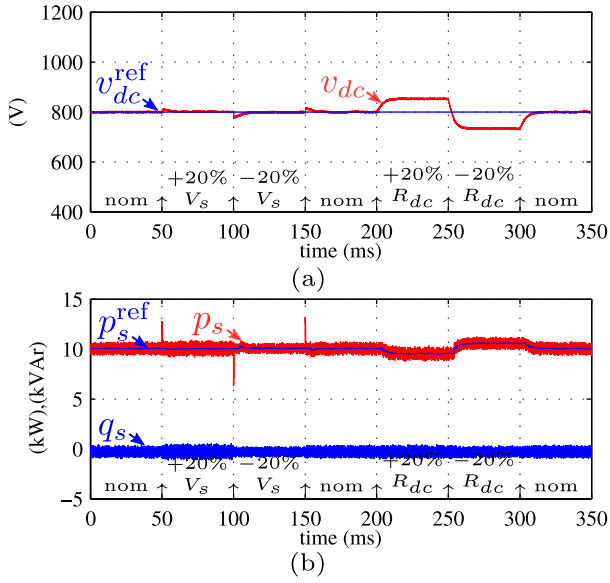

FIGURE 13. Proposed controller behavior under grid voltage and load resistor disturbances. (a) dc output voltage v_{dc} and its reference v_{dc}^{ref}, (b) instantaneous input active power p_s, its reference p_s^{ref}, and input reactive power q_s.

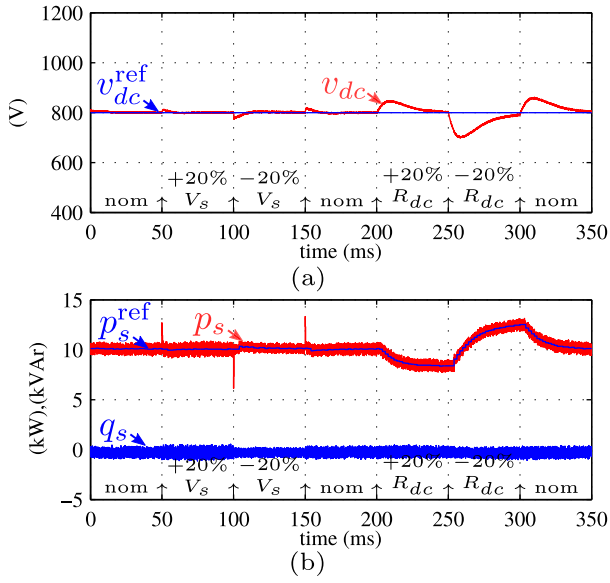

FIGURE 14. Proposed controller behavior under grid voltage and load resistor disturbances with steady-state error compensation. (a) dc output voltage v_{dc} and its reference v_{dc}^{ref}, (b) instantaneous input active power p_s, its reference p_s^{ref}, and input reactive power q_s.

in the ac mains during 50-100(ms), while Fig. 13 (b) shows the corresponding input powers. The output voltage is nearly unaffected by this change in the input voltage after a brief initial transient. Similar results are obtained for a 20% sag step change during 100-150(ms). A stable operation with small steady-state error is obtained even under these conditions.

Afterwards, during 200-350(ms), step changes of 20% of the nominal value are applied to the model load resistor value. Fig. 13 shows the controller behavior when its value

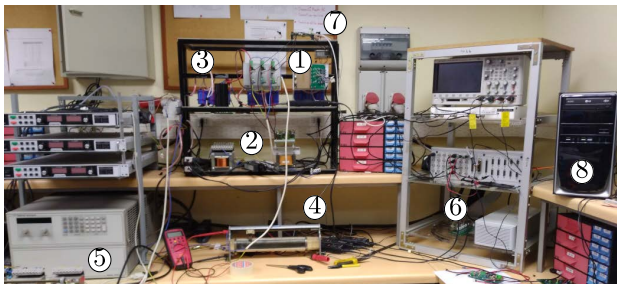

FIGURE 15. Experimental setup of the three-phase AFE rectifier. ①: three-phase AFE rectifier, ②: inductive filter, ③: dc-side capacitor, ④: converter load; ⑤: three-phase power supply; ⑥: dSPACE 1103, ⑦: electrical-optical interface, ⑧: control computer.

is increased and reduced during this time period. Stable operation is observed after the change in value, however a non-negligible steady state error appears. This is a natural consequence of the lack of integral action in the proposed predictive controller.

To overcome the aforementioned problem, a simple solution is to add integral action to the controller including a compensation term. The setpoint is modified by the addition of a weighted integral of the error. The new compensated voltage reference to be fed to the controller, denoted by v_{dcik}^{ref}, will therefore be:

$$v_{dcik}^{ref} = v_{dc\,k}^{ref} + \delta v_{dc\,k}^{ref}, \tag{46}$$

where $\delta v_{dc\,k}^{ref}$ is given by:

$$\delta v_{dc\,k}^{ref} = \delta v_{dc\,k-1}^{ref} + k_i T_{vdc} \left(v_{dc\,k}^{ref} - v_{dck} \right), \tag{47}$$

with k_i a positive constant. Using the compensation, the experiment is repeated using $k_i = 50$. The results are presented in Fig. 14. As can be seen, the compensation term successfully eliminates the steady state error.

VI. EXPERIMENTAL RESULTS

To verify the feasibility of the proposal, a prototype scaled-down grid-connected three-phase AFE rectifier system was built using G4BC20UD IGBTs with the parameters shown in Table 1. The rectifier is supplied by a California Instruments 4500iL three-phase power supply. Although due to limitations of our experimental setup the voltage levels are reduced, this does not mean a better -or more advantageous- condition with regards to a system with higher voltage levels. The control algorithms have been implemented in a dSPACE 1103 platform. The complete experimental setup is shown in Fig. 15, where the algorithm described in Fig. 4 and Fig. 9 has been developed in MATLAB using control computer ⑧, which is also used as a basic human-machine interface, and the controller runs in the dSPACE DS1103 ⑥.

A. PREDICTIVE POWER CONTROL

To implement the proposed voltage controller a working predictive power controller is required. To verify its correct operation, a step change in the power reference from 20 to 35 (W)

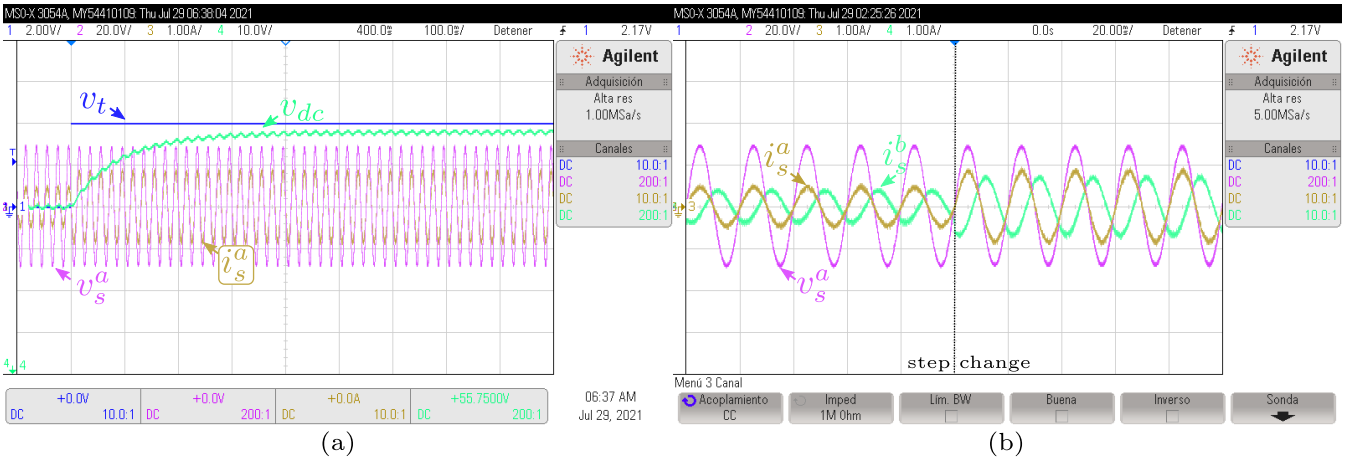

FIGURE 16. Horizon one model predictive power controller response to a step power reference change. (a) output voltage v_{dc}, phase a input voltage v_s^a, phase a input current i_s^a, and trigger signal v_t; (b) phase a input voltage v_s^a, phase a and phase b input currents i_s^a, i_s^b.

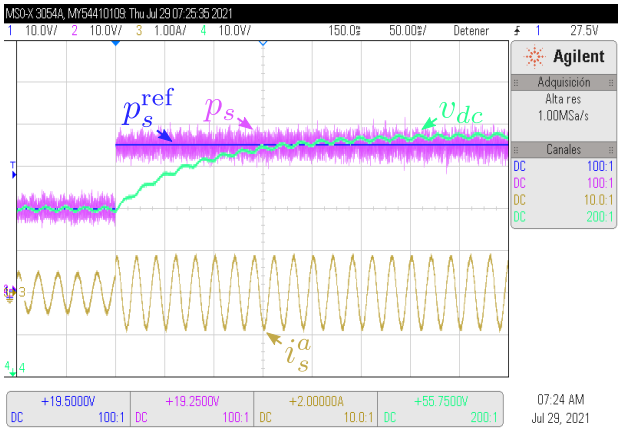

FIGURE 17. Power and voltage response of the horizon one model predictive power controller.

TABLE 1. Setup parameters.

System Description	Value
L_s: Rectifier filter inductance	12.5 (mH)
r_s: Inductor series resistor	0.3 (Ω)
C_{dc}: Rectifier dc-side filter capacitor	1000 (μF)
R_{dc}: Rectifier load	185.3 (Ω)
V_s: Input phase voltage rms value	20 (V)
f_s: Input voltage frequency	50 (Hz)
f_{pq}: Power sampling frequency	20 (kHz)
T_{pq}: Power sampling period	50 (μs)
T_{vdc}: Voltage sampling period	4 (ms)

is considered, in order to obtain output voltages of approximately 60 (V) and 80 (V), respectively. The results of this test are shown in Fig. 16. It can be verified from Fig. 16 (a) that the expected steady state voltage values are obtained after the step in the power reference p_s^{ref}. The output voltage response v_{dc} is approximately of first-order, confirming the theoretical analysis. Nevertheless, it is difficult to appreciate that the expected undershoot from the NMP zero is in fact present due to the time scale, this will be reexamined in the subsequent section. In addition, a small voltage ripple can be observed that is not present in the simulation results. One of the reasons for this ripple is the presence of small imbalances in the circuit elements, particularly the filter inductors, as they are rarely exactly the same, even when their nominal value is.

On the other hand, Fig. 16 (b) shows the phase a and b line currents, and the phase a mains voltage. The phase a current i_s^a is in phase with the mains voltage v_s^a and remains so even when the change of power reference is performed, as desired. After the change is produced, the line current magnitude increases, as expected from the increase of the desired input power. Also, phase a and b currents have a small difference, reflecting the small imbalance of the inductive filter.

The input power response p_s to the step change in the reference p_s^{ref} under the aforementioned conditions is presented in Fig. 17. It can be seen that the power response p_s is very quick when compared to the voltage one v_{dc}, given the use of the horizon one predictive power controller. Considering that the voltage v_{dc} is effectively operating in open loop, these results illustrate the intrinsic time decoupling characteristic of the different time constants. The phase a line current i_s^a remains in phase with the mains voltage after the change, which implies successful control of the reactive power of the rectifier.

B. PREDICTIVE VOLTAGE CONTROLLER SAMPLING TIME

After verifying the correct operation of the power controller, it is possible to specify the voltage loop sampling time based on the voltage dynamic response. Fig. 18 (a) and (b) illustrate the key dynamic characteristics of the power and voltage dynamics, respectively. As expected, the input power dynamic in Fig. 18 (a) exhibits a delay of two T_{pq} sampling periods, as the predictive power controller optimizes the value two time steps ahead. On the other hand, Fig. 18 (b) shows a zoom of the voltage response around the region immediately after the step change, where the NMP characteristic of the voltage response can be clearly observed. This aspect was not apparent in the previous results of Fig. 16 (a) and Fig. 17

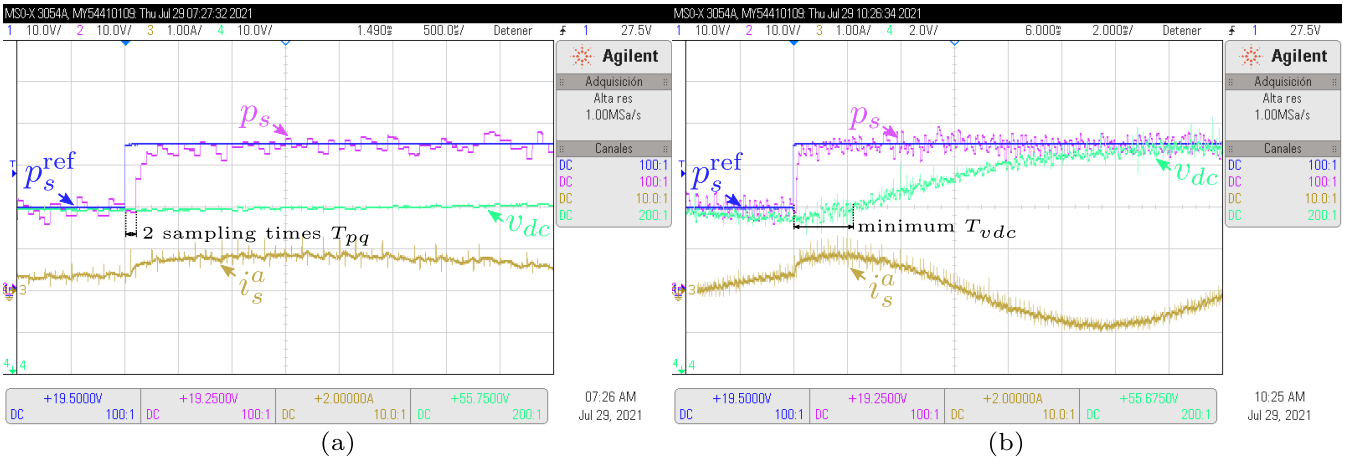

FIGURE 18. Horizon one model predictive power controller response delay and NMP zero characteristic. (a) illustration of the sampling time power controller delay, (b) NMP voltage undershoot and minimum voltage loop sampling time.

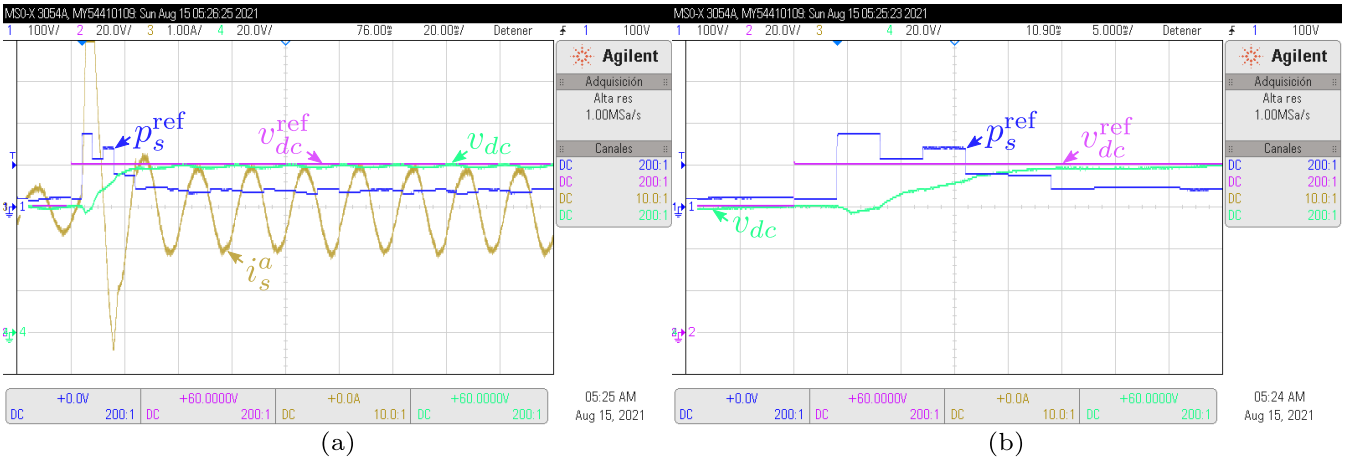

FIGURE 19. Response to a voltage reference step change of the proposed horizon one predictive voltage controller. (a) output voltage v_{dc}, its reference v_{dc}^{ref}, generated power command p_s^{ref}, and phase a input current i_s^a; (b) zoom of the generated power command p_s^{ref} and the output voltage v_{dc}.

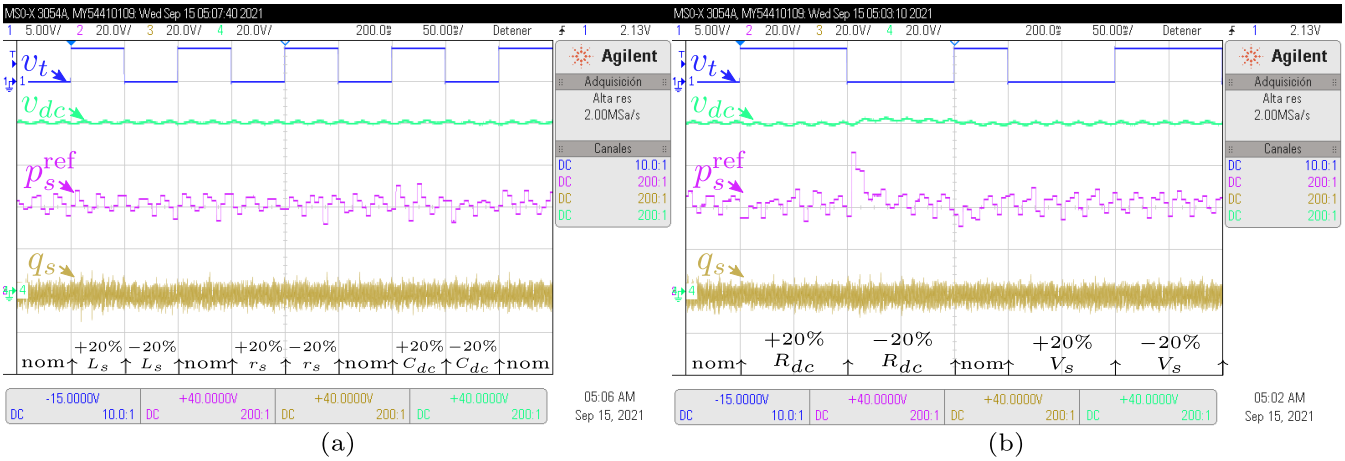

FIGURE 20. Response of the proposed horizon one predictive voltage controller to model mismatch. (a) model mismatch in inductive filter L_s, parasitic resistor r_s, and output capacitor C_{dc}; (b) model mismatch in load resistor R_{dc} and input voltage amplitude V_s.

due to the different time scales of the dynamic responses. Analyzing Fig. 18 (b), it can be concluded that the undershoot duration due to NMP zero is approximately 2 (ms). This simple procedure is used to adjust the sampling time of the

TABLE 2. Algorithm comparison.

Controller	Dynamic Response	Requires Modulator	Limiters	Requires Anti-windup	Complexity	Commutation Frequency	Tuning Difficulty	Steady-state Error	Coordinate Transformations
Voltage PI + PDPC [9], [12], [29]	Med	No	Input Power	Yes	Med	Variable	Med	None	Yes, $\alpha\beta$
Voltage PI + PCC [16]	Med	No	Input Current	Yes	Med	Variable	Med	None	Yes, $\alpha\beta$
Voltage PI + dq current PI [20]	Low	Yes	Input Current	Yes	Med	Fixed	High	None	Yes, dq
Proposed algorithm	High	No	Input Power	No	Med	Variable	Low	None (w/comp.)	Yes, $\alpha\beta$

*PI: Proportional Integral, PDPC: Predictive Direct Power Control, PCC: Predictive Current Control

predictive voltage controller T_{vdc}, which should be at least 4 (ms) for successful operation.

C. PREDICTIVE VOLTAGE AND POWER CONTROLLER

Having verified the correct operation of the predictive power controller and selected an appropriate sampling time T_{vdc} for the voltage loop as proposed, it is possible to proceed to the implementation and testing of the proposed voltage controller. To test the controller's operation, a step change from 60(V) to 80(V) in the voltage reference is applied, operating with a zero reactive power reference, i.e. $q_s^{\text{ref}} = 0$. The results are shown in Fig. 19 (a) and (b). Fig. 19 (a) shows that the output voltage v_{dc} follows its reference v_{dc}^{ref} in steady state after approximately 25 (ms). The power command p_s^{ref} generated by the voltage controller has an initial delay of two T_{vdc} sampling periods (8 (ms)), which is intrinsic to the control algorithm, as highlighted in Fig. 19 (b). After the initial delay, a transient increase in the power command is generated in order to follow the voltage reference, which begins to increase after an initial delay and the voltage undershoot. During the transient, the phase a current i_s^a sharply increases its value to quickly follow the voltage and power reference changes, as expected. The NMP characteristic of the voltage response remains present, Fig. 19 (b), even after the initial delay of the predictive controller. Additionally, it can be noted from Fig. 19 (a) that the power reference p_s^{ref} is not perfectly constant in steady-state. Due to non-ideal conditions -particularly unequal component values- the controller is always adjusting its output towards maintaining the voltage around its reference value. This is to be expected, taking into account the high bandwidth of the controller.

D. BEHAVIOR UNDER PARAMETER MISMATCH AND DISTURBANCES

To verify the behavior of the proposed controller under parameter mismatch step changes in the different model parameters is performed. Changes of 20% from each parameter nominal value are considered. The results are presented in Fig. 20. First, changes in the input inductor size L_s, parasitic resistor r_s and output capacitor C_{dc} are considered in the model, which are triggered by the signal v_t, Fig. 20 (a). The results already use the scheme presented in the previous section, with a compensation gain $k_i = 10$. It can be observed that due to the feedback action the effect of the parameter changes in the overall controller are small, in particular in the output voltage v_{dc} and the input reactive power q_s. On the other hand, Fig. 20 (b) shows the corresponding results for variations in the load resistor R_{dc} and the input voltage amplitude V_s. In this case, the change in the steady-state value of the output voltage v_{dc} is greater. However, the compensation scheme allows successful regulation at the desired value.

VII. DISCUSSION

From the simulation and experimental tests performed in the scaled-down prototype it can be concluded that the proposed algorithm is able to successfully handle the NMP behavior of the voltage dynamic, resulting in a stable controller as intended. Some remarks can be made regarding the results. First, the tuning of the controller is much simpler than when using a PI voltage controller, as the method ensures a stable behavior independent of the setting of the reference trajectory, if the sampling time of the voltage is correctly set. The implementation of the voltage controller is simple and does not significantly increase the computational burden of the predictive algorithm. The dynamic response is fast, given that all the invertible parts of the plant are inverted, and only depends on the specified reference trajectory. In addition, direct consideration of constraints in the actuation is provided by the predictive algorithm. Some of the drawbacks are the variable commutation frequency, and the appearance of steady-state error if model parameters are not exact, yet it can be compensated, as described in (47). A summary of the algorithm comparison is presented in Table 2.

VIII. CONCLUSION

The present work has shown a new way to deal with the non-minimum phase characteristic of the three-phase AFE rectifier when using a horizon one model predictive controller for output voltage control, avoiding regulation loss and overcurrents that can damage the converter. This new approach, based on the control principles of plant factorization and sampling, allows to obtain a stable controller using only horizon one predictive control. As such, longer prediction horizons are not required, only marginally increasing the computational effort required versus using a predictive power controller alone, adding the evaluation of three equations.

A fast dynamic response is obtained, given the use of a short prediction horizon, reducing the voltage response rise time to 10 (ms), versus 25 (ms) for a PI voltage controller for the parameters under evaluation. Furthermore, the tuning is straightforward, as the controller performance is specified by the reference trajectory filter time constant. The concept of dealing with the non-minimum phase behavior using a conveniently selected sampling time is intuitive to understand, which allows the direct determination of its value from the open-loop power-voltage response, sidestepping an explicit factorization of the plant. Simulated and experimental results confirm the feasibility of the proposed approach.

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